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Analysing Efficiency and Reliability of High Speed Drive Inverters Using Wide Band Gap Power Devices

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Abstract: Within the project 'ARIEL' an electrical turbo compressor unit for fuel cell applications is deeply investigated. The necessary drive inverter is especially designed for high fundamental frequency and high switching frequency to cope with the requirements of the implemented electrical machine. This paper presents investigations on the inverter's efficiency and its prospective lifetime at different stages of the development. In the design process different wide band gap power semiconductor devices in discrete packages are evaluated in terms of the achievable power density and efficiency, both by simulations and measurements. Finally, an optimised design using surface mount silicon carbide MOSFETs is developed. Compared to a former inverter design using silicon devices in a three-level topology, the power density of the inverter is significantly increased. The lifetime of power electronic systems is often limited by the lifetime of the power semiconductor devices. Based on loss calculations and the resulting temperature swing of the virtual junction the lifetime of the inverter is estimated for the most frequent operating points and for different mission profiles.

Keywords: high-speed drive system; high power density; wide band gap power semiconductors; high efficiency; lifetime estimation; thermal design

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1. Introduction

This article describes the research and development that is performed in the field of power electronics during the funded collaborative project 'ARIEL'. The main goal is the development of a drive inverter with special requirements in terms of switching frequency with a high power density, high efficiency and good reliability.

The target application is the electrical turbo compressor unit of an automotive fuel cell system. The high performance and high-speed electrical machine used in this application strictly defines some challenging requirements that are addressed by the presented investigations.

Figure 1 illustrates the performed design process and also represents the structure of this article. In a first part, the design of possible drive inverter implementations is described. Step by step, the requirements are collected, and possible solutions are defined. These are compared and evaluated based on theoretical analysis and power loss simulations. Afterwards, the most promising solutions are compared with each other based on the practical evaluation of power stage prototypes in a test bench. The execution and the results of these extensive measurements are described in detail in the second part of the article.

In parallel to this design process, the expected lifetime of different power semiconductor devices is determined. Therefore, the third section deals with a method for lifetime estimation of power electronics. A selection of wide band gap semiconductors is investigated for different operating points and different mission profiles.

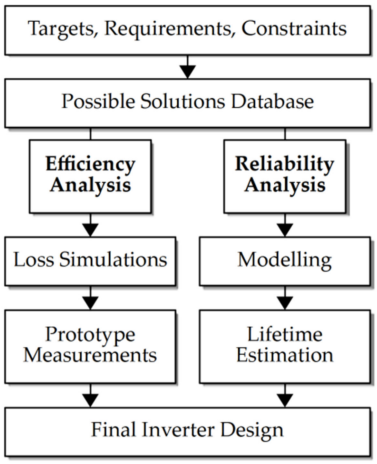

Figure 1. Basic design process.

2. Drive Inverter Design Procedure

The development and design of the specific electrical machine used in the target application is described in [1]. High speed permanent magnet synchronous machines with surface mount or solid magnets and small stator inductance are especially sensitive against higher frequency harmonic currents that cause additional losses [2–6]. This can be addressed by either multi-level inverter topologies or high switching frequencies [7,8]. To reach higher switching frequencies, wide band gap power devices with low switching losses can be utilised [9–13]. Many different devices based on silicon carbide (SiC) and gallium nitride (GaN) substrates are already available and [14–17] specifically focus on the use of GaN devices for high-speed drive applications.

After defining targets, requirements and constraints for the new design, a wide range of different possible inverter designs including two-level and three-level topologies using silicon, SiC and GaN devices is defined and compared within this project. Preliminary results are also published in [18–20] and are summarised in this section. Based on a theoretical evaluation and loss simulations, a selection of different wide band gap inverters is realised and operated in an inverter test bench. The results are shown in the next section.

2.1. Definition of Targets, Requirements and Constraints

In the first step of the design procedure, the most important targets, requirements and constraints are collected and evaluated. These arise from the general application, the specific motor design and the automotive background.

The drive system is supposed to operate from a DC power system with a voltage ranging from 250 V up to 500 V. The nominal power is defined as 15 kW with some safety margin. A liquid cooling system may be used. The main design targets are high efficiency as well as high power density.

The electrical machine integrated in the turbo-compressor-unit is a synchronous machine with a solid two-pole permanent magnet rotor. The electrical fundamental frequency is 2000 Hz at a mechanical speed of 120,000 rpm. The inductance of the machine's stator winding is small and the permanent magnet rotor is sensitive against harmonic content in the stator current. Since the permanent magnet cannot be segmented to reduce eddy currents due to mechanical reasons, and it cannot be cooled very efficiently, a high switching frequency of the drive inverter is mandatory to keep the ripple current as small as possible. Figure 2 shows predicted rotor losses as a function of the inverter's switching frequency. A minimum switching frequency of 60 kHz is selected. Nevertheless, a switching frequency of up to 120 kHz would further reduce the rotor losses and is the target of the following investigations. Table 1 summarises the collected requirements.

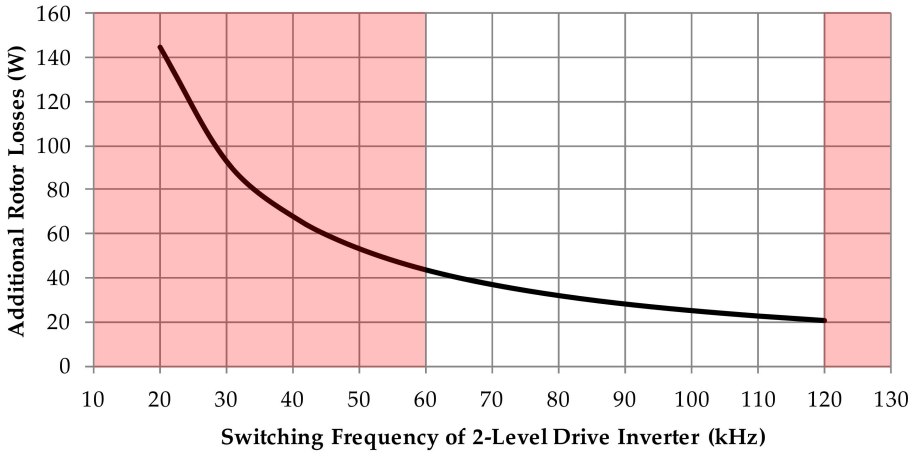

Figure 2. Additional rotor losses caused by high frequency stator currents.

Table 1. Basic functional requirements for the drive inverter [18].

Property	Value
DC voltage	250 V to 500 V
Load current	up to 60 A_{rms}
Load power	up to 15 kW
Load frequency	up to 2000 Hz
Switching frequency	at least 30 kHz (3-level) or 60 kHz (2-level)
Interfaces	CAN, resolver, HV-interlock
Ambient temperature	−25 °C to 90 °C
Coolant, temperature	water/glycol, −25 °C to 70 °C

For the performance analysis, three important operating points (OP) are defined. Representing the most typical steady state operation, OP (1) is defined at a load current of 30 A_{rms} and a high modulation index of 0.9. The highest efficiency is targeted for these conditions. OP (2) describes the static full load operation at 42 A_{rms}. This is the crucial operation for the thermal design and defines the maximum static thermal resistance of the cooling system. Finally, OP (3) represents the dynamic operation at the highest torque needed for rapid acceleration of the motor's shaft. The most important values for these three operating points are listed in Table 2.

Table 2. Typical operating points defined for evaluation of different inverter designs [18].

Property	OP (1)	OP (2)	OP (3)
DC voltage	400 V	400 V	400 V
Load current	30 A_{rms}	42 A_{rms}	60 A_{rms}
Modulation index	0.9	0.9	0.5

2.2. Theoretical Analysis and Loss Estimation

According to the defined requirements a large variety of possible solutions in terms of inverter circuit topology, power semiconductor technology and device packaging is defined. For the required voltage and power range, conventional two-level inverters (see Figure 3) or three-level designs either in NPC (neutral point clamped) I-type or T-type (see Figure 4) configuration can be selected. The current rating can be met using silicon IGBT (insulated gate bipolar transistor), silicon carbide MOSFET (metal oxide semiconductor field effect transistor) or gallium nitride devices. Especially with regard to the high switching speed demand, a strong focus is on wide band gap power devices. For all technologies, different devices with various packaging options are available, ranging from fully integrated six-pack power modules to discrete single devices in leaded or surface mount packages.

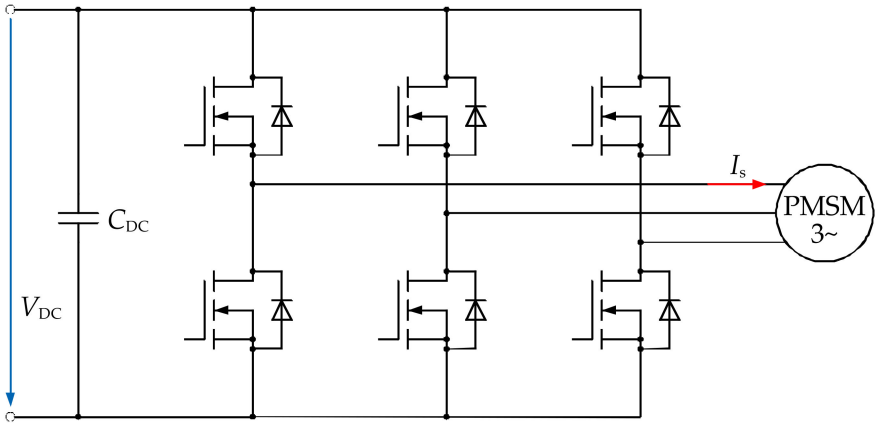

Figure 3. Two-level voltage source inverter (2L VSI) using MOSFET devices.

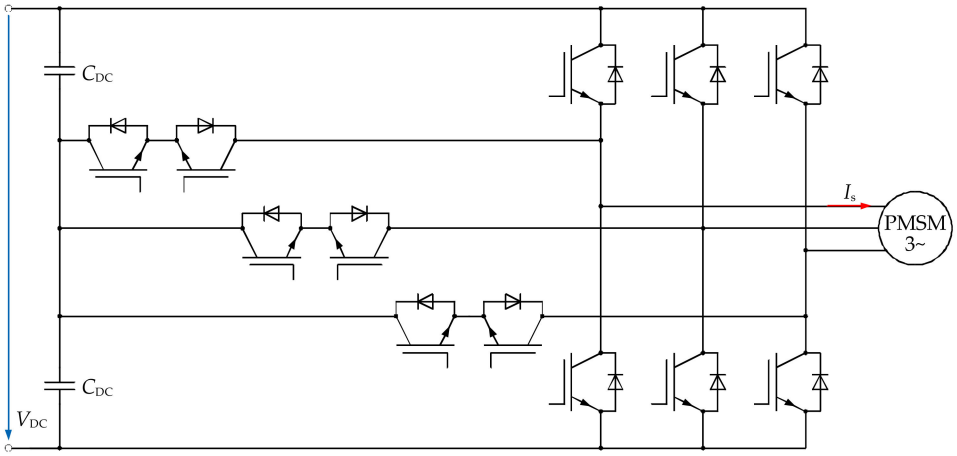

Figure 4. Three-level neutral point clamped inverter in T-configuration (3L NPC T-type) using IGBT and diode devices.

These very different solutions are compared and evaluated according to different criteria. One very important aspect is the expected efficiency. This is calculated using a loss estimation method developed especially for the flexible and fair comparison of different power semiconductor device technologies and large parameter studies on semiconductor losses. This novel calculation method is published in [21]. It is based on an analytical description of the different terms of the power devices' losses. The medium losses in a single operating point are then calculated using numerical integration. This allows a very flexible description of different power devices and operating strategies in a consistent environment and with short calculation times.

Figure 5 shows a small selection of the obtained results. The estimated power losses of some two-level voltage source inverter designs using different wide band gap power semiconductor devices are presented, taking into account the three operating points OP (1) to OP (3) defined in Table 2. For the solutions using discrete devices, two devices are always connected in parallel to meet the load current requirements.

It can be recognised that all selected wide band gap solutions can reduce the resulting power losses compared to a three-level inverter design using silicon based IGBT technology. At a switching frequency of 60 kHz the investigated silicon carbide devices show the best performance thanks to low conduction and switching losses. For operation at up to 120 kHz GaN devices have advantages due to their even lower switching losses.

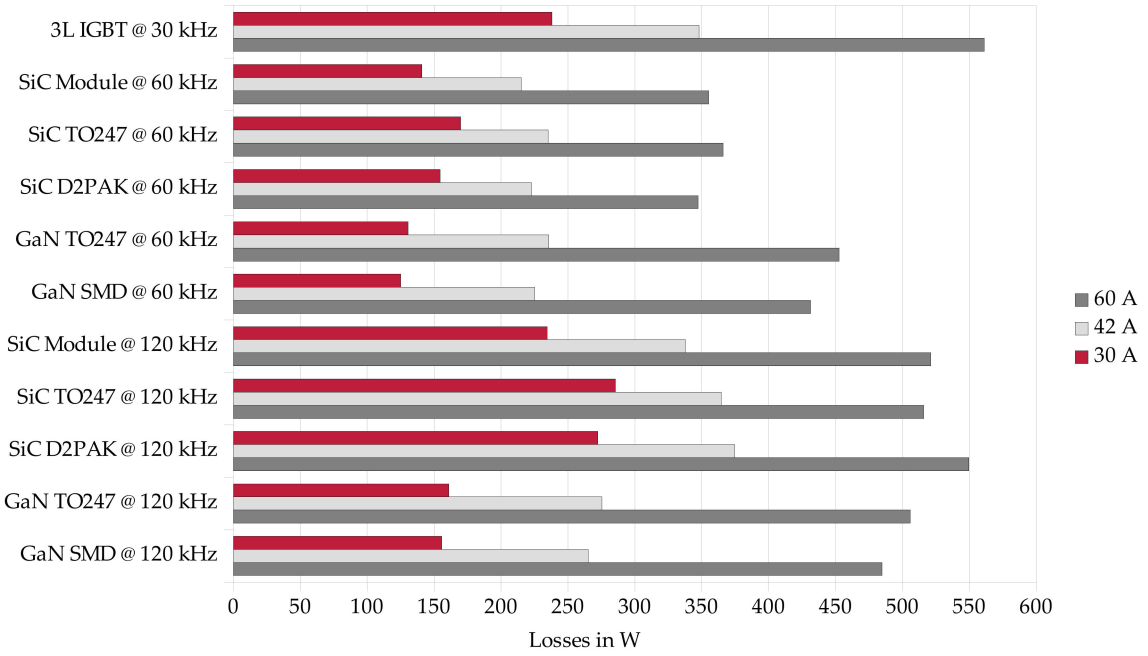

Figure 5. Estimated inverter losses for selected two-level wide band gap inverter solutions [18].

The key findings from the theoretical analysis and the loss predictions are:

- The requirements can be met with very different solutions.
- Silicon IGBT devices have to be used in a three-level circuit topology, since they cannot be operated at 60 kHz efficiently.
- Using wide band gap devices, the requirements can be met with a simple two-level topology, which gives a large potential for increased power density.
- Although the switching frequency needs to be high, high efficiency can be reached.

2.3. Design of Power Stage Prototypes

For a practical evaluation of different discrete power devices and a metrological validation of the loss calculation algorithm inverter, power stage prototypes are designed, built and set into operation in a test bench.

Drive inverter power stage prototypes are designed, built and set into operation in a test bench for a practical evaluation of different discrete power devices and a metrological validation of the loss calculation algorithm. The used components, the design and especially the PCB layouts are kept as similar as possible for the different power devices to have the best possible comparability. Therefore, the main differences between the individual prototypes can be found in the PCB layout in the direct environment of the power devices, the integration of different device packages and the thermal connection to the cold plate.

Figure 6 shows two of the prototypes, one using surface mount devices (D^2PAK), the other using through hole devices (TO-247). On both prototypes, two devices are connected in parallel for each switch position resulting in a total number of 12 discrete devices per inverter. The easy manufacturing process using surface mount devices comes with some challenges in terms of thermal management, since the device must be cooled through the PCB. This is to be optimised not only for its electrical properties like its low inductance commutation loop and small parasitic capacitances at the load terminals but also for its low thermal resistance from the power devices on top of the PCB to the cold plate on its bottom.

Figure 6. Power stage prototypes using D^{2}PAK (**left**) or TO-247 (**right**) device packages.

In general, wide band gap devices show fast switching behaviour and steep voltage gradients. This is advantageous in terms of switching losses but can be critical in terms of electromagnetic interferences (EMI). To avoid self-EMI issues the gate drivers and their power supplies are especially designed for a high common mode rejection rate (CMR). For future application, EMI and voltage overshoot at the motor terminals are not expected to be a major issue, since the drive inverter will be integrated very closely to the electrical machine with a completely closed aluminium housing. Therefore, the conducted EMI on the DC power system feeding the inverter is the only challenge to be addressed in a future investigation.

2.4. Thermal Optimisation

During a thermal optimisation process, two different designs using surface mount power devices are developed and compared with a conventional design using TO-247 devices. The initial PCB design for D^{2}PAK devices uses a FR4 based PCB with eight layers of copper, 70 µm each. The area under the tab of the power devices and the nearby surroundings is completely filled with an optimised pattern of thermal vias according to IPC 4761 type VII "filled and capped". This means the vias are filled with a special epoxy plugging and capped with copper to increase the thermal conductivity. The complete board is mounted to a liquid cold plate and electrically isolated using an appropriate thermal interface material (TIM). An evenly distributed mechanical pressure on the PCB and the TIM is of high importance for this kind of construction.

The resulting total thermal resistance R_{th} for every single device between the junction and coolant is calculated to be about 2.9 K/W. Different measurements show a slightly higher value of about 3.3 K/W, which is about twice the thermal resistance of a TO-247 device directly mounted to the same cold plate using the same TIM.

For the second design using D^{2}PAK surface mount power devices, an integrated metal substrate (IMS) PCB is used. It consists of a massive 1.5 mm aluminium core, a thin organic insulator with high thermal conductivity and a single structured copper layer on top. Figure 7 shows a designed half bridge power module with four D^{2}PAK power devices mounted on a high-performance liquid cold plate. Figure 8 shows a cross section of the resulting power stage prototype with the cold plate, the IMS PCB and the main FR4 PCB with gate drivers and DC link.

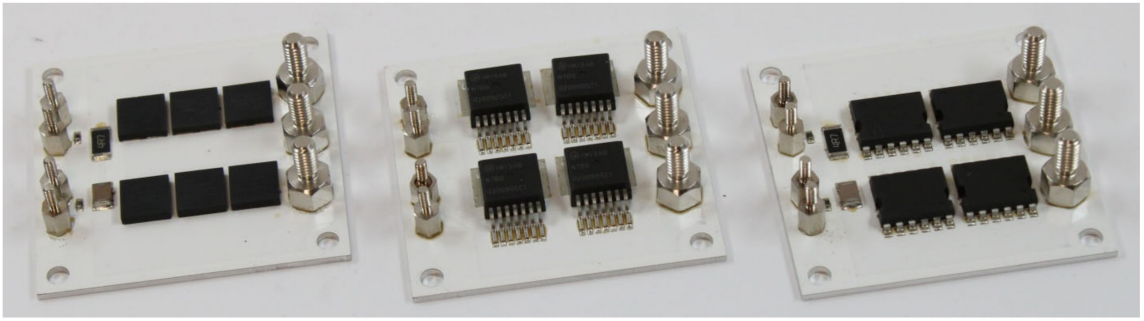

Figure 7. Half bridge power modules on IMS PCB, left to right: PQFN88, D^{2}PAK, CCPAK1212.

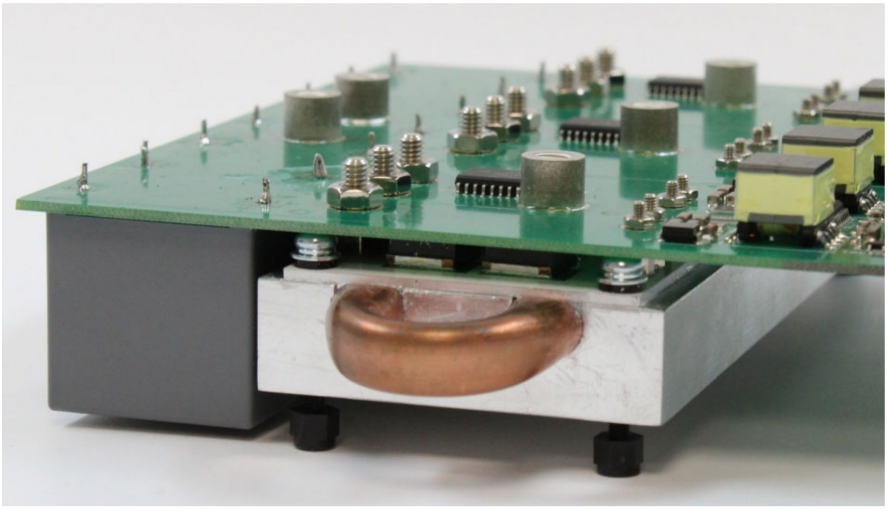

Figure 8. Thermally optimised inverter prototype.

Again, this novel design is thermally characterised. The total thermal resistance from junction to coolant is calculated to be only 1.0 K/W. Measurements show up a value of 1.5 K/W, which is similar to a design using TO-247 devices. A detailed analysis of the single thermal resistances shows that the use of thermal grease between the IMS and the cold plate instead of an electrically isolating pad has the largest impact on the total R_{th}. This is possible thanks to the internal electrical insulation of the IMS PCB.

3. Efficiency Analysis

Besides the thermal evaluation and optimisation of the power stage designs, the determination of the resulting power losses under typical operating conditions is a main task of the investigations. This is performed by electrical power measurements in a drive inverter test bench. Due to the high switching frequency, very fast switching transients and the high expected efficiency, these measurements come along with a couple of significant challenges that need to be addressed by appropriate measures.

In this section the realised measurement setup and selected test bench components are described. Afterwards, measurement results of a three-level IGBT inverter design and multiple two-level wide band gap inverter prototypes are presented and discussed.

3.1. Measurement Setup for the Efficiency Analysis of Different Prototypes

In the test bench the inverters are supplied using a high-performance DC power supply. An adjustable passive load is formed using a three-phase inductor and a high power load resistor array. A cooling system with adjustable coolant temperature and flow rate is used to realise different environmental conditions according to the application's requirements. The basic arrangement of these different components is shown in Figure 9.

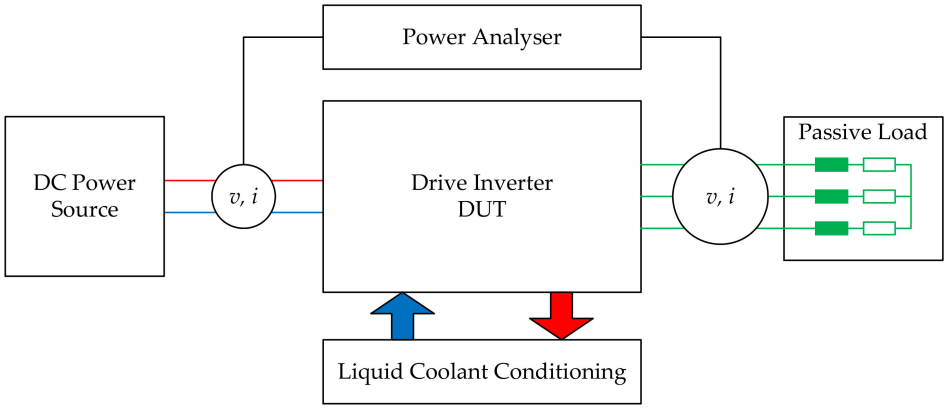

Figure 9. Inverter test bench scheme.

Since the power stage prototypes do not include control electronics, the switching signals for the gate drivers and power devices are generated by an external microcontroller circuit. A conventional symmetrical space vector modulation with a fixed modulation index is used to create a symmetrical three-phase system with constant voltage and frequency in each individual steady state operating point. Thanks to a good linearity of the passive load, the resulting phase currents are also symmetrical and sinusoidal even without current control.

Thermal supervision of the inverter prototypes and their power devices is realised using applied thermocouple sensors and infrared thermographical observation. The switching speed and voltage overshoot behaviour of the power semiconductor devices is permanently monitored using a high bandwidth oscilloscope.

The most relevant electrical measurements serve the determination of power and losses. A high precision power analyser Yokogawa WT3000 and high bandwidth and high precision current sensors Danisens DS200 are used to measure both input and output electrical power. Especially for the AC output power measurement at a high switching frequency high quality equipment is needed and care must be taken in setting up the measurement parameters.

3.2. Measurement Results of the Reference Design

As a first device under test, a drive inverter that realises the reference design with three-level T-type half bridges using 650 V/1200 V silicon IGBT technology is operated in the test bench. For this inverter, measurement data for a complete efficiency map are collected. The results are shown in Figure 10. The inverter is operated at 400 V DC and a switching frequency of 30 kHz.

In the previously defined full load static operating point OP (2) at 42 A output current the measured efficiency is about 97.1%. Based on the modelling and loss estimation, an optimal efficiency of 97.7% was expected. The difference can be explained by additional losses in the DC link, the implemented filter elements, connectors and slightly increased switching losses of the power devices. Nevertheless, the measurement prooves a successful setup of the test bench components and good consistency of the loss estimation method and the practical evaluation.

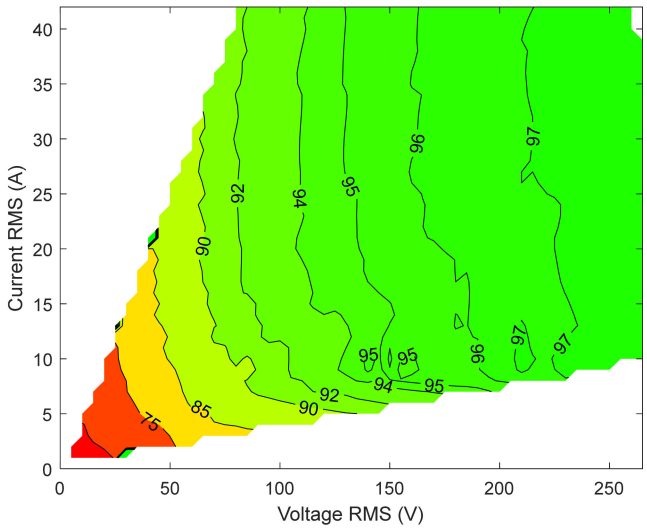

Figure 10. Measured efficiency map of the reference design (three-level NPC T-type, Si IGBT) [18].

3.3. Measurement Results of the Wide Band Gap Power Stage Prototypes

In the next step the developed power stage prototypes using different wide band gap power devices in a simple two-level B6 inverter topology are operated in the test bench. At first, the switching behaviour, switching speed and voltage overshoot characteristics are investigated and tuned by adjusting the respective gate resistors. Unfortunately, not all prototypes can be operated successfully. Especially the selected GaN devices in cascode configuration show some difficulties in parallel operation as they tend towards massive ringing and insufficiently damped oscillations. Finally, the five configurations listed in Table 3 can realise stable operation and perform the efficiency measurements. Compared to the other devices, the 650 V silicon carbide MOSFET is tuned to a lower switching speed due to the small breakdown voltage safety margin.

Table 3. Successfully operated power stage prototype device configurations.

Devices	Description	Gate Resistance (Ω)	Voltage Gradient (V/ns)	
(Always Two in Parallel)	**(Per Device)**	**(For Two Devices)**	**Rising**	**Falling**
SCTH100N65G2-7AG	SiC 650 V, 20 mΩ, D^2PAK	2.2	15.8	−14.4
NVBG020N090SC1	SiC 900 V, 20 mΩ, D^2PAK	1.5	28.3	−36.2
C3M0030090K	SiC 900 V, 30 mΩ, TO-247	2.7	32.4	−36.2
IMZ120R030M1H	SiC 1200 V, 30 mΩ, TO-247	2.2	34.5	−41.1
TP65H035WSQA	GaN 650 V, 35 mΩ, TO-247	15 (+3.9 per device)	37.1	−37.7

During the efficiency measurements it can be recognised that the common mode capacitance of the passive load has a significant impact on the inverter losses at the investigated switching frequencies in the range from 60 kHz to 120 kHz. Therefore, it is measured separately using a RCL meter and taken into account in the loss estimation. Figure 11 shows the results of the measurements and the improved calculations, both for OP (2) at 60 kHz switching frequency for the five prototypes listed in Table 3.

It can be recognised that the losses are underestimated for all inverter prototypes. These additional losses may again be caused by the DC link, connectors and PCB resistances and capacitances that are not taken into account in the simulations. The difference between simulated and measured losses is in the range from 9% to 13% for the four different SiC devices.

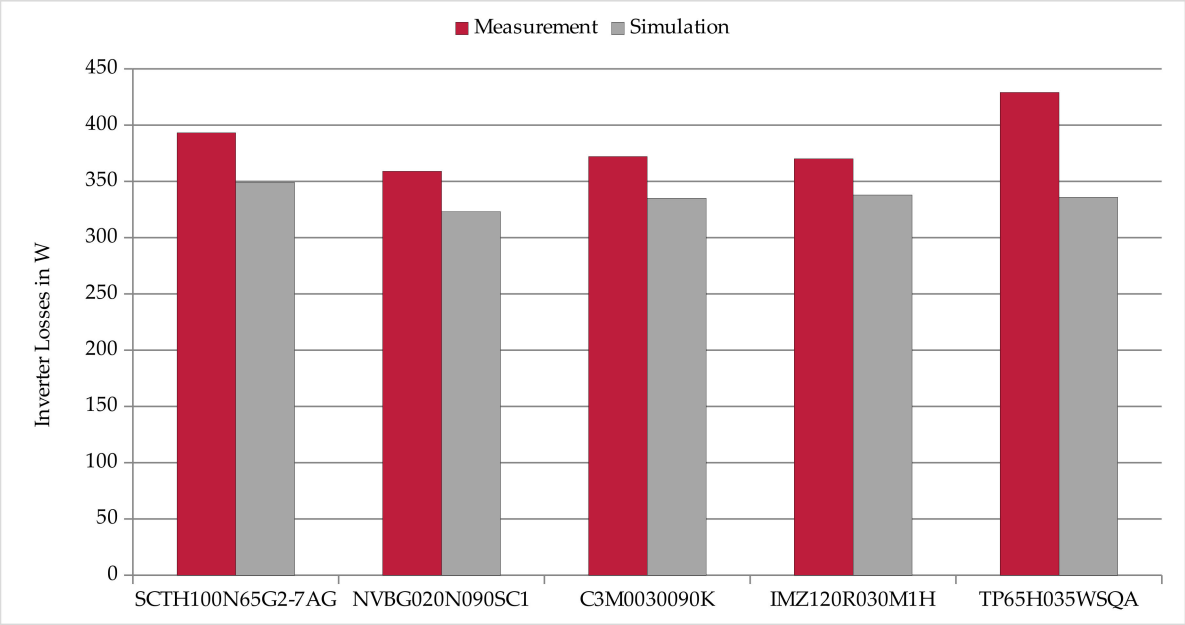

Figure 11. Inverter power losses determined by measurement and simulation for OP (2) at 60 kHz.

For the GaN design, with 28%, the deviation between simulated and measured losses is significantly larger. To a certain extent, it is expected to be caused by an additional snubber circuit that is included in the design to improve the stability of the switching behaviour. Furthermore, additional losses seem to be caused by a still non-optimal switching behaviour and ringing of the parallelised devices. The leaded TO-247 package, that is not well suited for very fast switching devices, also contributes to these problems.

The key findings from the measurement-based investigation of the inverter efficiency are:

- Silicon carbide MOSFETs can meet the requirements of this application and are easy to parallel.
- Switching frequencies of up to 120 kHz can be reached.
- The loss prediction is fairly accurate.
- The possible inverter efficiency is highly dependent on the load and its parasitic capacitance.
- Surface mount devices have benefits in terms of size, parasitic inductance and ease of assembly, but good care must be taken designing an efficient cooling structure.
- Certain GaN devices are difficult to operate in parallel, the TO-247 package is not well suited for these devices.

4. Reliability Analysis

New technologies for semiconductor materials, for example, wide band gap devices, offer many advantages in power density and weight. However, regarding lifetime performance considerations, they are relatively unknown. Semiconductors and their packaging technologies are tested with different tests. To find lifetime models concerning load cycles of a component, typically, power cycling tests must be performed. For resilient lifetime estimation, a large data basis consisting of many power cycling results is necessary. The number of published test results of discrete wide band gap devices is very low [22–25]. A power cycling test of one semiconductor can take several weeks or months depending on the test criteria.

The lifetime of power electronics and their components in the drive train of an electric vehicle or a hydrogen vehicle should achieve at least the same lifetime as a vehicle with

a combustion engine, which might be 5000 to 8000 operating hours [26]. The battery of an electric vehicle has to last 160,000 km [27]. Depending on the vehicle's medium speed of 30 km/h to 50 km/h, operating hour requirements between 3000 h and 5000 h can be derived. With 200 accelerations per hour the component has to last 6×10^5 to 1×10^6 cycles. Each cycle represents one temperature swing of the semiconductor chip.

In the following sections, lifetime calculations for discrete wide band gap power semiconductors are developed and presented. They are performed to check the different devices' suitability for the specific application of a high speed drive inverter.

4.1. Lifetime Estimation Process

Often, the lifetime estimation is the last step in the design process of a device and it is based on many factors. Based on [28], a similar estimation process is used (see Figure 12). Depending on the requirements, the voltage class or the number of output voltage levels has to be chosen. Then, the number of components in parallel has to be set. After this, the available technologies, packages and cooling technologies can be chosen. Depending on the calculated operating hours, recursive loops have to be done. For example, the number of parallel components is set higher, or the cooling has to be changed until the desired results can be achieved.

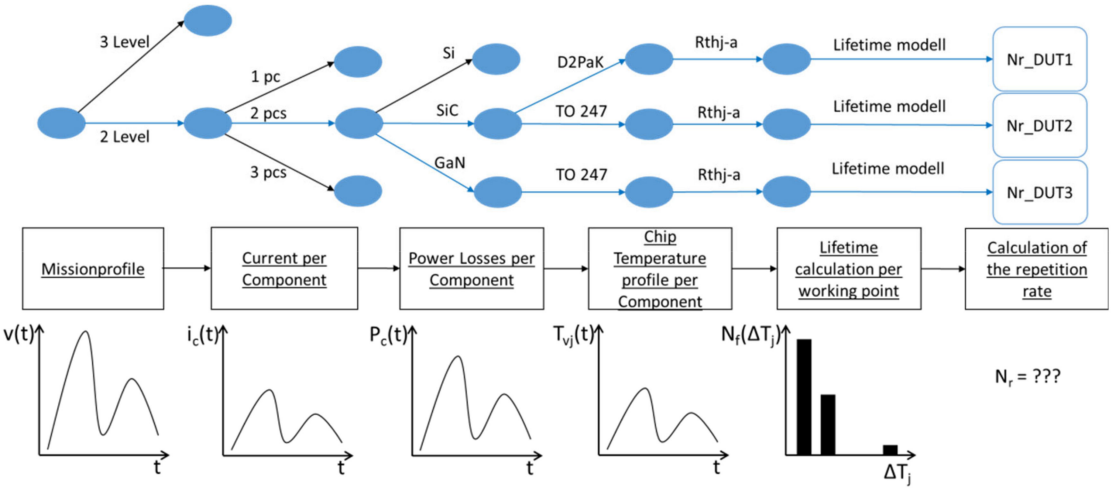

Figure 12. Lifetime estimation method.

Here, the lifetime estimation is done for a two-level inverter with two components in parallel (2 pcs) with ideal current distribution. This is the preferred configuration identified in the previous sections. Either silicon carbide (SiC) MOSFETs or gallium nitride (GaN) cascodes are used. The components have discrete packages like TO-247 and D^2PAK with different thermal resistances between the case and cold plate (ambient).

Liquid cooling is very common in automotive applications. It efficiently limits the maximum junction temperature and guarantees a high power density. The calculations are done for most frequently used operating points (compare Table 2: OP (1) at 30 A and OP (3) at 60 A) and two different mission profiles.

The cycle number N_f of static operating points is calculated with the following equation that has been established for silicon devices over many years [29]:

$$N_f = A \cdot \Delta T_j^{\beta 1} \cdot \exp(\beta 2/(T_{jmin} + 273\,\mathrm{K})) \cdot t_{on}^{\beta 3} \cdot I_b^{\beta 4} \cdot V_C^{\beta 5} \cdot D^{\beta 6} \quad (1)$$

For the calculations, the common values for a standard IGBT power module listed in Table 4 are used, as no data for the discrete GaN or SiC components are available and the typical failure modes like bond wire cracks or lift offs are expected to be similar. Nevertheless, it is a rough estimation to get a first overview.

Table 4. Parameters and values used for the calculations with the CIPS08-Modell.

Parameter	Value	Explanation	Limits
A	2.03×10^{14}	Technology Factor	
ΔTj	variable, depending on the loss calculations	Temperature swing of the chip	45–150 K
Tjmin	25 °C	Minimal Temperature of the chip	20–120 °C
ton	1 s	Pulse time	1–15 s
Ib	variable, divided by 3 [1]	Current per bond	3–23 A
Vc	variable, depending on the voltage class	Voltage class of the chip	600–3300 V
D	300 µm [2]	Diameter of the bonds	75–500 µm
β1	−4.416		
β2	1.258×10^3		
β3	−0.463		
β4	−0.716		
β5	−0.761		
β6	−0.5		

[1] Assumption for the number of bond wires is 3. [2] Assumption for the diameter of bond wires.

The limits are given by the parameters of the power cycling tests that have been done. The authors of [29] identified the parameters A and β1 to β6 by curve fitting of test results. For new technologies, they have to be adjusted.

Furthermore, it is assumed that all components are built up with three bond wires with a diameter of 300 µm, each. The bond wire current I_b should reach a maximum of 10 A_{rms}, because the number of devices in parallel is two and the maximum load current of the inverter is 60 A_{rms}. A bond wire lift off is expected to be the main failure mode, so the pulse time in power cycling tests is set to 1 s. For GaN cascodes, the inner structure is more complex since they are built using two different semiconductors.

Two different mission profiles are chosen for the dynamic stress calculations: One driving profile for the city (Figure 13) and one for the highway (Figure 14). Each profile has 3600 values and represents one operating hour.

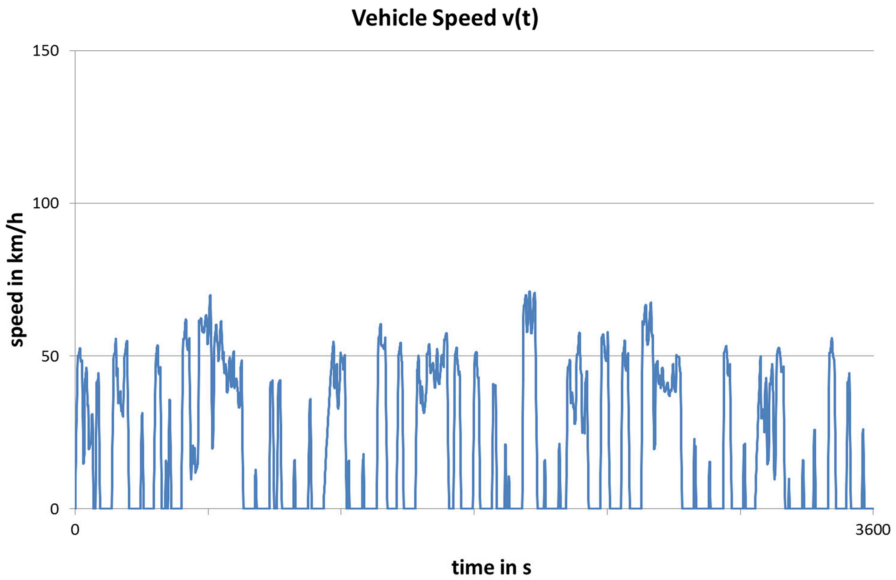

Figure 13. First mission profile of dynamic stress: City profile.

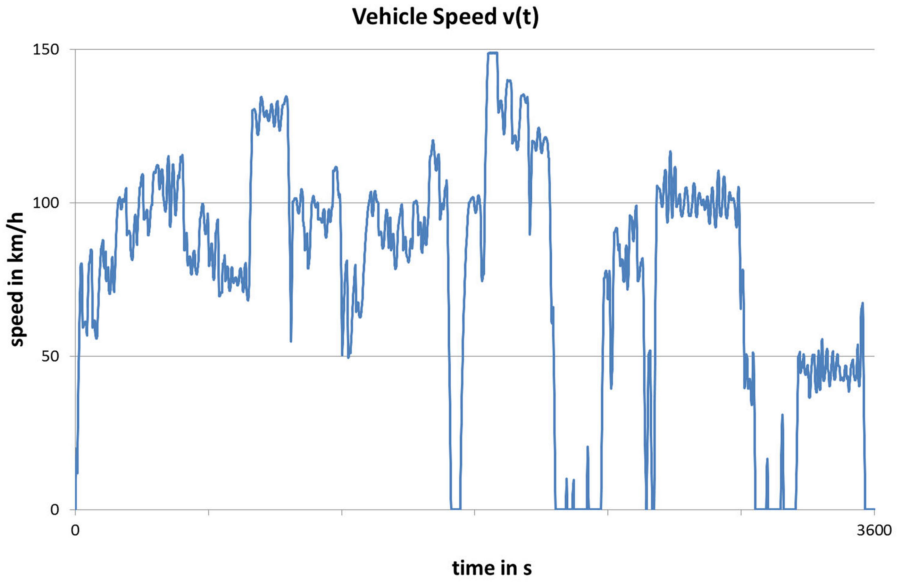

Figure 14. Second mission profile for dynamic stress: Highway profile.

The vehicle speed $v(t)$ is converted into the current per component $i(t)$. For every time step a loss calculation is done. Together with the individual thermal resistance of every component and the thermal resistance of the thermal foil and the cooling, the virtual junction temperature at every time step is calculated. The result is the temperature profile $T_{\mathrm{vj}}(t)$ of the chip temperature. This temperature profile is analysed with the rainflow algorithm which is explained in [30,31]. This gives a histogram with the numbers of different temperature swings. With the histogram and the following formula, the damage Q_i of each component is calculated [32]:

$$Q_i\left(\Delta T_j, T_{jmin}, t_{on}, I_b, V_C, \mathrm{D}\right) = \frac{N_i\left(\Delta T_j, T_{jmin}, t_{on}, I_b, V_C, \mathrm{D}\right)}{N_{fi}\left(\Delta T_j, T_{jmin},\ t_{on}, I_b, V_C, \mathrm{D}\right)} \tag{2}$$

Q_i is the damage, N_i is the number of cycles from the mission profile, N_{fi} is the maximum number of cycles calculated for this operating point with Formula (1). The component is expected to fail when the damage Q_i reaches the value 1.

To get the operating hours of the inverter, the reciprocal value of the damage Q_i is used as shown in Formula (3). This is the repetition rate N_r of the mission profile [33]:

$$N_r = \frac{1}{\sum_{i=1}^{n} Q_i} = \frac{1}{\left(\frac{N_1}{N_{f1}} + \ldots + \frac{N_n}{N_{fn}}\right)} \tag{3}$$

4.2. Lifetime Estimation

The calculations are done for most frequently used operating points at 30 A and 60 A, a constant cos(ϕ) = 0.9 and two different mission profiles. Measurements of the thermal path of the used discrete components have shown that, for the thermal resistance from case to ambient ($R_{\mathrm{th,c\text{-}a}}$), values of about 1.5 K/W and lower can be achieved. For the following calculations the value $R_{\mathrm{th,c\text{-}a}}$ = 1.5 K/W is used. A constant cooling temperature T_{coolant} = 25 °C is assumed. A list of the different semiconductor components that were considered for the inverter is shown in Table 5.

Table 5. Component overview for the lifetime estimations with their most relevant parameters.

No.	Component	Voltage	Current	Technology	Package	$R_{th,j-c}$
1	GAN063-650WSA	650 V	34.5 A	GaN	TO-247	1.05 K/W
2	TP65H035WSQA	650 V	47.2 A	GaN	TO-247	0.8 K/W
3	GAN041-650WSB	650 V	47.2 A	GaN	TO-247	0.8 K/W
4	SCTH100N65G2-7AG	650 V	95 A	SiC	D^2PAK	0.42 K/W
5	SCTW100N65G2AG	650 V	100 A	SiC	TO-247	0.42 K/W
6	C3M0065090J	900 V	35 A	SiC	D^2PAK	1.1 K/W
7	E3M0065090D	900 V	35 A	SiC	TO-247	1.0 K/W
8	C3M0030090K	900 V	63 A	SiC	TO-247	0.84 K/W
9	NTBG020N090SC1	900 V	112 A	SiC	D^2PAK	0.31 K/W
10	IMZ120R030M1H	1200 V	56 A	SiC	TO-247	0.51 K/W
11	SCT3030KLHR	1200 V	72 A	SiC	TO-247	0.34 K/W
12	SCT3022KLHR	1200 V	95 A	SiC	TO-247	0.27 K/W

4.2.1. Estimated Lifetime for Static Operating Points

The switching frequency and the load current are varied, which influences the power losses. The power losses influence the temperature swings of the virtual junction. The thermal resistance from case to ambient influences the maximum value of the virtual junction temperature. Some results for the components listed in Table 5 (No. 1–12) are shown in Figures 15–17.

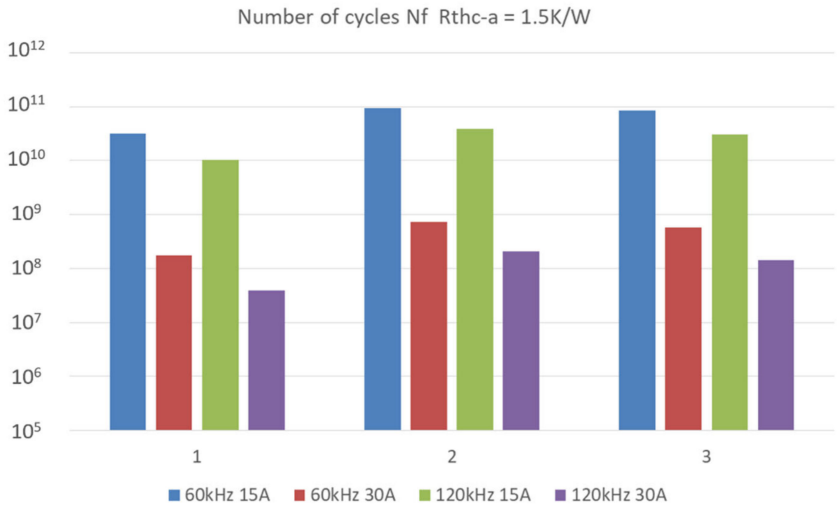

Figure 15. Number of cycles of GaN components in TO-247 package with different operating points, $R_{th,c-a}$ = 1.5 K/W, components 1, 2 and 3 with $R_{th,j-c}$ = 1.05 K/W and $R_{th,j-c}$ = 0.8 K/W.

Figure 15 shows the number of cycles of GaN components in the TO-247 package. The highest number of cycles is reached at 60 kHz and 15 A, which is the lightest load. The lowest number of cycles for each component is at 120 kHz and 30 A, which is the highest load. It can be seen that changing the load current from 15 A to 30 A has a bigger influence on the lifetime than changing the switching frequency from 60 kHz to 120 kHz.

The components are all in the same voltage class. The current rating, the on-state resistance $R_{ds,on}$ and the thermal impedance $R_{th,j-c}$ of component 1 are different from components 2 and 3. This leads to higher temperature swings of component 1 and a lower number of cycles for every operating point.

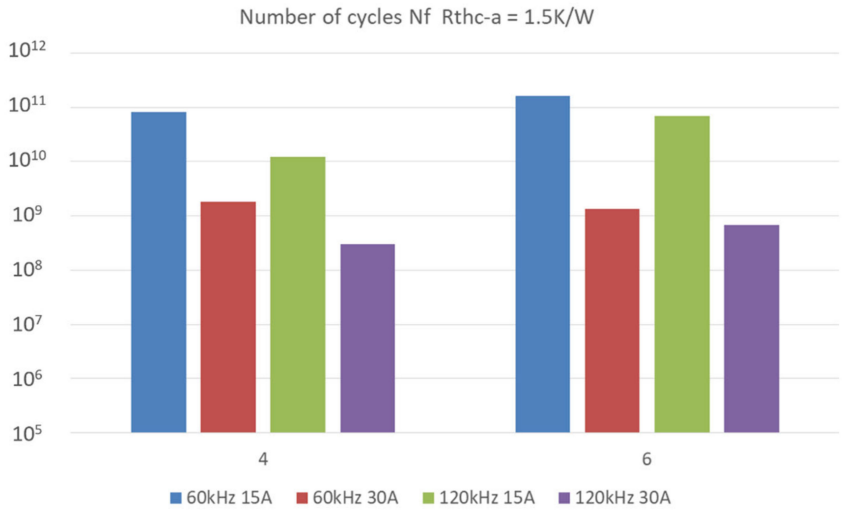

Figure 16. Number of cycles of SiC components in D^{2}PAK package with different operating points, $R_{th,c\text{-}a}$ = 1.5 K/W, components 4 and 6 with $R_{th,j\text{-}c}$ = 0.42 K/W and $R_{th,j\text{-}c}$ = 1.1 K/W.

Figure 16 shows the number of cycles of SiC components in D^{2}PAK. The components have different voltage classes, different current ratings, different on-state resistance $R_{ds,on}$ and different thermal impedances $R_{th,j\text{-}c}$. The lifetime of these components is similar for 60 kHz. At 120 kHz the cycle number of component 6 is higher.

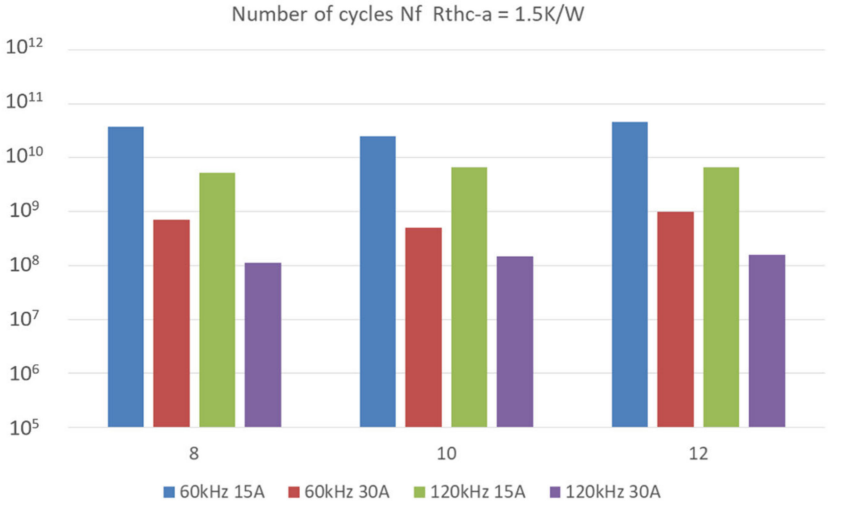

Figure 17. Number of cycles of SiC devices in TO-247 package with different operating points, $R_{th,c\text{-}a}$ = 1.5 K/W, components 8, 10 and 12 with $R_{th,j\text{-}c}$ = 0.84 K/W, $R_{th,j\text{-}c}$ = 0.51 K/W and $R_{th,j\text{-}c}$ = 0.27 K/W.

Figure 17 shows SiC components in TO-247 package. They belong to different voltage classes what means that the thickness of the dies is different. The current rating, the on-state resistance $R_{ds,on}$ and the thermal impedance $R_{th,j\text{-}c}$ are also different, so the power losses and the cooling are different. However, all togethers the values of the temperature swings of the junction are about the same. The number of cycles is similar for these components.

4.2.2. Estimated Lifetime for Mission Profiles

The lifetime estimation for variable stress of the components is done with two different mission profiles, a city mission profile (Figure 13) and a highway mission profile (Figure 14), which shall cover most of the use cases. The calculations are done with switching frequencies of 60 kHz and 120 kHz. The results for all components are shown in Figures 18 and 19.

The red lines indicate the required number of cycles for a medium speed of 30 km/h and 50 km/h and 3000 to 5000 operating hours.

The repetition rates N_r for the city profiles (Figure 18) are relatively high because the stress of the components is relatively low. Component 6 reaches the highest repetition rates, component 1 and 7 the lowest. Component 1 has higher power losses and component 7 has higher losses and a higher thermal resistance than the other components. The rainflow algorithm has detected 138 temperature swings for this city mission profile. All components are suitable for the inverter and this mission profile.

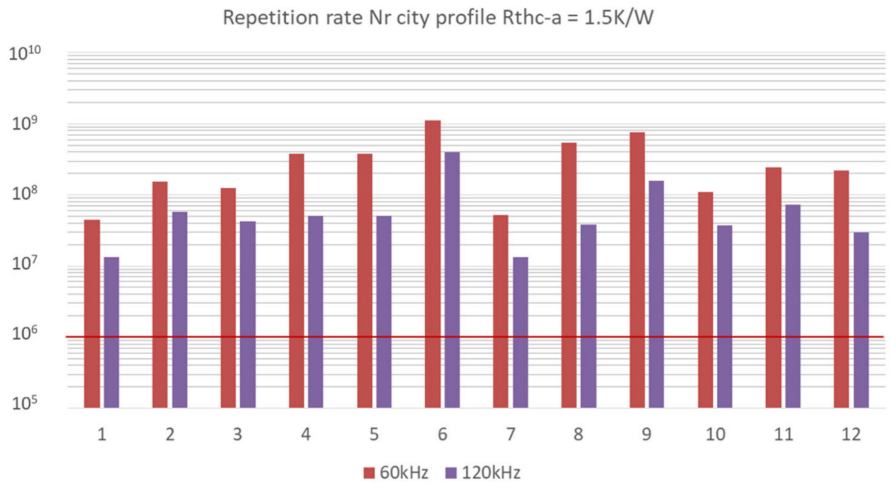

Figure 18. Repetition rate for a city mission profile, components 1 to 12.

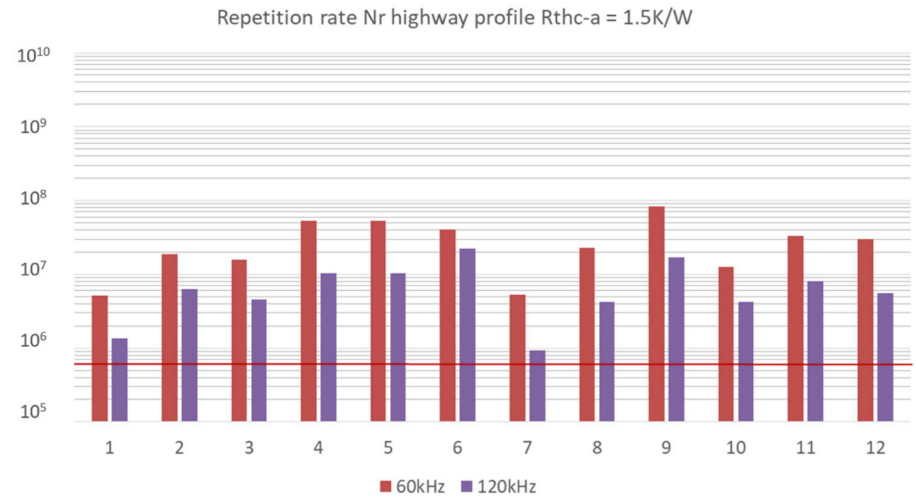

Figure 19. Repetition rate for a highway mission profile, components 1 to 12.

The repetition rates N_r for a highway profile (Figure 19) are lower than for the city profile. The stress for the components is higher because, at some time steps of the mission profile, the maximum load current is reached. Components 6 and 9 reach the highest repetition rates, component 1 and 7 the lowest. The rainflow algorithm detected 170 temperature swings for this highway mission profile. All components are suitable for the inverter and this mission profile.

4.3. Discussion of the Lifetime Estimation

A method for lifetime estimation for power electronics was presented. The lifetime estimation is based on a multitude of parameters. The parameters of the lifetime model have to be adjusted for SiC and GaN devices. That is why the presented results are a

first estimation. The needed power cycling tests are still ongoing. The internal structure of the components make the lifetime estimation more complicated, because complex structures might have more complex failure modes. Tolerances of the inner structure of the components or in the thermal resistance are neglected but can also result in a higher junction temperature and a shorter lifetime. The number of bond wires and the bond wire diameter might be different for each component. A temperature profile for the ambient temperature could be added to get a more realistic temperature profile of the junction temperature. Dynamic stress with thermal capacities might lead to harsher stress and a shorter lifetime. The used mission profiles are exemplary and not representative like WLTP or NEFZ. In the future, lifetime aspects can be integrated in the dimensioning process.

The presented lifetime estimation shows that a lower switching frequency and the resulting lower switching losses are a better choice regarding lifetime performance. Nevertheless, the results for 120 kHz still show sufficient repetition rates for the use in the target application. A good cooling mechanism is essential to get the best performance as well as an acceptable lifetime.

The key findings from the reliability analysis are:

- Since the connecting technologies of today's wide band gap devices are similar to conventional silicon IGBT devices, the same failure mechanisms are expected and the same formulas can be utilised.
- The number of possible cycles before a failure depends directly on the devices' losses and temperature swings. Therefore, it decreases with a higher current and higher switching frequency.
- Better cooling increases the number of possible cycles.
- Using the rainflow algorithm, an expected repetition rate for different mission profiles can be calculated.
- All devices are expected to meet the required reliability, even at a switching frequency of 120 kHz. Nevertheless, a design with low losses and good cooling should always be preferred.

5. Conclusions

In this article, recent research results on the design of a high performance, high speed drive inverter are presented. The given application of an electrical turbo compressor for automotive fuel cell systems gives challenging requirements like a high switching frequency as well as high efficiency and power density goals. Based on both simulations and measurements, it can be stated that solutions using wide band gap power semiconductor devices in a simple two-level inverter circuit can outperform a more complex three-level circuit of silicon IGBT devices in all of the defined evaluation criteria. The use of discrete surface mount power devices is the preferred solution for cost efficient mass production. It is shown that IMS PCB can help to reach low thermal resistances for these devices as well.

In addition to the device comparisons based on loss estimations, efficiency measurements and thermal investigations also comprehensive research on the lifetime and reliability of wide band gap power devices is performed and presented. It is shown that the selected devices are able to reach sufficient repetition rates and operating hours even at the highest expected switching frequency and under different mission profiles and load conditions. The parameterised lifetime models are currently validated by ongoing power cycling measurements.

All in all, the presented research covers many important aspects of future power electronics design processes. In particular, the consequent use of calculation methods, measurement equipment and lifetime models in the complete tool chain will be of increasing importance. With the maturing of SiC and GaN devices, design methods that can be used independently from a specific power device technology for all current and future devices that allows an easy and fair comparison of different devices for a specific application will be an urgent need.

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