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Comprehensive Evaluation and Optimization of Level Count for Cascaded H-Bridge Multilevel Inverters with Carrier-Phase-Shifted PWM

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Abstract

Cascaded H-bridge (CHB) multilevel inverters are pivotal in high-power applications, such as renewable energy subsystems and motor drives, due to their superior modularity and harmonic performance. However, selecting the optimal number of levels remains a complex engineering trade-off between power quality, switching losses, and system complexity. This study presents a systematic investigation into CHB inverters ranging from three to twenty-one levels under carrier-phase-shifted sinusoidal pulse width modulation (CPS-SPWM) control. A detailed MATLAB/Simulink framework in version R2023a was established, incorporating a zero-order hold (ZOH) data synchronization protocol and parameterized macro-model MOSFETs to accurately quantify total harmonic distortion (THD) and individual switching energy dissipation. To evaluate the efficiency–quality equilibrium, a novel comprehensive evaluation index, the performance-to-loss ratio (PLR), is proposed. Simulation results indicate that while THD improves significantly with higher level counts, the marginal gains diminish beyond the 13-level configuration. Utilizing the PLR framework, the nine-level configuration is identified as a local optimum for cost-sensitive modularity, whereas the twenty-one-level setup provides the global optimum for high-performance scenarios where spectral purity is paramount. Accordingly, this proof-of-concept study provides a quantitative roadmap for designers and experimentalists to navigate the complex design space of multilevel inverters, enabling optimal allocation of hardware resources toward the net-zero vision while guiding future experimental efforts away from costly, exhaustive hardware characterization.

Keywords: cascaded H-bridge; multilevel inverter; carrier-phase-shifted PWM; MOSFET switching loss; performance-to-loss ratio; power quality; motor drives; power electronics

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1. Introduction

Power electronics [1–4] establishes a fundamental link between electrical and electronic engineering, specifically within the domain of switching techniques [5–7], encompassing both hardware architectures [8–10] and control methodologies [11,12]. Instead of employing dissipative linear methods, such as resistive regulation, to manage power flow, modern power electronics utilizes semiconductor switches (e.g., MOSFETs [13] and IGBTs [14]) to turn power on and off at high frequencies. Built upon this foundational switching paradigm

and driven by the global imperative of carbon neutrality, multilevel inverters (MLIs) [15] have become pivotal in modern medium-to-high voltage power electronic systems. As macro-architectures of energy networks evolve toward cloud-edge-device collaborative paradigms [16], MLIs serve as the critical energy routing hubs. As conceptualized in Figure 1, they play an indispensable role in bridging decentralized DC sources—such as grid-connected renewable energy subsystems (solar photovoltaics and wind power [17]) and aerospace DC buses—with dynamic AC loads, including advanced motor drives [18] and electric vehicle (EV) propulsion systems [19,20].

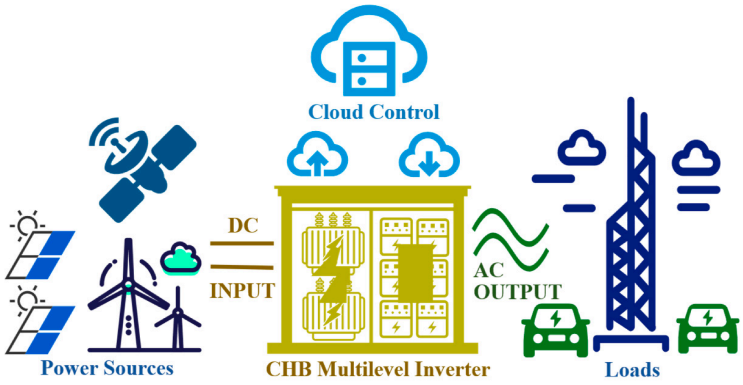


Figure 1. Macro-architecture of modern energy conversion systems, illustrating the pivotal role of multilevel inverters in bridging renewable energy subsystems and advanced motor drives.

Compared to conventional two-level inverters [21], MLIs synthesize a staircase output voltage waveform by combining multiple lower DC voltage levels. This fundamental structural shift provides significant advantages. As comparatively illustrated in Figure 2a, the conventional two-level topology subjects the semiconductor switches to the full DC-link voltage, resulting in extremely steep dv/dt gradients during switching transitions. This severe dv/dt stress accelerates the degradation of motor winding insulation and introduces significant common-mode currents [22]. By contrast, the refined staircase waveform of MLIs drastically reduces the voltage step size (ΔV), which fundamentally suppresses the dv/dt stress. Consequently, this yields a substantial reduction in high-frequency electromagnetic interference (EMI) emissions (Figure 2b) and superior total harmonic distortion (THD) profiles, while eliminating the need for bulky, expensive step-up transformers or heavy passive filters. These inherently translate to lower cost and reduced footprint, guiding the power electronics industry toward sustainability.

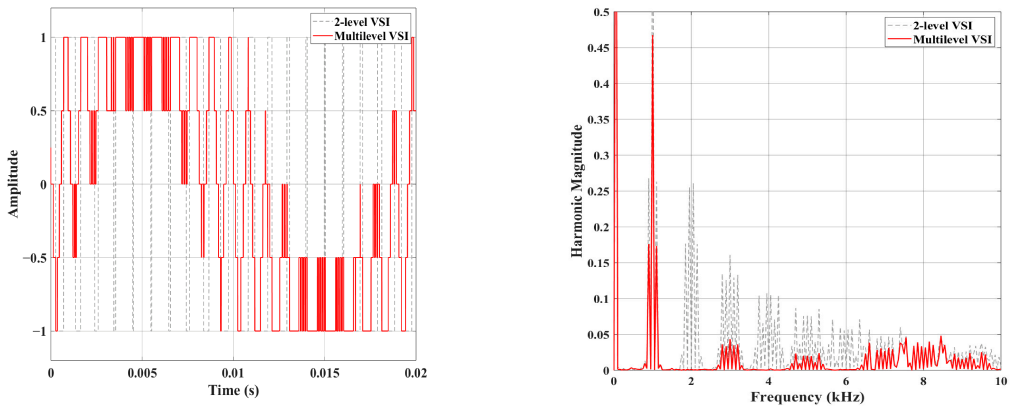
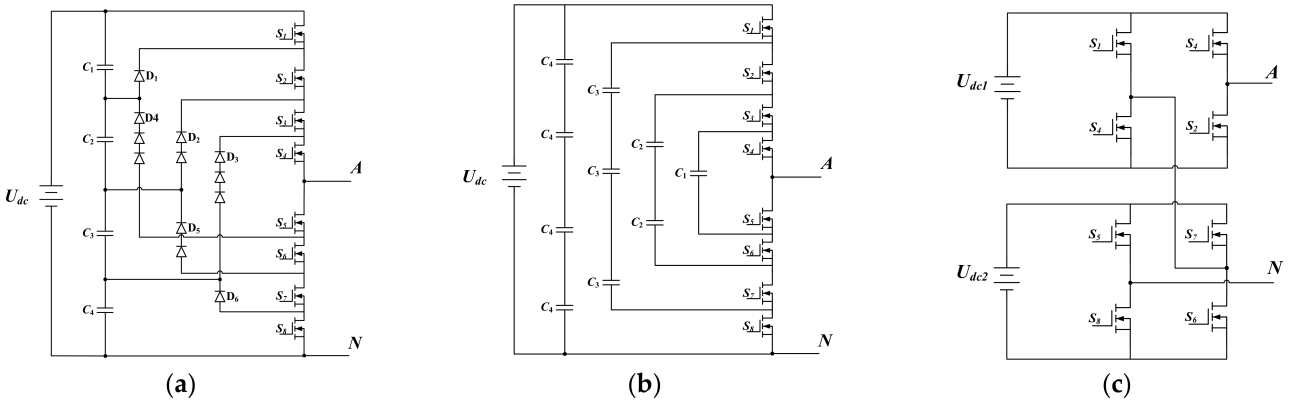


Figure 2. Comparative illustrations of conventional two-level and multilevel voltage source inverters (VSIs): (**a**) time-domain voltage waveforms highlighting the dv/dt stress reduction; (**b**) conceptual frequency-domain spectrum demonstrating the mitigation of high-frequency EMI.

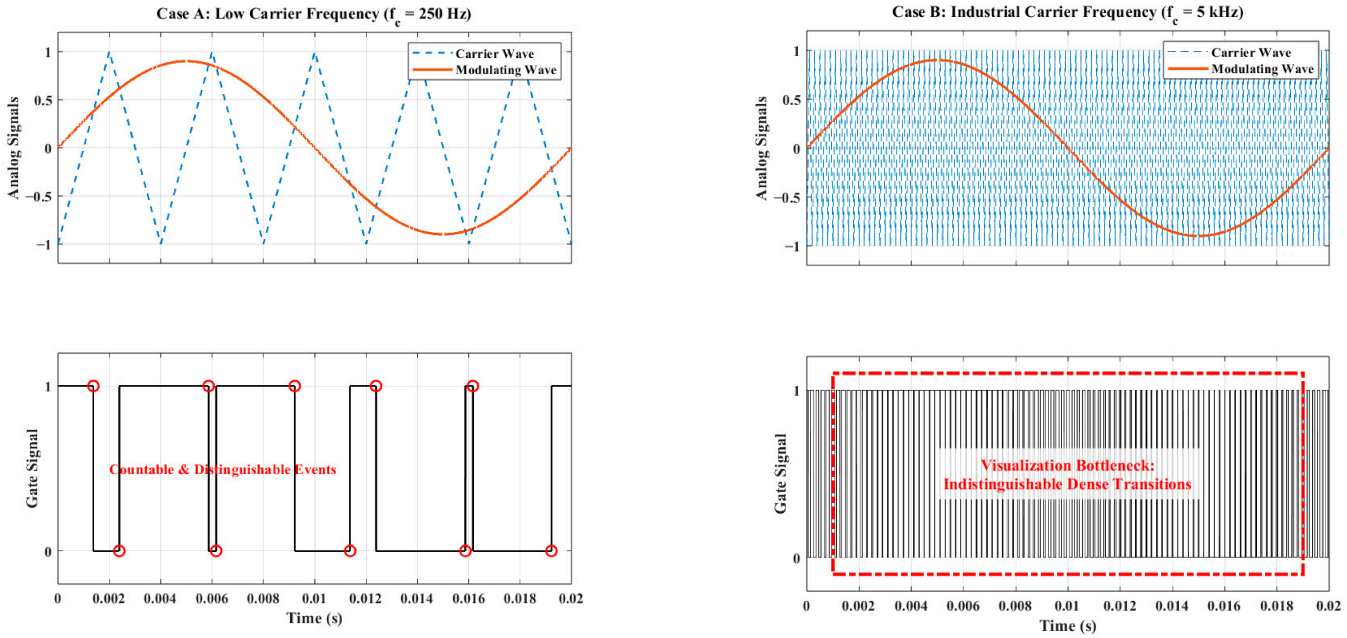
To physically realize these high-resolution multilevel waveforms, various topologies have been proposed. Figure 3 presents a structural comparison of the three classic MLI architectures. The neutral point clamped (NPC) [23,24] and flying capacitor (FC) [25] topologies rely on passive components (clamping diodes and flying capacitors, respectively) to synthesize intermediate voltage levels. However, as the required number of levels increases, these topologies suffer from exponential growth in hardware complexity and severe capacitor voltage balancing challenges. Among them, the cascaded H-Bridge (CHB) topology [26,27] stands out due to its exceptional modularity, high reliability, and linear scalability. By utilizing completely independent DC sources, CHB inverters entirely bypass the voltage balancing bottlenecks inherent in NPC and FC topologies. To effectively drive the metal-oxide-semiconductor field-effect transistors (MOSFETs) within the CHB architecture, carrier-phase-shifted sinusoidal pulse width modulation (CPS-SPWM) [28,29] is widely adopted as a core control strategy. By comparing a single modulating wave with multiple phase-shifted triangular carriers, CPS-SPWM effectively multiplies the equivalent output switching frequency, thereby significantly improving harmonic performance [30] without compromising the energy efficiency of individual MOSFETs.



(**a**) (**b**) (**c**)

Figure 3. Structural comparison of classic multilevel inverter topologies (exemplified with a 5-level configuration): (**a**) neutral point clamped (NPC); (**b**) flying capacitor (FC); and (**c**) cascaded H-Bridge (CHB).

Despite the well-documented advantages [31,32] of CHB inverters and CPS-SPWM, one of the critical unanswered questions in the field remains the optimum number of levels for practical industrial deployment. While increasing the level count monotonically improves the output power quality and decentralizes the thermal stress per cell, it simultaneously necessitates a linear increase in the number of active components and gate-drive isolation circuits. This escalating structural complexity [33] inherently amplifies the cumulative switching losses and introduces potential hardware failure points. Furthermore, accurately quantifying these switching losses—a prerequisite for solving this optimum-level puzzle and achieving reliable thermal management—is severely hindered by the "visualization bottleneck". As visually demonstrated in Figure 4, when the carrier frequency is relatively low, switching events are clearly distinguishable. However, as the carrier frequency increases to industrially relevant high frequencies (e.g., above 1 kHz), traditional timing diagrams become extremely dense blocks of ink. This makes it impossible to reliably identify individual switching transitions by manual or visual inspection, severely hindering precise switching count statistics and loss calculations. Conventional evaluation methods typically isolate THD or switching loss, failing to capture the holistic "system-level trade-off" required for modern cost-sensitive and high-performance applications.



(**a**) (**b**)

Figure 4. Demonstration of the "visualization bottleneck" in switching loss quantification: (**a**) at a low carrier frequency ($f_c = 100$ Hz), the intersection points and resulting gate transitions are clearly distinguishable and countable; (**b**) at an industrially relevant high carrier frequency ($f_c = 5$ kHz), the timing diagram degenerates into an indistinguishable dense block, rendering manual switching count statistics and direct loss observation unfeasible.

To bridge these research gaps, this study presents a comprehensive evaluation and optimization framework for CHB multilevel inverters ranging from 3 to 21 levels. The upper bound of 21 levels (i.e., cascading 10 H-bridge units per phase) is selected as a proof-of-concept ceiling, capturing the transition from diminishing returns in harmonic performance to escalating hardware complexity beyond this point. Given that experimental characterization of switching losses across multiple level configurations is technically demanding, time-consuming, and costly, this work introduces a simulation-driven framework that directly informs future experimental design. The main contributions of this paper are summarized as follows:

(1) A universal MOSFET switching count mathematical model under CPS-SPWM is derived and empirically validated through a novel proportional-scaling simulation methodology, effectively bypassing the high-frequency observability bottleneck.

(2) A detailed MATLAB/Simulink framework, incorporating non-ideal parameterized macro-models and a zero-order hold (ZOH) data synchronization protocol, is established to precisely quantify THD and individual transient switching energy dissipation across different level configurations.

(3) A multidimensional evaluation index, the performance-to-loss ratio (PLR), is proposed to mathematically penalize both harmonic distortion and hardware complexity. By applying the PLR framework, this research quantitatively identifies the nine-level configuration as a local optimum for economical modularity, and the twenty-one-level configuration as the global optimum for maximum spectral purity, providing a robust quantitative roadmap for the next generation of power converters.

Importantly, the proposed PLR-driven framework is not limited to simulation. By explicitly identifying which level configurations yield optimal trade-offs between performance and hardware complexity, it enables experimentalists to focus their efforts on the

most promising candidates (e.g., nine-level for economical designs, twenty-one-level for high-performance applications). This targeted approach bypasses the need for exhaustive experimental characterization of every possible level count—a process that is often impractical due to the high cost and technical difficulty of accurately measuring transient switching losses in multilevel inverters.

2. Materials and Methods

2.1. Theoretical Paradigms of CHB Multilevel Inverters and Boundary Condition Preservation

The cascaded H-Bridge (CHB) topology offers a modular alternative to traditional multilevel architectures by employing independent DC sources (as illustrated in Figure 5 for a representative 7-level configuration), achieving a linear scaling relationship with superior ease of control. From a mathematical perspective, the total output phase voltage U_{ab} of an N-cell cascaded inverter is the sum of the individual cell outputs. For a single-phase system with N cascaded units, each cell provides three discrete voltage levels ($+E$, 0, $-E$). Consequently, the maximum output voltage is NE, and the total number of phase voltage levels (L_{phase}) and the maximum possible number of distinct line-to-line voltage levels (L_{line}) in a star (Y) configuration are determined by (1) and (2), respectively:

$$L_{phase} = 2N + 1, \tag{1}$$

$$L_{line} = 4N + 1. \tag{2}$$

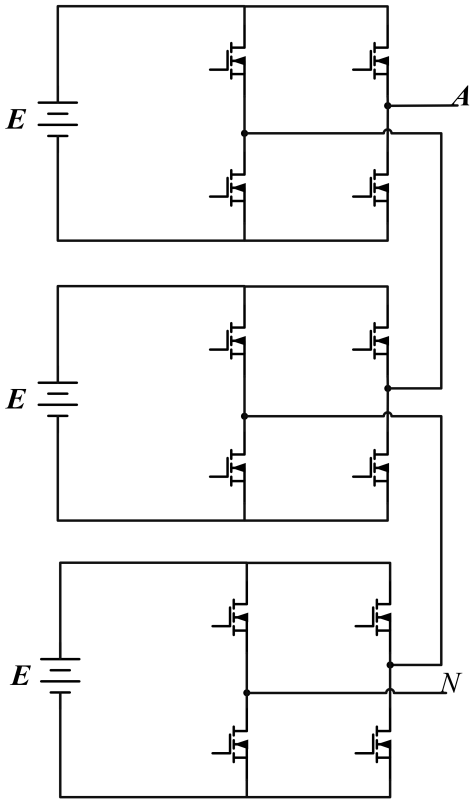


Figure 5. Circuit topology of a single-phase cascaded H-bridge (CHB) multilevel inverter (exemplified with a 3-cell, 7-level configuration).

To derive a scientifically valid comparison across different level counts (ranging from 3 to 21 levels), it is imperative to isolate the effect of the "level count" from the voltage magnitude. Therefore, a rigorous "Boundary Condition Preservation via DC-Link Scaling" protocol is implemented in this study. As the number of cascaded H-bridge cells (N)

increases, the DC-link voltage assigned to each individual cell (U_{dc_cell}) is inversely scaled following the relationship $U_{dc_cell} = U_{peak}/N$. The detailed scaling configurations for all investigated topologies are systematically tabulated in Table 1. This systematic adjustment ensures that the maximum output phase voltage remains fixed at a nominal 240 V regardless of the topology's complexity, allowing subsequent performance and loss analyses to reflect the intrinsic characteristics of the multilevel architecture rather than artifacts of varying voltage stress.

Table 1. DC-link voltage scaling protocol for the investigated CHB inverters to preserve a constant maximum phase voltage (U_{peak} = 240 V).

Level Count (L)	Number of Cell (N)	Cell Voltage U_{dc_cell} (V)
3-level	1	240
5-level	2	120
7-level	3	80
9-level	4	60
11-level	5	48
13-level	6	40
15-level	7	34.3
17-level	8	30
19-level	9	26.7
21-level	10	24

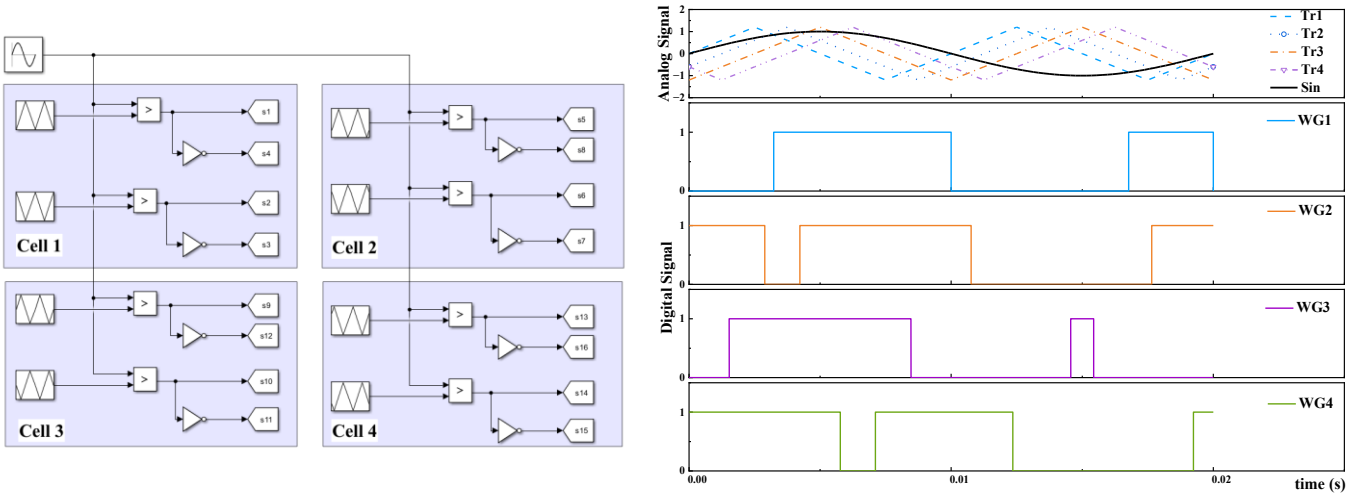
2.2. CPS-SPWM Control and Switching Count Mathematical Modeling

To effectively drive the MOSFETs within the CHB array, the carrier-phase-shifted sinusoidal pulse width modulation (CPS-SPWM) strategy is adopted. In this mechanism (exemplified by the 9-level control logic in Figure 6a), all H-bridge cells share the same sinusoidal modulating wave but utilize triangular carriers that are phase-shifted by a specific angle. For an N-cell system using unipolar modulation, the phase shift θ between adjacent carriers is $\theta = \pi/N$. This coordinated phase-shifting facilitates an equivalent output switching frequency of $2Nf_c$ (where f_c is the carrier frequency), significantly improving the harmonic performance without increasing the switching stress on individual MOSFETs.

Furthermore, accurately quantifying the switching events is critical for evaluating the thermal dissipation of the inverter. Under the CPS-SPWM paradigm, the triangular carrier intersects the modulating wave twice per period, resulting in one turn-on and one turn-off event per carrier cycle (as visually demonstrated in the timing diagram in Figure 6b). Given the carrier frequency (f_c) and the modulation frequency (f_m), the theoretical number of switching events for a single MOSFET per modulation cycle (N_{switch}) is formulated as (3):

$$N_{switch} = 2 \times \frac{f_c}{f_m}. \tag{3}$$

This universal formula proves that the phase-shifting manipulation only redistributes the switching events uniformly in the time domain without altering the total count per component. To overcome the "visualization bottleneck" at high frequencies (e.g., f_c = 1 kHz), a "Proportional Scaling Methodology" was employed in our preliminary validation. By executing a dedicated simulation benchmark at a reduced carrier frequency (f_c = 100 Hz) while maintaining f_m = 50 Hz (which corresponds to the exact waveforms plotted in Figure 6b), the manual count yielded exactly 4 events per cycle, achieving a 0% deviation from the theoretical prediction and thereby verifying the accuracy of (3).



(**a**) (**b**)

Figure 6. Carrier-phase-shifted sinusoidal pulse width modulation (CPS-SPWM) deployed for the CHB multilevel inverter: (**a**) control logic configuration modeled in MATLAB/Simulink (exemplified with a 9-level, 4-cell setup); (**b**) timing diagram illustrating the continuous modulating and phase-shifted carrier waves, alongside the resulting discrete gate driving signals under the proportional scaling condition (f_c = 100 Hz, f_m = 50 Hz).

2.3. Detailed Simulation Infrastructure and Data Synchronization

To bridge the gap between idealized circuit theory and practical engineering, a detailed physical-layer simulation framework was constructed using the MATLAB/Simulink Simscape Electrical library. The MOSFET components were implemented using parameterized macro-models, meticulously calibrated to account for non-ideal conduction characteristics, including the field-effect on-resistance (R_{on}) and the non-linear response of internal anti-parallel diodes. To validate the trustworthiness of these macro-models, the simulated switching loss characteristics were cross-referenced with the experimental data of equivalent MOSFETs documented in the existing literature. To ensure numerical convergence across the 10 cascaded cells in the 21-level model, a fixed-step solver (ode3, Bogacki–Shampine) was utilized with a fundamental sample time of 1 µs, providing a 1000-fold oversampling of the 1 kHz carrier signal.

A sophisticated challenge in power electronic modeling involves the interaction between the discrete-time PWM control domain and the continuous-time physical power stage. Preliminary tests identified a critical "sampling density mismatch" (as graphically illustrated in Figure 7a), which prevented the accurate element-wise multiplication required for instantaneous power calculation ($P = V_{ds} \cdot I_d$) and subsequent transient energy integration. To remediate this vulnerability, a specialized data synchronization protocol was established utilizing zero-order hold (ZOH) blocks (see the operational flowchart in Figure 7b).

The ZOH strategy serves as a temporal bridge, effectively freezing the discrete control signals at the 1 µs sampling intervals to align perfectly with the continuous-time feedback from the physical sensors. This methodology ensures that the switching energy dissipation integration is based on mathematically aligned data arrays, providing the precision necessary to evaluate marginal efficiency changes as the level count scales from 3 to 21 in this proof-of-concept study.

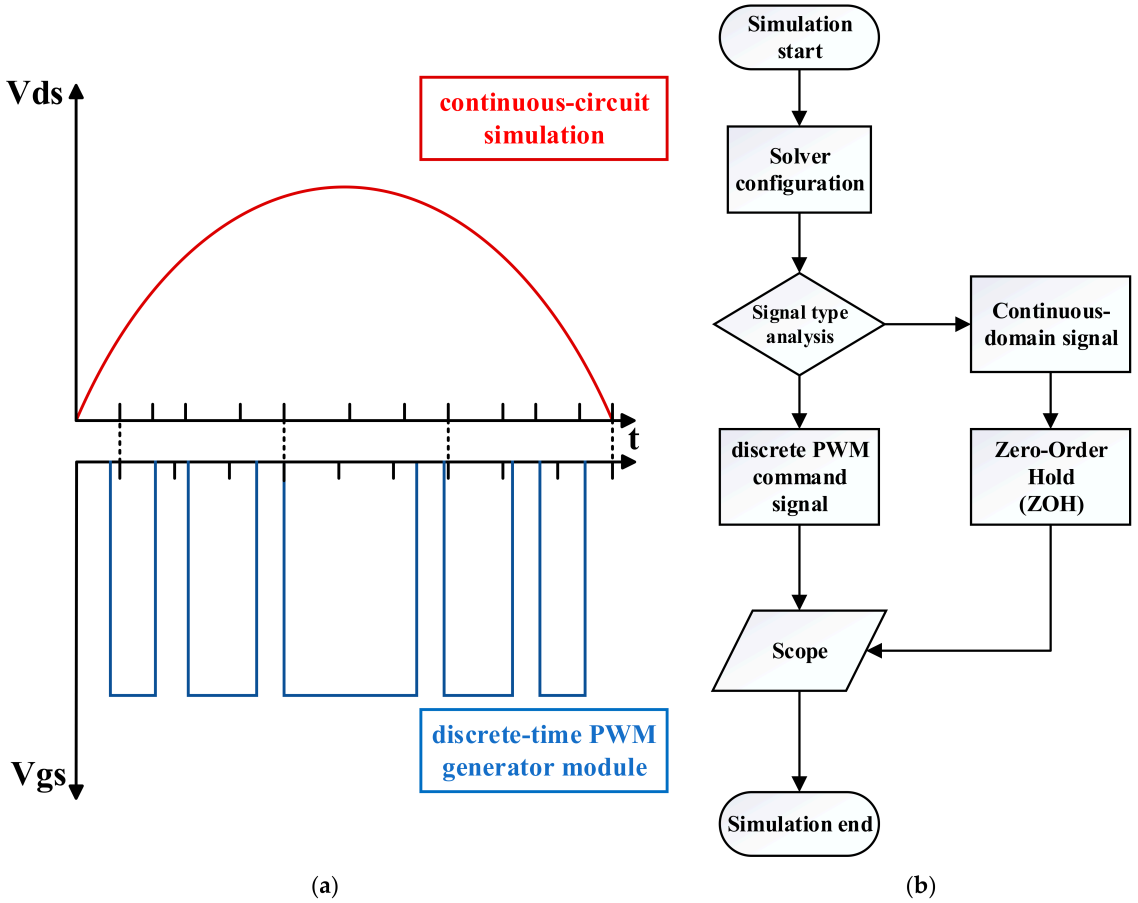


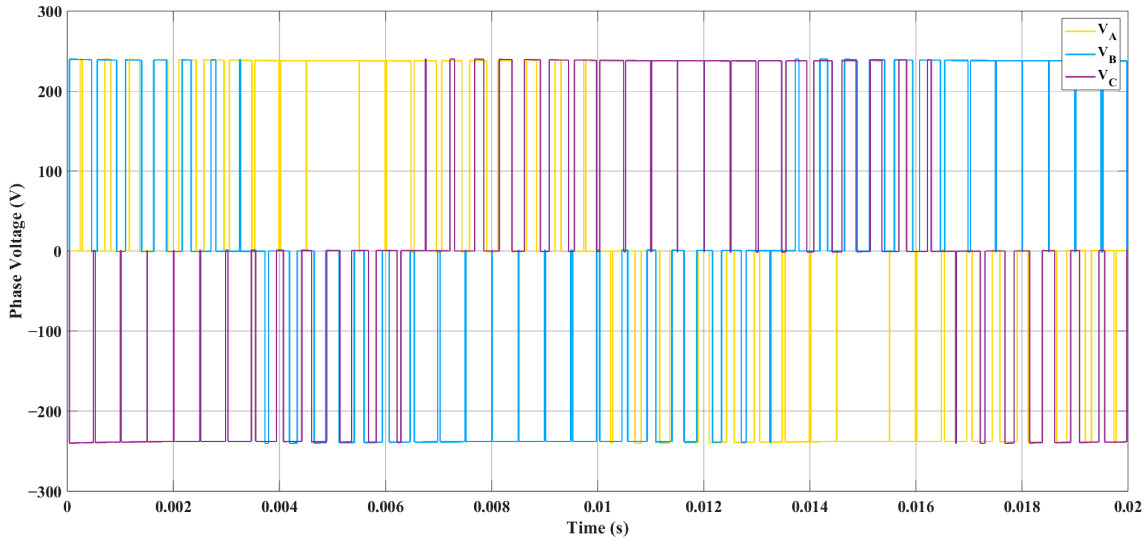
Figure 7. Data synchronization methodology for detailed electro-thermal co-simulation: (**a**) illustration of the sampling density mismatch between the continuous physical power stage (V_{ds}) and the discrete PWM control signal (V_{gs}); (**b**) flowchart of the proposed data synchronization protocol utilizing zero-order hold (ZOH) blocks.

3. Results and Analysis

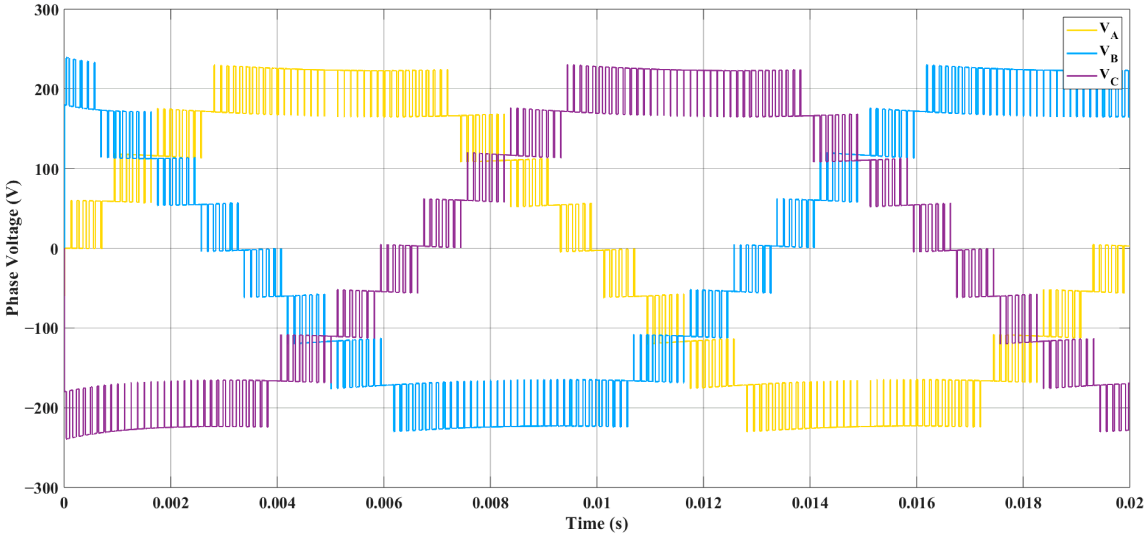
3.1. Detailed Waveform Synthesis and Harmonic Characterization

The empirical validation of the modular expansion protocol begins with the synthesis of output waveforms. A comprehensive sequence of simulations was conducted to capture the phase voltage and current profiles for configurations ranging from three to twenty-one levels. As the level count scales up, a clear "staircase refinement" trend is observable (as depicted in Figure 8 for representative three-level, nine-level, and twenty-one-level configurations). While the baseline three-level waveform exhibits pronounced discrete voltage steps, the twenty-one-level output achieves a near-sinusoidal profile even before the application of any inductive filtering. This progressive refinement significantly reduces the dv/dt stress on the load, serving as the primary justification for adopting higher-level architectures.

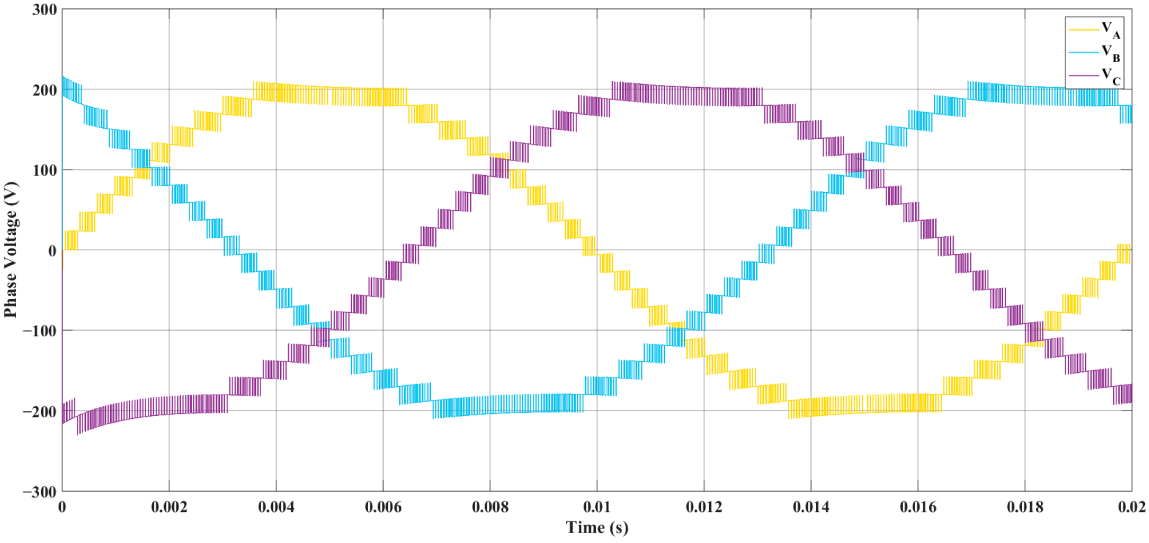
Beyond time-domain improvements, the spectral integrity of the CHB inverter was evaluated using fast Fourier transform (FFT) analysis. In accordance with the frequency multiplication theory of the CPS-SPWM strategy, the dominant harmonic clusters are strategically shifted toward the high-frequency sidebands centered around $2Nf_c$ (see Figure 9). For instance, in the nine-level system ($N = 4$), the dominant cluster appears around 8 kHz. Similarly, in the twenty-one-level system ($N = 10$) with a 1 kHz carrier, the primary harmonic noise is pushed to the vicinity of 20 kHz. This "spectral shifting" phenomenon leaves the low-frequency range near the 50 Hz fundamental remarkably clean, thereby drastically relaxing the size and cost requirements for output LC filters in grid-tied applications.



(**a**)

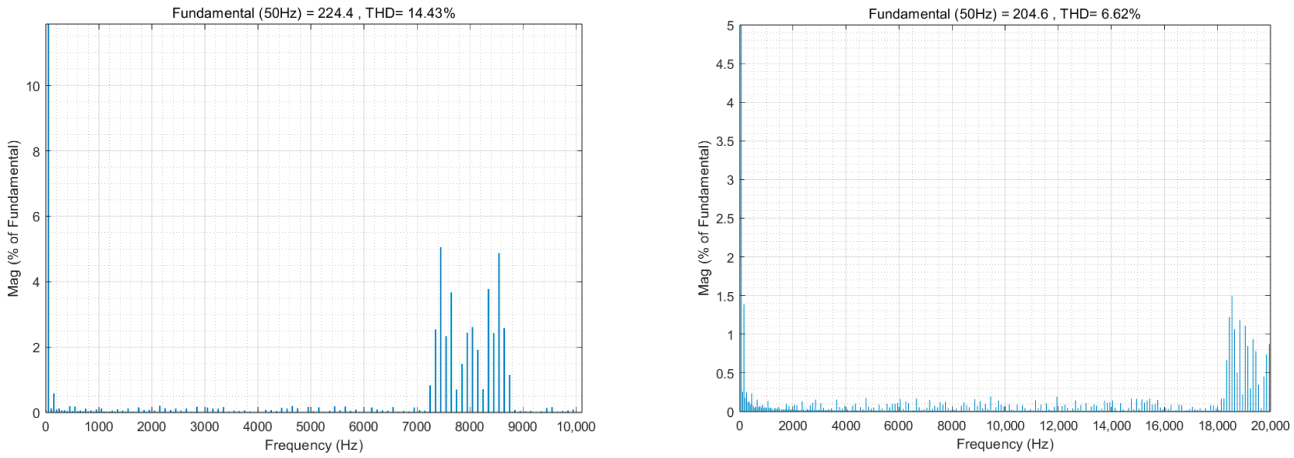


(**b**)



(**c**)

Figure 8. Evolution of the output phase voltage waveforms across representative CHB configurations: (**a**) 3-level; (**b**) 9-level; and (**c**) 21-level. The progressive staircase refinement distinctly illustrates the reduction in discrete voltage steps.



(**a**) (**b**)

Figure 9. Voltage harmonic spectra derived from FFT analysis, illustrating the spectral shifting phenomenon to high-frequency sidebands: (**a**) 9-level configuration with the dominant harmonic cluster centered around 8 kHz ($2Nf_c$); (**b**) 21-level configuration with the primary harmonic noise pushed to the vicinity of 20 kHz ($2Nf_c$).

Quantitatively, the relationship between the number of levels and the total harmonic distortion (THD) demonstrates a robust inverse correlation. As the level count increases from three to twenty-one, the voltage THD drops dramatically from 52.83% to 6.62% (illustrated in Figure 10). However, a critical non-linear asymptotic behavior is observed: the marginal gain in THD reduction becomes notably shallower beyond the 13-level mark. This diminishing return suggests that simply maximizing the level count for improved power quality may eventually be outweighed by the escalating system complexity.

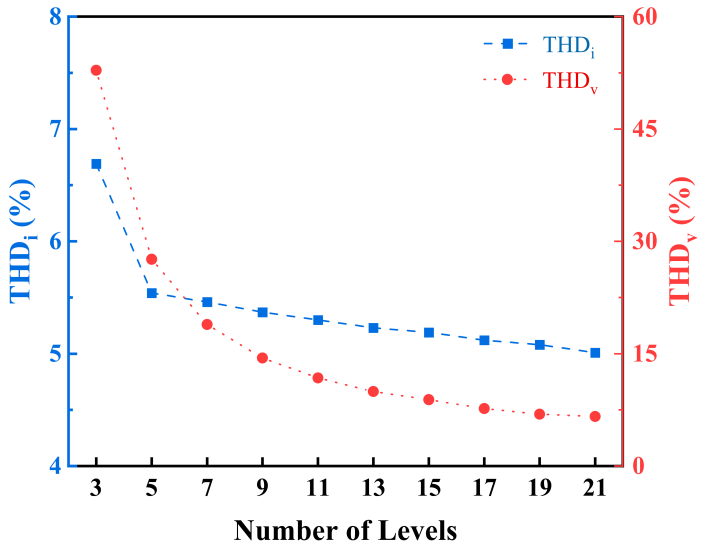


Figure 10. Evolution of total harmonic distortion (THD) in current (blue) and voltage (red) with respect to the number of cascaded levels.

3.2. Microscopic Assessment of Intra-Cell Switching Energy

While macroscopic power quality improves with modular expansion, evaluating the localized thermal stress on individual semiconductor devices is equally vital for system reliability. Utilizing the established precise integration windows, the transient energy dissipation during turn-on (E_{on}) and turn-off (E_{off}) transitions was captured. A microscopic breakdown of the switching losses for the four transistors ($S_1 - S_4$) within the first H-bridge unit (Cell 1) of the nine-level inverter is presented in Figure 11.

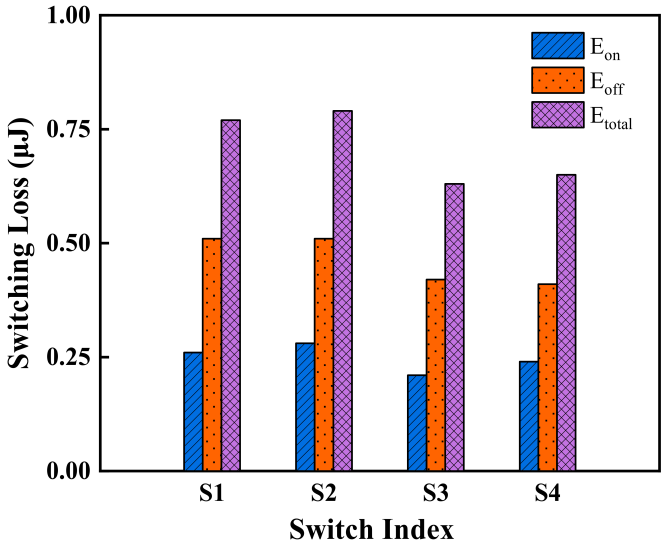


Figure 11. Microscopic switching loss distribution (turn-on, turn-off, and total) among the four MOSFETs (S1–S4) within Cell 1 of the 9-level CHB inverter.

A critical physical insight derived from these measurements is that the turn-off energy dissipation consistently exceeds the turn-on energy across all components, typically accounting for over 60% of the total switching loss. This discrepancy is attributed to the inherent capacitance and current-tailing effects during the MOSFET's transition from a saturated to a cutoff state. Furthermore, the total loss distribution is shown to be non-uniform within the cell. Under balanced load conditions, S_1 and S_2 handle a slightly higher proportion of the switching losses compared to S_3 and S_4. This intra-cell asymmetry highlights the necessity for component-specific thermal management strategies, particularly in space power applications where convective cooling is unavailable.

3.3. Macroscopic Scaling Effects on Total Power Dissipation

The implementation of the DC-link scaling protocol yields a profound impact on the switching energy dissipation. The evolution of switching losses as a function of level count is quantified in Table 2. A direct comparison (Figure 12) reveals a drastic, significant reduction in per-component switching energy as the topology scales up. Specifically, the total switching energy per event plummets from 10.66 μJ in the three-level baseline to 0.63 μJ in the nine-level configuration, and further down to a mere 0.21 μJ in the twenty-one-level case. This exceptional reduction is a direct consequence of the decentralized voltage stress, where each module in the 21-level system handles only a fraction (24 V) of the 240 V peak voltage.

Table 2. Measured switching energy dissipation per MOSFET across different level configurations.

Inverter Levels	Turn-On Energy E_{on} (μJ)	Turn-Off Energy E_{off} (μJ)	Total Switching Energy (μJ)	Switching Power Loss (mW)
3-level	4.04	6.62	10.66	10.66
5-level	1.54	1.66	3.20	3.20
7-level	0.84	1.28	2.12	2.12
9-level	0.21	0.42	0.63	0.63
11-level	0.33	0.38	0.70	0.70
13-level	0.14	0.32	0.46	0.46
15-level	0.23	0.23	0.46	0.46
17-level	0.11	0.18	0.28	0.28
19-level	0.19	0.14	0.33	0.33
21-level	0.09	0.11	0.21	0.21

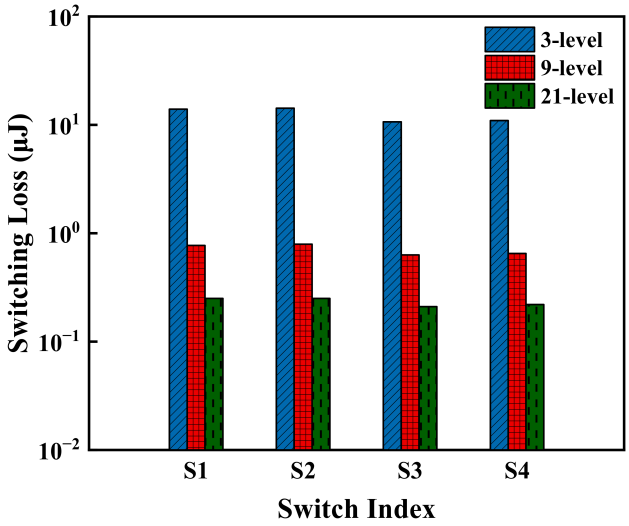


Figure 12. Direct comparison of total switching loss per MOSFET among the representative 3-level, 9-level, and 21-level CHB topologies.

However, a broader examination across the three to twenty-one level spectrum (plotted using a semi-logarithmic scale in Figure 13) reveals a complex trade-off. While the per-device switching losses decline monotonically from three to eleven levels, the absolute changes become extremely subtle and exhibit minor asymptotic fluctuations beyond the thirteen-level mark. Crucially, although the individual transistor efficiency is maximized in higher-level configurations, this benefit must be balanced against the cumulative loss penalty. For instance, the 21-level system employs 120 MOSFETs across three phases, resulting in a linear accumulation of baseline conduction losses and gate-drive power consumption. This contradiction between individual thermal relief and system-level structural penalty strictly limits the blind pursuit of higher-level counts.

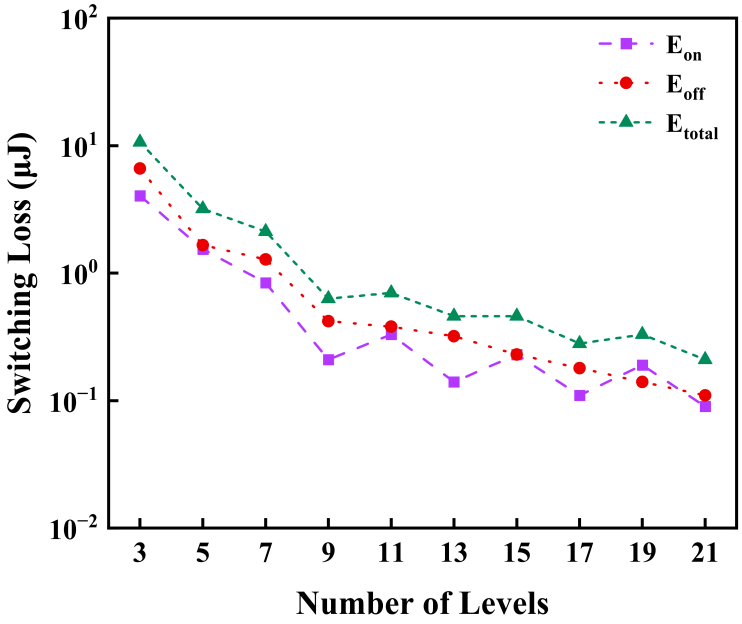


Figure 13. Evolution trend of turn-on, turn-off, and total switching energy loss per MOSFET versus the number of levels.

It should be noted that this study primarily evaluates transient switching losses. In practical deployments, the total system efficiency will be further degraded by conduction losses, gate-driver power consumption, and dead-time effects. For high-level configurations

such as the 21-level inverter (employing 120 MOSFETs), the linear accumulation of gate-driver losses will significantly amplify the total power dissipation, further justifying the necessity of penalizing the component count (N) in the evaluation metric.

4. Discussions and Outlook

4.1. The Engineering Dilemma: Power Quality vs. Hardware Complexity

The empirical results presented in Section 3 highlight a fundamental engineering conflict in the design of CHB multilevel inverters: the simultaneous pursuit of high power quality and high system efficiency. As the level count scales from three to twenty-one, a monotonic reduction in THD is achieved, accompanied by a significant decrease in individual MOSFET switching losses due to the decentralized voltage stress. However, these benefits are counterbalanced by the "law of diminishing marginal returns". Beyond the 13-level configuration, the gradient of improvement in THD becomes notably shallower. Concurrently, the system necessitates a linear increase in the number of active components (e.g., 40 MOSFETs per phase for a 21-level setup) and their associated gate-drive isolation complexities. Conventional evaluation methods that isolate THD or switching loss individually fail to capture this holistic system-level trade-off, making it strategically imperative to establish a unified metric that penalizes both harmonic distortion and hardware redundancy.

4.2. Formulation of the Performance-to-Loss Ratio (PLR) Framework

To bridge the gap between idealized simulation results and practical industrial decision-making, this research proposes the performance-to-loss ratio (PLR) as a comprehensive multidimensional figure-of-merit. Unlike standard efficiency metrics, the PLR integrates power quality (THD), thermal stress (individual switching power loss, P_{loss}), and structural complexity (total component count, N) into a single optimization objective. The indices for current (PLR_i) and voltage (PLR_v) are formulated as (4) and (5), respectively:

$$PLR_i = \frac{1}{(THD_i)^{\alpha} \times (P_{loss})^{\beta} \times N^{\gamma}} \, \mathrm{W}^{-1}, \tag{4}$$

$$PLR_v = \frac{1}{(THD_v)^{\alpha} \times (P_{loss})^{\beta} \times N^{\gamma}} \, \mathrm{W}^{-1}. \tag{5}$$

where α, β, and γ are empirical weighting factors representing the relative importance of power quality, thermal management, and system cost/complexity, respectively. In our baseline analysis, equal weights ($\alpha = \beta = \gamma = 1$) are assumed to establish a generalized framework.

In these expressions, the product in the denominator represents the composite system penalty. As the level count increases, the rapid decline in P_{loss} and THD must outpace the linear growth of N for the PLR to show an upward trend. The inclusion of N as a primary variable ensures that the index mathematically accounts for the heightened failure rate, procurement costs, and control latency associated with adding H-bridge cells.

4.3. Identification of Optimal Level Nodes: Local vs. Global Optima

The empirical evaluation of the PLR indices across the 3 to 21 level spectrum reveals a distinct non-monotonic optimization trajectory (as illustrated in Figure 14).

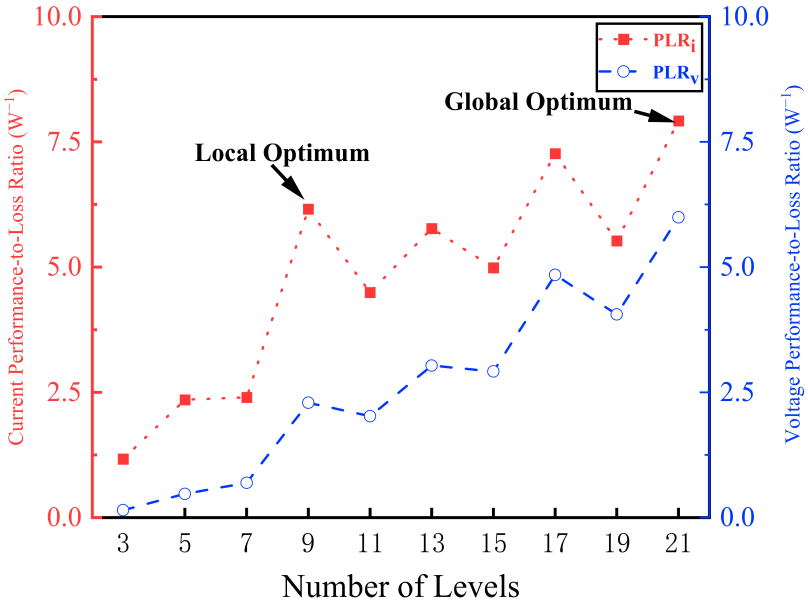


Figure 14. Current and voltage performance-to-loss ratios (PLR) versus the number of levels for CHB multilevel inverters. The non-monotonic optimization trajectory distinctly highlights the 9-level configuration as the local optimum and the 21-level configuration as the global optimum.

A rigorous analysis of the resulting curves identifies three critical engineering decision nodes:

- Local Optimum (Nine-Level Configuration): Up to the nine-level mark, the improvements in THD and the reduction in per-component voltage stress significantly outweigh the increase in hardware count. The system achieves a "sweet spot" where high performance is maintained with a relatively modest component count (four cells per phase). This node is particularly recommended for cost-sensitive applications, such as medium-voltage grid-connected renewable energy subsystems, where initial capital expenditure and maintenance are primary constraints.
- Global Optimum (21-Level Configuration): Beyond the nine-level mark, the PLR curves exhibit a plateau followed by a secondary surge, eventually reaching a global optimum at the twenty-one-level configuration. As the system scales toward 21 levels, the ultra-low dv/dt stress and near-sinusoidal profile drastically minimize switching losses, providing the highest performance-to-loss efficiency in the tested range. Although system complexity is maximized, individual component reliability is exceptionally enhanced. This makes the 21-level setup the definitive high-performance bound, ideally suited for mission-critical scenarios such as detailed space power electronics (e.g., 240 V spacecraft DC buses), where pure spectral output and stringent thermal radiation constraints are paramount.
- Sensitivity Analysis: Furthermore, a parametric sensitivity analysis reveals the adaptability of the PLR index. Through parametric sensitivity analysis, if economic constraints are prioritized (e.g., $\gamma = 2$), the nine-level configuration becomes the absolute global optimum. Conversely, if thermal dissipation is the strictest bottleneck (e.g., $\beta = 2$, such as in aerospace applications), the 21-level configuration retains its position as the global optimum. This demonstrates that the PLR is not merely a heuristic metric, but a tunable optimization criterion.

4.4. Implications and Future Research Directions

The proposed integrated methodology and the PLR framework offer a significant contribution to guiding the development of power conversion systems toward the global

net-zero [34,35] vision. By quantifying the efficiency–quality equilibrium, designers can navigate the complex design space of CHB inverters with quantitative confidence, selecting optimal hardware expenditure tailored to specific application constraints.

However, a limitation of this proof-of-concept study is the reliance on simulation-based validation. While the models incorporate non-ideal characteristics, future work will include hardware-in-the-loop (HIL) testing or low-power prototype experiments to capture real-world EMI phenomena and gate-driver delays. Furthermore, while this study establishes a robust foundation under balanced and linear load conditions, extending the PLR framework to account for unbalanced, non-linear inductive loads [36] and dynamic grid fault scenarios [37] is a critical next step. Such practical conditions introduce uneven harmonic distributions that could significantly shift the optimal level count outcomes. Finally, investigating the reliability implications and PLR shifts when substituting traditional silicon (Si) devices with advanced wide-bandgap (WBG) semiconductors [38], e.g., silicon carbide (SiC) [39,40] or gallium nitride (GaN) [41], in ultra-high-level configurations remains a compelling direction for next-generation power electronics.

5. Conclusions

This study established a comprehensive analytical and simulation-based framework to systematically evaluate and optimize cascaded H-Bridge (CHB) multilevel inverters ranging from three to twenty-one levels. By demystifying the intricate trade-offs between harmonic performance, component-level energy dissipation, and system complexity under CPS-SPWM control, the principal conclusions are drawn as follows:

- Theoretical Modeling Breakthrough: A universal MOSFET switching count mathematical model ($N_{switch} = 2 \times \frac{f_c}{f_m}$) was derived for CPS-SPWM. Its accuracy was empirically validated with 0% deviation through a novel "Proportional Scaling Methodology", providing a robust analytical tool that effectively overcomes the high-frequency visualization bottleneck in complex multilevel topologies.
- Quantification of the Engineering Trade-off: Utilizing a detailed, ZOH-synchronized electro-thermal simulation infrastructure, this study confirmed that modular expansion yields a significant reduction in individual switching losses and drastically relieves dv/dt stress. However, a critical law of diminishing marginal returns was identified: the gradient of THD improvement flattens significantly beyond the 13-level mark, directly conflicting with the linear escalation of hardware components.
- Multidimensional Evaluation Innovation: To resolve the aforementioned design dilemma, this research proposed the performance-to-loss ratio (PLR). This novel figure-of-merit mathematically integrates power quality, individual thermal stress, and total component count into a unified optimization objective, successfully penalizing both harmonic distortion and hardware redundancy.
- Identification of Definitive Design Boundaries: The PLR framework quantitatively mapped the complex design space, identifying two critical engineering nodes. The nine-level configuration emerges as a local optimum, offering the ideal "sweet spot" for cost-sensitive modular applications such as medium-voltage renewable energy subsystems. Conversely, the 21-level configuration is identified as the global optimum, providing the ultimate detailed performance and ultra-low thermal dissipation essential for mission-critical scenarios such as space power electronics.

Arguably, this research bridges the gap between theoretical pulse-width modulation principles and practical power electronic design, providing a quantitative roadmap for engineers to optimize hardware expenditure and accelerate the development of next-generation power converters toward the global net-zero vision.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
CHB	Cascaded H-Bridge
CPS-SPWM	Carrier-Phase-Shifted Sinusoidal Pulse Width Modulation
DC	Direct Current
EMI	Electromagnetic Interference
FC	Flying Capacitor
FFT	Fast Fourier Transform
GaN	Gallium Nitride
MLI	Multilevel Inverter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NPC	Neutral Point Clamped
PLR	Performance-to-Loss Ratio
PWM	Pulse Width Modulation
Si	Silicon
SiC	Silicon Carbide
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
WBG	Wide-Bandgap
ZOH	Zero-Order Hold

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