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Investigation of a Low-Speed Commutation Voltage Shock Problem in Three-Level ANPC Inverter with Hybrid Modulation Mode

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Abstract: With the development of the photovoltaic industry; there will be an increasing demand for efficient, high-power density, and low-cost grid interface converters. Compared with two-level inverters, multilevel inverters have the following advantages: (1) lower device voltage ratings; (2) better output filtering spectrum; (3) lower electromagnetic interference (EMI) noise; and (4) higher switching speed capability. However, the complex switching circuit of the multilevel inverter will bring more parasitic inductance, resulting in severe switching overvoltage (ringing). Especially in order to reduce the cost of the inverter, using the long-loop modulation mode, the commutation loop will introduce more parasitic inductance, which will make the overvoltage more serious. Consider that commonly used overvoltage absorption schemes are effective only for overvoltage or suppression of oscillations. Therefore, a new overvoltage absorption circuit is proposed in this paper, which can not only alleviate the overvoltage and ringing phenomena but also suppress the effect of voltage jumps during low-frequency switching on high-frequency input voltage. This overvoltage absorption circuit is characterized by low overvoltage, fast ringing damping, and minimum capacitance. Experiments and simulations are conducted to verify the effectiveness of this overvoltage absorption circuit using a three-level ANPC inverter as a prototype. The results show that the proposed overvoltage absorption circuit can significantly reduce the overvoltage level, shorten the oscillation time, and reduce the voltage difference between the upper and lower DC bus capacitors.

Keywords: multilevel inverter; parasitic effects; overvoltage; ringing; long-loop modulation mode; voltage jumps

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1. Introduction

As the share of photovoltaic (PV) power generation in the electricity supply continues to grow, so does the demand for efficient, high-power density, lightweight, and low-cost converters. The development of the photovoltaic industry reduces the need for fuel for traditional thermal power generation, reduces carbon emissions, and makes an important contribution to the protection of the environment. Currently, the energy crisis is worsening, the development of traditional energy sources such as coal and oil has received resistance, and the promotion and popularization of new energy generation, smart grid technology, and electric vehicles [1] have led to the industry's need for a more stable, higher-power, and lower-loss power system. As an important part of the energy conversion system, the inverter is an important object of research in the power system, in which the three-level inverter receives more extensive attention.

Three-level inverters are undoubtedly the most popular choice for high-power and medium-voltage applications, offering lower EMI noise, lower voltage ratings on semiconductor power devices, better power quality, and more flexible control than conventional

two-level inverters [2,3]. All the switches in a three-level ANPC inverter can be actively controlled, while different modulations can be applied to control the inverter [4,5] to achieve bidirectional power flow, thermal balance, and higher efficiency. Two commonly used modulation schemes are analyzed in detail in [5], where the parasitic inductance in the long-loop modulation mode is significantly larger than that in the short loop modulation mode, the overvoltage in the long-loop modulation mode is significantly higher than that in the short loop modulation mode due to the parasitic effect, and in the short loop modulation mode, the power switching devices have lower losses [6] and are subjected to lower stresses due to smaller parasitic inductance.

The efficiency of the inverter can be improved by using the hybrid modulation technique, a common three-level hybrid modulation technique, as shown in Table 1. In the first group (short loop commutation), the four switches in the first level are controlled by a high-frequency carrier, and the two switches in the second level are controlled by a low-frequency carrier. In the second group (long-loop commutation), the four switches in the first stage are controlled by a low-frequency carrier, and the two switches in the second stage are controlled by a high-frequency carrier. However, under low-frequency switching, the second stage of the first group will introduce more switching losses. Although the parasitic inductance is significantly higher than that of the short-loop current-switching mode in the long-loop current-switching mode [7], the parasitic inductance in the circuit can be optimized by optimizing the PCB layout, thus reducing the parasitic inductance in the circuit and minimizing the parasitic inductance in the long-loop current-switching mode. At the same time, only two high-frequency switches are needed in the long-loop commutation mode, which is less costly compared with the short-loop commutation mode. Therefore, the three-level ANPC in long-loop modulation mode is considered the research object in this paper.

Table 1. Different hybrid modulation techniques for three-level ANPC.

Hybrid Modulation Technology	LF Switches	HF Switches
Group I	S_5 and S_6	S_1, S_2, S_3 and S_4
Group II	S_1, S_2, S_3 and S_4	S_5 and S_6

In the long-loop current-switching mode, S_1 and S_3 synchronous switches, S_2 and S_4 synchronous switches, and S_1 and S_2 complementary switches, form a double-pole, double-throw switch as shown in Figure 1, with the red dashed line showing the direction of the current flow when S_1 and S_3 are on, and the blue dashed line showing the direction of the current flow when S_2 and S_4 are on, which results in a DC bus because there is only a single capacitor on the DC side used for charging or discharging. capacitor voltage imbalance. When switches S_1 and S_3 are switched to S_2 and S_4, the input voltages of switches S_5 and S_6 will undergo large jumps, reducing the system characteristics.

The switching topology circuits applied in this paper contain wide bandgap (WBG) power semiconductor devices, which exhibit faster di/dt and dv/dt and provide higher voltage blocking capability, better thermal performance, and lower switching losses compared with Si IGBT [8,9]. However, the stability of wide-bandgap power semiconductors is affected by the parasitic inductance of the circuit, which can easily cause overvoltage [10] and voltage oscillations. In the three-level ANPC inverter, the commutation of wide-bandgap (WBG) devices [11] introduces multiple switching oscillation components, which will lead to overvoltage during switching transients. Also, the EMI performance will be affected by the different oscillation components. Layout-optimized DC bus design and control methods are proposed in [12,13], respectively, so as to reduce the overvoltage. From the switching state of a three-level ANPC inverter, it can be seen that each phase can output three different voltage levels, i.e., $V_{dc}/2$, 0, and $-V_{dc}/2$. When one of the phases is clamped to neutral, the neutral voltage becomes unbalanced due to the current flowing through it. Various PWM modulation schemes were proposed in [14–16] to minimize the voltage

unbalance in the DC bus, but the approach improves the modulation difficulty of the converter system.

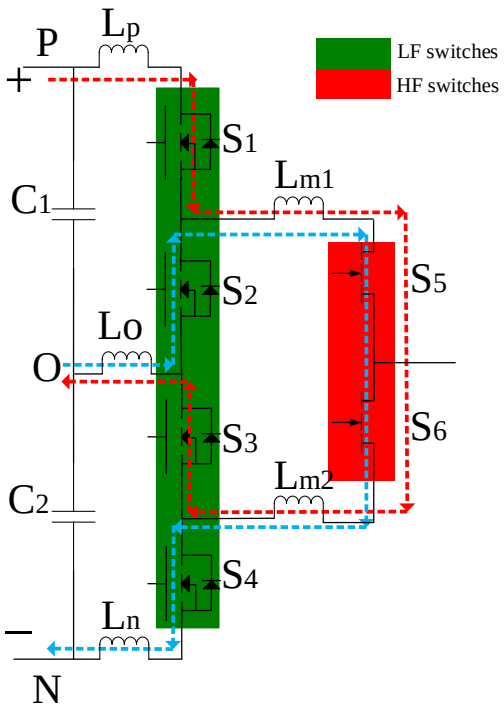


Figure 1. Commutation loop for the conventional ANPC converter.

In order to analyze the effect of voltage jumps on high-frequency switching, the three-level ANPC hybrid modulation mode is used, which produces three levels per phase at the output. Due to the ANPC structure, in which the voltage across the switching device is half of the dc bus voltage, a switching device that is subjected to a lower voltage can be used. Considering the need to operate at high switching frequencies, GaN metal oxide power switching devices are used as high-frequency switches and Si MOSFETs as low-frequency switches in the three-level ANPC unit, and the long-loop hybrid modulation technique is used in this paper. Meanwhile, the effect of parasitic parameters on the performance of GaN metal oxide power switching devices requires the use of electromagnetic field finite element analysis to extract the parasitic parameters and design the overvoltage absorption circuit.

The rest of the paper is organized as follows: in Section 2, common overvoltage (oscillation absorption) schemes are analyzed; in Section 3, a new overvoltage absorption scheme is proposed; in Section 4, the application system design is elaborated, including parasitic parameter extraction and component parameter determination; in Section 5, experimental simulations are performed; and finally, conclusions are provided in Section 6.

2. Analysis of Midpoint Voltage Unbalance Mechanism

2.1. Analysis of Midpoint Voltage Imbalance

In the inverter operation, when the load side of one phase or two is connected to the neutral point of the DC bus, the current will flow from the neutral point O of the bus through the load to the neutral point N, which will make the DC bus capacitor constantly charging or discharging. If the capacitor's charging is not equal to the amount of its discharge, this process will lead to the neutral point O of the voltage shift. As shown in Figure 2a, it is assumed that the current flows from top to bottom through capacitors C_1 and capacitors C_2, and the midpoint current is the direction of outflow from neutral O. It is also assumed that the direction of outflow from the neutral point is the positive direction of the current.

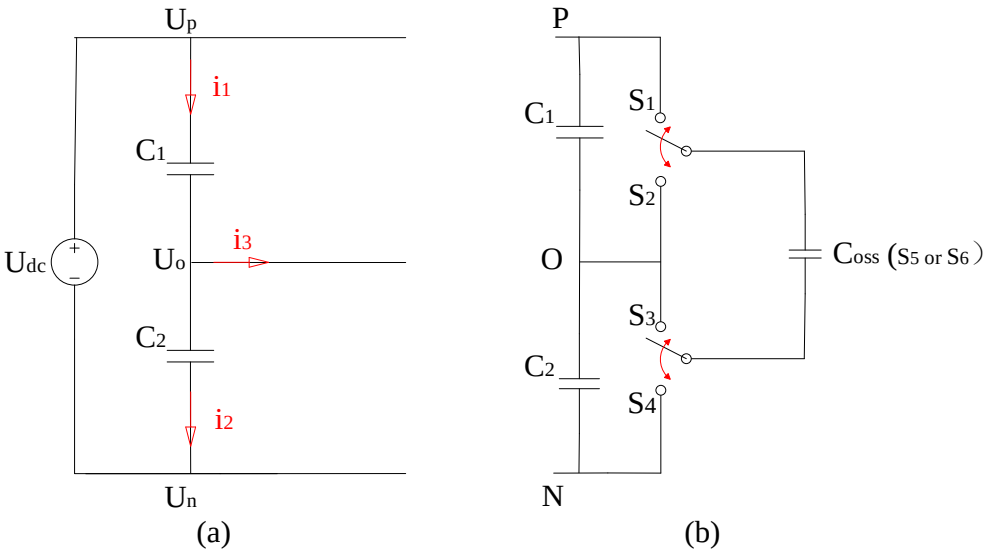


Figure 2. (**a**) DC capacitor voltage bias phenomenon. (**b**) Equivalent circuit on high-frequency switching at low-frequency commutation.

Then the voltage values of the capacitor C_1 and capacitor C_2 is:

$$\begin{cases} U_{C1} = \frac{1}{2}U_{dc} - U_O \\ U_{C2} = \frac{1}{2}U_{dc} + U_O \end{cases} \tag{1}$$

The current flowing through capacitor C_1 and capacitor C_2 is:

$$\begin{cases} i_1 = C_1 \frac{dU_{dc1}}{dt} = C_1 \frac{d\left(\frac{1}{2}U_{dc} - U_O\right)}{dt} \\ i_2 = C_2 \frac{dU_{dc2}}{dt} = C_2 \frac{d\left(\frac{1}{2}U_{dc} + U_O\right)}{dt} \end{cases} \tag{2}$$

Since the upper and lower capacitors have equal capacitance values C_1 and C_2:

$$C_1 = C_2 = C \tag{3}$$

List Kirchhoff's current law for neutral O:

$$i_3 = i_1 - i_2 = C_1 \frac{d\left(\frac{1}{2}U_{dc} - U_O\right)}{dt} - C_2 \frac{d\left(\frac{1}{2}U_{dc} + U_O\right)}{dt} = -2C\frac{dU_0}{dt} \tag{4}$$

Further simplifying the above equation yields the change in midpoint voltage U_O, $\triangle U$:

$$\triangle U = -\frac{1}{2C}\int_0^t i_3 dt \tag{5}$$

Ultimately, Eq. U_O is the initial value of midpoint voltage, and the expression of midpoint voltage $U_O{}'$ is obtained as:

$$U_O{}' = U_O + \triangle U = U_O - \frac{1}{2C}\int_0^t i_3 dt \tag{6}$$

When switches S_1 and S_3 are off and S_2 and S_4 are on, as shown in Figure 2b, the voltage source is switched from the original C_1 to C_2, and the voltages of U_{C1} and U_{C2} are not the same due to the imbalance of the upper and lower capacitor voltages. When switches S_1 and S_3 are switched, the high-frequency switches S_5 and S_6 input voltages will be switched from U_{C1} to U_{C2}.

The simulation results show that the maximum capacitance voltage in the upper and lower parts reaches 414.5 V and the minimum voltage reaches 385.9 V as shown in Figure 3. Since the charging or discharging of the capacitor leads to a large capacitance current shockwave that causes fluctuations in the DC bus voltage, the mid-point voltage imbalance problem will bring a lot of hazards to the system, for example:

(1) It will cause the voltage value of a DC bus capacitor to exceed a predetermined voltage value, and in serious cases, the DC bus capacitor will be damaged;
(2) The power switching devices are unevenly loaded, which poses a greater challenge to the voltage resistance of the power switching devices;
(3) The inverter output waveform contains low harmonics, which affect the output quality and reduce the power density.

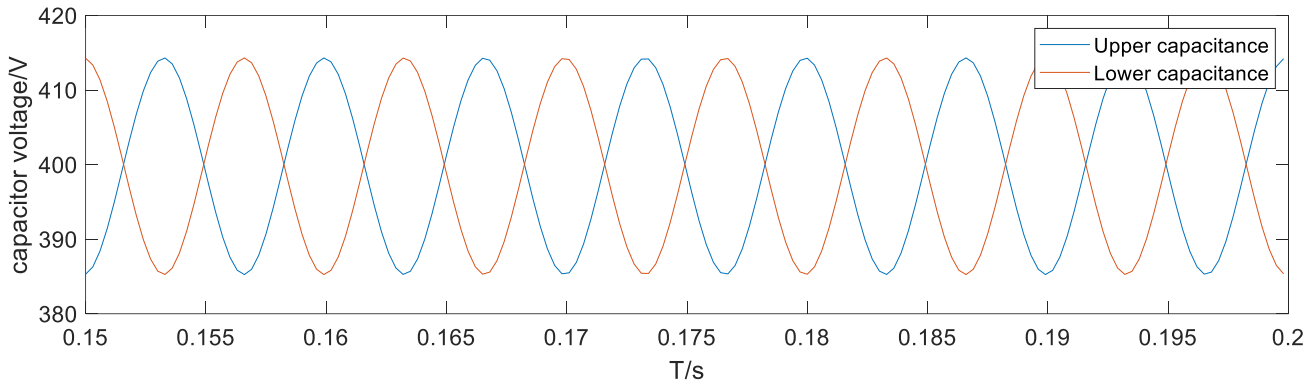


Figure 3. Simulation Results of DC Bus Capacitor Voltage.

2.2. High-Frequency Switching Input Voltage Jump Analysis

For the GaN three-stage, three-phase ANPC inverter power stage design module (TIDA-010210), the output is a 380 V three-phase voltage and the input is a DC-800 V voltage. In the adopted long-loop current switching mode, the LF switch forms a double-knife double-throw switch, and the DC-side capacitors C_1 and C_2 are equivalent to the voltage source, which changes from C_1 to C_2 when the LF switch operates. Due to the unbalanced capacitor voltage on the DC side, it will cause the high-frequency switch to experience large voltage jumps during operation. When the inverter operates, the voltage of the upper capacitor will be higher due to the limited PWM modulation method and the unidirectional diode. The low-frequency switches form a double-knife, double-throw switch so that the high-frequency switch input voltage jumps from a high voltage to a low voltage. Figure 4a shows that when the low-frequency switching occurs when the high-frequency switch is subjected to the voltage from the maximum value of 414.5 V suddenly dropping to the minimum value of 385.9 V, the one-phase load current polarity also changes, as shown in Figure 4b. At this time, the three-phase load current is sinusoidally transformed, as shown in Figure 4c.

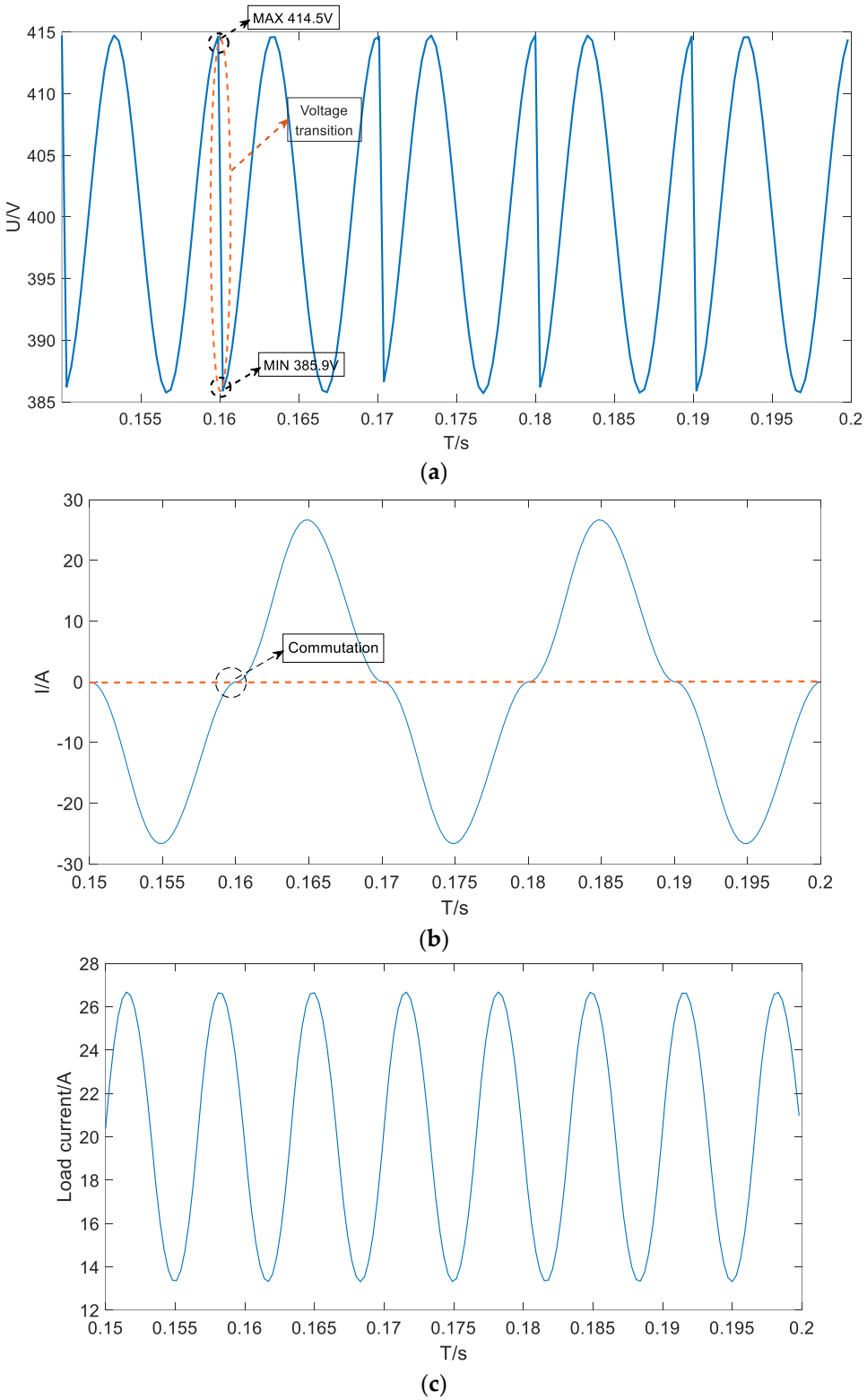


Figure 4. The phenomenon of high-frequency switch input voltage jumping during LF switch switching. (**a**) The voltage variation experienced by a high-frequency switch. (**b**) Polarity change of a phase load current. (**c**) Three-phase load current waveform.

It is empirically known that the dc bus capacitance voltage difference will be affected by the inverter DC side capacitance and power, although the larger the dc side capacitance, the smaller the voltage difference. Considering the requirements for the size of the inverter as well as the cost, the dc side capacitance selection needs to be considered for practical

applications. At a power (load) of 16 kW, the trend of the voltage difference with the size of capacitance is shown in Figure 5, and an empirical function is fitted, which shows that the rate of change of the voltage difference decreases gradually when the capacitance is larger than 300 μF.

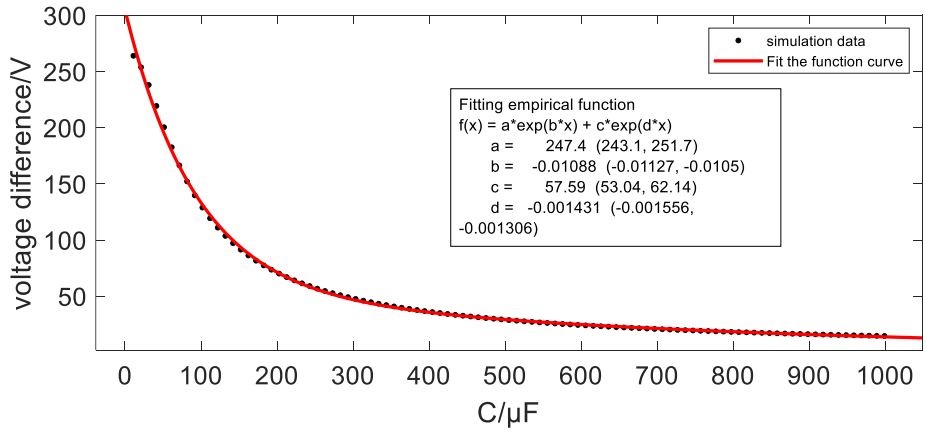


Figure 5. Plot of voltage difference with DC capacitance.

The voltage jumps with power (load) at a DC capacitor size of 500 μF shown in Figure 6.

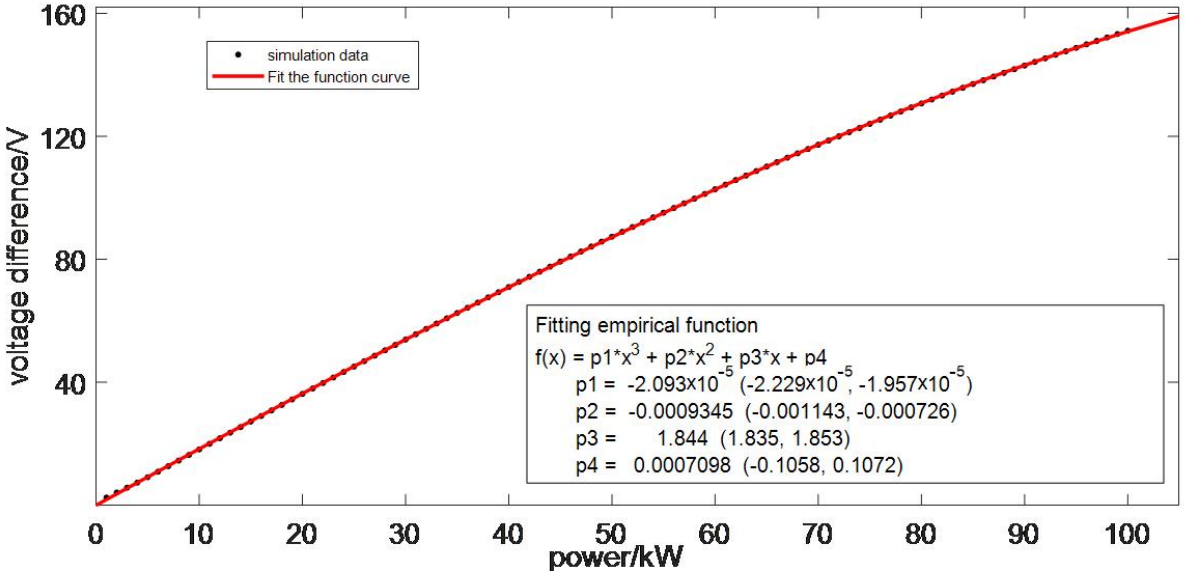


Figure 6. Plot of voltage difference with power.

It can be seen that the voltage difference decreases exponentially as the capacitance becomes increases, while it is linear with the power (load) change. If a suitable method is not taken, when the low-frequency switch is switching, the larger voltage difference will cause the high-frequency switch to withstand a larger voltage stress, which will damage the high-frequency switch in more serious cases, and at the same time, the larger voltage will damage the capacitance, affecting the quality of the power output from the inverter and even preventing it from working normally. In this paper, in order to solve the hazards of voltage jumps on the inverter system, a method is proposed to make the input voltage of the high-frequency switch to maintain stability, and at the same time, it has a good absorption effect on the over-voltage (oscillation). A three-dimensional surface diagram is established by the effect of capacitance and power on the voltage difference, as shown in Figure 7. The voltage difference decreases exponentially with the increase in capacitance

and increases with the increase in power (load). The DC bus capacitance size in the inverter used in this paper is 500μF. and the power is 16 kW. The measured voltage difference is 29 V, which is consistent with the data on the fitted three-dimensional surface.

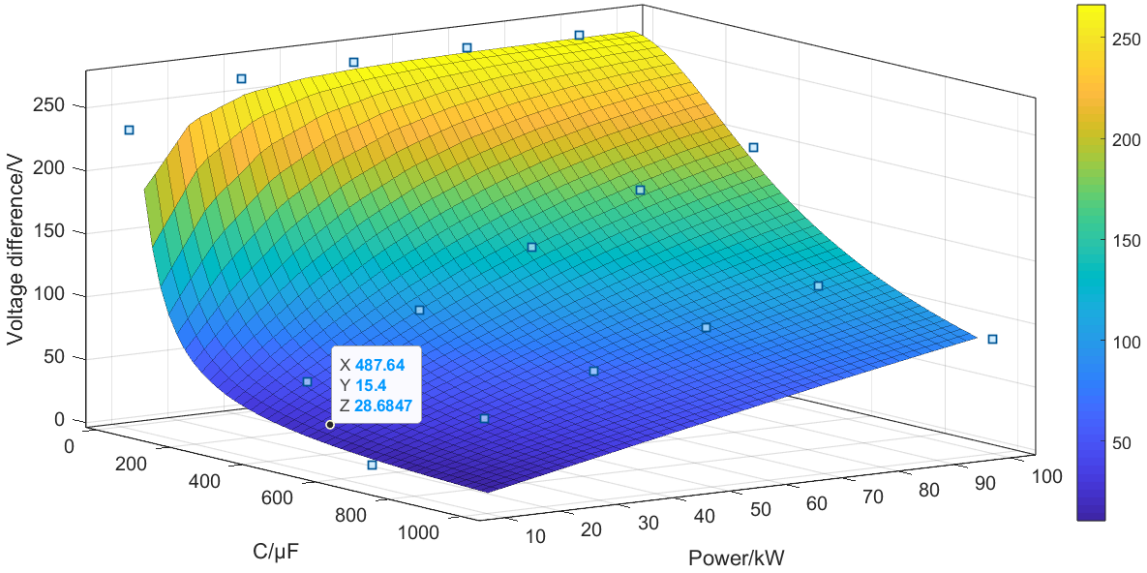


Figure 7. The effect of different capacitances and powers on the voltage difference is measured during low-frequency switching.

3. Overvoltage (Oscillation) Absorption Program Design

Oscillations occur between the parasitic inductance in the power circuit and the parasitic capacitance of the switching device in both on and off transients, and oscillations are unavoidable. In high-speed switching, ringing occurs due to sharp fluctuations in voltage and current during switching. Ringing leads to electromagnetic interference (EMI) noise and faults, which threaten system reliability. Therefore, it is necessary to solve the ringing noise problem, especially for MHz switching [17]. Due to the complexity of the three-level ANPC structure [18–20], more parasitic inductance is introduced into the circuit, which can easily lead to overvoltage in the switching devices. To suppress the switching oscillations, methods including optimizing the PCB layout, gate driving, adding oxide beads, and adding buffer circuits have been proposed. Since the parasitic parameters have a great influence on the parasitic oscillations, high-frequency paths should be established to take the parasitic parameters into account when designing the buffers. Optimizing the PCB layout can only reduce the parasitic parameters to a limited extent. Gate drive can reduce the switching oscillations by controlling dv/dt and di/dt, but it increases the complexity of the driver circuit and the difficulty of the circuit design. High-frequency noise can be suppressed by adding oxide beads; however, the oxide beads will introduce additional losses and the damping performance will deteriorate under high current conditions due to magnetic saturation. Through research in recent years, a variety of buffer circuits have been designed to suppress overvoltage and oscillations with good suppression effects, and the mainstream buffer circuits will be analyzed and compared in the following.

The RC snubber circuit consists of resistor R_s and capacitor C_s. The RC snubber circuit slows down the switching speed by dragging out the switching time and slowing down the switching speed. Thus, R_s can cause C_s to be completely discharged during the switching time period. In addition, C_s can cause the voltage to rise at a slower rate and extend the oscillation period, which can reduce the switching loss and overvoltage. RC snubber has excellent suppression of switching oscillation performance and limited overvoltage suppression performance and is highly regarded, and at the same time, RC snubber has almost no negative impact on the switching loss of the switching device. However, the snubber dissipation is inevitable in itself, and the RC snubber loss is reduced as the snubber

capacitance decreases or the snubber resistance increases [21]. Especially in the fields of high voltage, high current, and high frequency, RC snubber circuits generate additional thermal effects, and this loss will increase the difficulty of heat dissipation in the inverter. It is demonstrated in [22] that the RC snubber is not very suitable for high-frequency and high-speed applications because the snubber resistor R_s increases the absorption time of the snubber circuit and slows down the absorption speed of the snubber circuit.

While Joko et al. [23] proposed a combined C-RC snubber circuit where a single capacitor branch is responsible for absorbing overvoltage spikes and the RC branch is used to damp switching oscillations, it was shown that the C-RC snubber can overcome low-frequency oscillations, and it was demonstrated in [24] that the performance of suppressing the overvoltage can be significantly improved by increasing the values of C_{dec} and C_{snb} in the RC snubber, which is This is because the capacitance limits the severe voltage fluctuation of the bridge arm, but the DC bus capacitance voltage difference decreases slower and slower as the values of C_{dec} and C_{snb} increase, so it is not necessary to select larger capacitance (C_{dec} and C_{snb}) to slightly increase the suppression effect; otherwise, it will have adverse effects, e.g., additional parasites and a larger size of the inverter. It is shown that when C_{dec} and C_{snb} are kept constant, the increase in R_{snb} will weaken the suppression performance, and when R_{snb} and C_{snb} are kept constant, the decrease in C_{dec} does not have a great impact on the overvoltage suppression effect. Although the C-RC snubber circuit can realize an excellent overvoltage suppression effect compared with the traditional RC snubber circuit, its performance in suppressing turn-off overvoltage is still unsatisfactory. Theoretically, the power loss of C-RC snubber circuits is lower than that of RC snubber circuits, which is very beneficial in high-power, high-frequency areas.

Ref. [25] proposed an RC-D snubber circuit that evaluates the effect of wiring inductance on device switching, discusses the mechanism of ringing caused by wiring inductance, and suppresses ringing by an RC-D snubber circuit that takes into account the location of the wiring inductance. When the parasitic inductance is mainly concentrated at the source of the switching device, the RC-D snubber cannot suppress ringing, and the drain-source voltage oscillation will be more severe. The RC-D snubber circuits have excellent performance for suppressing the switch drain-source voltage ringing when the parasitic inductance is concentrated at either the switch gate or drain. However, the RC-D snubber circuits are not sufficient when the parasitic inductance is mainly concentrated at the switch gate to suppress switch drain-source voltage ringing and may cause malfunction or breakdown. Considering the location of the wiring inductance, the wires near the gate and source should be reduced as much as possible when optimizing the design of the RC-D snubber, and the parasitic inductance near the gate and drain terminals must be taken into account, while the RC-D snubber circuit does not have a significant effect on the reduction in the switch drain-source inter-voltage oscillation.

By analyzing the previous research ideas, most of them use a one-way absorption circuit to achieve the purpose of reducing the switch-off overvoltage or suppressing the oscillation. On this basis, it is proposed to hypothesize whether it is possible to reduce the switch-off overvoltage and suppress the voltage oscillation if another release circuit is added on top of the one-way absorption circuit. Therefore, in this paper, an overvoltage absorption circuit (RC-CD) is proposed, which is connected in parallel between the first and second stages as shown in Figure 8a. Under different PWM strategies, the two input capacitor (C_1 and C_2) voltages are always unbalanced because only one capacitor is used for charging or discharging, and the unbalance of the input voltage increases the output voltage waveform. Therefore, in order to minimize the effect of the input capacitor voltage imbalance on the system characteristics, the voltage of the absorbing capacitor C_3 is kept slightly above half of the DC voltage and maintained in a steady state by adding a voltage regulator diode to the release circuit. When the constituted double-knife double-throw switches S_1, S_3 and S_2, S_4 are switched at low frequency, the input voltages of the high-frequency switches S_5 and S_6 do not jump when low-frequency switching occurs due to the parallel connection of capacitance C_3 with the high-frequency switching input capacitance

while the RC-CD circuit is placed between the low-frequency stage and the high-frequency stage, which splits the large commutated circuit into two smaller circuits and is proposed to be the three-level ANPC structure used in the experiment.

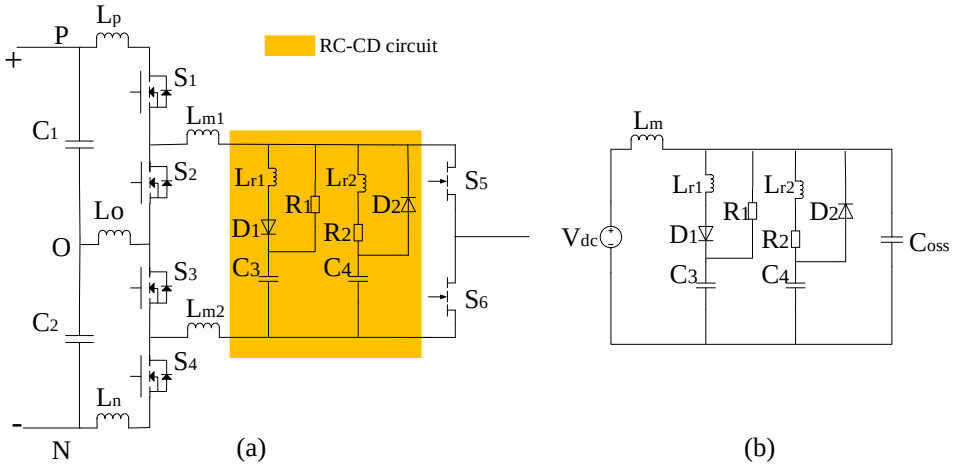


Figure 8. (**a**) Location of the proposed overvoltage protection circuit in the ANPC. (**b**) Equivalent circuit of the proposed overvoltage protection circuit in static operation.

When S_1 and S_3 are on, the equivalent circuit of this overvoltage (oscillation) absorption circuit is shown in Figure 8b, with V_{dc} as the equivalent circuit voltage source, C_{oss} as the parasitic capacitance on the drain-source stage of the high-frequency switch S_5 or S_6, and L_m, L_{r1}, and L_{r2} as the circuit parasitic inductors. Ideally, the voltage of the absorption capacitor C_3 is equal to half of the DC bus voltage, so the voltage difference between V_{dc} and C_3 is smaller, resulting in a smaller current flowing through the main circuit parasitic inductor L_m; in other words, the smaller the energy stored in the main circuit parasitic inductor L_m. When the low-frequency switching is switched, the RC-CD circuit suppresses the jump in the high-frequency switching input voltage caused by the DC bus capacitor voltage imbalance, thus improving the stability of system operation.

When the input current is positive, the current flows through the diode (D_1) and resistor (R_2) to C_3 and C_4, respectively, and the energy stored in the parasitic inductors will charge capacitors C_3 and C_4, which will reduce the energy flowing into the high-frequency switching input capacitor C_{oss}, thus reducing the high-frequency switching overvoltage. When the voltage on C_3 and C_4 is higher than C_{oss}, the voltage difference starts to drive a negative current, but the negative current will not flow directly into C_{oss}, but through resistor R_1, and the energy will be consumed through resistor R_1, thus reducing the voltage oscillations on the high-frequency switch.

This overvoltage absorption circuit effectively reduces the switching device turn-off overvoltage while oscillation suppressing the oscillation. At the same time, due to the addition of a high voltage capacitor C_3, the input voltage jump on the high-frequency switch can be suppressed during low-frequency switching. During system operation, if the voltages on the DC bus capacitors C_1 and C_2 are 415 V and 385 V, respectively, and the voltage of the high voltage capacitor C_3 is 400 V, When S_1 and S_3 are on, and V_{dc1} serves as the voltage source of the circuit (415 V), as shown in Figure 9a, the C_3 capacitor voltage is lower than that of V_{dc1}, and due to the reduction in the voltage difference, the energy stored in the parasitic inductance is reduced. The energy charged to C_3 and C_4 through the diode (D_1) and the resistor (R_2) will be reduced, and due to the small junction capacitance of the diode (D_1) in the CD loop, it will cause the circuit to have a high-frequency oscillation, but due to the addition of the RC loop, the energy stored in the parasitic inductance can be absorbed on the one hand, and on the other hand, it can inhibit the high-frequency oscillation caused by the junction capacitance of the diode (D_1). When the capacitance voltages of C_3 and C_4 are higher than V_{dc1}, the energy stored in C_3 and C_4 will be consumed by resistor R_1, as shown in Figure 9b, thus reducing the low-frequency oscillation on the

high-frequency switch. When the low-frequency switch switches, S_1 and S_3 turn off, S_2 and S_4 conduct, V_{dc2} is less than the C_3 capacitor voltage, the parasitic inductor is energized, and the high-frequency switch input voltage jump will be effectively suppressed because the absorption capacitor C_3 is kept at a high voltage level, as shown in Figure 9c. When the V_{dc2} voltage is higher than the C_3 capacitor voltage, the stored energy of the parasitic inductor will energize C_3 and C_4 through the diode (D_1) and the resistor (R_2), as shown in Figure 9d.

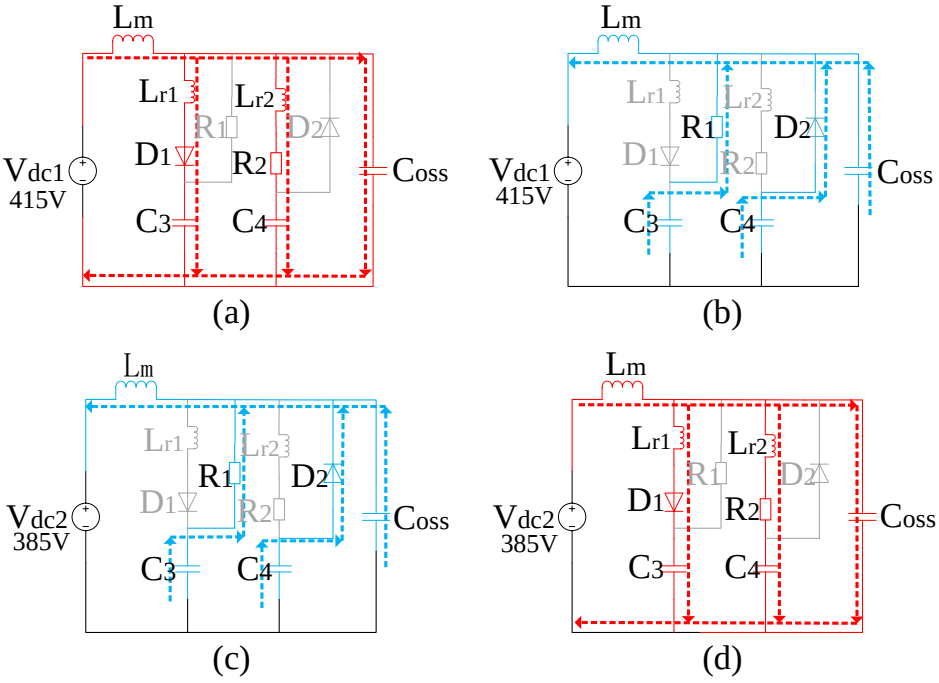


Figure 9. (**a**) When the capacitor voltage in the upper DC bus is high, current flows to the overvoltage absorption circuit. (**b**) When the capacitor voltage in the overvoltage absorption circuit is higher, current flows to the upper DC bus capacitor. (**c**) After low-frequency switching, the higher capacitor voltage in the overvoltage absorption circuit causes current to flow to the lower DC bus capacitor. (**d**) A higher capacitor voltage in the lower DC bus than in the overvoltage absorption circuit causes current to flow to the overvoltage absorption circuit.

In this paper, the hybrid modulation strategy in the long-loop mode is adopted, which results in a larger loop parasitic inductance. Although a larger loop parasitic inductance increases the switching device turn-off voltage, a larger loop parasitic inductance can reduce the switch on-state voltage and improve the switching response speed. Assuming that the main circuit parasitic inductance L_1 and the branch circuit parasitic inductance L_2 are the same, the inductors L_1 and L_2 store the same amount of energy, and when the switch turns on, the energy stored in L_2 will be released to the high-frequency switch, resulting in too high a voltage at the time of the high-frequency switch turn-on, and the overvoltage absorber circuit (RC) has to be used to lower the on-state voltage. However, when the parasitic inductor L_1 in the main circuit is much higher than the branch parasitic inductor L_2, the inductor L_1 will store a large amount of energy, while the energy stored in L_2 will be very limited. When the switch is on, the energy stored in the parasitic inductor L_1 will be absorbed only on the DC side of the high-frequency half-bridge, and there is no need for an additional over-voltage absorber circuit. and The high-frequency switch on-conducting voltage will be suppressed very well without causing damage to the switch.

The conclusion is drawn from the simulation experiment, which is consistent with the analysis results. As shown in Figure 10, when the parasitic inductance is low, the power device on-current curve is the red curve in the figure. When the parasitic inductance is high, the power device on-current curve is the yellow curve in the figure. In the low parasitic

inductance circuit, add the RC damping circuit; its on-current curve is the blue curve. It can be seen that when the loop parasitic inductance is high, there is no need to introduce an additional RC damping circuit, and at the same time, the higher parasitic inductance helps to optimize the power device on-state characteristics and reduce the power device on-state loss.

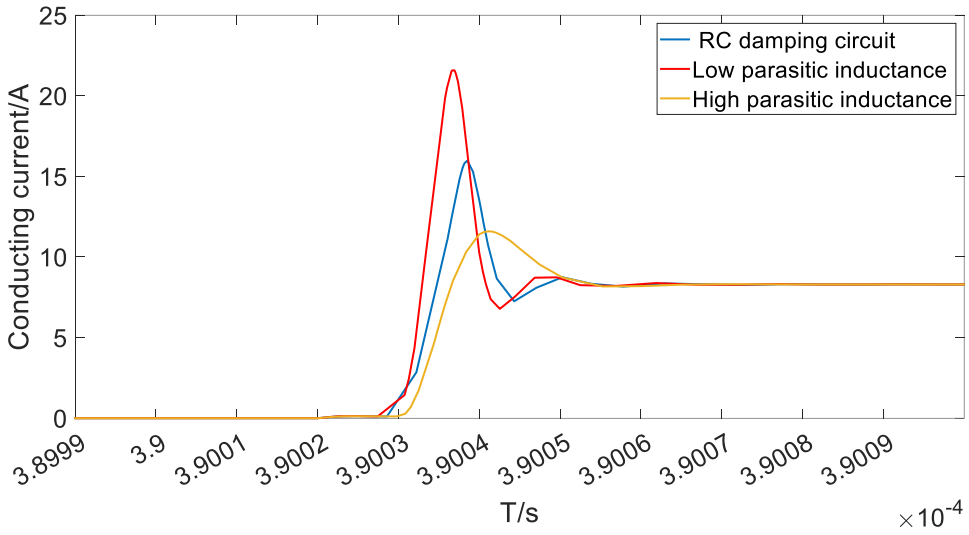


Figure 10. Current waveforms of different inductors in the loop.

4. Application System Design

4.1. Parasitic Parameter Extraction

In the three-level ANPC, due to the complexity of the device, and this paper chooses the long-loop modulation method as the object of this study, it is inevitable to introduce more parasitic inductance and parasitic resistance; however, the parasitic parameters play a key role in the voltage overshoot of the switching device. Therefore, in the process of circuit simulation, it is very necessary to consider the parasitic parameters. about The extraction of parasitic parameters in the previous study did not mention that in the inverter work, the frequency will also have an impact on the parasitic parameters. This paper through the establishment of an electromagnetic field simulation model and electromagnetic field finite element analysis.

Parasitic inductance and parasitic resistance are the main parasitic parameters, in the previous study, although the parasitic parameters are mentioned, the source of parasitic parameters is not analyzed, in [4] it is mentioned that the parasitic parameters of switching devices are introduced according to the datasheets, in the actual circuit, especially the current converter circuits in the three-level ANPC inverter system are complex, the data obtained from the datasheets differ from the actual circuit parasitic parameters, and this difference will lead to changes in the switching characteristics, in this paper, the magnetic field finite element analysis of the circuit is carried out by using electromagnetic field simulation software to obtain the parasitic parameters between the nodes of the circuit at a frequency of 100 kHz, and to establish the electromagnetic field simulation model of the corresponding circuit, as shown in Figure 11, where the copper curve replaces the capacitance in the established simulation model, where the green dashed box is the switching module, the blue color represents switching conduction, and the gray color represents switching off. Where A, B, and C correspond to the O, P, and N states of the circuit, respectively, and the desired parasitic parameters can be measured by measuring the nodes between A-3, 2–5, B-1, 4–7, and 6-C.

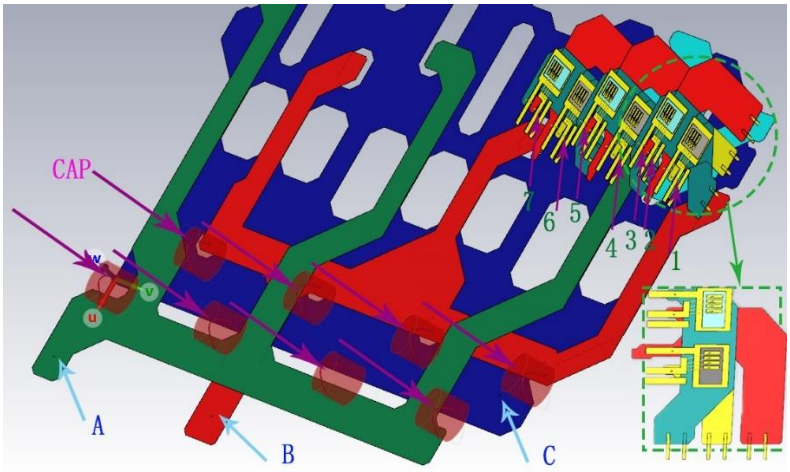


Figure 11. Analysis of the three-level ANPC Electromagnetic Field Model.

4.2. Parameter Selection

Suitable component parameters allow the damping circuit to be utilized to greater advantage, reducing overvoltage while suppressing oscillations. By analyzing the trend of overvoltage and oscillation with the variation in damping parameters, the preliminary component parameters can be derived. Through the parameter scanning, it is learned that capacitor C_4 has a greater impact on the switch-off overvoltage; as shown in Figure 12, the maximum voltage on the switching device decreases with the increase in capacitance C_4. After the capacitance value of C_4 is larger than 25 nF, the overvoltage absorption is not ideal, and it will also increase the size of the inverter and reduce the power density. Smaller capacitance values also do not have the effect of absorbing the overvoltage. In summary, the optimal parameter for capacitor C_4 is 25 nF, and using the same methodology, the values of C_3, R_1, and R_2 will also be determined (C_3 = 4 nF, C_4 = 25 nF, R_1 = 350 Ω, and R_2 = 40 Ω).

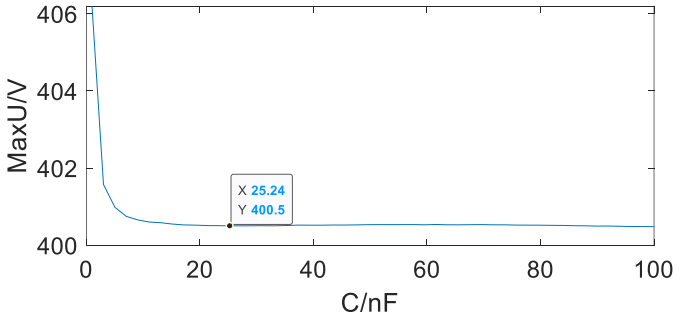


Figure 12. Maximum switch voltage at different C_4.

5. Experimental Results

5.1. Experimental Preparation

In this paper, a new overvoltage absorption scheme is proposed, as shown in Figure 10, which is used to suppress the overvoltage and oscillation of the switching devices during inverter operation. The setup hardware is a GaN-based three-phase ANPC inverter power stage design module (TIDA-010210) using two GaN HEMT modules on the DC side of the inverter (S_1ccS_2 and S_3, S_4), a Si MOSFET module connected in parallel on the AC side of the inverter (S_5 and S_6), and an 800 V DC voltage provided on the DC bus, which theoretically In theory, the two capacitors (C_1 and C_2) on the DC side will be subjected to 400 V. At the same time, this power design module uses a short-loop modulation scheme. During the operating phase, the value of the parasitic inductance in the circuit is much smaller than that of the long-loop modulation scheme, and the energy stored in the parasitic

inductance is smaller, resulting in a smaller switch-off overvoltage, so the original scheme adopts a simpler overvoltage absorption circuit. However, in order to reduce the cost of the inverter, the article proposes a scheme that uses a long-loop modulation scheme instead of the original scheme, where two Si MOSFET modules are used on the DC side of the inverter (S_1, S_2 and S_3, S_4), and one GaN HEMT module is connected in parallel on the AC side of the inverter (S_5 and S_6). The long-loop modulation scheme involves longer operating loops and more switching devices, which will lead to a larger parasitic inductance in the circuit, which in turn will substantially increase the switch-off overvoltage. and the original overvoltage absorber circuit is obviously no longer able to satisfy the demand, and new overvoltage absorber circuits need to be designed in order to reduce the switch-off overvoltage. The specific parasitic inductance value can be measured from Section 4, which is a process of visualizing the parasitic inductance and intuitively perceiving that the parasitic inductance in the long-loop is much larger than that in the short loop.

For the high switching frequency of the 100 kHz inverter used, a second modulation method is applied to the three-level ANPC unit in order to reduce the total switching losses of the three-level ANPC and to improve the efficiency. The proposed switching pattern is shown in Figure 13. The switching pattern of the three-level ANPC unit is a decoupled two-stage low-frequency and high-frequency modulation scheme. The LF (S_1, S_3) and (S_2, S_4) switching signals are generated by the over-zero detector as follows:

$$Z_c = \begin{cases} 1, & V_{ref} \geq 0 \\ 0, & V_{ref} < 0 \end{cases}$$

$$S_1 = S_3 = \overline{S_2} = \overline{S_4} = Z_c$$

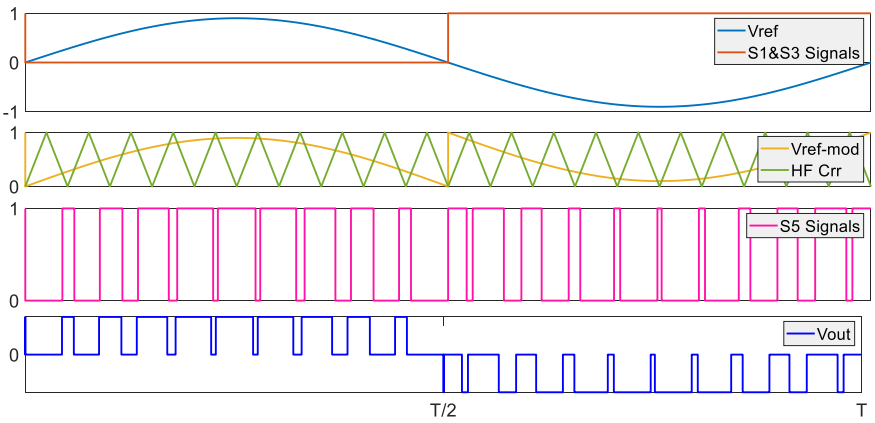


Figure 13. Three-level ANPC switching signal modulation.

Therefore, the LF (S_1, S_3) and (S_2, S_4) switches operate at the fundamental frequency.

To generate the high-frequency (S_5, S_6) switching signals, the modified reference voltage is defined as:

$$V_{ref-mod} = \begin{cases} V_{ref}, & V_{ref} \geq 0 \\ 1 + V_{ref}, & V_{ref} < 0 \end{cases}$$

The proposed switching pattern for each phase ANPC is shown in Figure 14, where the high-frequency triangular carrier signal of one phase is phase-shifted by $2\pi/3$ radians to generate a high-frequency switching signal for each three-level ANPC branch. The high-frequency signals are made to commutate only at 100 kHz to meet the desired requirements of the device. At the same time, each phase generates a 3-level output voltage. Thus, the number of output line-line voltage levels is 7, which makes the three-phase inverter have high power quality, and the load current is uniformly distributed in each branch of the three-level ANPC.

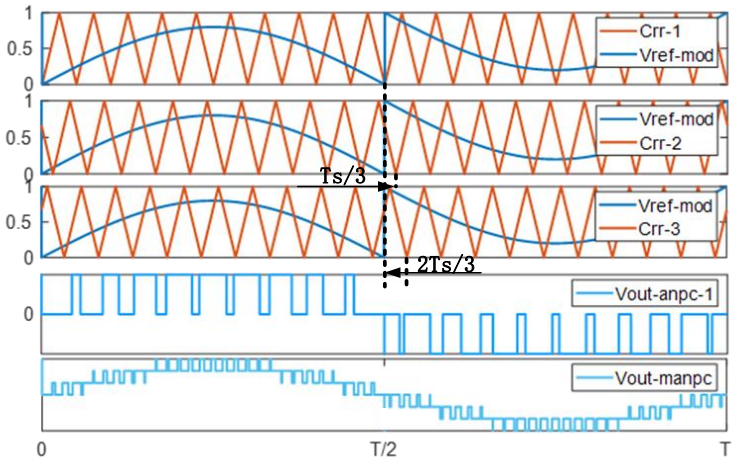


Figure 14. Switching mode of parallel three-level ANPC.

5.2. Test Results

From the experimental results, it can be seen that when no program is used to deal with the DC bus capacitor voltage, as shown in Figure 15a, the charging and discharging frequencies of the upper and lower capacitors are too high, and the voltage float is large. In low-frequency current exchange, the large voltage difference will cause a large current impact on the high-frequency switching device, which will damage the high-frequency switching device in serious cases. After using the overvoltage absorption circuit proposed in this paper, the DC bus capacitor voltage is shown in Figure 15b, the upper and lower capacitor charging and discharging frequencies are reduced, and at the same time, the voltage fluctuation is small, which will prolong the service life of the capacitor and improve the reliability of the inverter. In the event of low-frequency current switching, this circuit will reduce the current shock received by the high-frequency switch.

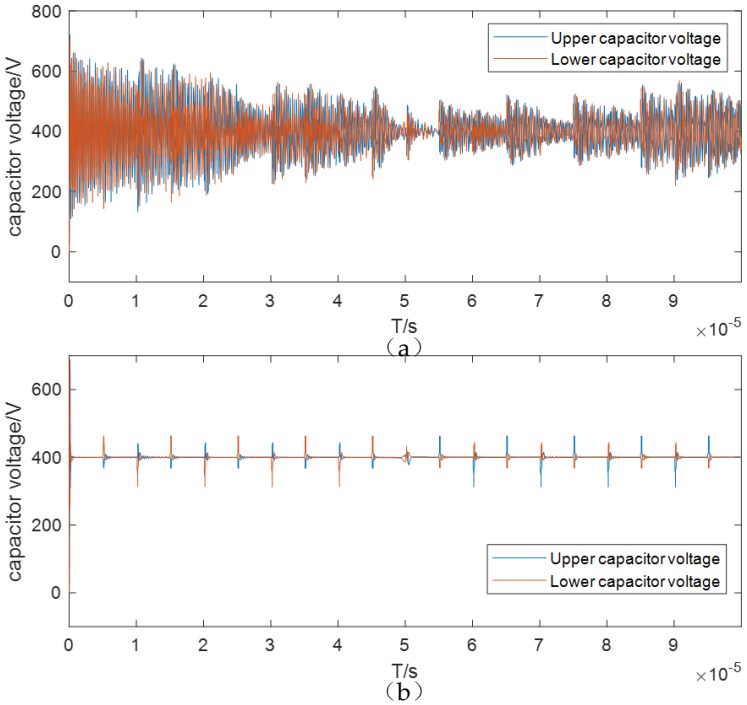


Figure 15. (**a**) DC bus capacitor voltage waveform without any scheme. (**b**) DC bus capacitor voltage waveform with the scheme proposed in this paper.

Based on the optimum component parameters obtained in Section 4, the optimum switching voltage waveform is obtained as shown in Figure 16. The maximum voltage is 400.5 V, and the oscillations are well-suppressed.

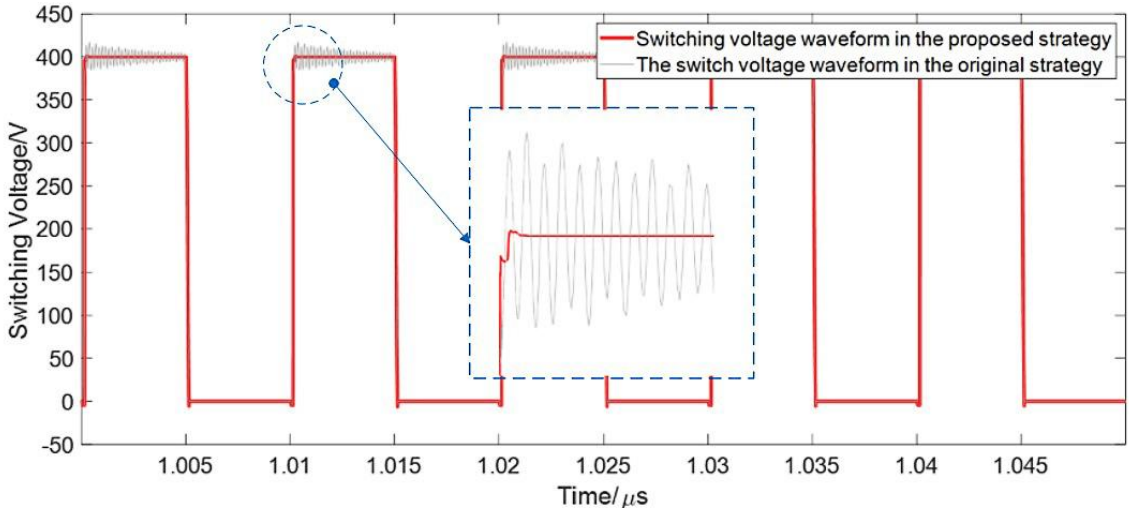


Figure 16. Switching off voltage waveform under optimal component parameter conditions.

6. Discussions

In this paper, a new overvoltage absorption circuit is proposed that is distinguished from the traditional overvoltage absorption circuit and realizes the functions of reducing overvoltage and suppressing oscillation at the same time. Traditional overvoltage absorber circuits (e.g., RC, C-RC, and R-CD) have a significant effect on reducing overvoltage or suppressing oscillations; however, with the increase in switching device operating frequency and operating voltage, the traditional overvoltage absorber circuits cannot meet the demand of inverters better. In order to reduce the switching loss and improve the efficiency of the inverter, this paper proposes an optimization of the overvoltage absorption circuit, which has two main circuits, absorbing the overvoltage on the one hand and releasing the overvoltage on the other. The main idea is that when the high-frequency switch is turned off, the absorption circuit absorbs the power stored in the parasitic inductor to reduce the switch-off overvoltage. Then, the release circuit feeds the stored power back into the DC bus capacitor through a diode. This has the advantage of releasing this excess power to the DC bus capacitor instead of charging and discharging it between the switching output capacitor and the capacitor in the overvoltage absorption circuit. On the other hand, the voltage of the upper and lower DC bus capacitors can be balanced by the release circuit to reduce the current impact on the high-frequency switch due to the voltage imbalance of the DC bus capacitors during low-frequency current conversion.

In this paper, a hybrid modulation strategy is also used, and the long-loop hybrid modulation mode is very suitable for the study due to the consideration of cost as well as efficiency. The cost and efficiency of the hybrid modulation mode are studied in detail in [26–28], where a large number of studies have proved that the hybrid modulation mode is undoubtedly the best solution to reduce the cost of the inverter, and the cost can be reduced by nearly half in the hybrid modulation mode of Si and SiC.

Although the cost can be reduced by using hybrid modulation mode, more parasitic inductance is introduced in the long-loop mode, which is detrimental to the reduction in the switch-off overvoltage and requires a redesign to optimize the overvoltage absorption circuit. While investigating the effect of high parasitic inductance on overvoltage, we find that higher parasitic inductance is beneficial for reducing the on-state current and also reduces the switch on-time, which can be further investigated for the effect of high parasitic inductance on the switch on-state loss. This phenomenon is slightly shown in Figure 10 of this paper, and it can be seen that high parasitic inductance significantly reduces the peak

current during switch on-time compared with low parasitic inductance, and the oscillation time is shorter.

At the moment of low-frequency current exchange, the size of the capacitor C_3 in the voltage absorption circuit directly affects the input voltage of the high-frequency switch. As shown in Figure 17, the high-frequency switch-off overvoltage is negatively correlated with the size of the capacitor C_3, and the optimal capacitance size is proposed by synthesizing the hardware cost and circuit layout through experimental data.

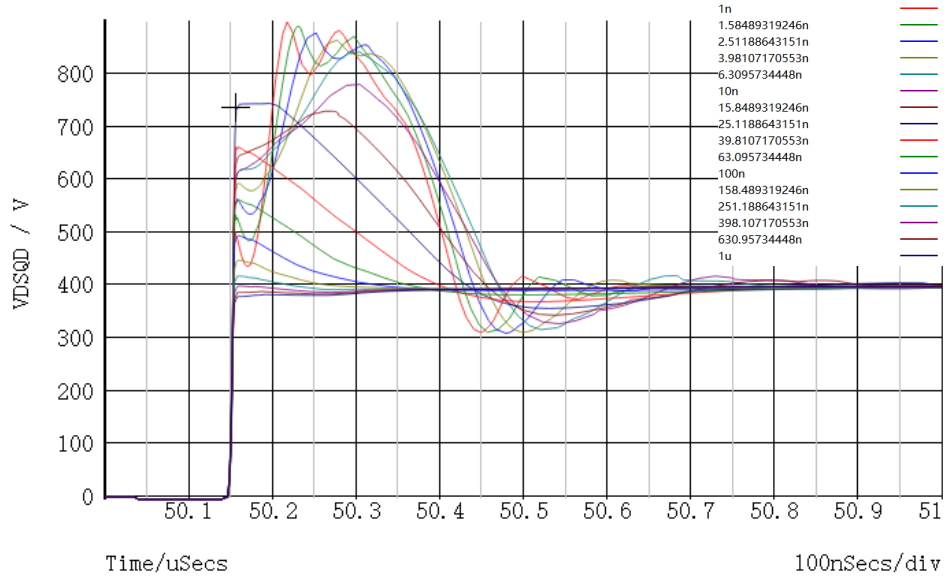


Figure 17. Effect of capacitor C_3 on high-frequency switching overvoltage.

In future research, it can be demonstrated experimentally that the value of parasitic inductance will balance the switch-off overvoltage and the switch conduction current, which will provide supporting data for further optimization of the overvoltage absorption circuit, thus reducing the switch-off loss and conduction loss and improving the efficiency of the inverter.

7. Conclusions

In this paper, a new overvoltage absorption circuit based on the 3L-ANPC hybrid modulation mode is presented, and in order to have a better observation of the high-frequency switching overvoltage phenomenon in the inverter, the corresponding three-dimensional electromagnetic simulation model is established to measure the value of the parasitic inductance in the circuit at a frequency of 100 kHz. Therefore, when analyzing the switching overvoltage, the influence of the parasitic inductance on the switch-off overvoltage at the actual operating frequency will have to be considered. The phenomenon of DC bus capacitor voltage imbalance can be determined by calculating the neutral current, and it can be seen that the DC bus capacitor voltage imbalance will reduce the efficiency of the inverter, and at the same time, the DC bus capacitor voltage imbalance will lead to a power switching loss imbalance. The long-loop hybrid modulation mode reduces the hardware cost by almost half compared with the short loop hybrid modulation mode, and the parasitic inductance of the long-loop hybrid modulation mode is multiplied due to the longer commutation loop, which will bring the switching overvoltage to a new high level, and we do not want to see such a serious overvoltage in the simulation and experimental process. The switch-off overvoltage is more sensitive to the parasitic inductance, and both the main circuit and branch circuit parasitic inductance should be taken into account. Conventional overvoltage absorption circuits provide guidance for the proposed scheme in this paper. Synthesizing the advantages shown by conventional overvoltage absorption

circuits [21,24,25], this paper introduces a novel overvoltage absorption circuit and analyzes its working principle. The advantages of this circuit include:

(1) Lower cost because the number of GaN power switching devices is smaller using the long-loop hybrid modulation technique.
(2) A smaller value of capacitance used, allowing the inverter to have a smaller size and increased power density.
(3) The C_3 capacitor voltage in this overvoltage absorption circuit is slightly higher than the theoretical DC bus capacitor voltage, which does not cause high-frequency switching input voltage jumps during low-frequency switching.

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