machines

MDPI

Article

Analysis and Improved Behavior of a Single-Phase Transformerless PV Inverter

Panfilo R. Martinez-Rodriguez [1], Gerardo Vazquez-Guzman [2,*], Gerardo O. Perez-Bustos [2], Jose M. Sosa-Zuñiga [2], Dalyndha Aztatzi-Pluma [3], Adolfo R. Lopez-Nuñez [2] and Christopher J. Rodriguez-Cortes [1]

1 School of Sciences, Universidad Autonoma de San Luis Potosi (UASLP), San Luis Potosi 78295, SLP, Mexico; panfilo.martinez@uaslp.mx (P.R.M.-R.); cjrcortes@ieee.org (C.J.R.-C.)
2 Laboratory of Electrical and Power Electronics, Tecnologico Nacional de Mexico/ITS de Irapuato, Irapuato 36821, GTO, Mexico; mip22110003@irapuato.tecnm.mx (G.O.P.-B.); adolfo_lopez@ieee.org (A.R.L.-N.)
3 Department of Mechatronics Engineering, Tecnologico Nacional de Mexico/ITS de Abasolo, Abasolo 36976, GTO, Mexico; dalyndha.ap@abasolo.tecnm.mx
* Correspondence: gerardo.vazquez@ieee.org

Abstract: Transformerless inverters have an important role in the electrical energy market. The high-efficiency and reliable inverter concept is one of the most widely used inverters in single-phase photovoltaic systems because of its high efficiency, low cost, and reduced leakage ground current. However, the leakage ground current behavior depends on the power and weather conditions, which can increase the parasitic capacitance value, thus producing an increase in the leakage ground current magnitude. In this paper, it is proposed to add a passive inductive–capacitive output filter to the inverter structure in order to reduce the dependency of the leakage ground current on the system power and weather conditions. The inductive–capacitive output filter is designed in such a way that it can provide a low impedance path for the leakage ground current, different from the ground path. The proposed system was evaluated both through simulations and experimentally in a 1 kW laboratory prototype.

Keywords: HERIC inverter; leakage ground current; passive filter; photovoltaic; transformerless

Citation: Martinez-Rodriguez, P.R.; Vazquez-Guzman, G.; Perez-Bustos, G.O.; Sosa-Zuñiga, J.M.; Aztatzi-Pluma, D.; Lopez-Nuñez, A.R.; Rodriguez-Cortes, C.J. Analysis and Improved Behavior of a Single-Phase Transformerless PV Inverter. *Machines* **2023**, *11*, 1091. https://doi.org/10.3390/machines11121091

Academic Editor: Davide Astolfi

Received: 16 November 2023
Revised: 6 December 2023
Accepted: 12 December 2023
Published: 16 December 2023

1. Introduction

Transformerless inverters are widely implemented in photovoltaic (PV) generation systems due to their high efficiency and low cost. However, the common mode behavior problem arises when there is no galvanic isolation in the coupling between the inverter and the electrical grid [1]. Then, leakage ground currents (LGCs) circulate through the system due to the fast dynamic variations of the voltage across the equivalent parasitic capacitance formed at the PV panel. The LGC behavior depends on several factors, for instance, moisture, system size, dust, and the PV panel structure, among others. These conditions and parameters establish the magnitude of the parasitic capacitance which has been studied, determining values from 60 nF/kW to 160 nF/kW according to references [2,3]. On the other hand, the LGC represents a safety and operation risk since it could be responsible for tripping protections or injuring users in contact with the PV system. Thus, there are several international norms that impose limits to the LGC, for instance, 300 mA_{RMS}, according to the German Standard DIN VDE 0126-1-1 [4].

The literature reports a wide range of solutions dealing with the LGC which, in general, can be classified as follows:

1. Redesign of the topology [5,6].
2. Design of a specific pulse width modulation (PWM) sequence [7].
3. Methods based on the design of the output filter [8].

4. Virtual grounding techniques [9].
5. Control techniques [10].

For transformerless single-phase PV power converters, a popular solution, based on modifying the inverter topology, is presented in [11], where an H-bridge is used with an additional switch on the DC side. The fifth switch is used to perform a decoupling action during the freewheeling periods of the load current, thus achieving a constant common mode voltage (CMV) and consequently reducing the magnitude of the LGC. A solution, based on the implementation of a bidirectional switch on the AC side, is presented in [12], where the topology is called the Highly Efficient and Reliable Inverter Concept (HERIC). The main idea is the same as that presented in [11], but in this case, the freewheeling period is enabled by the bidirectional switch, allowing constant common mode voltage and the reduction in the LGC. The HERIC inverter has been the object of study in several contributions reported in the literature, for instance, an improvement based on the design of the PWM strategy for the HERIC inverter is presented in [13]. Here, the authors proposed a hybrid unipolar PWM strategy to simultaneously achieve high efficiency, low harmonic distortion and reactive power management. During the positive half-cycle, the converter operates with the conventional unipolar PWM; however, during the negative half-cycle, a PWM using only the freewheeling switches is proposed. Moreover, the output voltage and the zero-crossing points of the inverter are improved by modifying the dead times of the PWM strategy. In [14], an improvement behavior regarding LGC for the HERIC inverter is proposed. The improvement is based on the modification of the topology, where an additional switch is implemented to connect the bidirectional switch to the midpoint of the input capacitor. Then, better common mode voltage and LGC performance is achieved; however, an additional cost is introduced to the inverter. Moreover, in [15], an improvement to the HERIC-based topology presented in [14] is proposed. Here, a PWM strategy is designed to provide flexible power compensation and also to compensate for the effects of the dead time and the distortions produced by the minimum pulse width of the PWM signals. Furthermore, in [16], a zero-voltage-transition (ZVT) HERIC inverter is proposed, where resonant tanks are implemented around the high-frequency switch. Resonant tanks mainly contribute to improve efficiency; however, additional resonant active–passive cells must be added to the inverter structure, making it costly. On the other hand, in [17], the leakage current reduction for a single-phase grid-interfaced inverter is proposed. The full-bridge inverter is modified by introducing an AC passive filter capable of operating bidirectionally and reducing the leakage current at the DC side while improving the EMI (Electromagnetic Interference) noise. However, six inductances plus three capacitances are used, and the robustness of the inverter against changes in the parasitic capacitance is not validated. In [8], the cascade multilevel inverter is analyzed to propose two passive filter-based solutions to mitigate the leakage ground current. The first solution introduces common mode chokes in both the AC-side and the DC-side, reducing the LGC magnitude at the two common mode loops formed in the structure of the cascade multilevel inverter. The second solution keeps the common mode chokes introduced in the first solution but adds two capacitors connected to the output of the inverter in parallel with the grid, whose middle point is connected to the middle point of the capacitor at the DC-side. Both methods effectively reduce the LGC; however, multiple passive components are used in the system. Reference [18] presents a solution for a three-phase system with the neutral point connected to the middle point of the DC link for modular multilevel converters, where this connection induces a zero-sequence circulating current resonance issue. The proposed solution for the LGC issue is a bypass capacitor applied to the parallel inverters with common AC and DC bus, ensuring the reduction in the LGC magnitude. In this paper, a new structure for the HERIC inverter based on the common mode model is proposed. The HERIC inverter is modified by providing a low impedance path through two capacitors, thus achieving a noticeable reduction in the leakage ground current magnitude. Therefore, no additional active or passive circuits are added, considering that a passive LCL filter is conventionally included in the inverter system, keeping the proven high efficiency

and improving the leakage ground current performance. The main contributions of this paper are the following:

1. An improved LC output filter is included in order to improve the LGC mitigation capability of the HERIC converter.
2. It is demonstrated through the mathematical models of common mode and differential mode that the modified LC filter improves the LGC mitigation capability.
3. The improvement of the LGC behavior by eliminating the dependency on power, size and weather conditions without the use of additional power semiconductors, special control design or specific modulation strategies.

2. Inverter Description and PWM Strategy

The topology under study, which is composed of a full bridge inverter with a bidirectional switch on the AC side, is shown in Figure 1 [12]. The main function of the bidirectional switch is to provide an output current path during the freewheeling states of the inverter. The list of all possible operation states is shown in Table 1.

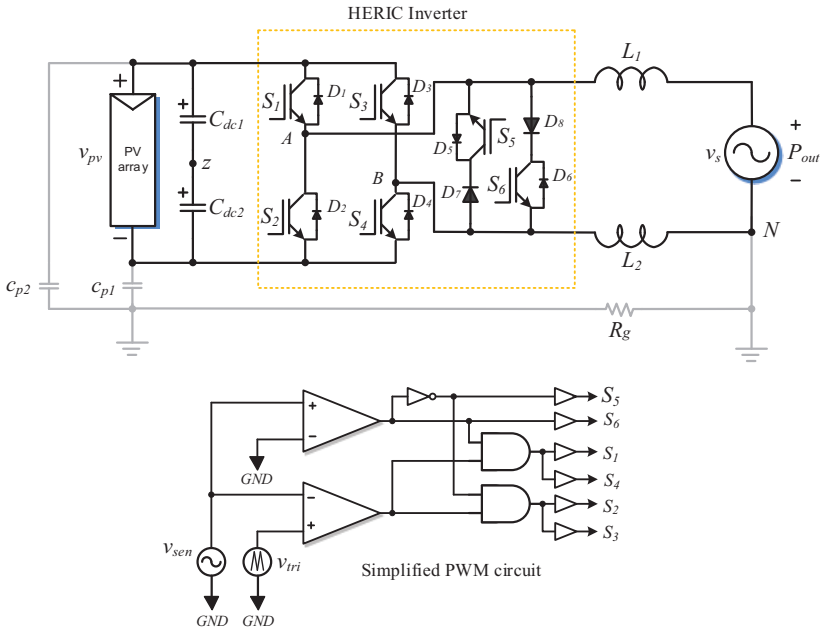

Figure 1. Simplified circuit of the topology under study and its simplified PWM circuit.

Table 1. Summary of the operation states of the HB-HERIC inverter.

State	S_1	S_2	S_3	S_4	S_5	S_6	V_{Az}	V_{Bz}	V_{AB}	V_{cm}
1	1	0	0	1	1	0	V_{pv}	0	V_{pv}	$V_{pv}/2$
2	1	0	1	0	1	0	V_{pv}	V_{pv}	0	V_{pv}
3	0	0	0	0	1	0	-	-	0	0
4	0	0	0	0	0	1	-	-	0	0
5	0	1	0	1	0	1	0	0	0	0
6	0	1	1	0	0	1	0	V_{pv}	$-V_{pv}$	$-V_{pv}/2$

The freewheeling state is enabled by disconnecting the four switches, S_1 to S_4, and connecting either S_5 or S_6 of the AC bidirectional switch, depending on the current direction. Conventionally, the states **1**, **2**, **5** and **6** are used to synthesize a three-level output voltage delivered by the inverter to the AC side. The signals to modulate the inverter are typically generated by a conventional PWM strategy that adds a simple digital circuit to generate the signals for switches S_1 to S_6 according to Figure 1. The proposed PWM control signals for the HERIC converter based on the states described in Table 1 are depicted in Figure 2.

As it can be noted, during half a period of the grid, the switches S_5 and S_6 do not perform any switching, and as a consequence, during the positive half period, only switches S_1 and S_4 are operating. A similar situation can be observed for the negative half period.

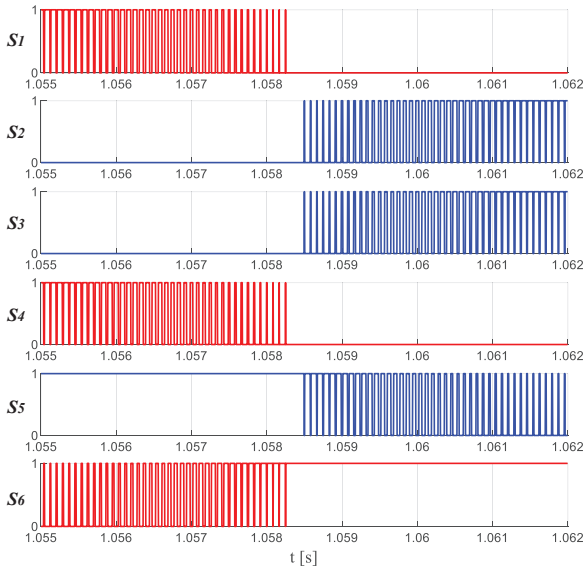

Figure 2. Modulation signals for the HERIC inverter.

3. Proposed Passive Method

The proposal is aimed at reducing the LGC by taking advantage of the properties that output filter passive elements present at different frequencies. Capacitors decrease their reactance as the frequency increases; if their capacitance value is high, the reactance reduction is greater. On the other hand, LGC in photovoltaic circuits occurs at frequencies higher than the switching frequency, which is typically on the order of kHz. Hence, it is proposed to place a new capacitive path for the flow of the LGC. Thus, the possibility of providing the LGC with a capacitive path arises, and in this way, enabling to return it without injecting it into the electrical grid.

The connection of the new trajectory can be seen in Figure 3, where the LGC flows from the photovoltaic panels to the grid and returns through the ground connection. The proposed route joins each output of the photovoltaic inverter with the positive and negative bus of the photovoltaic array using a capacitor. Hence, the capacitor is acting with a low impedance for these high-frequency currents, allowing their circulation and blocking all low-frequency current components, and is also preventing the flow of direct current due to the connection of the DC bus.

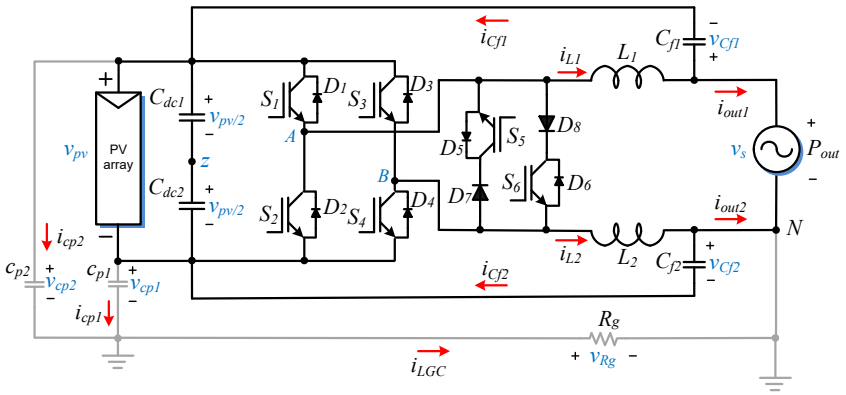

Figure 3. The HERIC inverter with the proposed output filter modification.

3.1. Common and Differential Mode Models

To analyze the behavior of the proposed passive trajectory and its influence on the LGC compensation, a mathematical modeling of the system is performed. The modeling technique is based on the well-known Kirchhoff's currents and voltages analysis, and yields

$$L_1\hat{\dot{i}}_{L1} = v_{Az} - v_{Cf1} - \frac{v_{pv}}{2}, \tag{1}$$

$$L_2\hat{\dot{i}}_{L2} = v_{Bz} - v_{Cf2} + \frac{v_{pv}}{2}, \tag{2}$$

$$C_{f1}\dot{v}_{Cf1} = i_{L1} - i_{out1}, \tag{3}$$

$$C_{f2}\dot{v}_{Cf2} = i_{L2} - i_{out2}, \tag{4}$$

$$i_{LGC} = c_{p1}\dot{v}_{cp1} + c_{p2}\dot{v}_{cp2}, \tag{5}$$

$$v_{pv} - v_s = v_{Cf2} - v_{Cf1}, \tag{6}$$

where the following restrictions for the capacitor voltages are considered:

$$v_{Cf1} = v_s - v_{cp2} - v_{Rg}, \tag{7}$$

$$v_{Cf2} = -v_{cp1} - v_{Rg}. \tag{8}$$

As is common practice in this kind of systems analysis, the values of the capacitors are assumed to be equal $C_{f1} = C_{f2} = C_{fT}$, and the values of the inductors are also assumed to be equal $L_1 = L_2 = L$. Also, the parasitic capacitances are considered of the same value, $c_{p1} = c_{p2} = c_{pT}$. Notice also that the DC input voltage of the converter is considered constant or with slow dynamic and is denoted by v_{pv}.

The output filter is designed by means of the common mode and differential mode variables and considering the following definitions:

$$v_{cpT} \triangleq \frac{v_{cp1} + v_{cp2}}{2}, \tag{9}$$

$$v_{CfT} \triangleq \frac{v_{Cf1} + v_{Cf2}}{2}, \tag{10}$$

$$v_{cm} \triangleq \frac{v_{Az} + v_{Bz}}{2}, \tag{11}$$

$$v_{dm} \triangleq v_{Az} - v_{Bz}, \tag{12}$$

$$i_{cm} \triangleq i_{L1} + i_{L2}, \tag{13}$$

$$i_{LGC} \triangleq i_{out1} + i_{out2}, \tag{14}$$

$$i_{idm} \triangleq \frac{i_{L1} + i_{L2}}{2}, \tag{15}$$

$$i_{rdm} \triangleq \frac{i_{out1} + i_{out2}}{2}, \tag{16}$$

where v_{cpT} is the total common mode voltage of the parasitic capacitance, v_{CfT} denotes the total common mode voltage of the filter capacitors, v_{cm} is the common mode voltage of the inverter, v_{dm} is the output differential voltage, i_{icm} denotes the common mode current at the inverter side, i_{LGC} is the leakage ground current at the ground path, i_{idm} is the differential current at the inverter side, and i_{rdm} is the differential current at the grid side.

According to the previous analysis related to the electrical variables and considering the definitions (9)–(16), a change of variables can be used to obtain the common mode and differential mode models for the output filter. As a result, the differential mode model can be defined by Equation (17) as follows:

$$2L\dot{\hat{i}}_{idm} = v_{dm} - v_s. \tag{17}$$

The equations that describe the common mode model are as follows:

$$\frac{L}{2}\dot{\hat{i}}_{cm} = v_{cm} - v_{CfT}, \tag{18}$$

$$2C_{fT}\dot{v}_{CfT} = i_{cm} - i_{LGC}, \tag{19}$$

$$2c_{pT}\dot{v}_{cpT} = i_{LGC}, \tag{20}$$

$$v_{CfT} = -v_{cpT} - v_{Rg} + \frac{v_s}{2}. \tag{21}$$

Taking into account the restrictions related to the capacitors of the output filter, it is possible to simplify the common mode model equations to obtain a new set of two equations, which are (22) and (23), defined as follows:

$$\frac{L}{2}\dot{\hat{i}}_{cm} = v_{cm} + v_{cpT} + v_{Rg} - \frac{v_s}{2}, \tag{22}$$

$$2C_{fT}\dot{v}_{cfT} = i_{cm} - 2c_{pT}\dot{v}_{CpT}. \tag{23}$$

From Equation (17), it is possible to derive an equivalent differential mode circuit, which is shown in Figure 4a, and from Equations (22) and (23), the common mode circuit depicted in Figure 4b can be also defined.

In the case of the differential mode model from Figure 4a, it is observed that the capacitors proposed for the output filter do not appear, so it can be expected that the addition of these capacitors to the inverter topology does not influence the differential output voltage.

On the other hand, considering the common mode model from Figure 4b, it can be noted that there is a low impedance path provided by the output filter capacitor, which conducts the LGC. This new trajectory avoids the circulation of the LGC throughout the ground path connected between the neutral point of the electrical grid and the terminals of the parasitic capacitors.

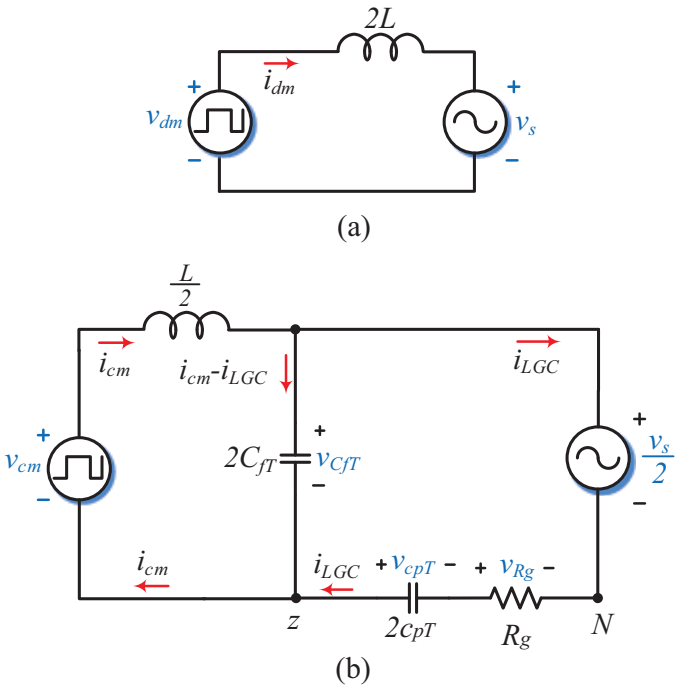

Figure 4. (**a**) Differential mode model, (**b**) common mode model.

3.2. LC Filter Analysis

The structure proposed for the connection of the output filter capacitors allows to take advantage of the frequency dependence behavior of these capacitors, which presents low impedance for LGC frequencies and high impedance to the grid frequency. On the other hand, the frequency behavior of the output inductive filter is also used since the inductor presents low impedance for the grid current and high impedance for the LGC frequency components. The design of this filter is described below.

From Equations (18) and (19), the model based on the state space presented in Equations (24) and (25) can be derived, which represents the behavior of the common mode current and the voltage through the output filter capacitors:

$$\dot{\hat{i}}_{cm} = -\frac{2v_{CfT}}{L} + \frac{2v_{cm}}{L}, \tag{24}$$

$$\dot{v}_{CfT} = \frac{i_{cm} - i_{LGC}}{2C_{fT}}, \tag{25}$$

The transfer function for the relation $I_{cm}(s)/V_{cm}(s)$ can be defined as:

$$G_{cm}(s) = \frac{2sC_{fT}}{LC_{fT}s^2 + 1}, \tag{26}$$

from which the characteristic polynomial is:

$$\Delta_{G_{cm}(s)} = s^2 + \frac{1}{LC_{fT}}. \tag{27}$$

Moreover, the cutoff frequency (ω_c) is:

$$\omega_c = \sqrt{\frac{1}{LC_{fT}}}. \tag{28}$$

From Equation (28), the value of the output filter capacitor C_{fT} can be obtained as a function of the cutoff frequency and the inductor value as follows:

$$C_{fT} = \frac{1}{\omega_c^2 L}. \tag{29}$$

On the other hand, the inductance value can be chosen as a function of the desired current ripple amplitude at the inverter side. The method is described in [19–22], where the analysis is based on the charge and discharge of the inductor. The required inductance value can be determined by means of Equation (30) as follows:

$$L_1 = \frac{v_{pv}}{8\Delta i_{L_{max}} f_c}, \tag{30}$$

where $\Delta i_{L_{max}}$ is the maximum ripple output current peak-to-peak value.

A ripple magnitude of 20% of the nominal current can be considered acceptable, as it guarantees a proper inductor size according to [21,23]. Additional design parameters for LCL filters can be determined from the values reported in [21,24]. From experimental tests, it is considered that the value of $L = L_1 + L_2$ must be lower than 10% than the base impedance defined as $L_b = v_{rms}^2/2\pi f_m S$, where L_b is the base inductance, v_{rms} is the RSM value of the grid voltage, f_m is the grid frequency, and S is the output apparent power.

Considering the above concepts and with 5 kHz as the cutoff frequency for the passive filter, the following values for the passive filter were calculated:

$$L_1 = L_2 = 1.45 \text{ mH}, \tag{31}$$

$$C_{fT} = 13.7 \text{ uF}. \tag{32}$$

In Figure 5, the Bode plot from (26) is presented, where this transfer function and the filter design are validated. As it can be observed, the cutoff frequency is around 5 kHz as established through the design. This means that only high-frequency components are allowed, while low-frequency components, such as the grid frequency, are attenuated.

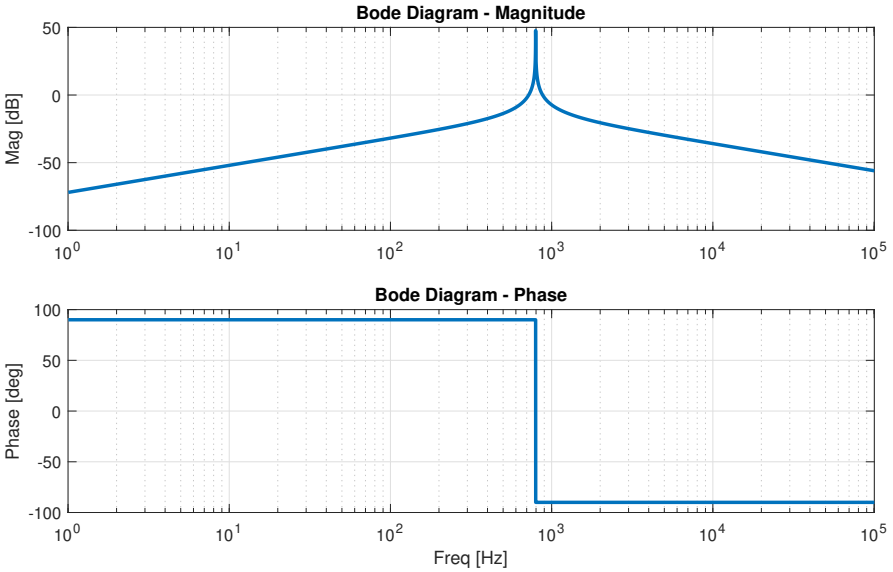

Figure 5. Bode diagram for $G_{cm}(s)$ transfer function.

4. Simulation Results

The numerical simulations were performed using PSIM software. The parameters used for both simulations and experimental test are defined in Table 2. Note that the values of L and C were adjusted according to the values available in the laboratory to have a fair comparison between the simulations and experiments.

Table 2. Converter parameters.

Parameters	Variable	Value
DC input voltage	v_{pv}	220 V
Rated power	S	1 kW
Modulation frequency	f_m	60 Hz
Modulation index	m_a	0.9
Switching frequency	f_c	12 kHz
Dead-time	t_d	4 µs
Active power	P	1 kW
Input capacitor value	C_{pv}	660 µF
Filter capacitor value	$C_{f1,2}$	5 µF
Filter inductor value	$L_{1,2}$	2 mH
Ground parasitic resistance value	R_g	10 Ω
Parasitic capacitance value	$c_{p1,2}$	20–840 nF

In Figure 6a, the output voltage and current behaviors of the inverter without the passive filter are shown. Note that these results were obtained in an open loop with an RL load. Moreover, Figure 6b shows the same variables as in Figure 6a, but now the passive filter is connected. As it can be observed, the proposed output filter is acting as a conventional output filter on the output parameters. Hence, both figures present similar output current and voltage waveforms.

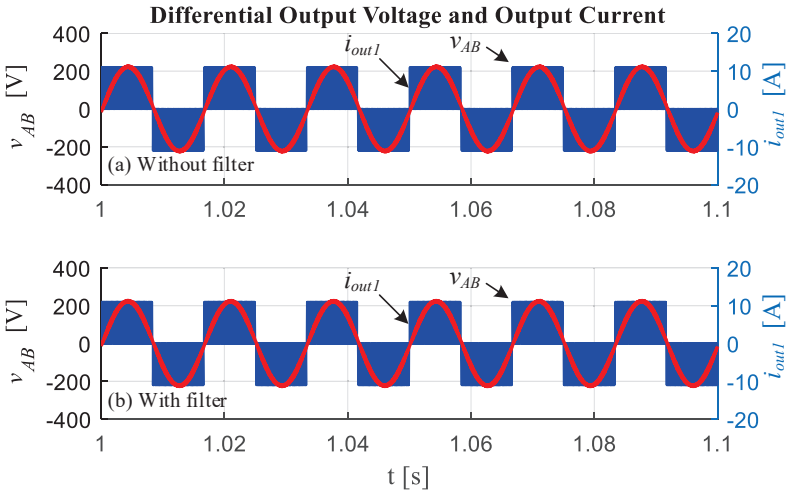

Figure 6. Differential voltage and output current, (**a**) without and (**b**) with filter.

Table 3 shows the THD measured for the load current waveform, where a small difference appears (0.13%) in the THD magnitude, which corresponds to an increase in the current ripple due to the leakage current trajectory provided by the implemented passive filter.

Table 3. THD_i values obtained with the numerical simulations with and without the output LC filter.

THD_i	Value
Without the output filter	2.91%
With the output filter	3.04%

Figures 7 and 8 show the FFT (Fast Fourier Transform) of the output current i_{out1}. The harmonics appearing in these plots correspond to the switching frequency f_c and its multiples. The results in Figure 7 correspond to the system without the passive filter. The harmonic components related to the switching frequency have lower magnitudes than the switching harmonic components of Figure 8 with the system, including the proposed passive filter. This effect is due to the circulating LGC through the power inverter.

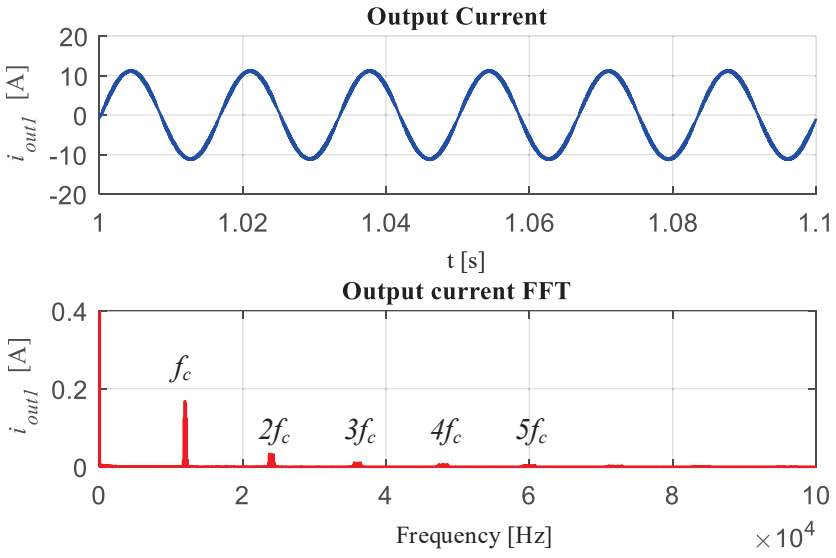

Figure 7. Output current FFT without the proposed filter.

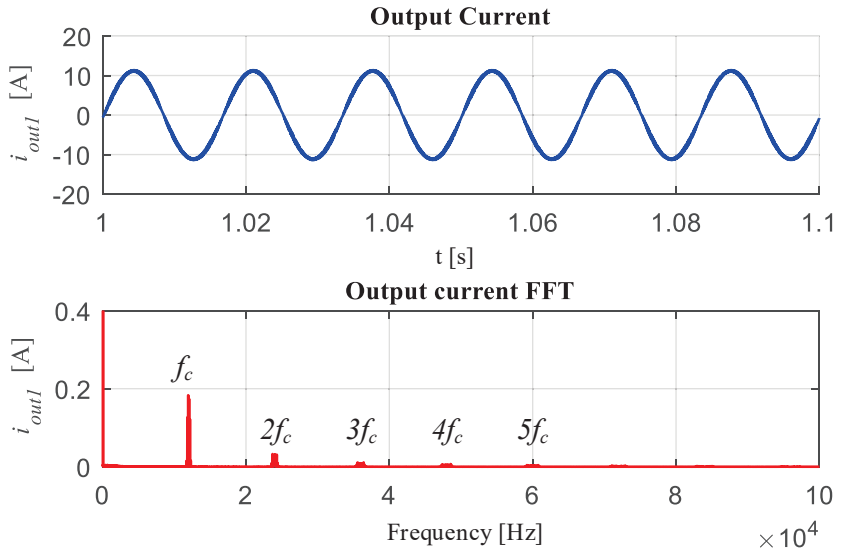

Figure 8. Output current FFT with the proposed filter.

Figure 9 shows the common mode voltage and leakage current behaviors without the connection of the passive filter in the HERIC topology. As it can be observed, there are excursions of the CMV along the grid period, which contribute to produce the LGC shown in the red plot below. The LGC magnitude in this case presents an *RMS* value around 31.24 mA. On the other hand, Figure 10 shows the same electrical variables but with the passive filter connected to the HERIC topology. As it can be noted, the CMV variations are reduced, and as a consequence, the magnitude of the LGC is now around 11 mA_{RMS}. These results demonstrate that, even when the topology is designed to deal with the LGC, it is possible to improve its behavior using a complementary technique without additional cost.

Figure 9. Common mode voltage and common mode current plots without the proposed filter.

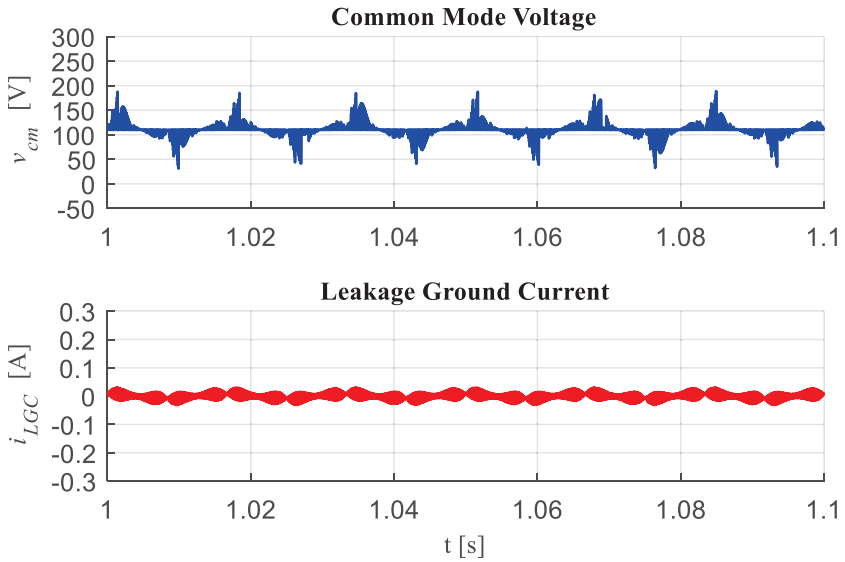

Figure 10. Common mode voltage and common mode current plots with the proposed filter.

Figures 11 and 12 show the dynamic test considering transitions for the output power and parasitic capacitance values, respectively. In Figure 11, from top to bottom, the C_{p1} voltage, C_{p2} voltage, output current and LGC are presented. Note that a power step from 347 W to 1014 W is applied at around 1.05 seconds without any influence on the LGC behavior. Moreover, Figure 12 shows, from top to bottom, the C_{p1} voltage, C_{p2} voltage and LGC under a step change in the parasitic capacitance from 20 nF to 840 nF that occurs at around 1.05 s without any disturbance on both parasitic capacitance voltages. However, the LGC increases from 1.04 mA_{RMS} to 35.41 mA_{RMS} as it is shown in Table 4, and notwithstanding the hard increment on the parasitic capacitance value, the magnitude of the LGC is still under the limit imposed by the international standard. This means that the proposed system is robust against changes in the rated power and increments of the parasitic capacitance value. It is worth noticing that there is a current spike when the parasitic capacitance value is increased, which corresponds with the general definition of the capacitor current; however, in a real implementation, the capacitor value will typically increase smoothly so that the current spike will not appear.

Table 4. Leakage current magnitude for different values of the parasitic capacitance.

Parasitic Capacitance Values	i_{LGC} Value
20 nF capacitance	1.04 mA_{RMS}
840 nF capacitance	35.41 mA_{RMS}

Regarding the behavior of the LGC when the switching frequency varies, it can be considered that the typical switching frequency interval in this kind of system for powers less than 10 kW in single-phase inverters is commonly defined in the interval of 5 kHz and 25 kHz due to the characteristics of the power semiconductors and the behavior of their power losses. Considering this interval, the impact on the behavior of the leakage ground current is as in Figure 13, where it can be observed that the magnitude of the LGC decreases as the switching frequency increases. On the other hand, the switching frequency of these systems is considered constant, so the analysis of the LGC current is commonly performed under this condition.

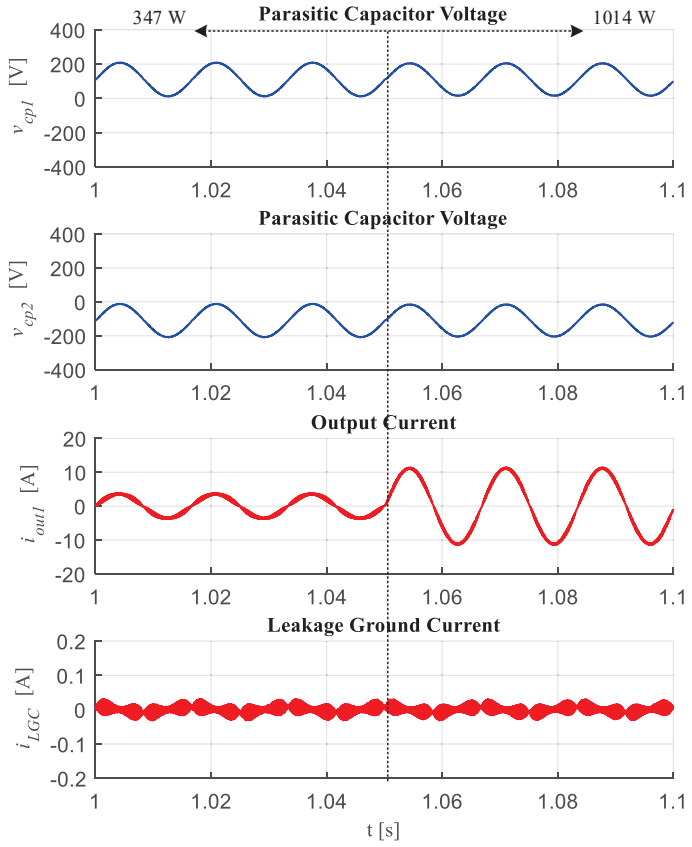

Figure 11. Dynamic response of the system increasing output power from 347 W to 1014 W.

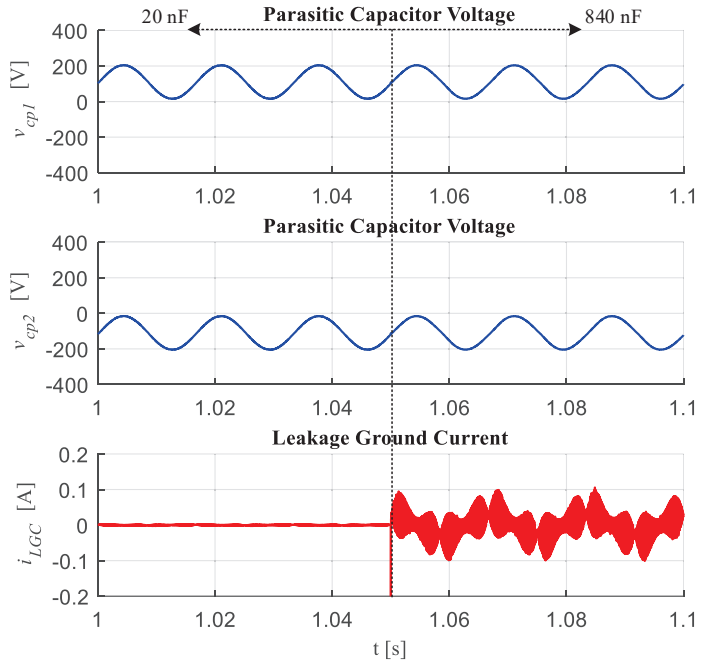

Figure 12. System response to an increment in the parasitic capacitance from 20 nF to 840 nF.

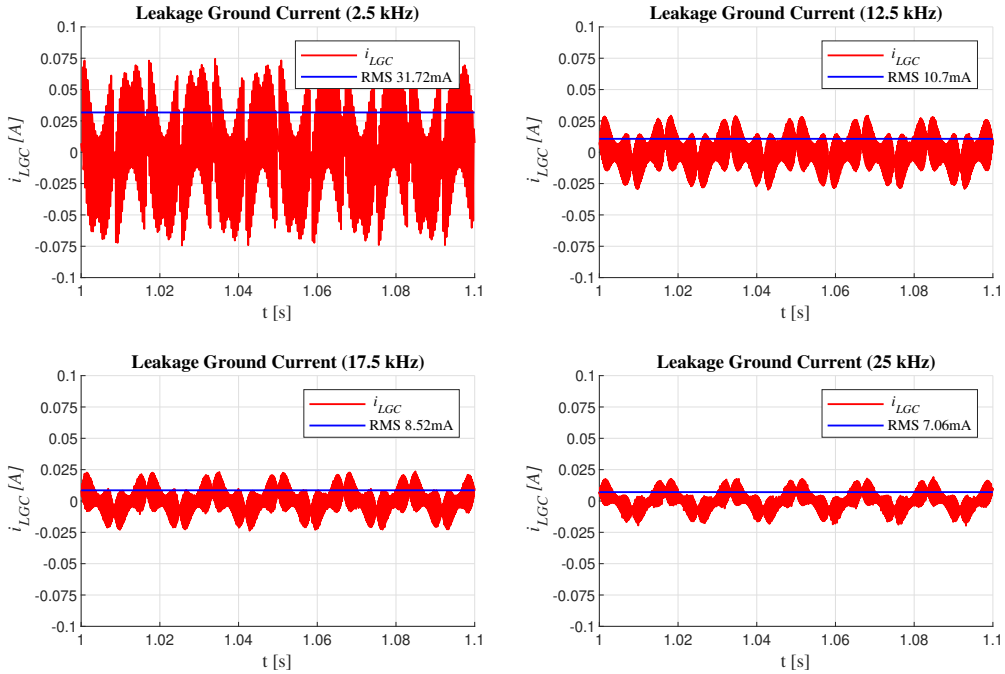

Figure 13. LGC behavior under different switching frequency scenarios.

5. Laboratory Implementation and Comparative Analysis

A laboratory prototype is designed and implemented to validate the proposed solution. The experimental parameters are fixed equal to those defined for the simulation results in Table 2. For the HERIC inverter design, the power semiconductors listed in Table 5 are used. The DSP TMS320F28335 from Texas Instruments is used as the platform to program the modulation sequence to control the HERIC inverter. The experimental setup is shown in Figure 14. As in the simulation results, the experimental test was performed in open loop; therefore, in the experimental setup, the grid voltage is implemented using a resistive load. In addition, the input DC voltage is considered constant and implemented using a constant DC source. Finally, in order to emulate the ground path resistance, R_G is connected between the grid neutral connection and the parasitic capacitances according to [25–27].

Table 5. List of components used in the experimental prototype.

Part Number	Description	Characteristics	Amount
G4PC40FD	IGBT (with ultra fast soft recovery diode)	600 V, 27 A.	6
IDH16S60C	SiC Schottky Diode	600 V, 16 A.	2
HFBR-2531	Fiber optic opto receiver	7 V, 25 mA.	6
HCPL-3120	Opto-coupler for IGBT gate drive	5 V, 16 mA, 1200 V.	6

The digital signals obtained using a SPWM technique are shown in Figure 15, where two grid cycles are considered. The six signals correspond to those obtained in the simulation results section.

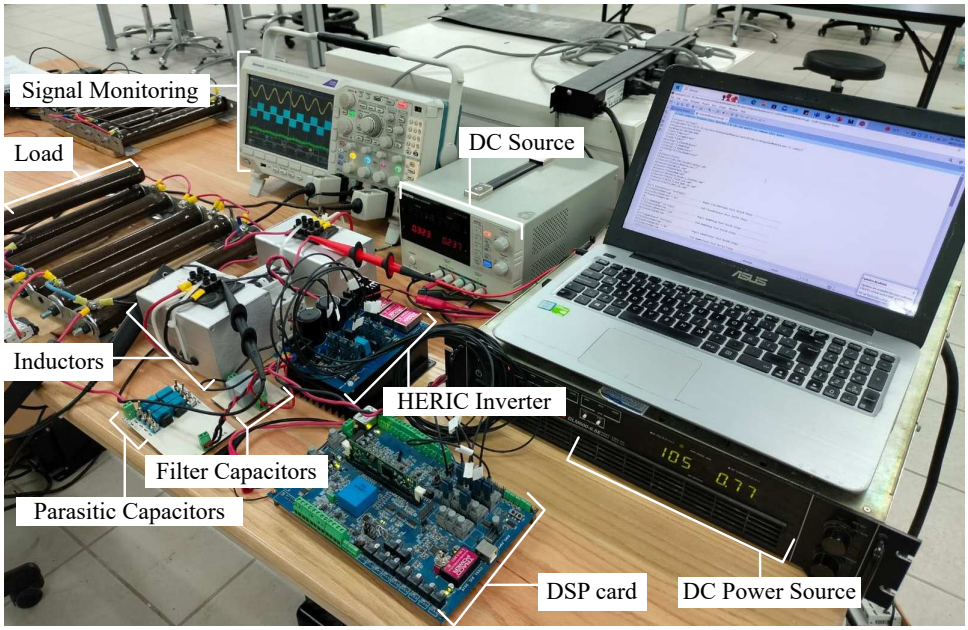

Figure 14. Laboratory experimental prototype.

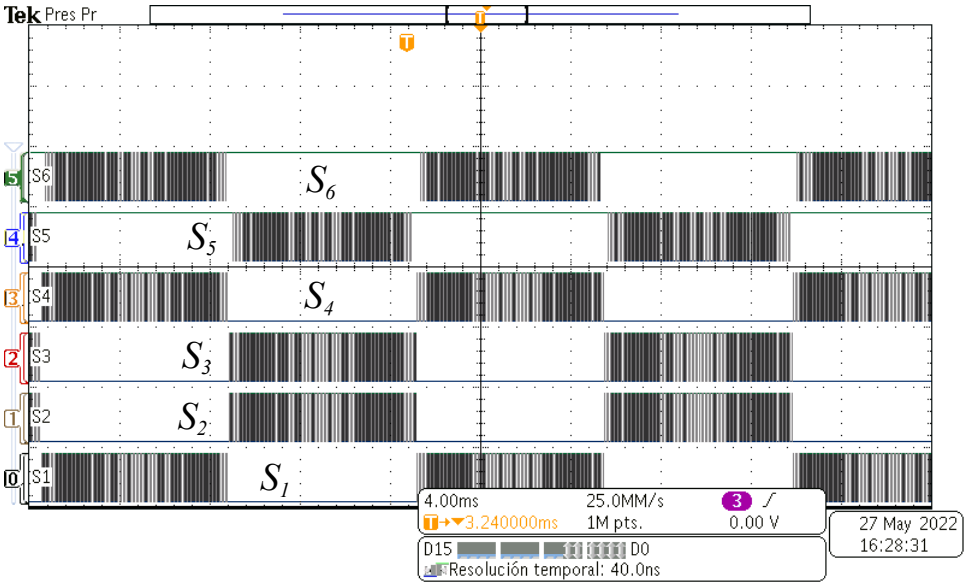

Figure 15. PWM signals to control the HERIC converter.

Figures 16 and 17 show the experimental plots for the differential output voltage v_{dm} and the load current i_{out} without and with the proposed LC output filter, respectively. The *RMS* values are around 158 V and 7.65 A for both cases, which correspond also with the simulation results. A small difference can be observed regarding the output current ripple, which is slightly higher when the output filter is considered. This is due to the addition of the trajectory for the CMC.

The above affirmation can be demonstrated by comparing the frequency spectrum for the output current. Figures 18 and 19 show the Fourier Fast Transform (FFT) of the output current with and without the output filter. As it can be noted, the magnitude of all harmonics is greater in the case of the connected filter than in the case when the filter is not connected. This will result in an increment of the THD as demonstrated in the simulation results section.

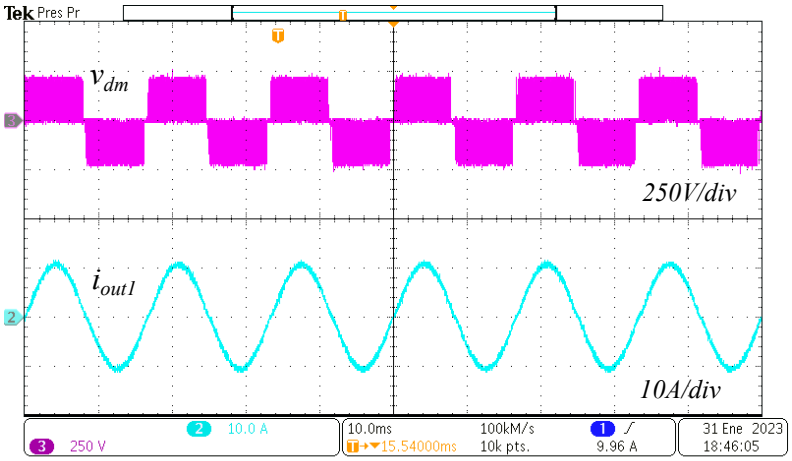

Figure 16. Experimental output voltage v_{dm} (**top**) and current i_{out1} (**bottom**) without the proposed filter.

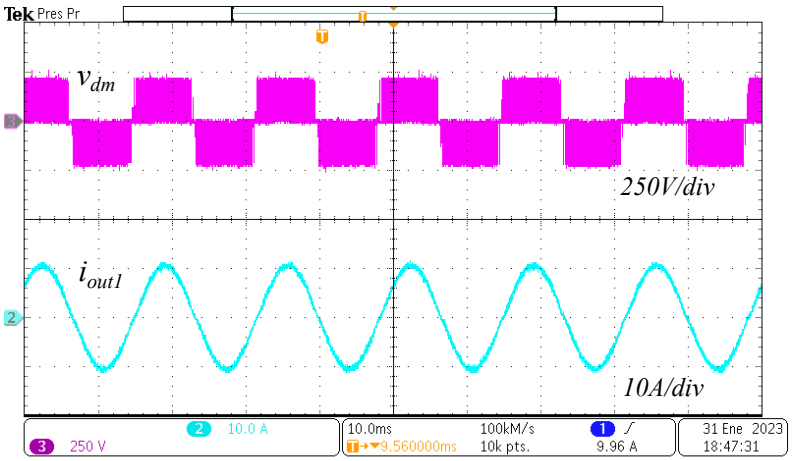

Figure 17. Experimental output voltage v_{dm} (**top**) and current i_{out1} (**bottom**) with the proposed filter.

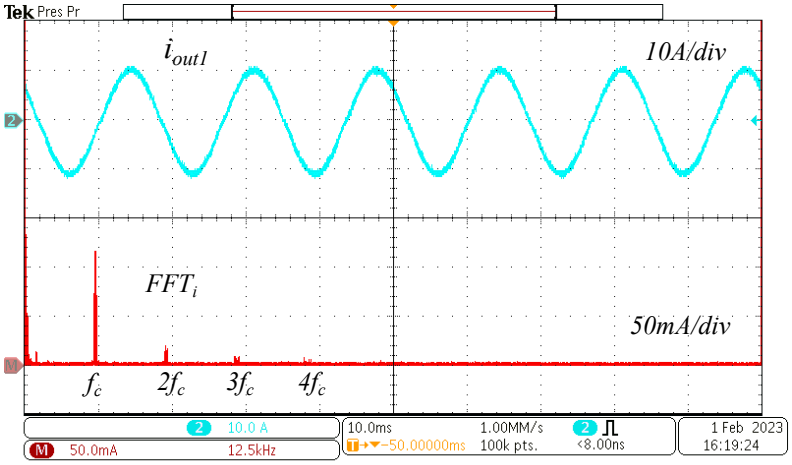

Figure 18. Output current FFT without the proposed filter.

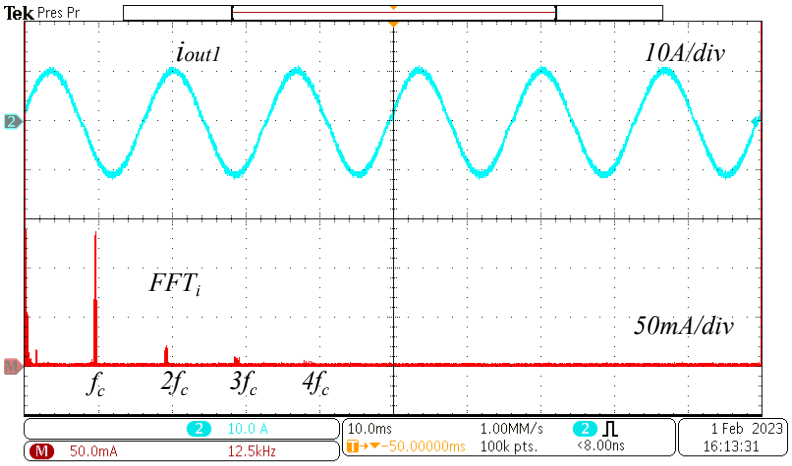

Figure 19. Output current FFT with the proposed filter.

The CMV and the CMC were also obtained from the prototype, which are depicted in Figures 20 and 21, with and without the passive filter, respectively. Note that the CMV behavior is different, with larger excursions for the first case. In consequence, the magnitude of the CMC is lower when the output filter is connected. This means that even when the HERIC topology is designed to deal with the CMC, a complementary method can be implemented to improve its performance.

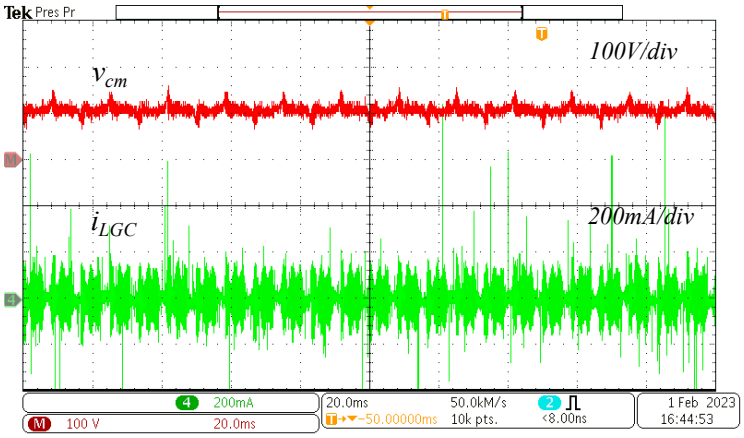

Figure 20. Common mode voltage and leakage ground current without the proposed filter.

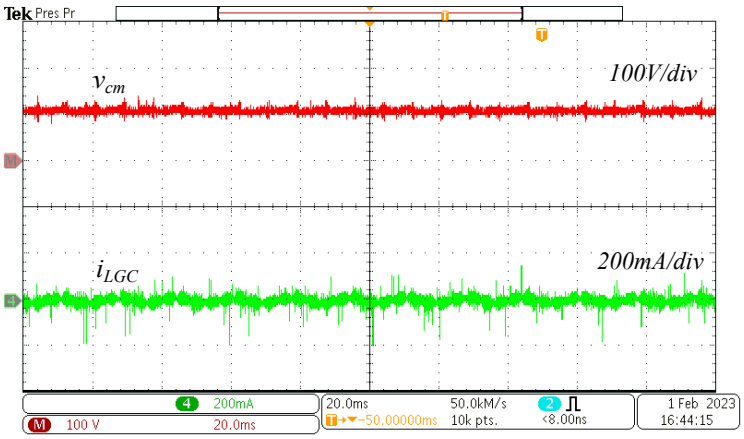

Figure 21. Common mode voltage and common mode current with the proposed filter.

Changes in the rated power were also performed. Figures 22 and 23 show the results obtained with and without the implemented filter. The power step was defined from 347 W to 1000 W. As it can be noted, the step of the output power when the filter is not connected produces a reduction in the CMC; however, when the filter is connected, there are no changes in the magnitude of the CMC. Table 6 summarizes the peak and *RMS* values. According to the results, the increment in the power does not imply an increment of the CMC in the proposed case.

Table 6. Leakage ground current magnitude under an output power step.

Power	i_{LGC} without Filter	i_{LGC} with Filter
	Peak Value–RMS Value	**Peak Value–RMS Value**
347 W	910 mA–127 mA	150 mA–20 mA
1000 W	710 mA–72.1 mA	130 mA–20.8 mA

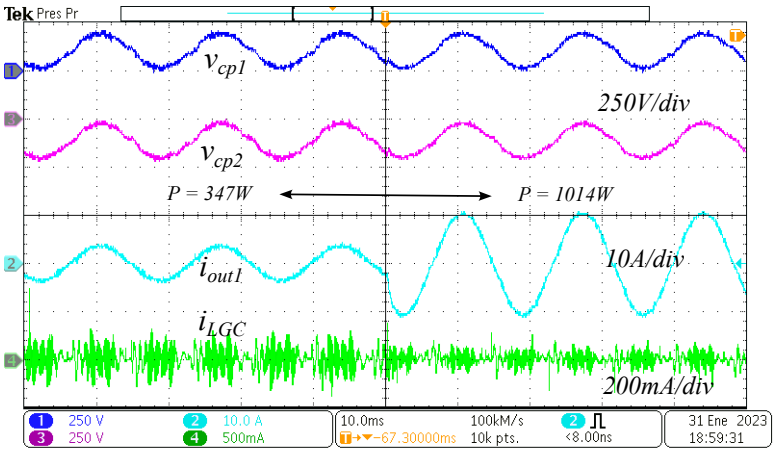

Figure 22. Power output step of the HERIC inverter without the proposed filter.

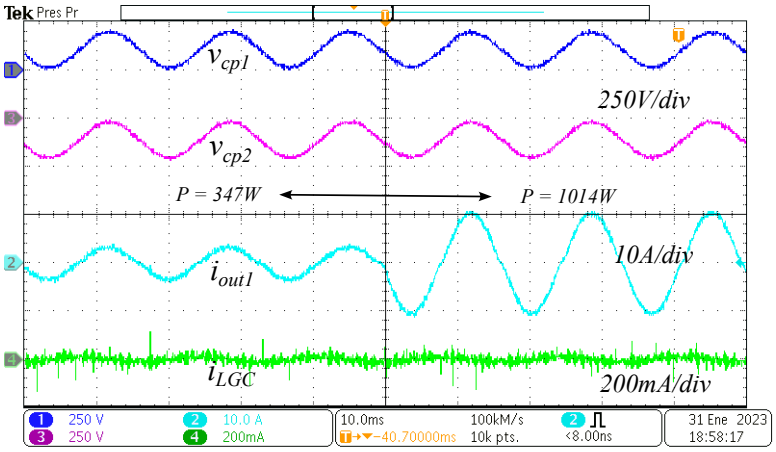

Figure 23. Power output step of the HERIC inverter with the proposed filter.

Moreover, an important plot is that related to the changes in the parasitic capacitance. In Figures 24 and 25, the results obtained without and with the filter for a step in the capacitance value from 20 nF to 840 nF are shown respectively. As can be noted, in the case where the filter is not implemented, the LGC increases until the *RMS* value is around 105 mA. On the other hand, when the filter is connected, the LGC also increases, but in this case, the increment is marginal, being 36.7 mA. This demonstrates that the dependency

regarding capacitance value is well reduced by the proposed passive filter. Table 7 summarizes the peak and *RMS* values for capacitance steps. In addition, in order to show that the implemented filter guarantees an additional path for the leakage ground current, Figure 26 is considered. It must be noted that, effectively, the leakage current flows through the low impedance provided by the capacitors implemented in the output filter.

Table 7. Leakage ground current magnitude under parasitic capacitance steps.

C_{pT}	i_{LGC} without Filter	i_{LGC} with Filter
	Peak Value–RMS Value	**Peak Value–RMS Value**
20 nf	850 mA–30.3 mA	230 mA–16 mA
840 nf	1.01 A–105 mA	170 mA–36.7 mA

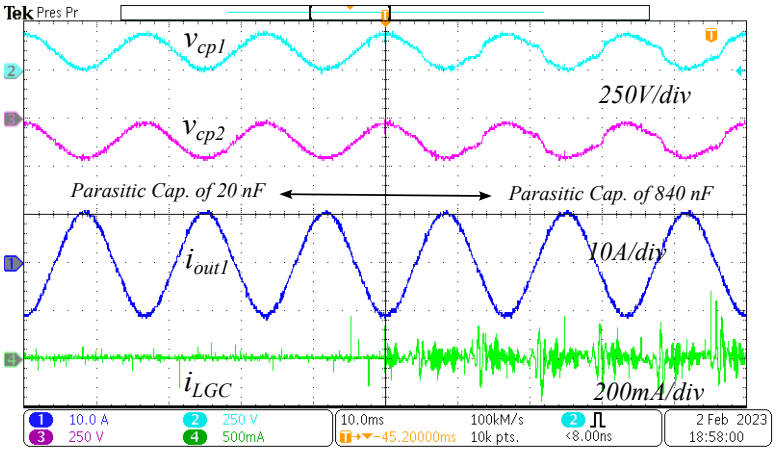

Figure 24. Parasitic capacitance step of the HERIC inverter without the proposed filter.

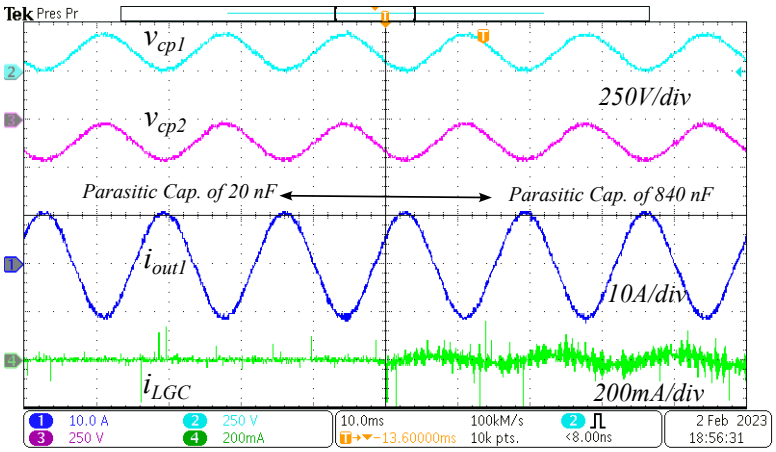

Figure 25. Parasitic capacitance step of the HERIC inverter with the proposed filter.

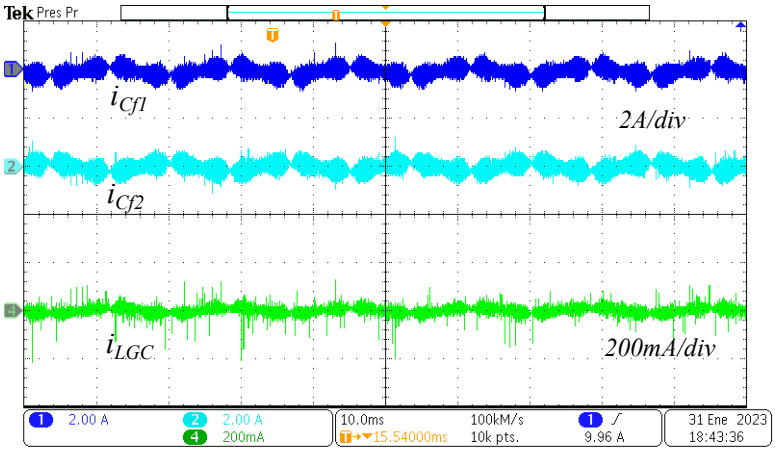

Figure 26. From top to bottom, current through C_{f1}, C_{f2} and common mode current i_{LGC}.

6. Conclusions

In this paper, a redundant solution to deal with the common mode problem in the HERIC transformerless photovoltaic inverter is proposed. The HERIC topology by itself has common mode currents, whose magnitude depends on the power and the magnitude of the parasitic capacitances. The proposed solution deals with the magnitude of the LGC when there is an increase in the rated power or magnitude of the parasitic capacitances. The LGC magnitude keeps the same value when the power increases. When the parasitic capacitance changes from 20 nF to 840 nF, the LGC increases 75 mA without the proposed filter. However, considering the solution proposed, the increase is marginal, and its value is around 20 mA. The proposed solution adds the passive filter components; however, a conventional PV inverter requires an output filter, which is generally third order. Therefore, the implementation does not imply an additional cost. It can be concluded that the redundant method presented in this paper effectively reduces the dependence of the leakage currents of the HERIC inverter with respect to the power and the magnitude of the parasitic capacitance.

Author Contributions: All authors contributed to the development of the overall document, proposal of the leakage current solution, common mode and differential mode analysis, simulations and experimental validation. All authors have read and agreed to the published version of this manuscript.

Funding: This research was partially funded by Tecnologico Nacional de Mexico under the project 17319.23-PD.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Acknowledgments: The authors want to acknowledge the administrative support including the laboratory personal provided by the Tecnologico Nacional de Mexico/ITS de Irapuato.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

3P-CMI	Three-phase cascade multilevel inverter
3P-FB	Six-switch three-phase inverter
3P-FBSC	Six-switch three-phase inverter with split capacitor
3P-NPC	Three-phase neutral point clamped inverter
CASVM	Conventional asymmetric space vector modulation
CMC	Common-mode current
CMM	Common-mode model

CMV	Common-mode voltage
CPLD	Complex Programmable Logic Device
CSSVM	Conventional symmetric space vector modulation
DC	Direct Current
DC-AC	Direct Current–Alternating Current
DSP	Digital Signal Processor
DSVMMAX	Discontinuous space vector modulation maximum
HERIC	Highly efficient and reliable inverter concept
IGBT	Isolated Gate Bipolar Transistor
LKC	Leakage currents
MOSFET	Metal-oxide-semiconductor field-effect transistor
NPC	Neutral Point Clamped
NSPWM	Near-state pulse width modulation
PWM	Pulse Width Modulation
PV	Photovoltaic
RMS	Root Mean Square
SVM	Space Vector Modulation
SVPWM	Space vector pulse width modulation
THD	Total Harmonic Distortion

References

1. Khan, M.N.H.; Siwakoti, Y.P.; Li, L.; Suan, F.T.K. Constant Common-Mode Voltage Transformerless Inverter for Grid-Tied Photovoltaic Application. In Proceedings of the 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 29 September–3 October 2019; pp. 616–621.
2. Gunsal, I.; Stone, D.A.; Foster, M.P. Suppressing Leakage Current for Cascaded H-Bridge Inverters in Renewable Energy and Storage Systems. *IEEE Trans. Ind. Electron.* **2021**, *68*, 11035–11043. [CrossRef]
3. Chen, W.; Yang, X.; Zhang, W.; Song, X. Leakage Current Calculation for PV Inverter System Based on a Parasitic Capacitor Model. *IEEE Trans. Power Electron.* **2016**, *31*, 8205–8217. [CrossRef]
4. *DIN VDE 0126-1-1*; Automatic Disconnection Device between a Generator and the Public Low-Voltage Grid. DKE German Commission for Electrical, Electronic and Information Technologies of DIN and VDE: Offenbach am Main, Germany, 2006; Paragraph 4.7.1. Photovoltaik.
5. Jahan, S.; Kibria, M.F.; Biswas, S.P.; Islam, M.R.; Rahman, M.A.; Muttaqi, K.M. H9 and H10 Transformer-less Solar Photovoltaic Inverters for Leakage Current Suppression and Harmonic Current Reduction. *IEEE Trans. Ind. Appl.* **2022**, *59*, 2446–2457. [CrossRef]
6. Lorenzani, E.; Migliazza, G.; Immovilli, F.; Gerada, C.; Zhang, H.; Buticchi, G. Internal Current Return Path for Ground Leakage Current Mitigation in Current Source Inverters. *IEEE Access* **2019**, *7*, 96540–96548. [CrossRef]
7. Gao, H. High-frequency common-mode voltage mitigation for current-source inverter in transformerless photovoltaic system using active zero-state space vector modulation. *IET Electr. Power Appl.* **2023**, *17*, 245–255. [CrossRef]
8. Zhou, Y.; Li, H. Analysis and Suppression of Leakage Current in Cascaded-Multilevel-Inverter-Based PV Systems. *IEEE Trans. Power Electron.* **2014**, *29*, 5265–5277. [CrossRef]
9. Barzegarkhoo, R.; Siwakoti, Y.P.; Vosoughi, N.; Blaabjerg, F. Six-Switch Step-Up Common-Grounded Five-Level Inverter with Switched-Capacitor Cell for Transformerless Grid-Tied PV Applications. *IEEE Trans. Ind. Electron.* **2021**, *68*, 1374–1387. [CrossRef]
10. Buticchi, G.; Franceschini, G.; Lorenzani, E. Compensation strategy of actual commutations for PV transformerless grid-connected converters. In Proceedings of the XIX International Conference on Electrical Machines—ICEM 2010, Rome, Italy, 6–8 September 2010; pp. 1–5.
11. Mattias, V.; Greizer, F.; Bremicker, A.; Hubler, K. Method of Converting Direct Current Voltage from a Source of Direct Current Voltage, More Specifically from a Photovoltaic Couse of Direct Current Voltage, into Alternating Current Voltage. European Patent 0286281 A1, 29 December 2005.
12. Schmidt, H.; Siedle, C.; Ketterer, J. DC/AC Converter to Convert Direct Electric Voltage into Alternating Voltage or into Alternating Current. European Patent EP 1 369 985 A2, 11 August 2005.
13. Tang, Z.; Su, M.; Sun, Y.; Cheng, B.; Yang, Y.; Blaabjerg, F.; Wang, L. Hybrid UP-PWM Scheme for HERIC Inverter to Improve Power Quality and Efficiency. *IEEE Trans. Power Electron.* **2019**, *34*, 4292–4303. [CrossRef]
14. Li, W.; Gu, Y.; Luo, H.; Cui, W.; He, X.; Xia, C. Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4537–4551. [CrossRef]
15. Tang, Z.; Yang, Y.; Su, M.; Jiang, T.; Blaabjerg, F.; Dan, H.; Liang, X. Modulation for the AVC-HERIC Inverter to Compensate for Deadtime and Minimum Pulsewidth Limitation Distortions. *IEEE Trans. Power Electron.* **2019**, *35*, 2571–2584. [CrossRef]
16. Xiao, H.F.; Zhang, L.; Li, Y. A Zero-Voltage-Transition HERIC-Type Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Trans. Ind. Electron.* **2017**, *64*, 1222–1232. [CrossRef]

17. Dong, D.; Luo, F.; Boroyevich, D.; Mattavelli, P. Leakage Current Reduction in a Single-Phase Bidirectional AC-DC Full-Bridge Inverter. *IEEE Trans. Power Electron.* **2012**, *27*, 4281–4291. [CrossRef]
18. He, S.; Wang, F.; Wang, Y.; Liu, B. Modeling and Suppression of Zero-Sequence Circulating Current Resonance for Parallel Interleaved Inverters with Bypass Capacitor-Based Leakage Current Mitigation. *IEEE J. Emerg. Sel. Top. Power Electron.* **2023**, *11*, 3097–3107. [CrossRef]
19. Kim, H.; Kim, K.-H. Filter design for grid connected PV inverters. In Proceedings of the 2008 IEEE International Conference on Sustainable Energy Technologies, Singapore, 24–27 November 2008; pp. 1070–1075.
20. Liserre, M.; Blaabjerg, F.; Dell Aquila, A. Step-by-step design procedure for a grid-connected three-phase PWM voltage source converter. *Int. J. Electron.* **2004**, *91*, 445–460. [CrossRef]
21. Sosa, J.M.; Escobar, G.; Martínez-Rodriguez, P.R.; Vazquez, G.; Juarez, M.A.; Diosdado, M. Comparative evaluation of L and LCL filters in transformerless grid tied converters for active power injection. In Proceedings of the 2014 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC), Ixtapa, Mexico, 5–7 November 2014; pp. 1–6.
22. Farzamkia, S.; Khoshkbar-Sadigh, A.; Forestieri, J.R.N.; Farasat, M.; Dargahi, V. Analytical Approach to Calculate Inductor Current Ripple Cancellation in Two-Phase Interleaved Single-phase Inverter. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020; pp. 3472–3477.
23. Mandrioli, R.; Viatkin, A.; Hammami, M.; Ricco, M.; Grandi, G. A Comprehensive AC Current Ripple Analysis and Performance Enhancement via Discontinuous PWM in Three-Phase Four-Leg Grid-Connected Inverters. *Energies* **2020**, *13*, 4352. [CrossRef]
24. Beres, R.; Wang, X.; Blaabjerg, F.; Bak, C.; Liserre, M. A review of passive filters for grid-connected voltage source converters. In Proceedings of the Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE, Fort Worth, TX, USA, 16–20 March 2014; pp. 2208–2215.
25. Lee, J.; Lee, K. New Modulation Techniques for a Leakage Current Reduction and a Neutral-Point Voltage Balance in Transformerless Photovoltaic Systems Using a Three-Level Inverter. *IEEE Trans. Power Electron.* **2014**, *29*, 1720–1732. [CrossRef]
26. Bae, Y.; Kim, R. Suppression of Common-Mode Voltage Using a Multicentral Photovoltaic Inverter Topology with Synchronized PWM. *IEEE Trans. Ind. Electron.* **2014**, *61*, 4722–4733. [CrossRef]
27. Salam, M.A.; Rahman, Q.M.; Ang, S.P.; Wen, F. Soil resistivity and ground resistance for dry and wet soil. *J. Mod. Power Syst. Clean Energy* **2017**, *5*, 290–297. [CrossRef]