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High-Frequency Harmonic Suppression by Switching-Sequence Optimization in a Topologically Asymmetric Three-Phase-to-Single-Phase Matrix Converter

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Abstract

To address output-side high-frequency harmonics in a three-phase-to-single-phase matrix converter (3-1MC) with an inductive compensation unit and topological port asymmetry, two PWM switching-sequence optimization methods are proposed. Without power decoupling, the pulsating power associated with the single-phase output is coupled to the input side through the bidirectional switching network because the converter has no large energy-storage DC link. Under conventional modulation, the state sequence can produce large output-voltage steps and nonuniform commutation paths, thereby increasing switching-frequency harmonic components. The first proposed method avoids direct commutation of the line voltage with the largest instantaneous magnitude to the zero state by inserting line-voltage segments with smaller instantaneous magnitudes. The second method rearranges the switching-state sequence without changing the effective-vector durations, thereby reducing the number of switching transitions within each switching cycle. Compared with the conventional modulation method, Method 1 reduces the output-voltage THD from 35.4% to 31.4%, corresponding to a relative reduction of 11.3%. Method 2 reduces the THD from 35.4% to 27.5%, corresponding to a relative reduction of 22.3%.

Keywords: asymmetric port topology; switching-sequence optimization; power decoupling; three-phase-to-single-phase matrix converter; high-frequency harmonics; pulse-width modulation

1. Introduction

A matrix converter (MC) is a direct AC-AC converter that has the characteristics of low grid-side harmonic pollution, convenient power factor adjustment, and an output frequency that is not limited by the input frequency [1]. Compared with traditional AC-DC-AC converters [2,3], owing to the lack of large-capacity energy-storage capacitors, it also has the advantages of high reliability and high power density. Research on matrix converters not only includes theoretical aspects such as improving modulation methods [4] and optimizing control strategies [5], but also extends to practical engineering problems such as modular multilevel topology [6] and fault tolerance and diagnosis under abnormal switching states [7]. In recent years, the application of matrix converters has expanded from the field of motor drives [8] to wind power generation [9], wireless energy transmission [10], and unified power flow controllers [11].

The 3-1MC has an inherently asymmetric port topology: it interfaces a three-phase input with a single-phase main output and an auxiliary compensation branch. Unlike a

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three-phase-to-three-phase matrix converter, the single-phase output power contains a second-order pulsating component. Because the 3-1MC performs direct AC-AC conversion without a large DC-link energy-storage element, this pulsating-power component is coupled to the input side through the bidirectional switching network. The resulting topological port asymmetry motivates the use of a compensation unit to achieve input-output power decoupling and suppress the associated low-frequency disturbances. Several studies have addressed these inherent characteristics of 3-1MCs [12–19]. These studies cover three-phase-to-single-phase matrix-converter modulation, input-output power decoupling, single-phase matrix-converter control, high-power-factor operation, and soft-switching techniques. Broader active-power-decoupling research for single-phase converter systems also provides useful design references for compensation-branch control [20–22]. Although the port asymmetry primarily manifests itself in power-decoupling and low-frequency behavior, the switching states and commutation paths available under the 3-1MC topology also affect the output-side switching harmonics. This study therefore focuses on reducing these harmonics by optimizing state ordering and limiting large commutation-voltage steps.

Existing discontinuous PWM and optimized switching-sequence studies for three-phase-to-three-phase matrix converters provide useful references for reducing switching loss and output-side harmonics [23–25]. Recent research has further explored carrier-based PWM, predictive modulation, switching-optimized modulation, direct modulation with optimized transitions, and harmonic suppression under distorted supply conditions [26–30]. Spread-spectrum modulation, repetitive control, and harmonic attenuation methods provide complementary approaches for reducing matrix-converter harmonic components [31–33]. In addition, recent studies of soft-switching and high-frequency modulation for matrix-converter-based AC-DC and DAB converter systems demonstrate continued progress in commutation and modulation design [34,35]. In contrast, output-side high-frequency harmonic suppression through switching-sequence optimization in a 3-1MC with an inductive compensation unit remains insufficiently explored. The methods reported for three-phase-to-three-phase matrix converters do not directly address the asymmetric-port constraints and power-decoupling requirement of the 3-1MC considered here.

On the basis of the conventional dual-space-vector modulation method, this article proposes two PWM switching-sequence optimization methods for suppressing output-side high-frequency harmonics in a 3-1MC with an inductive compensation unit. Method 1 avoids direct commutation of the input line voltage with the largest instantaneous magnitude to the zero state by inserting lower-magnitude line-voltage segments. Method 2 preserves the effective-vector dwell times but rearranges the switching states according to the parity of the input and output sectors to reduce switching transitions. Thus, the novelty of this work is not a new set of voltage vectors or a new compensation topology; rather, it is a 3-1MC-specific sequence-design approach that simultaneously preserves the established power-decoupling modulation principle and targets the unfavorable commutation paths caused by asymmetric-port constraints.

2. Principle and Implementation of 3-1MC Power Decoupling

2.1. Analysis of 6-Switch Transistors 3-1MC Topology and Input Performance

The traditional 6-switch transistor 3-1MC topology with independent midlines is shown in Figure 1, which includes 6 bidirectional switching transistors S_{ij} (i = a, b, c; j = u, w). Each bidirectional switching transistor is composed of two power transistors in reverse series. The input uses a second-order low-pass filter composed of an inductor L_f and a capacitor C_f to attenuate high-frequency harmonic components in the input current, and the load is composed of a resistor R and an inductor L in series.

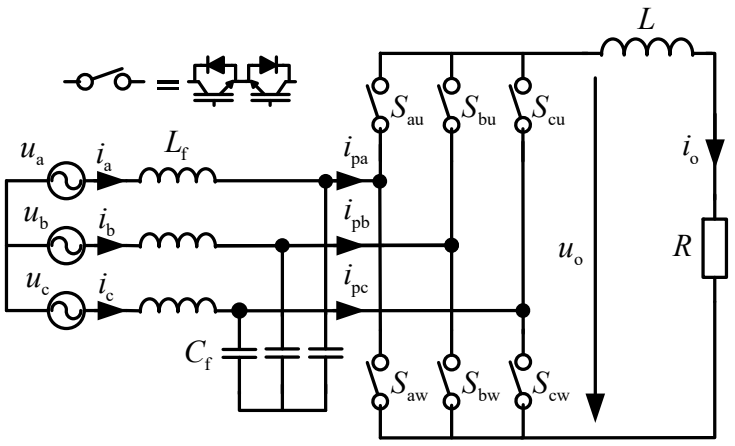


Figure 1. 6-switch 3-1MC topology.

Ignoring the high-frequency components in the output voltage and current, the expressions for the output voltage u_o(t) and current i_o(t) are shown in Equation (1).

$$\begin{cases} u_o(t) = U_o \cos(\omega_o t) \\ i_o(t) = I_o \cos(\omega_o t + \varphi_1) \end{cases} \tag{1}$$

where U_o is the amplitude of the output voltage; I_o is the amplitude of the output current; ω_o is the output angular frequency; φ_1 is the phase difference between the output voltage and current.

The expression for the output power $P_o(t)$ can be obtained from Equation (1) as shown in Equation (2).

$$\begin{aligned} P_o(t) &= u_o(t) \times i_o(t) \\ &= \tfrac{U_o I_o}{2} \cos(\varphi_1) + \tfrac{U_o I_o}{2} \cos(2\omega_o t + \varphi_1) \\ &= \overline{P}_o(t) + \widetilde{P}_o(t) \end{aligned} \tag{2}$$

where $\overline{P}_o(t)$ and $\widetilde{P}_o(t)$ represent the DC and AC components of the output power $P_o(t)$, respectively.

Assuming the expression of the ideal three-phase input voltage $u_{abc}(t)$ is shown in Equation (3).

$$\begin{cases} u_a(t) = U_i \cos(\omega_i t) \\ u_b(t) = U_i \cos(\omega_i t - \frac{2}{3}\pi) \\ u_c(t) = U_i \cos(\omega_i t + \frac{2}{3}\pi) \end{cases} \tag{3}$$

where U_i is the amplitude of the three-phase input voltage; ω_i is the input angular frequency.

Ignoring system losses and based on the principle of instantaneous power conservation between input and output, it can be inferred from Equations (2) and (3) that, in addition to the fundamental component with the same rotational speed and direction as the input voltage vector, there must be low-frequency harmonic currents in the three-phase input current $i_{abc}(t)$. If the high-frequency harmonic components in the input current are ignored, the expression for the three-phase input current $i_{abc}(t)$ of the 6-switch transistors 3-1MC shown in Figure 1 is given in Equation (4).

$$\begin{cases} i_a(t) = I_i \cos(\omega_i t) + I_2 \cos(\omega_2 t) + I_3 \cos(\omega_3 t) \\ i_b(t) = I_i \cos(\omega_i t - \frac{2}{3}\pi) + I_2 \cos(\omega_2 t - \frac{2}{3}\pi) + I_3 \cos(\omega_3 t + \frac{2}{3}\pi) \\ i_c(t) = I_i \cos(\omega_i t + \frac{2}{3}\pi) + I_2 \cos(\omega_2 t + \frac{2}{3}\pi) + I_3 \cos(\omega_3 t - \frac{2}{3}\pi) \end{cases} \tag{4}$$

where I_{i} is the amplitude of the fundamental current in the three-phase input current; ω_2 and ω_3 are the angular frequencies of two low-frequency harmonics in the input current, respectively; I_2 and I_3 are the amplitudes of the angular frequency ω_2 and ω_3 currents in the input current, respectively.

Assuming that the amplitude of the low-frequency harmonics in Equation (4) satisfies $I_2 = I_3$, while ignoring the phase difference φ_1 between the output voltage and current, according to the principle of instantaneous power conservation between input and output, i.e., $P_{\mathrm{o}}(t) = P_{\mathrm{i}}(t) = \sum_{j=\mathrm{a,b,c}} \left[u_j(t) \times i_j(t)\right]$, the relationship between the amplitude and angular frequency of the two low-frequency harmonic currents in Equation (4) can be obtained as shown in Equation (5).

$$\begin{cases} I_{\mathrm{i}} = \frac{U_{\mathrm{o}} I_{\mathrm{o}}}{3U_i} \\ I_2 = I_3 = \frac{U_{\mathrm{o}} I_{\mathrm{o}}}{6U_{\mathrm{i}}} \\ \omega_2 = 2\omega_{\mathrm{o}} + \omega_{\mathrm{i}} \\ \omega_3 = 2\omega_{\mathrm{o}} - \omega_{\mathrm{i}} \end{cases} \tag{5}$$

According to Equation (5), the input current contains low-frequency harmonic components that are related to both the input and output angular frequencies. Ignoring the high-frequency harmonic components in the input current, an approximate expression for the *THD* value of the input current can be obtained from the above equation, as shown in Equation (6).

$$THD \approx \frac{\sqrt{I_2^2 + I_3^2}}{I_{\mathrm{i}}} = 70.7\% \tag{6}$$

According to Equation (6), the *THD* value of the input current is relatively high and constant.

2.2. Principle of 3-1MC Power Decoupling with Compensation Units

To suppress the two low-frequency harmonics with angular frequencies of $2\omega_{\mathrm{o}} - \omega_{\mathrm{i}}$ and $2\omega_{\mathrm{o}} + \omega_{\mathrm{i}}$ in the input current, a compensation inductor L and a set of bidirectional switch arrays (bidirectional switches S_{av}, S_{bv}, and S_{cv}) are added to the output side of the topology shown in Figure 1 to form the compensation side. By reasonable modulation, the decoupling of input and output power can be achieved; that is, the DC component $\overline{P}_{\mathrm{o}}(t)$ in the output power is transmitted to the input side, and the AC component $\widetilde{P}_{\mathrm{o}}(t)$ only forms a closed loop on the output side, without affecting input performance. The direct 3-1MC topology with an inductance compensation unit and the virtual AC-DC-AC equivalent topology are shown in Figure 2.

To achieve power decoupling between input and output, it is necessary to modulate the output side and compensation side of the virtual inverter appropriately. Assuming that the modulation function expressions of the output side and compensation side are shown in Equation (7).

$$\begin{cases} \xi_{\mathrm{o}}(t) = M_{\mathrm{o}} \cos(\omega_{\mathrm{o}} t) \\ \xi_{\mathrm{L}}(t) = M_{\mathrm{L}} \cos(\omega_{\mathrm{o}} t + \varphi_2) \end{cases} \tag{7}$$

where M_{o} and M_{L} are the modulation coefficients of the modulation functions on the output side and compensation side, respectively; φ_2 is the initial phase of the compensation side modulation function.

According to the description of the mutual constraints between the modulation functions on the output side and the compensation side, the constraint relationship shown in Equation (8) can be obtained.

$$\begin{cases} M_{\mathrm{L}} = gM_{\mathrm{o}} \\ g = \sqrt{\frac{\omega_{\mathrm{o}} L_{\mathrm{c}}}{\sqrt{R^2+(\omega_{\mathrm{o}} L)^2}}} \\ \varphi_2 = -\frac{\pi}{4} - \frac{\varphi_1}{2} \end{cases} \tag{8}$$

where g is the ratio of modulation coefficients on the output side and compensation side. Generally, $\omega_{\mathrm{o}} L << R$, so the coefficient g in Equation (8) can be simplified as $g \approx \sqrt{\omega_{\mathrm{o}} L_{\mathrm{c}}/R}$. Ignoring the phase difference φ_1 between the output-side voltage and current, the initial phase on the compensation side can be simplified as $\varphi_2 \approx -\pi/4$.

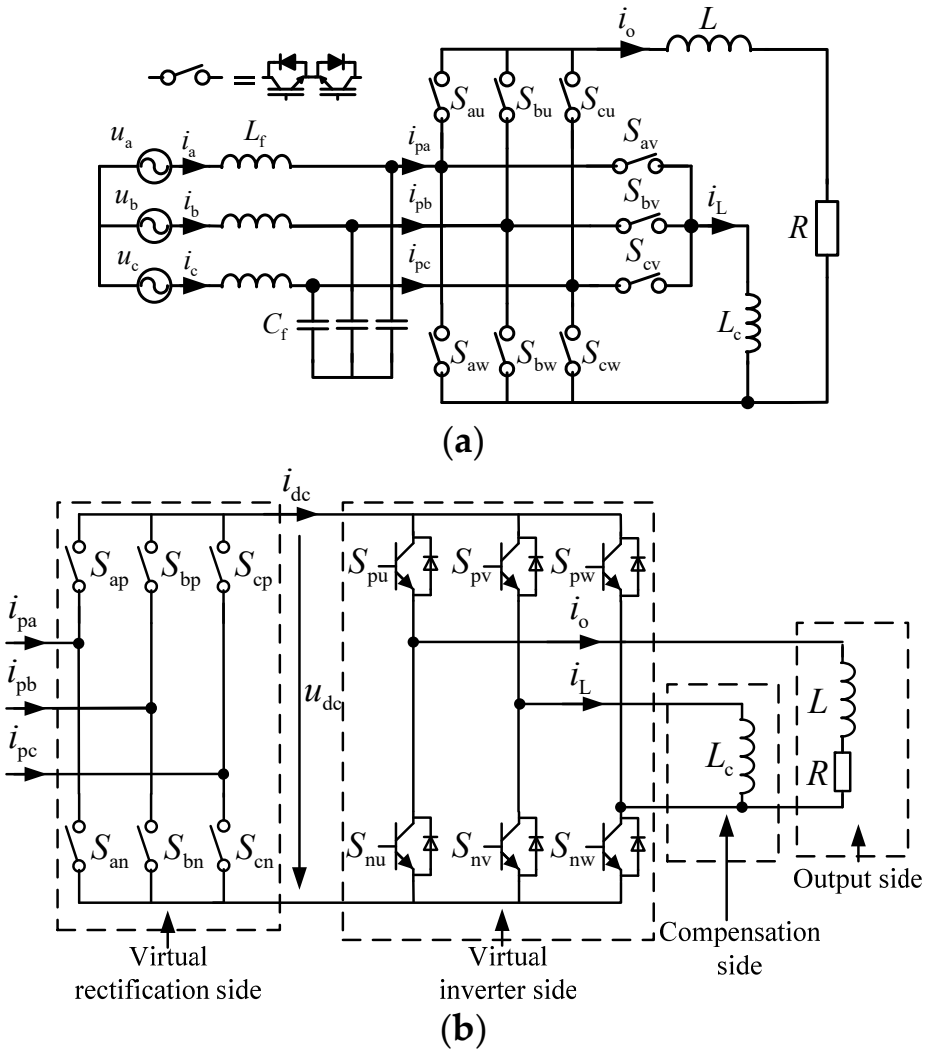


Figure 2. 3-1MC topology with an inductance compensation unit: (**a**) Direct 3-1MC topology with an inductance compensation unit; (**b**) Virtual AC-DC-AC equivalent topology.

To achieve the maximum voltage transfer rate, the time required for zero-vector modulation during dual space vector modulation should be reduced. Therefore, the modulation functions on the output side and compensation side need to satisfy the constraint relationship shown in Equation (9).

$$|\xi_{\mathrm{o}}(t)| + |\xi_{\mathrm{L}}(t)| = M_{\mathrm{o}}|\cos(\omega_{\mathrm{o}} t)| + M_{\mathrm{L}}|\cos(\omega_{\mathrm{o}} t + \varphi_2)| \leq 1 \tag{9}$$

The expression for the maximum value M_{o_max} of the modulation coefficient M_o can be further derived from Equations (8) and (9), as shown in Equation (10).

$$M_{o_max} = \sqrt{\frac{1}{g^2 + 2g\cos(\varphi_2) + 1}} \tag{10}$$

The expression for the voltage transfer rate λ of 3-1MC with an inductance compensation unit can be obtained from the above equation, as shown in Equation (11).

$$\begin{aligned} \lambda &= \frac{M_{o_max} u_{dc}}{U_i} \le \frac{3}{2} M_{rec} \cos(\theta_r) M_{o_max} \\ &\le \frac{3}{2}\sqrt{\frac{1}{g^2+2g\cos(\varphi_2)+1}} \approx \frac{3}{2}\left(\sqrt{\frac{2\pi f_o L_c}{R}+2\sqrt{\frac{\pi f_o L_c}{R}}+1}\right)^{-1} \end{aligned} \tag{11}$$

where M_{rec} is the modulation coefficient of the virtual rectification side, $M_{rec} \le 1$; $\cos(\theta_r)$ is the input power factor, $\cos(\theta_r) \le 1$; u_{dc} represents the virtual DC bus voltage in Figure 2b.

The parameter setting for the compensating inductance L_c is L_c = 15 mH, and the relationship curve between the maximum voltage transfer rate λ max and the output frequency f_o under different load resistances R can be obtained from Equation (11) as shown in Figure 3. From Figure 3, it can be seen that both the output frequency f_o and the load resistance R have an impact on the maximum voltage transfer rate λ_{max}, and the smaller the load resistance R, the greater the maximum voltage transfer rate λ_{max}. At the same time, λ_{max} increases with the decrease in output frequency f_o. When the output side is DC flow, λ_{max} reaches a maximum value of 1.5, and the power compensation unit no longer plays a role. The purple horizontal line in Figure 3 denotes the limiting value λ_{max} = 1.5 under the DC-output condition f_o = 0, where the power compensation unit no longer plays a role.

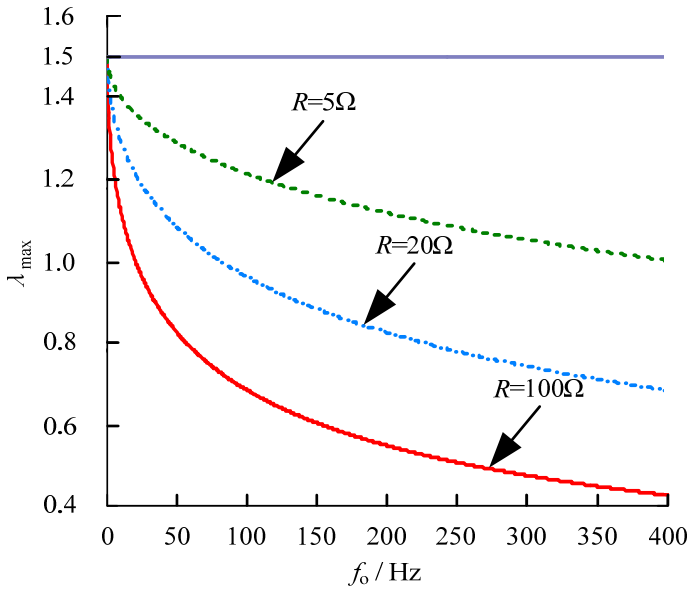


Figure 3. Relationship between maximum voltage utilization and output frequency.

2.3. 3-1MC Conventional Modulation Method with Compensation Unit

For the convenience of studying the modulation method of 3-1MC with compensation units, the direct 3-1MC topology shown in Figure 2a is equivalent to the virtual AC-DC-AC equivalent topology shown in Figure 2b. Ref. [17] proposed a dual space vector modulation method (conventional modulation method) for 3-1MC. As the input side is a current-

source rectifier, the distribution of the input current space vector $\vec{I}_r$ and the sector division method are shown in Figure 4. The areas labeled I–VI represent four input-current sectors determined by the angular position of the input current reference vector; the corresponding effective current vectors are selected according to the sector in which the reference vector is located. The expressions for the duty cycles d_α, d_β, and d_{01} corresponding to the effective vectors I_α, I_β, and the zero vector I_0 on the input-side current are shown in Equation (12).

$$\begin{cases} d_\alpha = M_{rec}\ \sin(\theta_r) \\ d_\beta = M_{rec}\ \sin\left(\frac{\pi}{3} - \theta_r\right) \\ d_{01} = 1\ - d_\alpha - d_\beta \end{cases} \tag{12}$$

where θ_r is the angle between the current space vector and the β coordinate axis in the corresponding sector, $\theta_r \in [0, \pi/3]$.

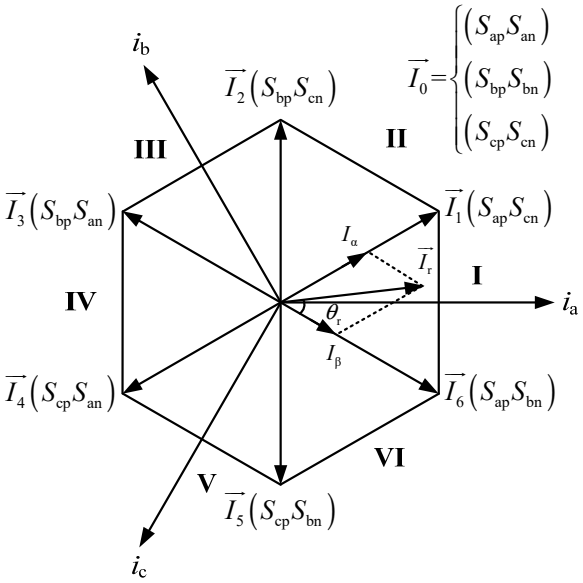


Figure 4. Schematic diagram of input current control vector distribution and sector division mode.

The virtual inverter side uses the zero-crossing points of the modulation functions ξ_o and ξ_L on the output side and compensation side as the basis for dividing the output sector. The division method of the output sector is shown in Figure 5. When the output voltage control vector is located within any output sector, the effective voltage vector and zero-vector duty cycles d_m, d_c, and d_{02} are expressed as Equation (13).

$$\begin{cases} d_m = M_o|\cos(\omega_o t)| \\ d_c = M_L|\cos(\omega_o t + \varphi_2)| = M_L\left|\cos(\omega_o t - \frac{\pi}{4} - \frac{\varphi_1}{2})\right| \\ d_{02} = 1\ - d_m - d_c \end{cases} \tag{13}$$

The expressions for the effective vector and zero vector action times under the dual space vector modulation method can be obtained from Equations (12) and (13), as shown in Equation (14).

$$\begin{cases} T_1 = T_{\alpha m} = d_\alpha d_m T_s \\ T_2 = T_{\alpha c} = d_\alpha d_c T_s \\ T_3 = T_{\beta m} = d_\beta d_m T_s \\ T_4 = T_{\beta c} = d_\beta d_c T_s \\ T_0 = T_s - T_1 - T_2 - T_3 - T_4 \end{cases} \tag{14}$$

where T_1, T_2, T_3, and T_4 are the effective vector action times; T_0 is the zero vector action time; T_s is the switching period, with a value of 100 μs in the experiment.

According to Equation (14), conventional modulation methods divide a switching cycle into 4 effective vector action-time slices and 1 zero-vector action-time slice. That is, there are 5 switch combination states in a switching cycle, and the switch state selected by the zero vector is based on the minimum number of switches between the effective vector and the zero vector. Taking both input and output sectors as an example and ignoring the influence of the input *LC* filter, the PWM switch state and output voltage waveform at this time are shown in Figure 6.

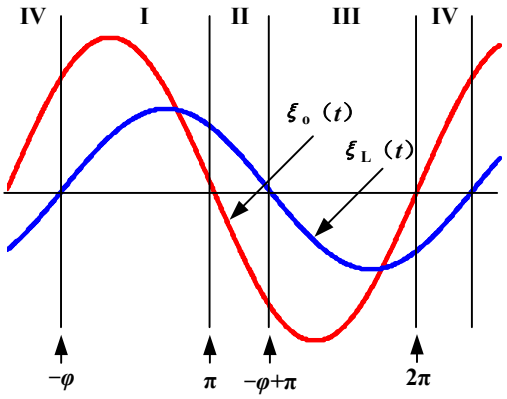


Figure 5. Schematic diagram of output sector division mode.

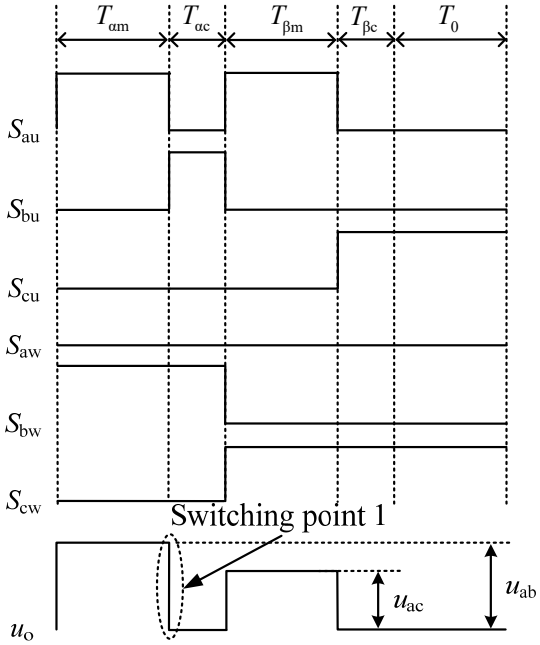


Figure 6. PWM switch state and output voltage waveform under conventional modulation.

From Figure 6, it can be seen that when the input and output are both located in sector I, the output side voltage u_o is alternately affected by the line voltage corresponding to the input current space vectors $\vec{I}_6$ and $\vec{I}_1$. When the angle $\theta_r \in [0, \pi/6]$, the amplitude of the output-side voltage under the action of the input current space vector $\vec{I}_1$ is the maximum phase u_{ab} of the input voltage amplitude. At the switching point 1 in Figure 6, there is a situation where the maximum amplitude phase u_{ab} directly switches to zero voltage; In a similar situation, when the angle $\theta_r \in (\pi/6, \pi/3]$, under the action of the input current

space vector $\vec{I_1}$, there will be a situation where the maximum amplitude of the input line voltage is directly switched to zero voltage in the output voltage. Switching between the maximum-amplitude phase and zero voltage under the conventional modulation method mentioned above will lead to an increase in high-frequency harmonics in the system.

Taking the input vector located in sector I and the output vector located in sectors I and II as examples, the switch combinations under the conventional modulation method can be obtained from Equation (14), as shown in Table 1. For two adjacent switch combinations, the number of switching transitions is obtained by counting the positions that change in their three-letter codes. According to Table 1, the number of switching transitions from the switch combination bab to the switch combination acc is 3, whereas that from the switch combination bab to the switch combination caa is 2. Here, bab denotes the switch combination for which Sbu = Sav = Sbw = 1, as illustrated in Figure 2a. These relatively large numbers of switching transitions can produce larger output-voltage steps and consequently increase the output-side high-frequency harmonic content.

Table 1. Switch combination state table under the conventional modulation method.

Input Sector	Output Sector	Switch Combination	Number of Switching Tubes
I	I	abb → bab → acc → cac → ccc	8
	II	baa → bab → caa → cac → ccc	5

3. A Class of Switch Sequence Optimization Methods for Reducing High-Frequency Harmonics

From the research results of existing literature, it can be seen that under certain switching frequencies and commutation methods, avoiding direct switching of the phase with the maximum voltage amplitude in the input vector and reducing the number of switching times per unit switching cycle are two effective ways to suppress high-frequency harmonics.

3.1. Optimization Method for Switching Sequence to Avoid Direct Switching of Phase with Maximum Amplitude

The conventional modulation method of 3-1MC is essentially the modulation of the input line voltage on the output and compensation sides. When the input is located in sector I, if the angle $\theta_r \in [0, \pi/6]$, the maximum amplitude line voltage in the input vector is u_{ab}; if the angle $\theta_r \in (\pi/6, \pi/3)$, the maximum amplitude line voltage in the input vector is u_{ac}. In order to avoid the increase in high-frequency harmonics caused by direct modulation of the phase with the maximum amplitude, this section proposes a new modulation method (modulation method 1). When synthesizing the output-side voltage through effective vector modulation, this method alternates the adjustment of the two input line voltages. When turning the switch on and off, the smaller-amplitude line voltage is first used to adjust to avoid high-frequency harmonics generated by the output-side voltage due to direct switching of the maximum line voltage, further improving output-side performance.

The magnitude of the input line voltage amplitude can be determined by the position of the input vector in the sector. Therefore, it is necessary to further subdivide the original input sectors I to VI based on the original zero-crossing point as the division basis, and add the intersection point of the input three-phase voltage as the division basis. Under this method, the input sector can be divided into a total of 12 sectors, I-1 to VI-2. The schematic diagram of the new division method for the input sector is shown in Figure 7.

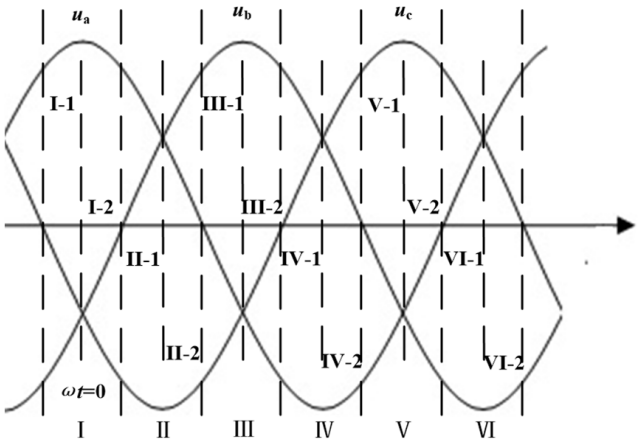


Figure 7. Schematic diagram of the new division method of the input sector.

The modulation method in this section essentially avoids direct switching of the maximum amplitude line voltage; therefore, it is necessary to further refine the time-slice signal corresponding to the effective vector. When the input vector is located in sector I-1 of Figure 7, the effective vector and zero vector action time expressions under modulation method 1 are shown in Equation (15).

$$\begin{cases} T_1 = \frac{T_{\alpha m}}{2} = \frac{d_\alpha d_m}{2} T_s \\ T_2 = T_{\beta m} = d_\beta d_m T_s \\ T_3 = \frac{T_{\alpha m}}{2} = \frac{d_\alpha d_m}{2} T_s \\ T_4 = \frac{T_{\alpha c}}{2} = \frac{d_\alpha d_c}{2} T_s \\ T_5 = T_{\beta c} = d_\beta d_c T_s \\ T_6 = \frac{T_{\alpha c}}{2} = \frac{d_\alpha d_c}{2} T_s \\ T_0 = T_s - \sum_{i=1}^{6} T_i \end{cases} \tag{15}$$

where T_1, T_2, T_3, T_4, T_5, T_6 are the effective vector action times, and T_0 is the zero vector action time.

When the input vector is located in sector I-2, the expressions for the effective vector and zero vector action times are shown in Equation (16).

$$\begin{cases} T_1 = \frac{T_{\beta m}}{2} = \frac{d_\beta d_m}{2} T_s \\ T_2 = T_{\alpha m} = d_\alpha d_m T_s \\ T_3 = \frac{T_{\beta m}}{2} = \frac{d_\beta d_m}{2} T_s \\ T_4 = \frac{T_{\beta c}}{2} = \frac{d_\beta d_c}{2} T_s \\ T_5 = T_{\alpha c} = d_\alpha d_c T_s \\ T_6 = \frac{T_{\beta c}}{2} = \frac{d_\beta d_c}{2} T_s \\ T_0 = T_s - \sum_{i=1}^{6} T_i \end{cases} \tag{16}$$

According to Equations (15) and (16), modulation method 1 divides a switching cycle into 6 effective vector action-time slices and 1 zero vector action-time slice. T_1, T_2, T_3, and T_6 are all effective vector action times with smaller line-voltage amplitudes. Taking the input in sectors I-1 and I-2 respectively and the output in sector I as an example, ignoring the influence of the input *LC* filter, the PWM switch state and output side voltage waveform at this time are shown in Figure 8. Compared with Figure 6, under modulation method 1, the input line voltage with the smaller amplitude is always used to modulate the output-side voltage first. This method can effectively reduce the high-frequency harmonics caused

by the direct switching of the maximum-amplitude phase. Compared with conventional methods, modulation method 1 only refines the effective vector action time and order, so the average effect of the two methods on the output side is consistent; that is, modulation method 1 does not affect the fundamental component of the output side.

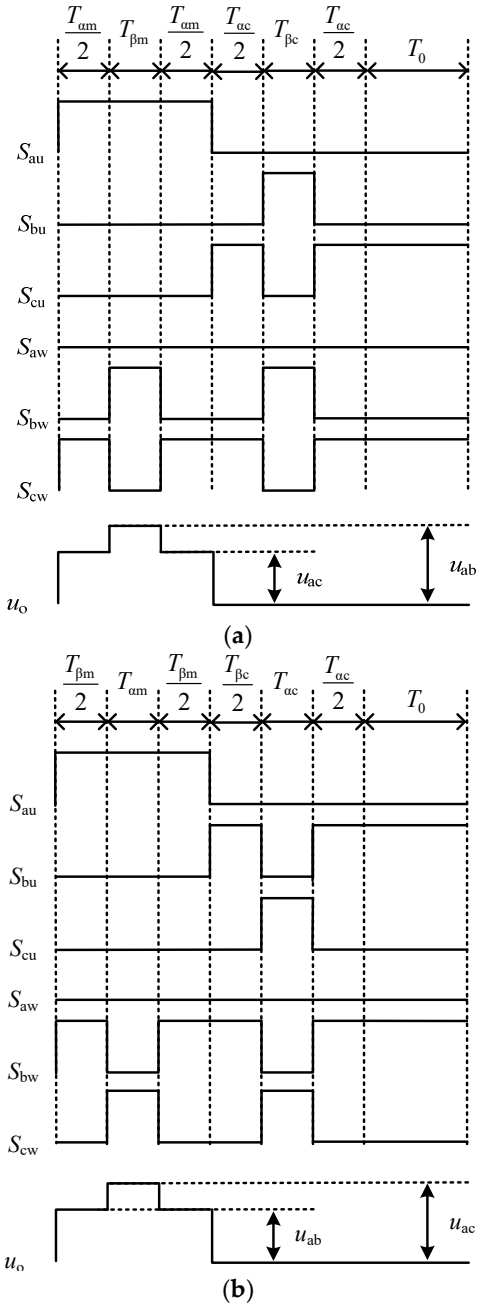


Figure 8. PWM switching state and output voltage waveform under modulation method 1: (**a**) Input I-1 sector and output I sector; (**b**) Input I-2 sector and output I sector.

3.2. Optimization Method for Switching Sequence to Reduce Switching Times per Unit Switching Cycle

According to the expressions of effective vector action time under the conventional modulation method and modulation method 1, modulation method 1 divides the action time of one effective vector equally, which increases the probability of narrow pulses appearing. Therefore, modulation method 1 has limited suppression of high-frequency harmonics on the output side.

To reduce the switching frequency within one switching cycle, this section proposes to recombine the switch combination sequences under different input and output sectors without increasing the number of effective vector action time slices (modulation method 2). The specific steps are as follows: when the sum of the input and output sectors is odd, swap the switch combination order corresponding to the effective vector action times T_1 and T_2 in Equation (14), and the switch combination order corresponding to the effective vector action times T_3 and T_4 remains unchanged; When the sum of the input sector and the output sector is even, swap the switch combination order corresponding to the effective vector action times T_3 and T_4 in Equation (14). The switch combination order corresponding to the effective vector action times T_1 and T_2 remains unchanged, ignoring the influence of the input *LC* filter. The PWM switch state and output-side voltage schematic diagram of modulation method 2 in different sectors are shown in Figure 9.

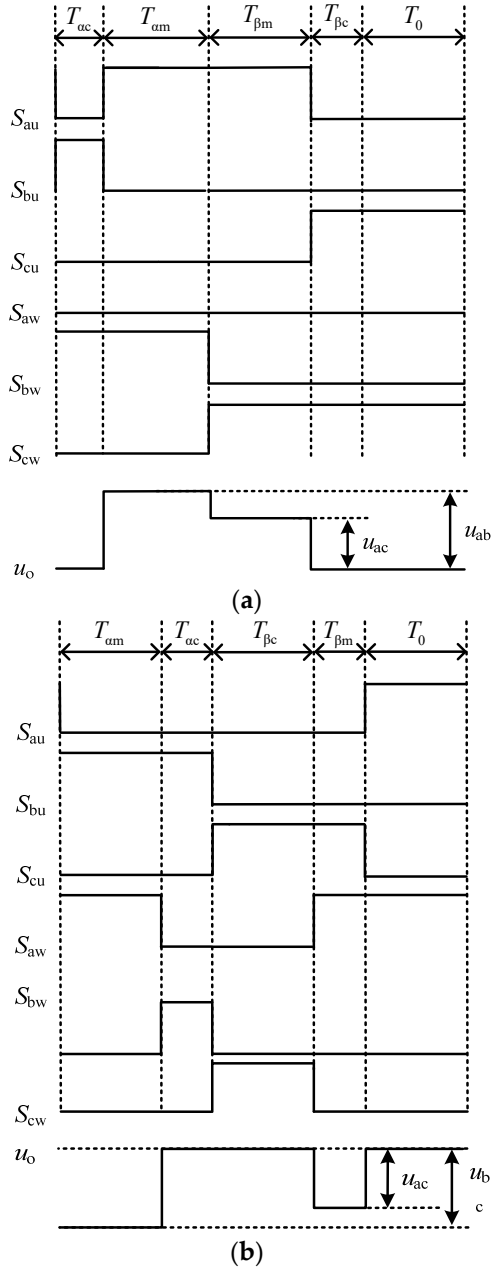


Figure 9. PWM switching state and output voltage waveform under modulation method 2: (**a**) Input I sector and output I sector; (**b**) Input I sector and output II sector.

Taking input in sector I and output in sector I and sector II, respectively, as examples, the switch combinations and switching times for the conventional modulation method and modulation method 2 can be obtained as shown in Table 2. From Table 2, it can be seen that compared with the conventional method and modulation method 1, modulation method 2 minimizes the number of switching times of the switching transistor per unit cycle. From Figures 4 and 5, it can be seen that there are a total of 24 sector combinations in the conventional modulation method (CM) and modulation method 2. Through analysis, it can be concluded that the total switching times under the 24 sector combinations mentioned above have decreased from 207 times in the conventional modulation method to 177 times in modulation method 2. Therefore, modulation method 2 aims to reduce the high-frequency harmonics on the output side by reducing the switching times.

Table 2. Switch combination state table under different modulation methods.

	Input Sector	Output Sector	Switch Combination	Number of Switching Tubes
CM	I	I	abb → bab → acc → cac → ccc	8
		II	baa → bab → caa → cac → ccc	5
Method 1	I-1	I	acc → abb → acc → cac → bab → cac → ccc	11
	I-2	I	abb → acc → abb → bab → cac → bab → bbb	11
	I-1	II	caa → baa → caa → cac → bab → cac → ccc	8
	I-2	II	baa → caa → baa → bab → cac → bab → bbb	8
Method 2	I	I	bab → abb → acc → cac → ccc	7
		II	baa → bab → cac → caa → aaa	5

4. Experimental Research and Results Analysis

To verify the effectiveness and feasibility of the proposed switch sequence optimization method for reducing high-frequency harmonics on the output side, an experimental platform based on four-step commutation with TMS320F28335 + LV4256 as the core is constructed, shown in Figure 10. Comparative analysis was conducted on the experimental results of the output side under different modulation methods. The experimental parameters are shown in Table 3, where the damping resistor R_d is connected in parallel with the input-side filtering inductor L_f to suppress the resonance of the input current.

Table 3. Experimental parameters.

Parameter	Description	Value
U_i	Input voltage amplitude (V)	$110\sqrt{2}$
f_i	Input voltage frequency (Hz)	50
L_f	Input side filtering inductance (mH)	3
C_f	Input side filtering capacitor (μF)	13.2
R_d	Damping resistor (Ω)	31
f_o	Output current frequency (Hz)	120
L	Load inductance (mH)	7.5
R	Load resistance (Ω)	20
L_c	Compensating inductance (mH)	15
f_s	Switching frequency (kHz)	10
T_c	Four-step commutation time (μs)	2.67
M	Total modulation ratio	0.654

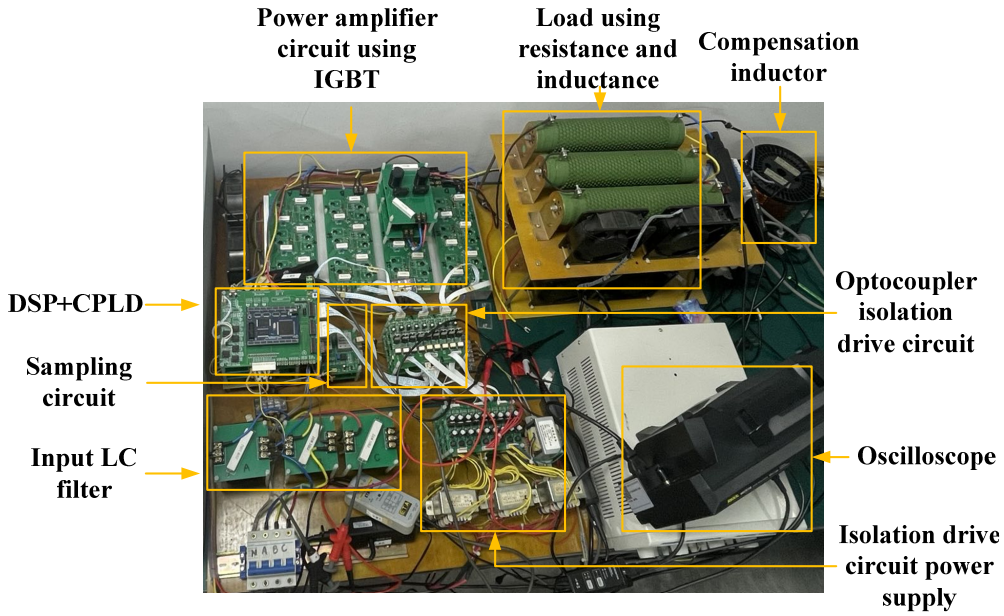


Figure 10. Experimental 3-1MC platform.

4.1. 3-1MC Experiment Under Conventional Modulation Method

Figure 11 shows the static experimental results of input and output under conventional modulation methods. As shown in Figure 11a, both the input and output currents have high sinusoidal degrees, indicating that conventional modulation methods can achieve decoupling of input and output power. Figure 11b shows the experimental waveforms of the output side voltage, current, and compensation side current. It can be seen from this figure that conventional modulation methods can maintain good static performance on the output side; According to the FFT analysis results of the output side line voltage u_o in Figure 11c, it can be seen that due to the conventional modulation method not optimizing the arrangement of the switch sequence, the *THD* value of the output side voltage reaches 35.4%, indicating a high content of high-frequency harmonics near the switch frequency in the output side voltage.

4.2. 3-1MC Experiments Under a New Type of Modulation Method

Figure 12 shows the static experimental waveforms of the 3-1MC under Method 1. As shown in Figure 12a, Method 1 maintains input-output power decoupling. Figure 12b presents the voltage and current waveforms on the output side and the compensation side, indicating satisfactory steady-state performance. A comparison of the FFT results in Figures 11c and 12c shows that the fundamental output-voltage component is comparable under the two modulation methods. Although Method 1 introduces more switching transitions per switching cycle than the conventional method, it reduces the high-frequency harmonics associated with direct commutation of the maximum-magnitude input line voltage to the zero state. The output-voltage THD decreases from 35.4% to 31.4%, corresponding to a relative reduction of 11.3%, demonstrating the effectiveness of Method 1 in suppressing output-side high-frequency harmonics in the 3-1MC.

Figure 13 shows the experimental results for the output side voltage u_o with both input and output in sector I. Compared with Figure 8, the experimental and theoretical analysis results are consistent; that is, the output-side voltage is modulated using a zero-vector switch with a smaller input amplitude and a larger phase, which avoids high-frequency harmonics caused by direct switching at the maximum-amplitude phase.

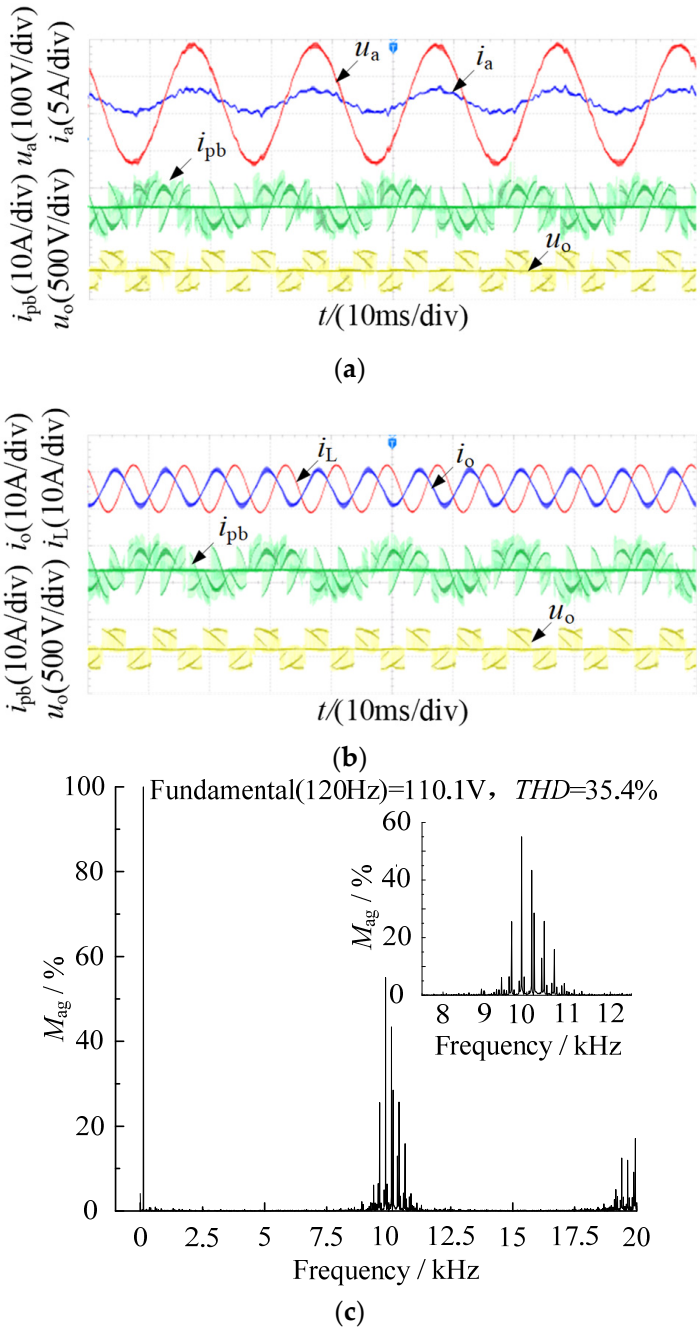


Figure 11. Experimental results of input and output under the conventional modulation method: (**a**) Input and output voltage and current experimental waveforms; (**b**) Output side and compensation side experimental waveforms; (**c**) FFT analysis of output side voltage.

Figure 14 shows the static experimental waveforms of the 3-1MC under Method 2. As shown in Figure 14a, Method 2 maintains input-output power decoupling. The FFT results in Figure 14c show that the fundamental output-voltage component obtained with Method 2 is comparable to that obtained with the conventional modulation method. By rearranging the switching-state sequence to reduce the number of switching transitions per switching cycle, Method 2 reduces the output-voltage THD from 35.4% to 27.5%, corresponding to a relative reduction of 22.3%. These results demonstrate that Method 2 effectively suppresses output-side high-frequency harmonics in the 3-1MC.

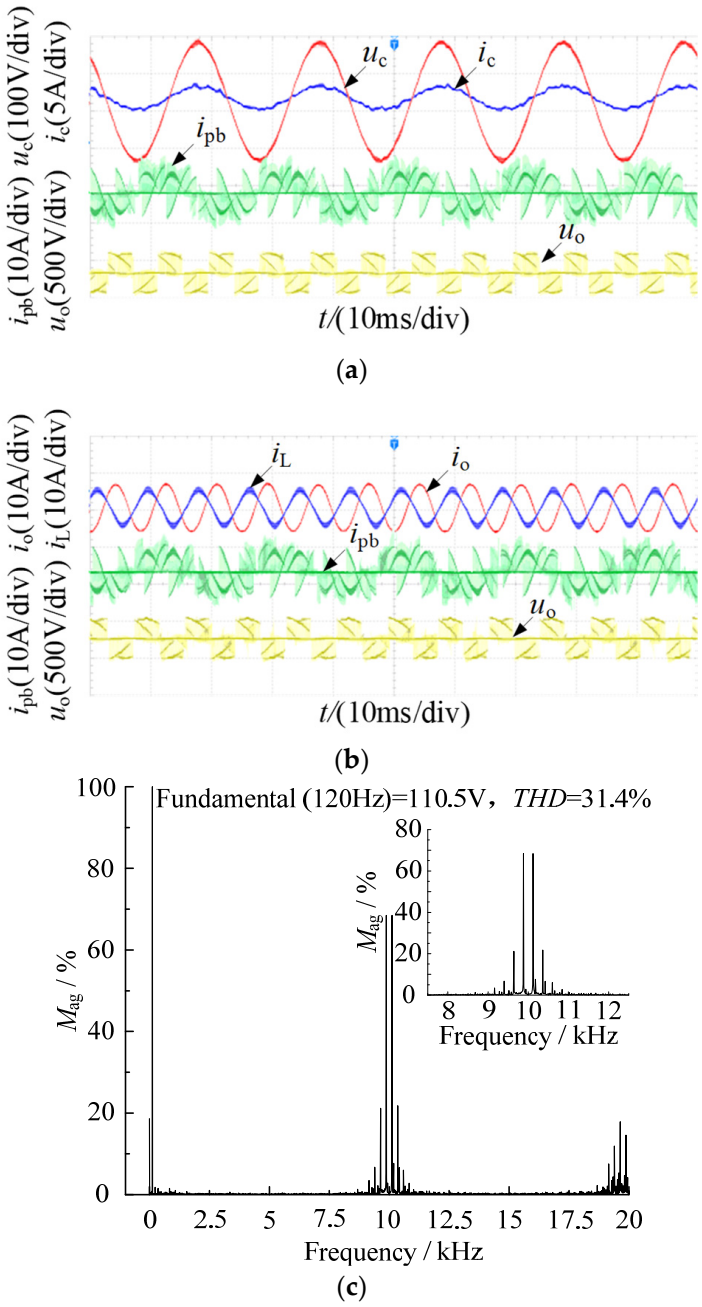


Figure 12. Experimental results of input and output under modulation method 1: (**a**) Input and output voltage and current experimental waveforms; (**b**) Output side and compensation side experimental waveforms; (**c**) FFT analysis of output side voltage.

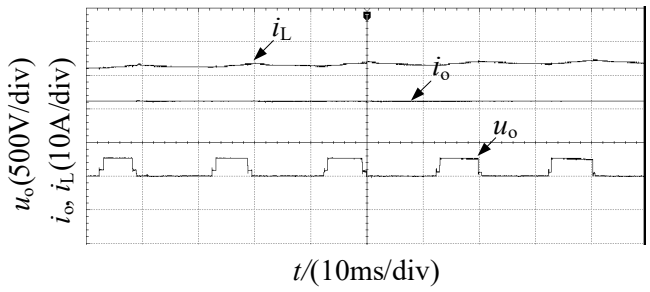


Figure 13. Experimental results of output-side voltage in input I sector-output I sector.

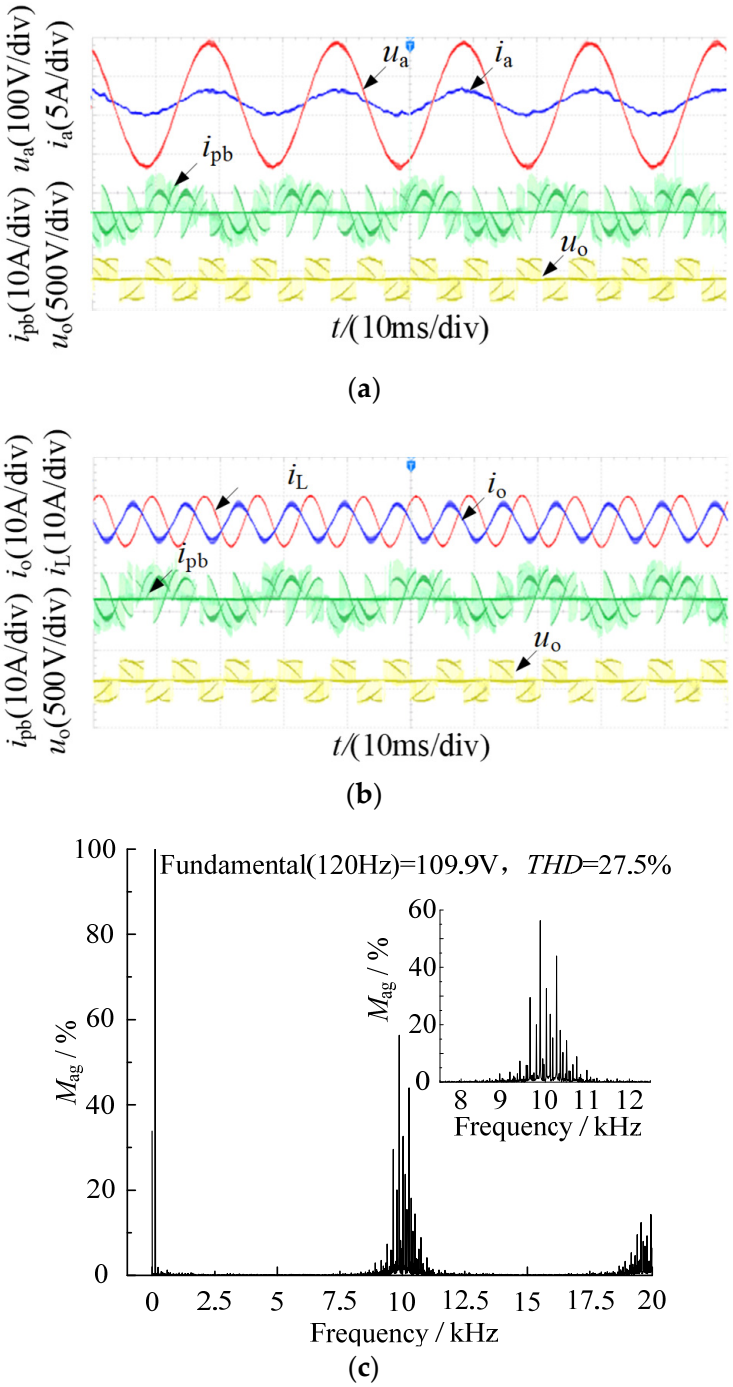


Figure 14. Experimental results of input and output under modulation method 2: (**a**) Input and output voltage and current experimental waveforms; (**b**) Output side and compensation side experimental waveforms; (**c**) FFT analysis of output side voltage.

Analyze the main high-frequency harmonics near 10 kHz and 20 kHz in Figures 11c, 12c and 14c, and list the frequency and content of the main harmonics in the above figures, as shown in Tables 4 and 5. From the frequency and content of the following harmonics, it can be seen that the main harmonics are mostly concentrated near the center of 10 kHz and 20 kHz. The main high-frequency harmonics are related to the input and output frequencies, and the high-frequency harmonics in the 10 kHz and 20 kHz ranges have the highest content in $f_s \pm f_o$ and $2f_s \pm f_o + 6f_i$.

Table 4. Main harmonic components near 10 kHz.

Harmonic Frequency f(kHz)	$f_s \pm k_2 f_o \pm k_3 f_i$	Harmonic Content/%		
		Conventional Method	Method 1	Method 2
9.64/10.36	$f_s \pm 3f_o$	25.6/12.9	21.2/21.8	29.5/18.1
9.88/10.12	$f_s \pm f_o$	55/43.4	68.5/68.5	56.3/23.7
10.18/10.42	$f_s \pm f_o + 6f_i$	28.5/25.7	7.6/6.6	15.5/10.4
10.66	$f_s + 3f_o + 6f_i$	15.9	2.1	6.2

Table 5. Main harmonic components near 20 kHz.

Harmonic Frequency f(kHz)	$2f_s \pm k_2 f_o \pm k_3 f_i$	Harmonic Content/%		
		Conventional Method	Method 1	Method 2
19.64	$2f_s - 3f_o$	12	17.9	8
19.88/20.12	$2f_s \pm f_o + 3f_i$	9.1/19.1	14.5/14.4	3.4/17
19.94/20.66	$2f_s \pm 3f_o + 6f_i$	17.1/23.7	4.2/4.2	14.3/7
20.18/20.42	$2f_s \pm f_o + 6f_i$	24.5/19.4	7.7/8.2	8/1.7
20.9	$2f_s + 5f_o + 6f_i$	14	1.7	3.1

Figure 15 shows the simulation (Matlab/Simulink R2009b) and experimental comparison results of the *THD* values of the output-side voltage under three modulation methods. From the data in the figure, it can be seen that both the simulation and experimental results show that proposed modulation methods 1 and 2 reduce high-frequency harmonics in the output-side voltage. The high-frequency harmonic suppression effect of the switch sequence optimization method (modulation method 2), which reduces the switching frequency per unit switching cycle, is more significant.

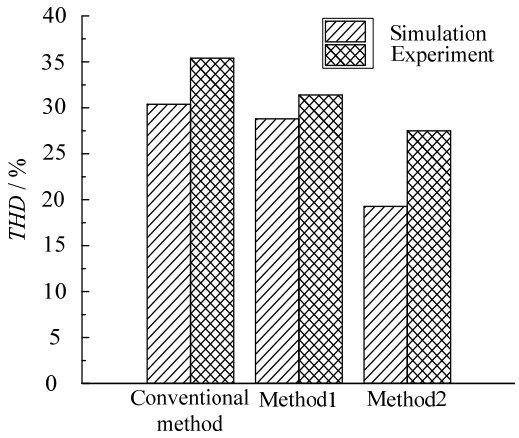


Figure 15. *THD* analysis results under different modulation methods.

5. Conclusions

To suppress the high-frequency harmonics on the output side of a three-phase-to-single-phase matrix converter (3-1MC) under conventional modulation, two PWM switching-sequence optimization methods were proposed. Method 1 avoids the direct commutation of the maximum-magnitude input line voltage to the zero state by inserting two lower-magnitude line-voltage segments. Method 2 rearranges the existing switching-state sequence without changing the total action times of the effective vectors, thereby reducing the total number of switching transitions over the 24 sector combinations from 207 to 177.

Both methods require no additional switching-state combinations and preserve input-output power decoupling. The simulation and experimental results in Figure 11 show consistent trends. The simulated output-voltage THD values for the conventional modulation method, Method 1, and Method 2 are 30.38%, 28.80%, and 19.26%, respectively, while the corresponding experimental values are 35.4%, 31.4%, and 27.5%. These results confirm that both proposed methods effectively suppress output-side high-frequency harmonics, with Method 2 providing the greater reduction.

However, the validation is mainly limited to the tested operating conditions. The effects of different loads, modulation indices, input voltages, switching frequencies, and transient operating states have not been systematically investigated. Future work will evaluate the proposed methods over a wider range of operating points and further study their switching losses, efficiency, thermal performance, and applicability to other converter configurations and more demanding experimental scenarios.

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