

Article

Rational Symmetry-Guided Design of Resonant DC–DC Converters: Topology Screening, Feasible-Region Synthesis, and Tolerance-Aware LLC Assessment

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Abstract

Resonant DC–DC converter design requires family selection, feasible operating regions and component targets to be evaluated consistently. ResoSym-RD links topology-aware normalized screening to physical-unit synthesis based on the fundamental-harmonic approximation (FHA), rounded component targets and independently tested timing schedules. Series resonant (SRC), parallel-loaded resonant (PLRC), inductor–capacitor–capacitor (LCC) and inductor–inductor–capacitor (LLC) families retain their native reduced models. Nested search domains expose boundary-dependent coverage and trade-offs rather than a universal topology ranking. For a 360–420 V/48 V, 1 kW LLC case, the retained 20 μH /88 nF/106 μH targets have a minimum nominal normalized margin of 1.441. A prespecified rounded FHA comparator has a lower nominal margin and a higher ranking proxy, but a higher fixed-timing sampled pass fraction. With matched timing perturbations, an independent 20,000-realization test gives 99.925% charge-only feasibility for the locked schedule versus 98.860% for fixed 250 ns timing. A new common parasitic switched-circuit assessment compares both tanks over all nine corners. At equal 48 V output, the ResoSym-RD tank has 1.42% lower uniformly averaged modeled dissipation, but not at every corner. The uncorrected FHA schedule produces output errors up to 5.61%, and the ResoSym-RD peak-current error reaches 21.06%, establishing the need for time-domain closure. Executed commutation traces, step refinement and a separate numerical integrator support the declared generic circuit results. The study is an auditable pre-synthesis methodology, not a claim of measured efficiency, field reliability, electromagnetic interference (EMI) compliance or hardware qualification.

Keywords: adaptive dead time; design automation; feasible region; LLC resonant converter; resonant DC–DC converters; robustness; soft switching; symmetry-guided design; tolerance analysis; topology screening



Academic Editors: Vasilis K. Oikonomou, Gerardo Mino-Aguilar, Jesús Linares-Flores and Edgar Peralta-Sánchez

Received: 25 August 2026

Revised: 15 September 2026

Accepted: 24 September 2026

Published: 26 September 2026

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1. Introduction

Resonant DC–DC conversion uses reactive energy storage to shape current and voltage around switching events [1,2]. Classical network analyses establish the series, parallel and series–parallel relationships [3,4], and the LLC resonant tank combines a series branch with transformer magnetizing participation [5]. Zero-voltage switching (ZVS) and zero-current switching (ZCS) nevertheless depend on device-transition conditions. Reaching a nominal

gain is not, by itself, proof that the switching path has the required current, charge or timing reserve.

Established LLC design methods already go beyond undirected trial and error. Operation mode analysis resolves conduction intervals and gain limits [6], whereas fundamental-harmonic approximation (FHA) offers a compact impedance and reflected-load description [7]. Wide output range synthesis, tank current inspection and computer-aided efficiency optimization make different parts of the coupled design problem explicit [8–10]. The unresolved task addressed here is therefore not the invention of analytical design or optimization. It is the auditable connection between family choice, the declared search domain, simultaneous operating corner constraints, rounded component targets and independently assessed timing statistics.

The mode-resolved work by Grigorova and Vuchev is directly relevant to that distinction. Their state plane-based design methodology treats a frequency-controlled full-bridge LLC converter above resonance and uses analytical quantities for component selection [11]. Vuchev, Grigorova and Vuchev subsequently address ideal-component LLC boost operation explicitly [12]. These are different operating domains, not interchangeable descriptions of one universal gain curve. For the present half-bridge benchmark, their relevance is methodological: the low-line boost corner and the above-resonance corners require separate scrutiny before a common FHA screen is interpreted as an implementation-level result.

The 2023 optimal trajectory studies further distinguish the operating solution from the controller realization. The basic characteristics study considers above-series-resonance operation with continuous rectifier input current and derives output/control characteristics from state-space analysis [13]. The companion modeling paper describes an OrCAD PSpice functional model, including steady operation, large control changes and an output short circuit [14]. These investigations motivate control-specific regime assessment; they do not provide numerical validation of the different converter and the scheduling law used here.

In 2024, Grigorova and Vuchev examine how the parallel-to-series inductance ratio and switching-to-resonant frequency ratio affect commutation under phase-shift regulation in continuous conduction mode [15]. This identifies a joint dependence on tank parameters, operating point and modulation, rather than a ZVS property attached to the topology name. Their simple trajectory current source study also relates the control range and output characteristics to the inductance ratio [16]. Its state plane and simulation results caution against assigning an immutable voltage source or current source function solely from the label LLC. Accordingly, the present family comparison retains native models and a declared voltage regulation task; it does not transfer phase-shift or current source operating limits to the frequency-controlled half bridge.

Optimization objectives must be distinguished just as carefully. Wei et al. combine time-domain analysis, RMS-current minimization and an automatic design tool, with a 2.5 kW prototype reported for their selected design [17]. Yin and Luo use a time-domain model and stepwise constraints: gain, ZVS and capacitor voltage requirements accompany minimization of frequency range and current-related objectives [18]. These are substantive prior design procedures, not merely nominal gain fitting. ResoSym-RD instead makes the worst-corner normalized reserve the primary selection criterion and reports the resulting trade-off with a prespecified FHA hand-calculated comparator; it does not claim to outperform a reimplement of either published optimizer.

Recent application-driven studies also show why a single numerical ranking cannot be generalized. Zaikin et al. combine constant-power gain analysis, gain/turns-ratio optimization and multi-channel phase-shift operation, and report a four-channel 5 kW prototype [19]. That load law and control architecture differ from the present nine-corner, fixed-output half-bridge benchmark. Leone et al. integrate tank synthesis with constructive

transformer/inductor selection and thermal and winding constraints, supported by a 1 kW prototype [20]. Their work identifies the additional engineering required to convert feasible inductance targets into qualified magnetic components. The present voltage, flux and dissipation estimates cannot be substituted for that constructive and experimental evidence.

Dead time design requires a similarly explicit evidence boundary. Jiao et al. incorporate switch and transformer capacitances into a time-domain analysis, derive a permissible dead time range and compare predictions with a 10 kW prototype [21]. A sufficient-charge estimate is therefore only a screening condition, not a complete lower and upper timing window. Lange et al. describe adaptive timing based on body diode conduction detection under hybrid pulse-frequency/phase-shift modulation [22]. That observed-event approach differs from the present offline quantile-derived schedule: the latter is frozen before holdout testing and is not a demonstrated cycle-by-cycle feedback controller. Abbasi and Ghayebloo compare a two-harmonic dynamic model with other approximations and an experimental reference [23], reinforcing the distinction between repeatable calculations and validated waveform accuracy.

These studies define the role of the present contribution. Native mode equations, trajectory control, current-oriented optimization, parasitic timing analysis and magnetic design are established but answer different questions. ResoSym-RD combines domain-aware family screening with simultaneous corner margins, a full re-evaluation of rounded targets, matched timing perturbations and a locked independent test, followed by a common generic switched-circuit comparison. Resonance-centered and symmetry-oriented work motivates the shared questions [24–26], but does not justify universal circuit equivalence or universal superiority. The numerical results explicitly retain unfavorable comparisons and model discrepancies. Hardware measurements and device-specific magnetic, thermal and control closure remain the subsequent research stage.

The term symmetry-guided is used here in a restricted engineering sense. Candidate families are embedded into common normalized coordinates centered on resonance, and equivalent design questions are asked of every family: Can the required gain be reached? How far is the selected frequency from the usable boundaries? Where is the reactive burden transferred? Is the input impedance sufficiently inductive? Which constraint becomes active when parameters vary? The method does not claim that SRC, parallel-loaded, LCC, and LLC networks are exact duals or circuit isomorphisms. Instead, a topology-dependent embedding and an implicit applicability mask preserve family-specific physics while supporting a common screening logic.

The paper makes the following contributions:

- A two-level workflow connects normalized family screening with physical-unit LLC feasible-region synthesis and tolerance-aware assessment.
- Nested family-tuning domains and a local refinement separate parameter-bound dependence from the declared frequency, phase and burden constraints.
- A physical LLC design region is constructed in the (Q, m) plane, where Q is the full-load quality factor and $m = L_m/L_r$ is the magnetizing ratio. Gain, ZVS charge, inductive operation, frequency headroom, current, capacitor voltage, flux, and sensitivity limits are intersected before component values are selected.
- A max-min normalized margin is used as the primary design objective. Loss and circulation proxies are used only after feasibility has been secured.
- A selected rounded component-target triplet is re-evaluated explicitly; an automatic catalog-selection algorithm is not claimed.
- A 20,000-realization calibration population is complemented by an independent 20,000-realization test population and a prespecified rounded FHA comparator.

- Locked dead time commands are compared with fixed timing under the same perturbations; a 5 ns command grid and a stricter guard-retention criterion are reported separately.
- A matched generic switched-circuit comparison tests both rounded tanks beyond FHA, with calculated commutation records, explicit model-error reporting and separate numerical convergence checks.

The scope is deliberately limited to unidirectional resonant DC–DC conversion. The bidirectional SEPIC/ZETA line is kept separate because commutation overlap, duty loss, and direction-dependent dynamics require a distinct treatment. CLLC and other bidirectional resonant structures are reserved for a later extension after the present LLC-centered design methodology is established.

2. Position Relative to Existing Design Methods

Table 1 compares the actual scope, design decision and evidence level of the closest studies. A topology-local method is not marked deficient merely because it does not solve cross-family selection, and a hardware result is not treated as directly transferable to the present circuit. The numerical comparator in Section 6.3 remains an independently specified FHA reference design, not a reproduction of any cited control or optimization algorithm.

Table 1. Study-specific positioning of ResoSym-RD relative to analytical, control, optimization and validation methods.

Study/Year	Established Decision or Scope	Evidence Level	Consequence for This Study
Grigorova et al. (2021); Vuchev et al. (2023) [11,12]	Above-resonance state plane synthesis versus an ideal-component boost analysis.	Analytical regime-specific treatment; simulation reported for the 2021 design.	Keep boost and above-resonance domains distinct; do not promote one reduced description to all-mode validity.
Vuchev et al.; Vuchev and Grigorova (2023) [13,14]	Optimal trajectory characteristics and a functional model above resonance with continuous rectifier input current.	State-space analysis and OrCAD PSpice scenarios.	Control realization is separate from steady-state gain screening; the present schedule is not that trajectory controller.
Grigorova and Vuchev (2024; 2023) [15,16]	Inductance/frequency ratios and phase-shift commutation; current source behavior under simple trajectory control.	Parameter analysis and state plane/simulation evidence.	Modulation and output objective must accompany a family label. Published operating boundaries are not transferred numerically.
Wei et al. (2022) [17]	Automatic time-domain, RMS-current-oriented LLC parameter optimization.	Analytical design and a reported 2.5 kW prototype.	Automation and current-based optimization are prior art; max–min reserve is a different objective.
Yin and Luo (2024) [18]	Stepwise gain, ZVS and capacitor voltage constraints; frequency-span and current objectives.	Time-domain multi-objective design.	A genuine constrained-design baseline, not trial and error; no numerical replication is claimed here.
Zaikin et al. (2024) [19]	Constant-power gain and turns-ratio optimization for multi-channel phase-shift LLC.	Analysis, supplied code and a reported 5 kW prototype.	Load law and channel/control architecture differ; comparison is methodological, not a matched efficiency ranking.
Jiao et al. (2023); Lange et al. (2025) [21,22]	Parasitic-aware dead time window versus body diode detection-based adaptation.	Time-domain/prototype evidence in Jiao; detection-based control reported by Lange.	Charge-only feasibility and an offline quantile lookup are not a qualified timing window or demonstrated feedback.
Abbasi and Ghayebloo (2025) [23]	Two-harmonic dynamic approximation compared with other models.	Experimental-reference model comparison.	Integrator agreement does not determine physical model accuracy; assess waveform and regime errors separately.

Table 1. Cont.

Study/Year	Established Decision or Scope	Evidence Level	Consequence for This Study
Leone et al. (2025) [20]	Joint tank and constructive magnetic design with flux, winding and thermal constraints.	Constructed magnetics and a reported 1 kW prototype.	Rounded inductances and a flux screen remain pre-synthesis targets, not completed magnetic/thermal design.
ResoSym-RD	Family/domain audit → simultaneous margins → rounded targets → independent timing assessment.	FHA screening, holdout sampling and matched generic switched-circuit calculations.	Traceable selection and explicit trade-offs; no universal dominance, prototype qualification or field reliability claim.

The relevant comparison is therefore functional: what is selected, under which operating and control assumptions, and with what evidence? The method-specific differences below justify the combined pre-synthesis workflow while delimiting what it does not establish.

This separation is important for both scientific clarity and practical use. A family map can show that LLC is a bridge structure, but it does not determine L_r , C_r , L_m , or the switching frequency schedule. A modal map can identify a desirable PO region, but it does not quantify whether standard components retain sufficient current, voltage, flux, and tolerance margins. A cross-family corridor can compare reduced networks, but its topology-neutral thresholds may penalize a family whose native output objective differs. ResoSym-RD therefore uses two related but distinct models: a normalized screening model for family choice and a physical LLC model for final synthesis.

Closed Design Workflow

The transition from comparative resonant converter theory to an auditable design procedure is organized through the closed workflow shown in Figure 1. The scheme separates early family rejection from physical LLC synthesis and explicitly includes a return path when the common feasible corridor is empty.

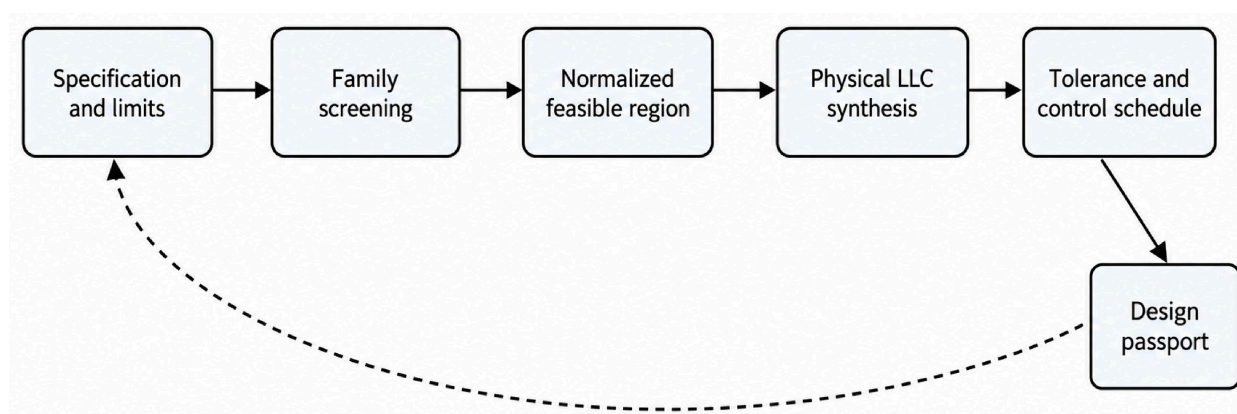


Figure 1. ResoSym-RD rational design workflow. Solid arrows indicate progression from specifications and family screening through feasible-region synthesis, physical LLC design and tolerance assessment to the design passport. The dashed arrow indicates a return to the specifications and limits when the feasible region is empty or the requirements need revision. The common screening stage can reject a family before detailed simulation; the physical stage produces a standard-values design, tolerance statistics and a design passport.

The workflow in Figure 1 contains a deliberate return path. If the common corridor is empty, the designer must revise the specification, device envelope, transformer ratio, frequency band, or family choice. The algorithm is not forced to return a superficially optimal point when the requirements are mutually incompatible.

3. Topology-Aware Normalized Screening

3.1. Common Coordinates and Assumptions

A consolidated list of symbols and conventions is provided in Table A1 immediately before the References section.

The family screening stage uses normalized angular frequency:

$$F = \frac{\omega}{\omega_r}, \quad \omega_r = 1, \quad Z_r = 1, \quad Q = \frac{Z_r}{R} = \frac{1}{R}. \quad (1)$$

Here, ω is the operating angular frequency, ω_r is the reference resonant angular frequency, Z_r is the characteristic impedance, R is the normalized load resistance, and Q is the corresponding quality factor. The assignments $\omega_r = 1$ and $Z_r = 1$ are per-unit bases used only in the family screening model.

The normalized load is therefore $R = 1/Q$. Every family is represented as a series impedance Z_s followed by an output-side impedance Z_p . The normalized transfer function is:

$$H_{\mathcal{T}}(F, Q, \eta) = \frac{Z_p}{Z_s + Z_p}, \quad (2)$$

In this expression, $\mathcal{T}$ identifies the candidate family, η is its active structural coordinate, Z_s and Z_p are the topology-specific series and output-side impedances, and $Z_{in} = Z_s + Z_p$. The complex transfer ratio is $H_{\mathcal{T}}$. For cross-family comparison, $H_{ref} = |H_{\mathcal{T}}(1, Q_{full}, \eta)|$ and $G_{\mathcal{T}} = |H_{\mathcal{T}}| / H_{ref}$; the symbol j denotes $\sqrt{-1}$.

Here, $\mathcal{T}$ identifies the topology and η is a family-specific structural parameter. For LCC, $\eta = \alpha = C_p / C_s$; for LLC, $\eta = m = L_m / L_r$; SRC and the selected parallel-loaded form do not require an additional structural coordinate.

C_s is the LCC series capacitance and C_p is its output-side shunt capacitance, both in farads before normalization; α is their dimensionless ratio. T and $\mathcal{T}$ identify the same converter family.

The four candidate families cannot be compared by forcing them into an identical circuit model; instead, each is mapped through a topology-aware embedding into a shared set of screening coordinates. Figure 2 illustrates the native reduced model retained for each family and the common coordinates used for cross-family evaluation.

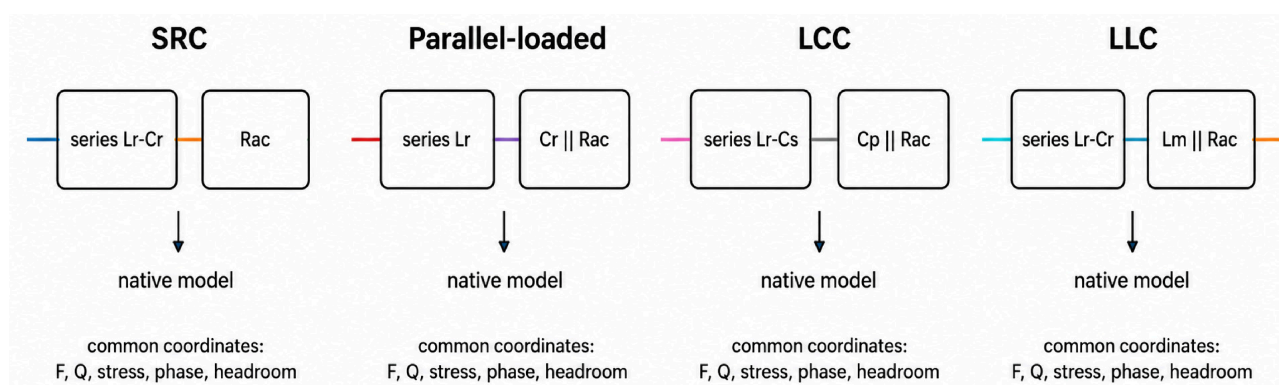


Figure 2. Topology-aware reduced embeddings used for SRC, parallel-loaded, LCC, and LLC screening. Common coordinates support comparison, whereas the native model and structural parameter remain topology dependent. The colored line segments distinguish the four topology diagrams and do not encode additional circuit parameters. The black arrows indicate the mapping from each topology's native model to the common screening coordinates.

To make the common screening stage reproducible while preserving topology-specific physics, Table 2 collects the normalized series and output-side impedances and the structural coordinate used for each candidate family. The complex operator is denoted by j .

Table 2. Normalized reduced tank models used in family screening.

Family	Series Impedance Z_s	Output-Side Impedance Z_p	Structural Coordinate
SRC	$j(F - 1/F)$	R	none
Parallel-loaded (PLRC)	jF	$(1/R + jF)^{-1}$	none
LCC	$j(F - 1/F)$	$(1/R + j\alpha F)^{-1}$	$\alpha = C_p/C_s$
LLC	$j(F - 1/F)$	$R \parallel j\alpha F$	$m = L_m/L_r$

For each family, the following normalized quantities are computed:

$$K_I = \frac{\max\{|I_{in}|, |I_{load}|, |I_{sh}|\}}{|I_{load,ref}|},$$

$$K_{circ}^{scr} = \frac{\sqrt{|I_{in}|^2 + |I_{sh}|^2}}{|I_{load,ref}|},$$

$$K_V = \max\{|V_C|, |V_L|, |H|\}. \quad (3)$$

The three current symbols denote the complex normalized RMS phasors obtained from the corresponding native reduced network. The reference load-current magnitude is the product of the resonance-centered transfer reference and the full-load quality factor. The voltage symbols denote the maximum capacitor- and inductor-voltage phasors. The displayed current-burden, screening-circulation, and voltage-burden indices are therefore dimensionless phasor-based coordinates, not semiconductor loss models.

Throughout Section 3, H is shorthand for $H_{\mathcal{T}}$ of the family under evaluation, whereas G is the resonance-centered gain $G_{\mathcal{T}} = |H_{\mathcal{T}}|/H_{ref}$. Thus, $|H|$ in Equation (3) is not interchangeable with G . All impedances, currents and voltages in this screening stage use the declared per-unit bases.

The current and voltage measures are not loss models. They are burden coordinates that reveal where the price of regulation and soft-switching potential is transferred. A low gain-stress family may pay through circulating current; another may retain moderate current at the price of a capacitor or inductor voltage excursion.

3.2. Specification-Driven Gain Requirement

The normalized screening is anchored at the nominal input voltage. For a regulated output and fixed nominal transformation, the required normalized gain is:

$$G_{req}(V_{in}) = \frac{V_{in,nom}}{V_{in}}. \quad (4)$$

The nominal input $V_{in,nom}$ used to normalize the required gain is 400 V, whereas V_{in} is the line voltage at the evaluated corner. The prescribed load fraction ℓ is the output power at regulated V_o divided by the rated output power $P_{o,rated}$. The corner set combines the three line values with $\ell = 0.25, 0.50$ and 1.00 .

For the case study, $V_{in} \in \{360, 400, 420\}$ V, so the three gain levels are 1.1111, 1.0000, and 0.95238. The load set is $\ell \in \{0.25, 0.50, 1.00\}$, producing nine screening corners.

A gain root is retained only if it lies in:

$$F \in [F_{min}, F_{max}] = [0.625, 1.50], \quad (5)$$

and satisfies the preliminary restrictions:

$$\angle Z_{in} \geq 2^\circ, \quad K_I \leq 4, \quad K_V \leq 4. \quad (6)$$

These thresholds are screening limits, not universal design constants.

3.3. Resonance-Centered Control Headroom

A frequency root located close to a boundary is less useful than a root with the same gain near the center of the usable interval. The normalized headroom is defined as:

$$H_c(F) = \text{clip} \left[\min \left(\frac{F - F_{\min}}{1 - F_{\min}}, \frac{F_{\max} - F}{F_{\max} - 1} \right), 0, 1 \right]. \quad (7)$$

The clipping operator limits headroom to the unit interval. The lower and upper frequency bounds are those in Equation (5).

Thus, $H_c = 1$ at $F = 1$ and $H_c = 0$ at either frequency limit. The local gain slope look like this:

$$S_G = \left| \frac{dG}{dF} \right| \quad (8)$$

In Equation (8), $G \equiv G_{\mathcal{T}}$ is the transfer magnitude divided by its resonance-centered reference. The derivative with respect to F is evaluated at fixed load quality factor Q and structural coordinate η , using a centered finite difference around each candidate root.

The slope is included because a root on a steep branch can be sensitive to control quantization, parameter drift and numerical interpolation.

For each corner, the root-selection cost is:

$$J_{\text{scr}} = 0.28(1 - H_c) + 0.13|F - 1| + 0.24 \frac{\max(K_{\text{circ}}^{\text{scr}} - 1, 0)}{3} + 0.17 \frac{\max(K_V - 1, 0)}{3} + 0.18 \min \left(\frac{S_G}{5}, 1 \right). \quad (9)$$

The five numerical weights sum to unity and encode declared screening preferences. Division by three scales the excess-burden penalties; it does not impose an additional admissibility bound. The voltage-burden penalty is at most unity when $K_V \leq 4$, whereas the circulation penalty may exceed unity because no $K_{\text{circ}}^{\text{scr}} \leq 4$ condition is imposed. The gain-slope contribution is explicitly capped by $\min(S_G/5, 1)$. Consequently, the weight sum does not itself bound J_{scr} to $[0, 1]$.

The coefficients are declared design preferences. Coverage is maximized first; among equal-coverage candidates, the algorithm favors larger minimum headroom, lower mean cost, and lower maximum burden.

3.4. Family-Tuning Domain

The initial domain D0 is retained as an auditable baseline: $Q_{\text{full}} = 0.18\text{--}0.85$, LCC $\alpha = 0.05\text{--}2.0$ and LLC $m = 3\text{--}12$. D1 extends these to $0.09\text{--}1.70$, $0.025\text{--}4$ and $1.5\text{--}24$; D2 to $0.03\text{--}3.40$, $0.01\text{--}8$ and $1\text{--}48$; and D3 to $0.03\text{--}8.0$, $0.01\text{--}8$ and $0.1\text{--}48$. All preceding nodes are retained. The frequency band $0.625\text{--}1.50$, phase floor and K_I/K_V limits do not change. The outer domains are exploratory sensitivity domains, not assertions that all such magnetic ratios are practical.

$$Q(\ell) = Q_{\text{full}} \ell. \quad (10)$$

Thus, the full-load quantity is the quality factor at unit load fraction, while the load-dependent quantity is the value used by the normalized screening code at each operating corner.

This convention follows the normalized model used in the code and must be retained when reproducing the reported results. Alternative conventions are possible, but mixing definitions across family models would invalidate the comparison.

Gain roots in this audit are obtained from the positive-real roots of the exact native transfer-magnitude polynomials in F^2 . Root gain residuals are checked below 10^{-7} . This

removes the previous nearest-frequency-grid acceptance shortcut while retaining the native impedances and lexicographic ranking. A local 61-level refinement around each D3 winner tests local sampling sensitivity. All selected D3 points lie inside the expanded parameter bounds; several approach active K_I or K_V constraints instead. Nested finite searches and local refinement do not certify a global continuous optimum.

The explicit decision order is gain-corner coverage, minimum frequency headroom, mean screening cost, maximum circulation and maximum voltage burden. A different priority can retain a different family. The audit therefore reports both the original bounded result and the expanded result rather than treating the initial search box as a physical impossibility boundary.

A first visual comparison is obtained by evaluating all four reduced models at a common baseline parameter set. Figure 3 superimposes their normalized gain characteristics on the gain band required by the 360–420 V input envelope, revealing that gain intersection alone does not guarantee acceptable control headroom or reactive burden.

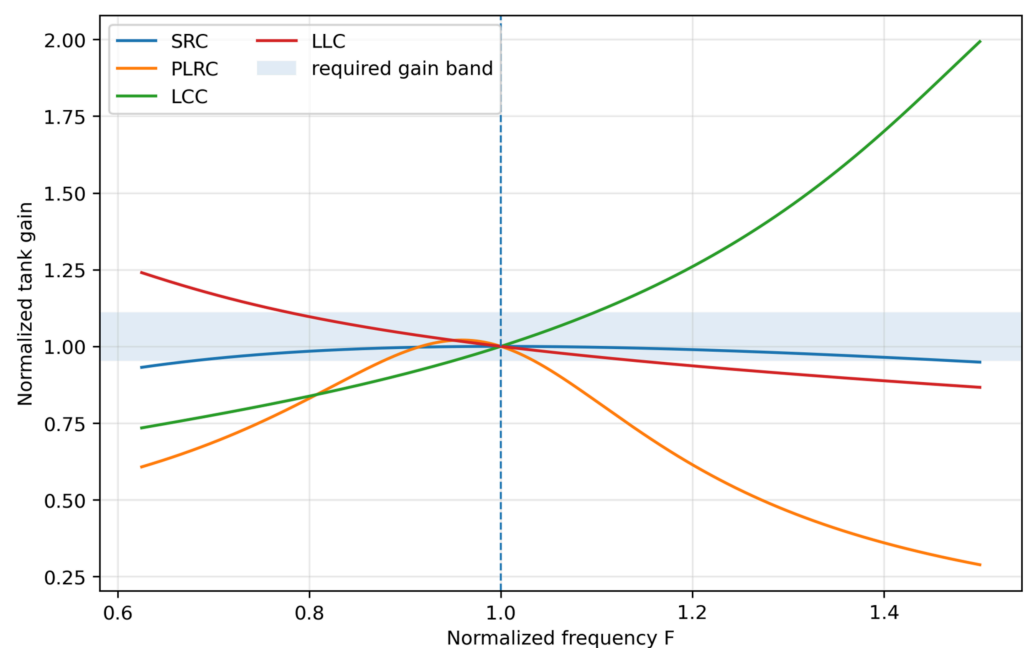


Figure 3. Common-baseline normalized gain curves at $Q = 0.4$. The shaded band is the gain range required by the 360–420 V input envelope.

4. Physical LLC Synthesis

4.1. Case Specification

Before the physical LLC synthesis is carried out, the numerical specification and the screening-level electrical, magnetic, and control limits must be fixed. Table 3 consolidates these quantities and defines the nine input–load corners used throughout the subsequent analysis.

Table 3. Physical LLC specification and screening-level device envelope.

Quantity	Value	Role	Symbol
Input voltage	360, 400, 420 V	line corners	V_{in}
Output voltage	48 V	regulated output	V_o
Rated power	1 kW	full-load point	$P_{o, rated}$
Load fractions	25%, 50%, 100%	load corners	ℓ
Target resonant frequency	120 kHz	nominal center	f_r^*

Table 3. Cont.

Quantity	Value	Role	Symbol
Allowed switching frequency	75–180 kHz	control band	$f_s \in [f_{\min}, f_{\max}]$
Transformer ratio $n = N_p/N_s$	4.1667	nominal half-bridge match	$n = N_p/N_s$
Primary turns N_p	20	idealized flux reference; winding closure pending	N_p
Effective core area A_e	200 mm ²	flux screening	A_e
Flux-density limit	0.18 T	preliminary magnetic bound	$B_{\max}$
Total commutated $Q_{\text{oss},\Sigma}$	250 nC	device-envelope charge	$Q_{\text{oss},\Sigma}$
Fixed dead time	250 ns	baseline control setting	$t_{d,\text{fix}}$
Charge safety factor	1.20	ZVS charge reserve	k_Q
Dead time guard	25 ns	scheduling reserve	t_{guard}
Primary peak-current limit	13 A	stress bound	$I_{r,\text{pk},\max}$
Resonant capacitor peak limit	650 V	FHA AC-amplitude screen; not full capacitor rating	$V_{C_r,\text{pk},\max}$
Minimum inductive angle	5 degrees	commutation screen	$\varphi_{\text{deg},\min}$
Minimum control headroom	0.25	regulation reserve	$H_{f,\min}$
Gain-sensitivity limit	3.5	control robustness	$S_{F,\max}$

Table 3 separates a declared benchmark from a qualified component design. Input/output ratings and the nine corners define the task; $n = 400/(2 \times 48)$ aligns the ideal nominal half-bridge gain; 120 kHz and 75–180 kHz define an illustrative resonance and control band. The 250 nC charge, 250 ns timing, 20% charge reserve, 25 ns allowance, 13 A current, 650 V harmonic-voltage envelope, 0.18 T flux screen, 5° phase floor, 0.25 headroom and 3.5 sensitivity limit are engineering scenario choices, not universal device limits. Their effects must be re-evaluated for the selected components and controller.

The magnetic quantities require particular care: $N_p = 20$ and $n = 4.1667$ form an idealized volt-second reference, not a completed integer-turn winding design. A realizable turns pair, core material, gap and winding arrangement must be selected and all magnetic margins recomputed before implementation. Likewise, the reported V_{C_r} peak is the FHA AC-component amplitude; a physical capacitor rating must account for its actual DC bias, transients and derating. The present 650 V comparison is a screening envelope, not component qualification.

4.2. FHA Tank Model

The use of FHA here is a deliberate pre-synthesis choice, not a claim of state plane accuracy. The above-resonance design and boost analyses of Grigorova and Vuchev address their declared regimes explicitly [11,12], while the multiharmonic comparison of Abbasi and Ghayebloo addresses a different model-fidelity question [23]. The same-command and equal-output checks in Section 6.8 test the present approximation at the actual benchmark corners; they do not inherit a validity range from those other circuits.

The physical model uses complex root-mean-square (RMS) phasors under the fundamental-harmonic approximation. The angular frequency is $\omega = 2\pi f_s$; vertical bars denote phasor magnitude and the parallel symbol denotes the product-over-sum combination. At the regulated benchmark voltage $V_o = 48$ V, $P_o(\ell) = \ell P_{o,\text{rated}}$, with $P_{o,\text{rated}} = 1$ kW.

The full-load reference DC resistance is:

$$R_o = \frac{V_o^2}{P_{o,\text{rated}}}. \quad (11)$$

For load fraction ℓ , the primary-referred fundamental AC resistance is:

$$R_{ac}(\ell) = \frac{8}{\pi^2} \frac{n^2 R_o}{\ell}. \quad (12)$$

Here R_o is fixed at the full-load reference, not recomputed from the partial-load power. The physical load at a prescribed fraction ℓ is R_o/ℓ , so Equation (12) accounts for load variation exactly once. The turns ratio is $n = N_p/N_s$, and $R_{ac,full} = R_{ac}(1)$. In the unregulated same-command circuit tests of Section 6.8, ℓ labels this prescribed resistance; actual delivered power changes with the calculated output voltage.

The resonant and magnetizing impedances are:

$$\begin{aligned} Z_s &= j\omega L_r + \frac{1}{j\omega C_r}, & Z_m &= j\omega L_m, \\ Z_p &= Z_m \parallel R_{ac}, & Z_{in} &= Z_s + Z_p. \end{aligned} \quad (13)$$

The tank transfer ratio is:

$$H(\omega) = \frac{Z_p}{Z_{in}}. \quad (14)$$

In this physical LLC model, Z_s , Z_m , Z_p and Z_{in} are impedances in ohms; $Z_m = j\omega L_m$ is the magnetizing branch impedance. $H(\omega)$ is the dimensionless complex transfer of this physical FHA network, not the normalized family screening transfer H_T . When switching frequency is used as the argument, $H(f_s)$ means $H(\omega)$ evaluated at $\omega = 2\pi f_s$.

For a half-bridge square-wave excitation, the first harmonic RMS voltage is

$$V_{1,rms} = \frac{\sqrt{2}}{\pi} V_{in}. \quad (15)$$

The resonant, load, and magnetizing currents are:

$$I_r = \frac{V_{1,rms}}{Z_{in}}, \quad I_{load} = \frac{V_{1,rms} H}{R_{ac}}, \quad I_m = \frac{V_{1,rms} H}{Z_m}. \quad (16)$$

The voltage in the first relation is the first harmonic RMS bridge excitation. The three current symbols are the complex RMS phasors of the resonant tank current, the current through the reflected load, and the magnetizing current, respectively; their vertical-bar values are RMS magnitudes.

The required tank gain at each input voltage is:

$$|H|_{req} = \frac{2nV_o}{V_{in}}. \quad (17)$$

All roots of $|H(f_s)| = |H|_{req}$ inside the allowed frequency range are identified. Roots with an input-impedance phase below 2 degrees are rejected. When multiple roots remain, a secondary cost selects the point with the best combination of headroom, circulation, current, capacitor stress, sensitivity, and proximity to resonance.

4.3. Parameterization in the (Q, m) Plane

At full load,

$$Q_{full} = \frac{Z_r}{R_{ac,full}}, \quad Z_r = \sqrt{\frac{L_r}{C_r}}, \quad m = \frac{L_m}{L_r}. \quad (18)$$

Given Q_{full} , m , and target $\omega_r = 2\pi f_r$, the continuous components follow directly:

$$Z_r = Q_{full} R_{ac,full},$$

$$L_r = \frac{Z_r}{\omega_r}, \quad C_r = \frac{1}{\omega_r Z_r}, \quad L_m = mL_r. \quad (19)$$

This parameterization is rational because the search variables have immediate physical meanings. Q_{full} sets the tank impedance relative to the reflected load, m controls magnetizing participation and light load commutation current, and f_r establishes the resonant time scale. Component values are recovered only after a candidate passes the multidimensional constraint screen.

In Equation (19), ω_r is the target angular resonance, $2\pi f_r^*$. After rounding the components, f_r is recomputed from the selected L_r and C_r ; the resulting actual value is reported in Equation (42).

4.4. Control Headroom and Gain Sensitivity

The physical frequency headroom is normalized around the actual resonant frequency:

$$H_f = \text{clip} \left[\min \left(\frac{f_s - f_{\min}}{f_r - f_{\min}}, \frac{f_{\max} - f_s}{f_{\max} - f_r} \right), 0, 1 \right]. \quad (20)$$

A point at f_r has $H_f = 1$, whereas a point at either control boundary has $H_f = 0$. The normalized frequency sensitivity is:

$$S_F = \left| \frac{f_s}{|H|} \frac{d|H|}{df_s} \right|. \quad (21)$$

The headroom condition is $H_f \geq 0.25$, and the sensitivity condition is $S_F \leq 3.5$. These two constraints prevent the design from satisfying gain only through a narrow or steep portion of the control surface.

H_f is the dimensionless physical frequency headroom within $[f_{\min}, f_{\max}]$, using one common frequency unit. S_F is the dimensionless magnitude of relative gain sensitivity to switching frequency, evaluated with the component values and corner load held fixed. These quantities differ from the screening headroom H_c and absolute normalized-gain slope S_G .

4.5. Commutation-Charge Margin

The phase-shift study of Grigorova and Vuchev relates commutation to both inductance and frequency ratios [15]. Jiao et al. additionally resolve parasitic-capacitance dynamics and a bounded dead time window [21]. The scalar charge margin below therefore expresses a necessary design-screening reserve within the adopted approximation, not a proof that arbitrarily increasing dead time preserves ZVS.

Let

$$\phi = \max \{ \angle Z_{\text{in}}, 0 \}. \quad (22)$$

The non-negative angle is expressed in radians in the sine function. Its degree-valued counterpart is obtained by multiplying by $180/\pi$ and is used only in the inductive-angle margin, thereby removing any radians/degrees ambiguity.

The screening-level peak commutation current is approximated from the inductive component of the FHA tank current:

$$I_{\text{com,pk}} = \sqrt{2} |I_r| \sin \phi. \quad (23)$$

The commutation-charge margin is:

$$M_Q = \frac{I_{\text{com,pk}} t_d}{k_Q Q_{\text{oss},\Sigma}}, \quad (24)$$

where $k_Q = 1.20$ is the charge safety factor. The retained design must satisfy $M_Q \geq 1$ at every corner. The required scheduled dead time is estimated as

$$t_{d,\text{req}} = \frac{k_Q Q_{\text{oss},\Sigma}}{I_{\text{com,pk}}} + t_{\text{guard}}. \quad (25)$$

$I_{\text{com,pk}}$ is the FHA peak commutation-current estimate in amperes, M_Q is the dimensionless charge margin, and $t_{d,\text{req}}$ is the estimated charge-transfer time plus t_{guard} , in seconds. The subscripts com, pk, req and fix denote commutation, peak, required and fixed-command quantities. Q denotes dimensionless quality factor; $Q_{\text{oss},\Sigma}$ is aggregate electrical charge in coulombs.

The original feasibility criterion requires the applied dead time to exceed the charge-transfer estimate $k_Q Q_{\text{oss},\Sigma} / I_{\text{com,pk}}$. The 25 ns allowance is added when forming scheduled commands; it is not implicitly subtracted in the original MQ definition. A separate stricter sensitivity test requires this allowance to remain after timing perturbations. These two acceptance definitions are reported independently.

Equations (23)–(25) are FHA screening relations. They do not establish either the minimum and maximum safe dead time window of a device-level converter or the time evolution of nonlinear output-capacitance charge [21]. A favorable input phase and sufficient estimated charge must be followed by a turn-on-voltage check in a switched model or hardware; rectifier ZCS cannot be inferred from the same scalar criterion.

4.6. Current, Voltage, Flux, and Circulation Measures

Peak resonant current is:

$$I_{r,\text{pk}} = \sqrt{2} |I_r|. \quad (26)$$

The resonant capacitor and resonant inductor peak voltages are:

$$V_{\text{Cr,pk}} = \sqrt{2} \left| \frac{I_r}{j\omega C_r} \right|, \quad V_{\text{Lr,pk}} = \sqrt{2} |j\omega L_r I_r|. \quad (27)$$

A preliminary half-bridge transformer flux estimate is:

$$B_{\text{pk}} = \frac{V_{\text{in}}}{8N_p A_e f_s}. \quad (28)$$

The circulation index is:

$$K_{\text{tank}}^{\text{LLC}} = \frac{|I_r|}{|I_{\text{load}}|}. \quad (29)$$

A conduction-loss proxy is:

$$P_{\text{cond}}^{\text{proxy}} = |I_r|^2 R_{\text{path}}. \quad (30)$$

The aggregate ranking proxy used after feasibility is established is:

$$P_{\Sigma}^{\text{proxy}} = \overline{P_{\text{cond}}^{\text{proxy}}} + 0.15 \overline{|I_m|^2} + 0.002 \overline{f_s [\text{kHz}]}. \quad (31)$$

The path resistance is the equivalent primary path resistance and the overbar denotes the arithmetic mean across the nine nominal corners. In Equation (31), 0.15 has units of ohms and 0.002 has units of W/kHz. The resulting watts are the units of an aggregate ranking proxy, not calibrated total converter loss. The physical circulation ratio in Equation (29) differs from the normalized family screening burden in Equation (3).

The proxy coefficients distinguish candidate designs only after feasibility is established. A lower proxy is not reported as higher measured efficiency; magnetic, semiconductor-transition and thermal losses remain uncalibrated.

4.7. Normalized Margin and Feasible Region

Seven normalized corner margins are defined:

$$\begin{aligned} M_1 &= M_Q, & M_2 &= \frac{H_f}{0.25}, & M_3 &= \frac{\phi_{\text{deg}}}{5^\circ}, \\ M_4 &= \frac{13}{I_{r,\text{pk}}}, & M_5 &= \frac{650}{V_{\text{Cr,pk}}}, & M_6 &= \frac{0.18}{B_{\text{pk}}}, \\ M_7 &= \frac{3.5}{S_F}. \end{aligned} \quad (32)$$

The seven margins represent, in order, commutation charge, control headroom, inductive angle, peak current, resonant capacitor voltage, flux density, and gain sensitivity. A margin not smaller than unity satisfies its constraint, while unity is the corresponding feasibility boundary. The third margin uses the degree-valued phase defined above.

The numerical limits 13, 650 and 0.18 in Equation (32) stand for 13 A, 650 V and 0.18 T, respectively, as declared in Table 3. The corresponding denominator values use the same units; 650 V applies to the FHA AC-voltage amplitude. The headroom and gain-sensitivity limits are dimensionless, and the angle limit is 5° . Each ratio is therefore dimensionless.

For design vector $x = (Q_{\text{full}}, m)$ and corner $c = (V_{\text{in}}, \ell)$, the robust nominal margin is:

$$\rho(x) = \min_{c \in \mathcal{C}} \min_{j=1,\dots,7} M_j(x, c). \quad (33)$$

The required operating corner set contains every combination of 360, 400, and 420 V with load fractions of 0.25, 0.50, and 1.00. The robust reserve is therefore the smallest of all seven normalized margins over every required corner.

The feasible region is:

$$\Omega = \{x : \rho(x) \geq 1\}. \quad (34)$$

The feasible-set symbol Ω is deliberately distinguished from the scalar normalized frequency F .

The primary synthesis is max-min:

$$x_\rho = \operatorname{argmax}_{x \in \Omega} \rho(x). \quad (35)$$

The vector x_ρ denotes a design attaining the largest minimum reserve ρ within Ω ; it is not the scalar reserve itself. In Equation (33), $j = 1, \dots, 7$ is a constraint index, distinct from the imaginary unit j used in impedance expressions. The implemented finite grid selection and its lack of a certified global optimum are stated in Section 5.2.

The loss proxy is used as a tie-breaker rather than being mixed with feasibility from the beginning. This ordering avoids selecting a low-loss point that is unacceptably close to one physical boundary.

5. Reproducible Numerical Procedure

5.1. Family Screening

The original D0 result is preserved in Supplementary Material S1. The revision evaluates the nested D0–D3 node sets declared in Section 3.4 with exact native transfer-magnitude roots. The domain summary records every bound, node count and selected

boundary flag. Each corner retains the minimum-cost admissible root; candidates are ranked by coverage, minimum headroom, mean cost, maximum circulation and maximum voltage burden. Local refinement is applied after the largest-domain search. These records make changes caused by domain expansion distinct from a change in numerical root policy.

5.2. LLC Feasible Grid and Standard-Value Projection

The physical LLC grid uses are described below:

$$Q_{\text{full}} \in [0.22, 0.65], \quad m \in [3.2, 9.0]. \quad (36)$$

For each sampled point, components are reconstructed from Equation (19), and all nine corners are solved within 75–180 kHz. A point is retained only when every corner has an inductive gain root. The minimum reserve in Equation (33) then ranks the retained points. The reported physical synthesis point is the best point of the stated finite grid, not a certified continuous global optimum.

The selected rounded targets are 20 μH , 88 nF and 106 μH . This triplet is a declared engineering selection near the high-margin ridge, not the result of an automatic catalog search. Its gain roots, currents, voltage amplitudes and margins are recalculated from the rounded targets. Winding construction and component availability remain implementation tasks.

5.3. Bounded Tolerance Study

The calibration population uses 20,000 realizations with seed 20260825. Each primitive deviation is drawn from a zero-mean normal distribution and clipped at the listed bounds. This is a clipped-normal model, with boundary point masses; it is not a continuously truncated-normal distribution. The perturbations are independent as a coverage convention, not a calibrated manufacturing law. The same sampling convention and matched timing perturbations are used for a separate 20,000-realization test population with seed 20260913. Table 4 summarizes the perturbed parameters, the standard deviations of the underlying normal draws, and the hard clipping bounds used for both the calibration and independent test populations.

Table 4. Bounded tolerance model used in the 20,000-run study.

Parameter	Standard Deviation	Hard Bound
L_r	2%	$\pm 5\%$
C_r	2%	$\pm 5\%$
L_m	3.5%	$\pm 8\%$
turns ratio n	0.4%	$\pm 1\%$
$Q_{\text{oss},\Sigma}$	8%	$\pm 20\%$
fixed dead time	5 ns	± 12 ns
primary path resistance	5%	$\pm 12\%$

For each realization and each corner, gain is solved on a 421-point frequency grid. The minimum normalized margin, maximum gain error, minimum and maximum operating frequencies, peak current, capacitor voltage, required dead time, loss proxy, worst corner, and active constraint are stored. Fixed dead time feasibility requires:

$$\rho_{MC} \geq 1, \max_{c \in \mathcal{C}} |\Delta G(c)| \leq 0.003. \quad (37)$$

For a fixed tolerance realization, $\Delta G(c) = |H(f_s(c))| - |H|_{\text{req}}(c)$ is the signed physical LLC gain-magnitude deviation at corner c . The maximum in Equation (37) is taken over the nine required corners $\mathcal{C}$; the archived maximum-gain-error field stores this maximum abso-

lute deviation. It is not the family screening gain $G_{\mathcal{T}}$. N_{feasible} counts realizations passing all stated corner conditions, N_{MC} is the evaluated population size, and $Y = 100N_{\text{feasible}}/N_{\text{MC}}$ is reported in percent.

One realization passes only when all seven declared margins at all nine corners and the maximum gain-error requirement are satisfied. The reported fraction is empirical model-based joint feasibility, not manufacturing yield or a probability of experimentally successful ZVS. Calibration and test fractions are identified separately.

The Supplementary Materials contains run-level data, aggregate tables, figure-generation code, and the complete deterministic configuration.

5.4. Adaptive Dead Time Schedule

The calibration population determines one continuous-valued command for each input-load corner:

$$t_d^*(c) = \text{Quant}_{0.995}\{t_{d,\text{req}}(c)\} + 5 \text{ ns}. \quad (38)$$

For a fixed corner c , $\text{Quant}_{0.995}$ in Equation (38) is the empirical 99.5th percentile over the calibration realizations of $t_{d,\text{req}}(c)$, not over the corners. The superscript $*$ identifies the selected and subsequently locked command, not an experimentally optimal or loss-minimizing setting. Adding 5 ns is an allowance; the separate implementable grid scenario rounds the locked command upward to a multiple of 5 ns.

The nine commands are locked before evaluation on the independent test population; no test observation is used to refit them. The same clipped timing deviation, including its sign, is applied to fixed and scheduled commands for each realization. Results are reported for the original charge-only criterion and, separately, for retention of the additional 25 ns guard. No switching-loss optimum or closed-loop adaptive controller is demonstrated.

The labels fixed, locked and test refer to the constant-command case, the frozen schedule and the independent test population. Y_{fixed} in Equation (43) is the fixed-command calibration fraction, whereas $Y_{\text{locked,test}}$ in Equation (44) is the locked-schedule independent-test fraction. The extension in Equation (45) denotes a future implementation map, not an additional controller demonstrated here.

6. Results

6.1. Topology Screening

Table 5 reports the expanded-domain result after local refinement, including K_{I} as a separate quantity from K_{circ} . The original D0 result remains in Supplementary Material S2. The comparison holds the frequency band and admissibility criteria fixed; it changes the permitted parameter domain rather than quietly changing the specification.

Table 5. Expanded and locally refined normalized screening results (D3). All values are reduced-model screening quantities.

Family	Q_{full}	α or m	Covered	Min. H_c	Max. K_{I}	Max. K_{circ}	Max. K_{V}
SRC	4.0347	—	3/9	0.6576	0.9524	0.9524	3.9980
PLRC	0.8733	—	9/9	0.2672	1.6972	2.3840	2.2333
LCC	1.6553	1.7037	9/9	0.0523	1.8570	2.3796	3.9998
LLC	0.9840	0.2983	9/9	0.9609	3.9987	5.5448	3.9933

Domain expansion changes a substantive conclusion: PLRC reaches all nine corners, so its previous 8/9 coverage was a search-bound result, not a structural impossibility. SRC increases from 2/9 to 3/9 but still cannot meet the complete gain set under the common inductive constraints. LLC retains the greatest minimum frequency headroom

among complete-coverage candidates under the stated lexicographic priority; however, its expanded winner approaches both current and voltage burden limits. PLRC has lower circulation and voltage burden than that winner. LLC is therefore selected conditionally by the declared priority, not because it dominates every metric.

Figure 4 connects each original-domain result to its expanded, locally refined result. This makes changes in corner coverage and the transfer of burden explicit. The small-m LLC screening winner is not substituted into the physical design passport.

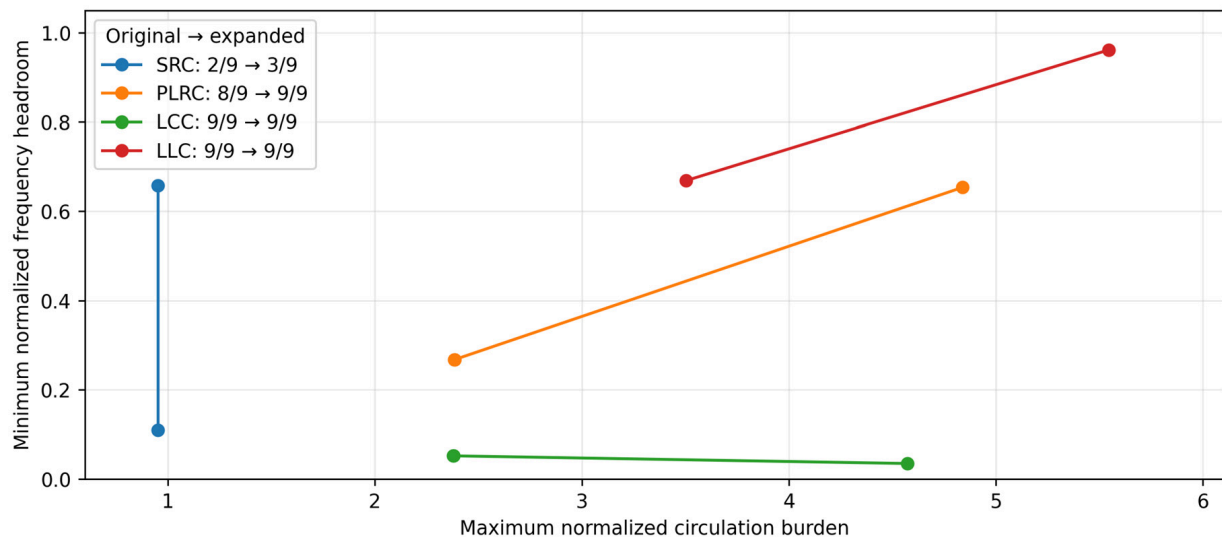


Figure 4. Domain-aware family screening: each line joins the original D0 point to the expanded and locally refined point. Legend entries give original → expanded corner coverage. The frequency band and admissibility thresholds are fixed; this is not a hardware ranking.

Family-level screening and physical synthesis are distinct decisions. The expanded LLC point has a much smaller magnetizing ratio and a larger normalized circulation burden than the selected physical design. The physical-stage search independently applies absolute current, voltage, flux and charge constraints and its declared Q_{full-m} domain. The retained 20 μH /88 nF/106 μH triplet is not presented as the physical realization of the normalized family winner.

6.2. LLC Gain and Feasible Region

After LLC is retained, the rounded physical design is mapped onto its gain surface to verify where each line-load corner is regulated relative to resonance and the inductive operating boundary. Figure 5 shows the nine operating points and their movement below, near, or above resonance as the input voltage changes.

The physical Q_{full-m} grid in Figure 6 retains its original benchmark role. Its best sampled nominal max–min point is:

$$Q_{full} = 0.480, \quad m = 5.10, \quad (39)$$

with the corresponding continuous-valued component targets:

$$L_r = 20.641 \mu\text{H}, \quad C_r = 85.221 \text{ nF}, \quad L_m = 105.269 \mu\text{H}. \quad (40)$$

The sampled map shows a ridge of high worst-corner margin rather than establishing a unique global continuous optimum. The selected rounded point is re-evaluated rather than assigned the margin of a neighboring unrounded point.

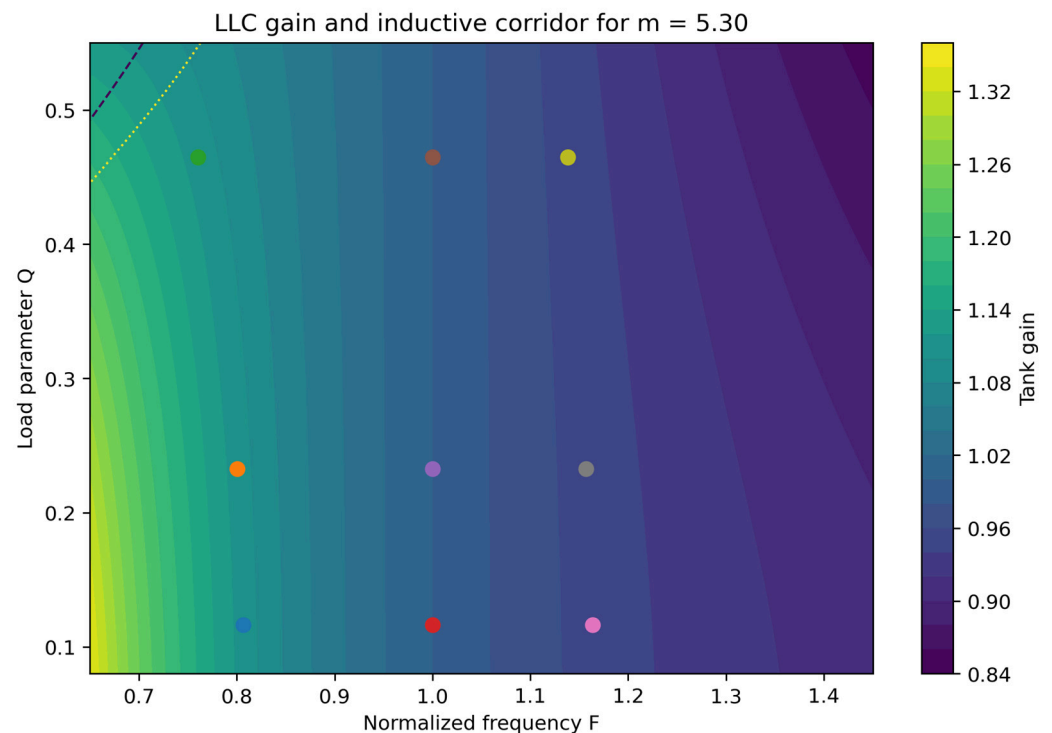


Figure 5. LLC gain and inductive operating corridor for $m = 5.30$. The colored circular markers denote the nine (V_{in}, ℓ) input-load operating corners of the rounded design; marker colors are used only to distinguish the individual corners and do not encode an additional variable. The dashed line denotes the zero-phase boundary ($\phi = 0$) separating capacitive and inductive input impedance, whereas the dotted line denotes the adopted minimum inductive-angle boundary ($\phi = 5^\circ$). The background color map represents the FHA tank-gain magnitude.

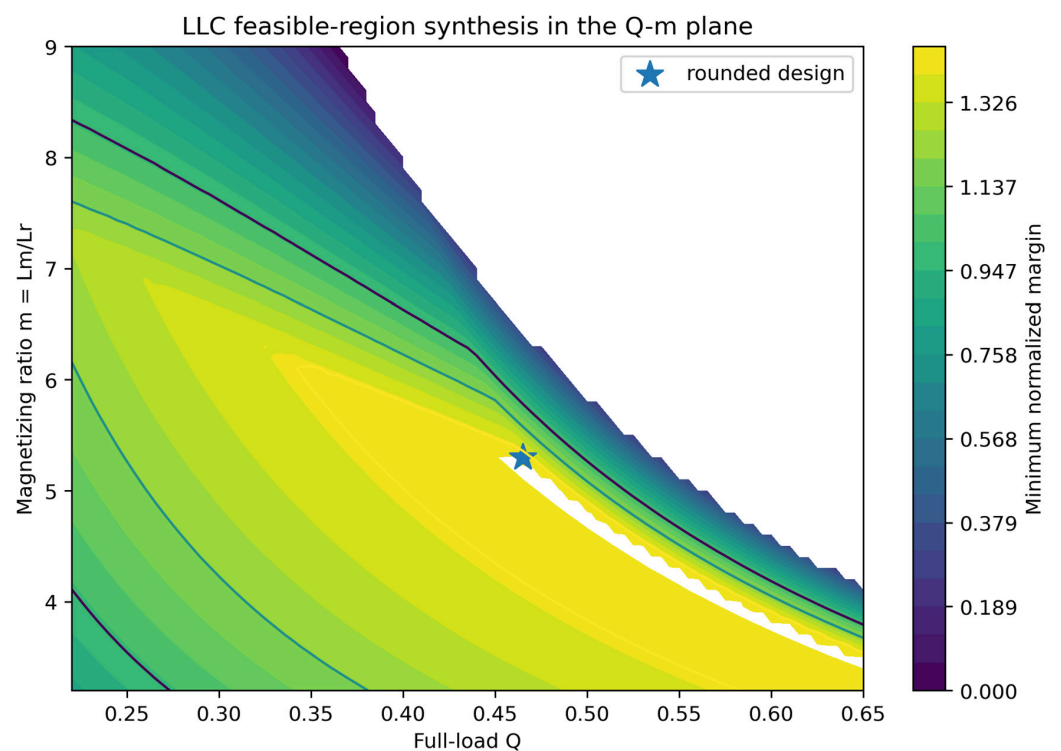


Figure 6. LLC feasible-region synthesis in the (Q, m) plane. Color represents the minimum normalized margin across all nine corners. The star marks the selected rounded design.

6.3. Rounded Targets and a Prespecified FHA Comparator

The retained engineering component targets are:

$$L_r = 20.0 \mu\text{H}, \quad C_r = 88.0 \text{ nF}, \quad L_m = 106 \mu\text{H}. \quad (41)$$

They give:

$$f_r = 119.968 \text{ kHz}, \quad Z_r = 15.076 \Omega, \quad Q_{\text{full}} = 0.46497, \quad m = 5.30. \quad (42)$$

Table 6 compares the best sampled physical synthesis point, the retained rounded targets and a prespecified conventional FHA hand-calculated comparator. For the comparator, $Q_{\text{full}} = 0.40$ and $m = 5.00$ are fixed before evaluation, with the same rated specification and 120 kHz target. The derived 17.201 μH /102.265 nF/86.004 μH values are rounded to 17 μH /102 nF/86 μH at a declared 1 μH /1 nF resolution. The comparator is not adjusted to lose and is not claimed to reproduce a particular published optimization algorithm.

Table 6. Nominal comparison and independent sampled feasibility. Proxies are not measured or calibrated total losses.

Quantity	Best Sampled RD Point	Rounded RD	Rounded FHA Hand-Calculated Design
Q_{full}	0.480	0.46497	0.39818
m	5.10	5.30	5.0588
L_r	20.641 μH	20.0 μH	17 μH
C_r	85.221 nF	88.0 nF	102 nF
L_m	105.269 μH	106 μH	86 μH
f_r	120.000 kHz	119.968 kHz	120.864 kHz
Minimum normalized margin	1.461	1.441	1.4005
Minimum control headroom	0.377	0.360	0.4416
Worst charge margin	1.461	1.469	2.6364
Loss proxy	3.213 W	3.199 W	3.9013 W
Fixed 250 ns; calibration pass fraction	Not re-evaluated here	98.850% (19,770/20,000)	100% (20,000/20,000)
Fixed 250 ns; independent test pass fraction	Not re-evaluated here	98.860% (19,772/20,000)	100% (20,000/20,000)

Relative to the rounded hand-calculated comparator, the retained RD targets increase the minimum nominal reserve from 1.4005 to 1.4407 and reduce the ranking proxy from 3.9013 W to 3.1993 W. The comparator nevertheless passes all 20,000 fixed-timing calibration and all 20,000 independent test realizations, whereas the RD fixed-timing fractions are 98.850% and 98.860%. Neither candidate dominates every criterion. A nominal max–min design is not automatically a yield-optimal design, and a 100% sampled pass fraction is not a worst-case certificate.

Once standard components are fixed, the regulator must still reach every required operating point within the allowed switching frequency band. Figure 7 presents the resulting frequency schedule and shows the expected shift below resonance at 360 V and above resonance at 420 V.

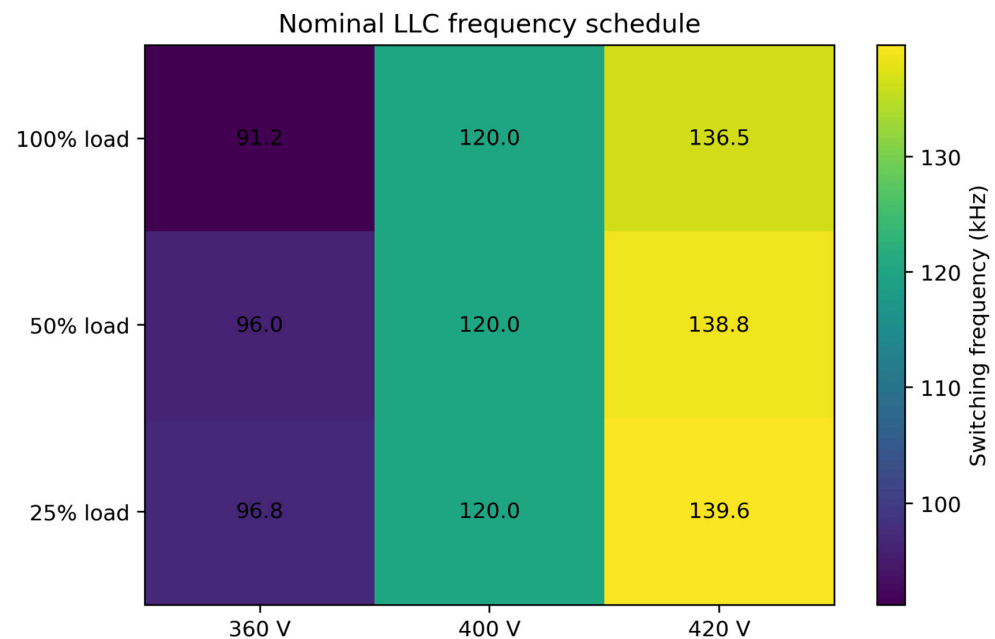


Figure 7. Nominal switching frequency schedule for the selected standard-value LLC design.

6.4. Nominal Corner Margins

The performance of the rounded LLC design must be checked at every combination of input voltage and load, rather than only at the nominal point. Table 7 reports the operating frequency, phase, stresses, commutation margin, control headroom, and required dead time for all nine corners.

Table 7. Nominal operating corners of the rounded LLC design.

V_{in}	Load	f_s (kHz)	Phase (deg)	$I_{r,pk}$ (A)	$V_{Cr,pk}$ (V)	B_{pk} (T)	M_Q	H_f	$t_{d,req}$ (ns)
360	25%	96.8	60.4	4.41	82.5	0.116	3.20	0.484	103.2
360	50%	96.0	38.7	5.59	105.4	0.117	2.92	0.467	110.7
360	100%	91.2	11.4	8.90	176.6	0.123	1.47	0.360	195.2
400	25%	120.0	58.4	3.74	56.4	0.104	2.66	1.000	119.1
400	50%	120.0	39.1	5.06	76.2	0.104	2.66	1.000	119.1
400	100%	120.0	22.1	8.48	127.8	0.104	2.66	1.000	119.1
420	25%	139.6	56.3	3.37	43.6	0.094	2.34	0.673	132.0
420	50%	138.8	38.8	4.80	62.5	0.095	2.50	0.686	124.9
420	100%	136.5	26.2	8.34	110.4	0.096	3.07	0.724	106.4

The adequacy of the rounded design is evaluated through normalized corner margins, so that different physical constraints can be compared against the same feasibility threshold. Figure 8 shows which constraint is closest to becoming active at each operating point and confirms that all nominal margins remain above unity.

The final nominal design passport is:

- all nine gain-load corners solved inside 75–180 kHz;
- minimum normalized margin: 1.441;
- minimum frequency headroom: 0.360;
- worst fixed-dead time charge margin: 1.469;
- maximum primary resonant peak current: 8.903 A;
- maximum FHA AC resonant capacitor amplitude: 176.562 V (not the full physical voltage rating);
- maximum preliminary flux density: 0.1234 T;

- maximum normalized gain sensitivity: 0.629;
- mean circulation index: 1.453;
- maximum nominal required dead time: 195.2 ns.

Nominal corner margins of the rounded LLC design

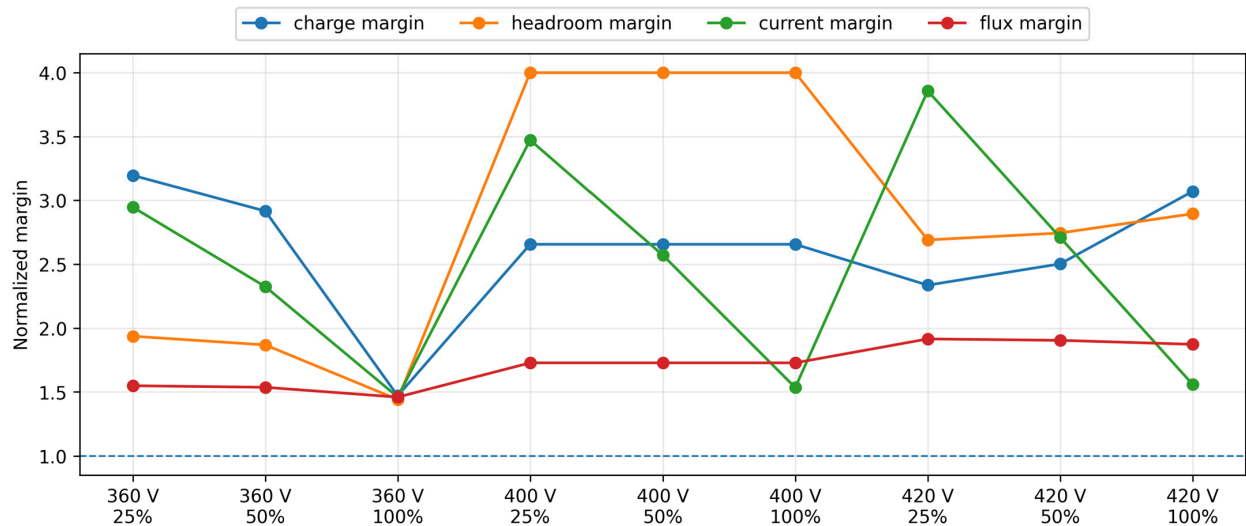


Figure 8. Nominal normalized margin profiles for the rounded LLC design. The horizontal line at one is the feasibility boundary.

6.5. Monte Carlo Feasibility

The bounded 20,000-run study gives a fixed-250 ns feasibility yield of

$$Y_{\text{fixed}} = 98.85\%. \quad (43)$$

Figure 9 retains the original calibration-population distribution of the minimum normalized margin. The independent test population is assessed separately and is not used to fit the timing schedule.

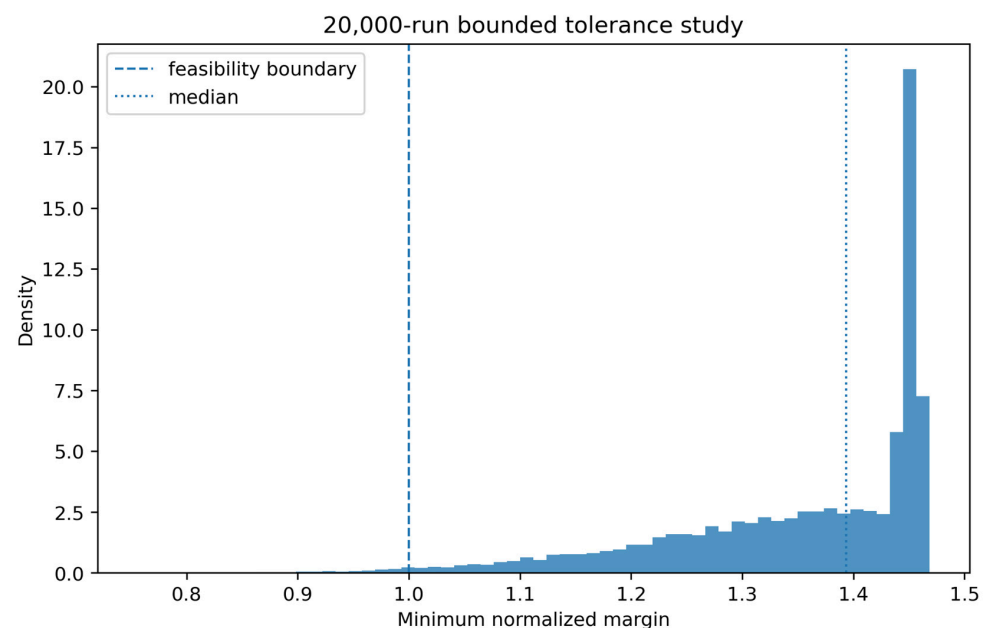


Figure 9. Distribution of minimum normalized margin in the 20,000-run bounded tolerance study.

The histogram in Figure 9 describes the global distribution of the minimum margin, whereas a fuller assessment requires the corresponding distributions of frequency, gain error, current, capacitor voltage, and required dead time. These summary statistics are compiled in Table 8.

Table 8. Selected Monte Carlo result distributions.

Metric	Minimum	P01	P05	Median	P95	P99	Maximum
Minimum normalized margin	0.756	0.992	1.110	1.394	1.459	1.462	1.469
Maximum gain error	0.00010	0.00023	0.00030	0.00061	0.00087	0.00092	0.00101
Minimum frequency (kHz)	85.5	87.5	88.5	91.3	94.0	95.0	97.3
Maximum frequency (kHz)	128.5	132.8	134.8	139.8	145.3	147.8	153.5
Maximum $I_{r,pk}$ (A)	8.780	8.813	8.834	8.903	8.989	9.020	9.082
Maximum $V_{Cr,pk}$ (V)	166.5	170.2	172.0	176.6	181.7	184.0	189.6
Maximum required dead time (ns)	125.9	146.8	158.4	194.9	248.3	276.6	357.4

The gain, current, capacitor voltage, and control-frequency distributions remain compact. The wide upper tail of required dead time explains most fixed-schedule failures. At the 360 V/full-load corner, the 95th and 99.5th percentile required dead times are 248.3 ns and 287.3 ns, respectively. At eight other corners, the 99.5th percentile is below 158 ns.

The archived minimum-margin record selects 360 V/full load throughout this population. That label identifies the minimum of the declared seven-margin screen; it does not establish that every physical failure mechanism or thermal stress is worst at the same corner.

6.6. Sensitivity and Active Constraints

Because the minimum margin alone does not identify the parameters responsible for robustness loss, a sensitivity ranking is required. Figure 10 reports the Spearman correlations between each sampled parameter and the minimum robust margin, thereby identifying the variables that deserve the most detailed device and magnetic validation.

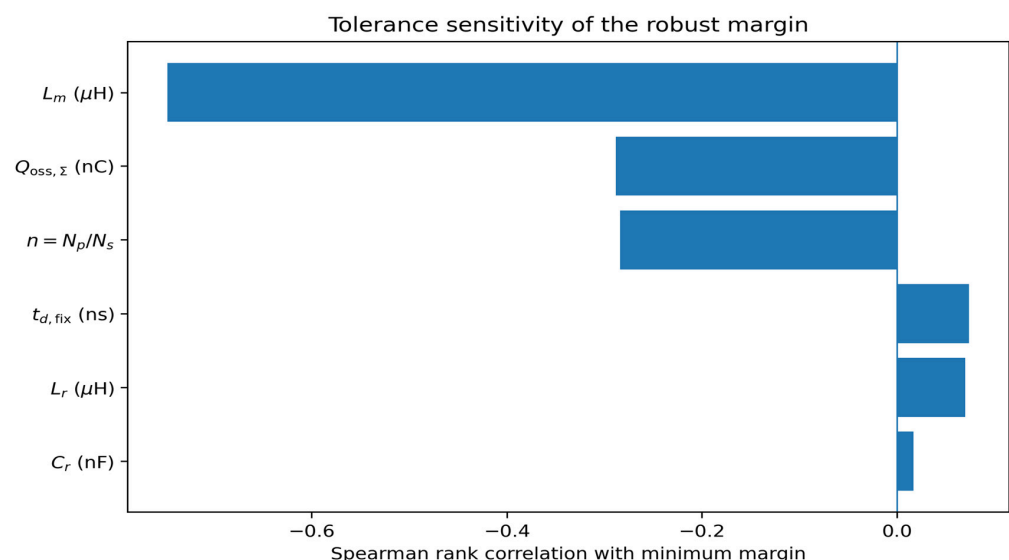


Figure 10. Spearman sensitivity of the minimum robust margin to the sampled parameters.

Magnetizing inductance has the strongest rank association with the minimum margin (−0.7474). Total output charge and effective transformer ratio follow (−0.2885 and −0.2840). L_r and C_r have weaker direct associations with the overall minimum margin in this bounded neighborhood, while strongly affecting the required switching fre-

quency. These are correlations within the specified clipped-normal screen, not universal causal rankings.

Active-constraint counts are distributed mainly among commutation charge, control headroom, and peak current. Flux becomes active in a small subset; capacitor voltage, phase, and sensitivity do not become the minimum constraint in the sampled domain. The result should not be generalized outside the stated envelope. It indicates which variables deserve detailed switched and magnetic validation for this design.

6.7. Locked Schedule, Independent Test and Timer Quantization

Table 9 preserves the continuous command fitted only to the original calibration population and adds a separate 5 ns ceiling-quantized realization. The same timing error convention is applied to fixed and scheduled operation in Table 10.

Table 9. Locked corner-dependent commands. The quantized column is a separate implementation-grid scenario.

V_{in} (V)	Load	Fixed (ns)	Locked (ns)	5 ns Ceiling (ns)	Ceiling Change
360	25%	250	125.3	130	−48.0%
360	50%	250	135.1	140	−44.0%
360	100%	250	292.3	295	+18.0%
400	25%	250	145.4	150	−40.0%
400	50%	250	145.2	150	−40.0%
400	100%	250	145.0	150	−40.0%
420	25%	250	162.2	165	−34.0%
420	50%	250	152.0	155	−38.0%
420	100%	250	128.2	130	−48.0%

Table 10. Paired timing evaluation: empirical joint nine-corner pass fractions under the stated FHA model.

Acceptance Test	Command	Calibration %	Independent Test %	Mean ns
charge only	Fixed	98.850	98.860	250.00
guard retained	Fixed	95.200	95.455	250.00
charge only	Locked continuous	99.950	99.925	158.95
guard retained	Locked continuous	99.150	99.105	158.95
charge only	Locked 5 ns ceiling	99.955	99.935	162.78
guard retained	Locked 5 ns ceiling	99.460	99.465	162.78

The continuous command averages 158.95 ns, a 36.42% reduction from 250 ns. With matched timing perturbations, the independently tested joint charge-only feasibility of this locked schedule is:

$$Y_{\text{locked,test}} = 99.925\% \quad (44)$$

The calibration value with the same timing perturbations is 99.950%. The previously reported 99.955% used the calibration population and omitted timing jitter for the scheduled case; it is retained only in the historical audit. The 5 ns ceiling scenario averages 162.78 ns (34.89% below 250 ns) and reaches 99.935% independent charge-only feasibility. The stricter guard-retention results are lower and are reported as a different acceptance test, not a silent redefinition. Figure 11 visualizes the continuous-valued locked dead time commands across the nine input–load corners. The map highlights the longer command at 360 V and full load and is distinct from the 5 ns ceiling-quantized settings reported in Table 9.

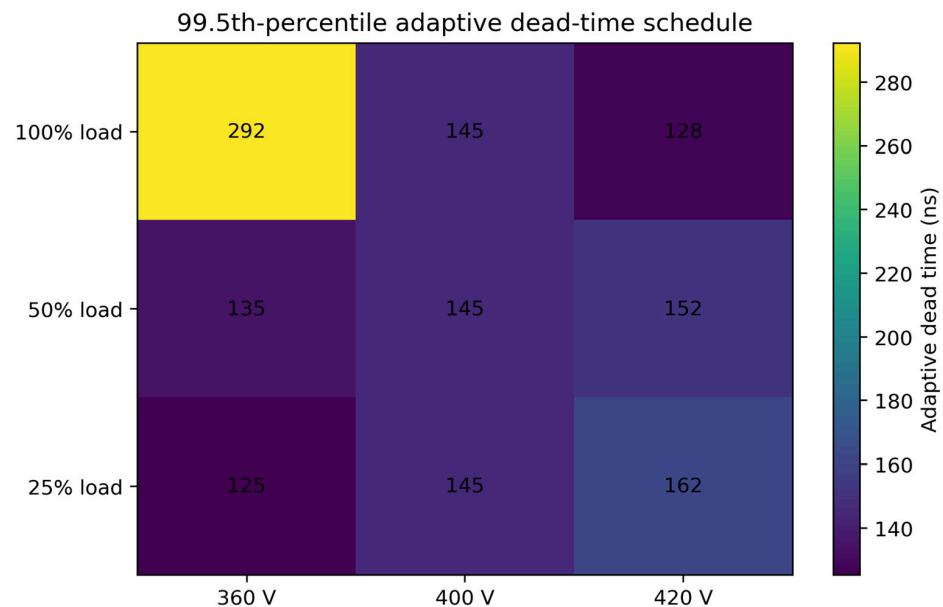


Figure 11. Continuous-valued locked schedule fitted to the calibration population. It is not the 5 ns-quantized column in Table 9 and does not represent an online adaptive-controller experiment.

Joint feasibility is checked across all nine corners for each realization. Equal timing perturbations are imposed on the fixed and scheduled commands; this paired comparison isolates the schedule from unequal uncertainty treatment. No upper safe dead time boundary, reverse-conduction loss or device-level ZVS rate is established by these fractions.

6.8. Matched Parasitic Switched-Circuit Assessment

To test the two rounded tanks beyond FHA, a new six-state time-domain circuit model is applied with identical parasitic assumptions. It resolves the physical resonant capacitor voltage, tank and magnetizing currents, transformer-port voltage, output voltage and half-bridge node. Both channels have finite conductance, distinct body diode paths and explicit dead time. Primary winding capacitance and reflected rectifier-junction capacitance are represented as a differential shunt; the full bridge uses symmetric piecewise-linear diode-pair paths. The generic assumptions in Table 11 are not measurements or manufacturer-macromodel parameters. They allow a controlled comparison, not a claim that the actual implementation will have these losses.

Table 11. Common generic parasitic scenario used for both frozen tank designs. These values supplement, rather than replace, the FHA benchmark.

Element	Value	Interpretation
Additional series-referred leakage	0.5 μ H	Added to each tank's stated L_r
Tank/primary series resistance; channel resistance	70 m Ω ; 40 m Ω	Dissipative lumped paths
Secondary winding; rectifier diode	10 m Ω ; 0.70 V + 5 m $\Omega \times i$	Each conducting pair contains two diodes
Body diode	0.70 V + 40 m $\Omega \times i$	Separate from bidirectional channel
Differential winding; rectifier junction capacitance	100 pF; 200 pF/diode	Junction capacitance is lumped by bridge symmetry
Output capacitor and ESR	470 μ F; 10 m Ω	Passive load: $48^2/(1000\ell) \Omega$
Bridge-node stray capacitance	20 pF	Additional to both C_{oss} branches

Table 11. Cont.

Element	Value	Interpretation
Linear/nonlinear output-charge alternatives	125 nC/device at 400 V	312.5 pF or declared nonlinear $Q(v)$; Supplementary Material S3.2
Dead time; channel-command edge	250 ns; 20 ns	Command ramps are not a gate-loop model

In the diode voltage-drop expressions in Table 11, i is the forward conduction current through the particular diode, in amperes; it is not automatically i_r or a primary-referred current. C_{oss} is the device output capacitance in farads. $Q(v)$ is the per-device output charge in coulombs as a function of that device's drain-source voltage v in volts, with $C_{oss}(v) = dQ(v)/dv$ in the declared model. This $Q(v)$ is distinct from the dimensionless quality factor Q . The complete charge law is specified in Section S3.2 of Supplementary Material S3.

The nonlinear output-charge curve and its charge-equivalent linear alternative have the same 250 nC aggregate requirement at 400 V. Dead time behavior nevertheless depends on current and the entire charge trajectory, not solely an inductive input angle [27]. The circuit equations and their implementation are provided in Supplementary Material S3. Both alternatives are evaluated at the original FHA commands (36 cases); the nonlinear model is then solved at a separate steady-state frequency root for 48 V in every design/corner combination (18 cases). This frequency correction is a numerical regulation calculation, not resonance tracking or a validated dynamic controller.

Charge-form integration by the implicit second-order backward differentiation formula (BDF2) uses a maximum 2 ns step and 640 periods. Period-to-period and 32-period state checks establish settling. All 18 equal-output cases are repeated at 1 ns; six are also repeated at 0.5 ns and cross-checked with a separately implemented differential formulation integrated by SciPy Radau. The maximum step-refinement changes are 0.0805% in peak current and 0.0223% in modeled dissipation; the largest main-campaign energy-balance residual is 0.00413% of output power. Against the 0.5 ns traces, the separate integrator differs by at most 0.0060% in peak current and 0.426 V in switch-node voltage. These are numerical consistency checks, not independent experimental validation.

6.8.1. FHA Error and Equal-Output Comparison

Figure 12 reports the open-loop output error when the original FHA frequencies are transferred unchanged. The RD error spans -5.58% to $+0.04\%$; the comparator spans -5.61% to -2.09% . RD peak-current error spans -8.90% to $+21.06\%$ and resonant capacitor AC-amplitude error spans -6.41% to $+10.54\%$. Thus a small output error can coexist with a substantial stress error. These nine-point results establish a tested comparison, not a universal FHA-valid frequency band. In particular, the most demanding RD low-line/full-load point should not be closed using its FHA peak-current estimate alone.

Table 12 compares the independently corrected frequency roots at equal 48 V output. All roots remain within 75–180 kHz and peak current remains below the declared 13 A screen in this scenario. The RD uniformly averaged modeled dissipation is 25.457 W versus 25.824 W for the comparator, a 1.42% difference; RD is lower at eight corners, but slightly higher at 360 V/full load. This is neither the original loss-ranking proxy nor a duty-weighted efficiency result. Four additional common-parameter scenarios—half and 1.5-times resistive paths, 20% more output charge, and 1 μ H added leakage—retain the comparison signs at three selected corners (24 further equal-output cases; Supplementary Material S3). They do not certify performance over all possible components.

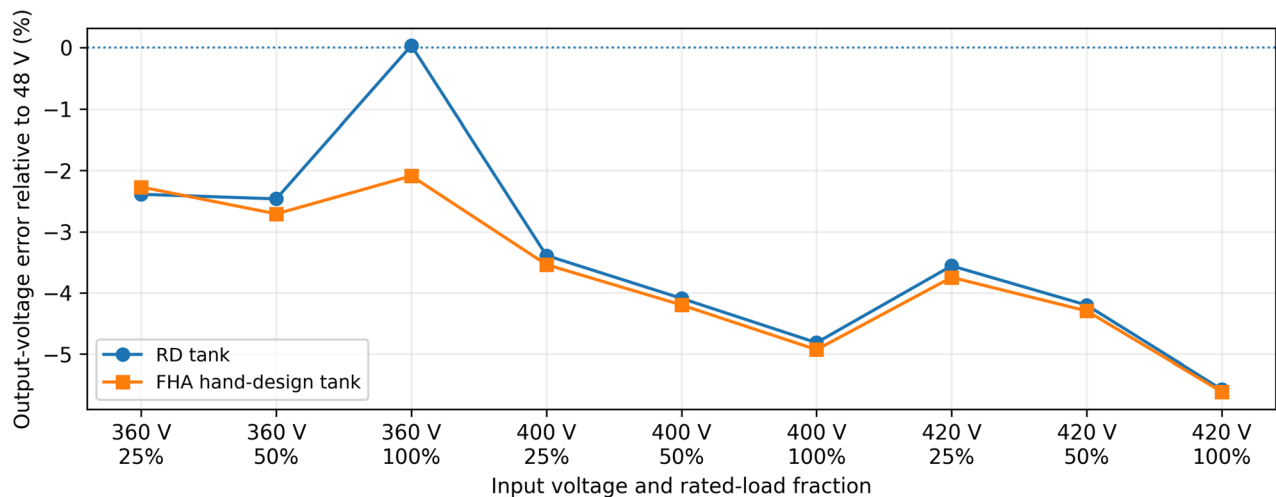


Figure 12. Output error from the new nonlinear-charge parasitic circuit at each tank’s original FHA frequency. The load resistance is fixed at its rated corner value; actual output power therefore changes with the output voltage. No dynamic regulator is included in this direct-transfer test.

Table 12. Equal-output generic switched-circuit comparison. RD denotes ResoSym-RD; H denotes the prespecified FHA hand-calculated design comparator. P_{dis} is integrated modeled dissipation, not a measured loss.

V_{in} (V)	Load	$f_{s,RD}$ (kHz)	$f_{s,H}$ (kHz)	$I_{r,pk,RD}$ (A)	$I_{r,pk,H}$ (A)	$P_{dis,RD}$ (W)	$P_{dis,H}$ (W)
360	25%	93.770	95.353	4.816	5.895	9.500	10.105
360	50%	92.641	94.366	5.525	6.051	20.233	20.685
360	100%	91.233	92.922	10.766	10.754	51.152	51.049
400	25%	110.992	111.960	4.095	5.050	9.125	9.588
400	50%	110.035	111.056	5.334	5.905	19.487	19.932
400	100%	108.251	109.371	9.260	9.538	47.007	47.335
420	25%	124.131	125.258	3.795	4.666	8.893	9.124
420	50%	122.597	122.982	5.062	5.665	18.953	19.379
420	100%	120.247	120.771	8.417	8.801	44.764	45.217

6.8.2. Executed Commutation Evidence and Its Limits

Figure 13 shows the computed upper-switch commutation at 360 V/full load after frequency correction. Its drain–source voltage collapses before channel enhancement, the upper body diode clamps the node, and the enhanced channel takes over the reverse current. The complementary transition is also retained in Supplementary Material S3. Both incoming devices reach the low-voltage condition in all 54 principal cases; the screening threshold is 2% of input voltage, and the recorded nominal values are actually body diode-clamped. The normalized signals u_1 and u_2 are imposed channel commands, not simulated gate–source voltages.

The secondary evidence is deliberately mode-dependent. At 360 V/full load, the forward current extinguishes about 1.2 μ s before the next primary turn-off begins (Figure 14), providing a modeled zero-current interval. At 420 V/full load with the uncorrected FHA frequency, approximately 10.99 A remains in the outgoing diode path at the start of primary turn-off (Figure 15). Not every point therefore has a pre-transition zero-current interval. Because minority-carrier storage and calibrated reverse recovery are not included, these traces do not establish recovery-free hardware ZCS or universal rectifier soft switching.

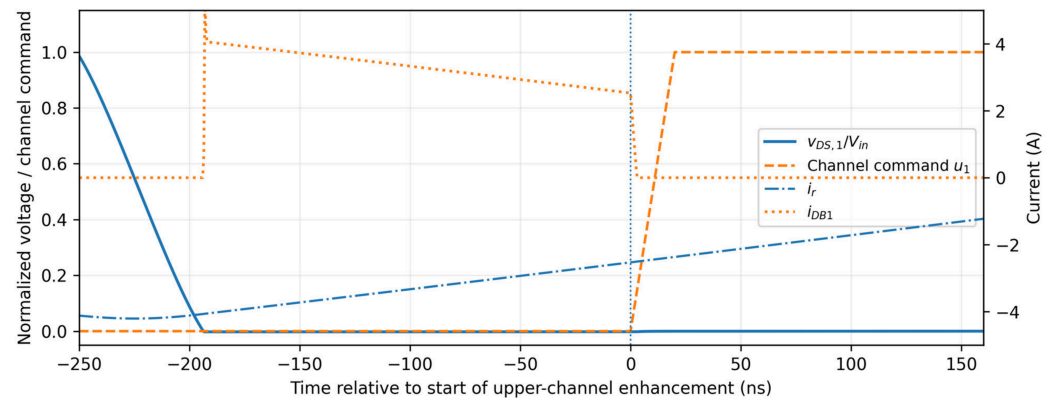


Figure 13. Computed RD upper-switch commutation at 360 V/full load, $f_s = 91.233$ kHz and $t_d = 250$ ns. The 0.5 ns record distinguishes capacitor discharge, body diode conduction and channel takeover. Negative pre-turn-on v_{DS} is the modeled body diode clamp, not a negative residual-energy claim. Here $v_{DS,1} = V_{in} - v_{sw}$ is the upper MOSFET drain-to-source voltage (V); i_{DB1} is positive from the switch node to the positive DC rail (A), and i_r is positive from the switch node into the resonant tank (A). The signals u_1, u_2 are dimensionless upper/lower channel commands.

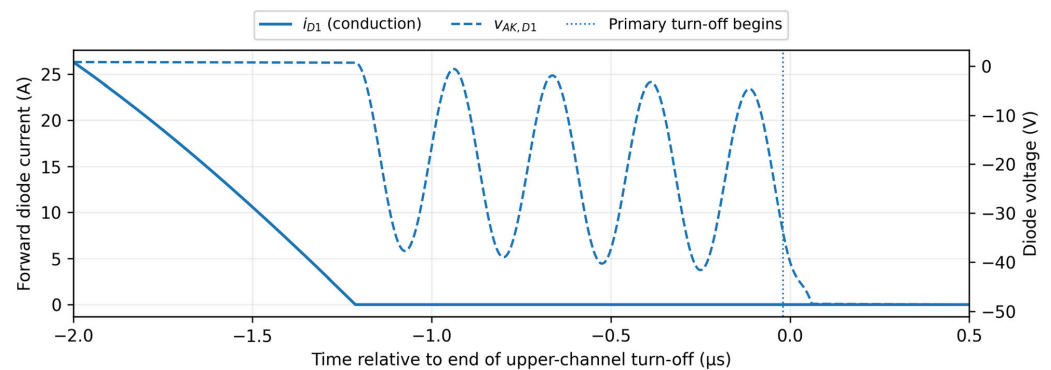


Figure 14. Modeled rectifier forward-current extinction and subsequent blocking-voltage ringing at 360 V/full load in the corrected-frequency RD case. D_1 and its complementary series diode share the conduction current. The voltage reflects the declared differential capacitance model; carrier-storage recovery is absent. The current i_{D1} is the forward conduction current from anode to cathode of D_1 (A), not total current including junction-capacitance displacement. The voltage $v_{AK,D1} = v_{A,D1} - v_{K,D1}$ (V) is negative under reverse bias.

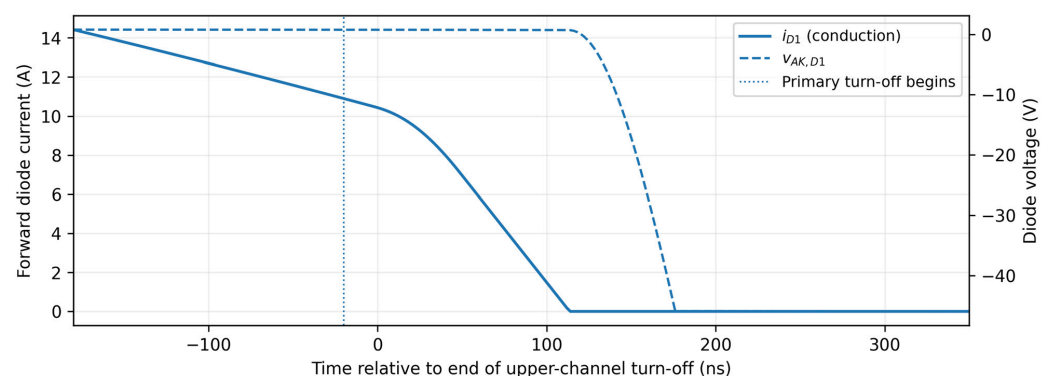


Figure 15. Contrasting secondary commutation at 420 V/full load using the original FHA command, $f_s = 136.547$ kHz. The outgoing forward current is nonzero when the primary turn-off starts. This direct-transfer point is not at regulated 48 V output and is not used for the equal-output loss ranking. The i_{D1} and $v_{AK,D1}$ sign conventions are the same as in Figure 14.

Finally, the locked 5 ns ceiling RD schedule is transferred to the previously corrected frequencies without refitting. All nine nominal cases and the same nine cases with a 20% increased output charge remain body diode-clamped before turn-on; mean output spans 47.972–48.006 V. This limited circuit test supports the nominal timing transfer under the declared assumptions. It does not promote the earlier 20,000-realization FHA pass fractions into switched-circuit yield or hardware reliability statistics.

7. Rational Design Procedure

The proposed method can be implemented as the following auditable sequence.

7.1. Step 1: Define the Specification and Non-Negotiable Limits

Specify input voltage, output voltage, power, load range, isolation, switching frequency band, current and voltage envelopes, magnetic limits, device charge, and allowable control sensitivity. Separate hard constraints from preferences.

7.2. Step 2: Build the Operating Corner Set

Construct all combinations of line and load that must be guaranteed. Additional corners can include temperature, aging, burst-mode entry, startup, and hold-up conditions. The present benchmark uses nine electrical corners.

7.3. Step 3: Perform Topology-Aware Normalized Screening

Embed SRC, parallel-loaded, LCC, and LLC models in the common resonance-centered coordinates. Tune family-specific parameters within declared ranges. Maximize coverage first and record burden transfer rather than using gain coverage alone.

7.4. Step 4: Reject Unsuitable Families Early

A family with incomplete coverage, insufficient headroom, or excessive normalized burden is not carried into physical synthesis. This step reduces detailed simulation effort and makes family choice traceable.

7.5. Step 5: Construct the Physical LLC Design Space

Select the target resonance, transformer ratio and physical Q_{full} -m search domain. Reconstruct L_r , C_r and L_m with Equation (19), and solve all admissible gain roots at every corner.

7.6. Step 6: Evaluate Simultaneous Margins

Calculate charge, headroom, inductive-angle, current, capacitor voltage, flux, and sensitivity margins. Form the max-min reserve ρ . An empty feasible region is a valid output; it means that the specification or device envelope must be revised.

7.7. Step 7: Select a Continuous Margin-Optimal Corridor

Maximize ρ before considering a loss proxy. Inspect whether the optimum is isolated or lies on a broad ridge. A broad corridor is preferable for component availability and tolerance robustness.

7.8. Step 8: Select and Reevaluate Rounded Component Targets

Declare the rounding or component selection rule and re-evaluate the chosen targets, including resonance, quality factor, magnetizing ratio, gain roots and all margins. A catalog or magnetic-construction optimizer is a subsequent implementation layer, not an implicit output of the present fixed triplet.

7.9. Step 9: Perform Tolerance-Aware Reevaluation

Use bounded component, transformer, device-charge, timing, and resistance variations. Store run-level results, active constraints, and worst corners. Report the tolerance model explicitly.

7.10. Step 10: Generate Control Schedules and a Design Passport

Fit the corner-dependent command only on the calibration population, lock it, and test it with the same uncertainty treatment as fixed timing. Include the component targets, frequency schedule, guard definition, command quantization, nominal margins, sample sizes, test results and outstanding validation in the design passport.

This sequence converts a difficult iterative task into a decision process with visible rejection criteria. It does not eliminate engineering judgment; it directs that judgment toward the constraints that remain active after analytical screening.

8. Discussion

8.1. Why LLC Is Retained

The expanded-domain audit changes the interpretation of family selection. PLRC reaches complete coverage and has lower burden than the high-headroom LLC screening winner. LLC remains the first choice only under the stated priority that maximizes corner coverage and then minimum frequency headroom. A voltage-, circulation- or implementation-cost-first decision can retain PLRC or LCC. The initial domain must therefore not be used to label an excluded family structurally incapable.

This distinction is central to rational topology screening. Converter families should not be ranked by one universal score. They should be screened by common questions and then interpreted through topology-specific limits. The applicability mask is therefore conceptual even when it is not written as a binary vector in the code: m is active only for LLC, α only for LCC, and native output-stress meanings remain family dependent.

8.2. Magnetizing Inductance as a Competing Design Mechanism

The tolerance study confirms a result already suggested by LLC modal-symmetry analysis: magnetizing inductance is not merely a gain-shaping element. A larger L_m can reduce magnetizing current and circulation, but it can also reduce the current available to commutate switch output charge at light load or high gain. In the present design, L_m is the dominant parameter for the minimum robust margin.

The feasible-region ridge in Figure 6 is a practical visualization of this competition. Moving along the ridge trades quality factor, magnetizing ratio, current, headroom, and commutation reserve without immediately losing feasibility. The best engineering point is therefore not necessarily the point with the largest m , the lowest circulation, or the most symmetric gain curve. It is a point with sufficient reserve in all active domains.

8.3. Margin-First Versus Weighted Optimization

The difference from prior optimization is the selected decision rule, not the existence of constraints. Wei et al. minimize RMS current within a time-domain design procedure [17], and Yin and Luo impose stepwise constraints with several current/frequency objectives [18]. Such methods need not accept infeasible solutions. In ResoSym-RD, feasibility is enforced first and the nominal minimum normalized margin defines the primary preference; the matched comparator demonstrates that this preference need not maximize sampled timing yield.

An unconstrained weighted score or an insufficient penalty can conceal a violated physical limit; this is not a criticism of properly constrained optimization. ResoSym-RD

separates feasibility from preference: the common admissible region is constructed first, the minimum normalized margin is maximized within the declared search, and the ranking proxy is used only afterward. Table 6 makes the resulting trade-offs visible rather than claiming that this ordering is universally optimal.

A scalar weighted preference must not hide a failed hard constraint, but maximizing nominal reserve also does not maximize sampled feasibility. The rounded FHA comparator in Table 6 exposes this distinction: it has a less favorable nominal reserve and proxy, yet a higher fixed-timing pass fraction. ResoSym-RD documents this trade-off instead of claiming universal superiority. A probability-oriented design would require a separately specified objective and independently assessed uncertainty law.

8.4. Control Headroom as a First-Class Design Variable

Traditional resonant design often reports a required frequency range after the tank is chosen. Here, frequency headroom participates in synthesis. The LCC screening result demonstrates why this matters: full gain coverage is achieved, but one corner lies close to the control boundary. Such a design may have little reserve for tolerance drift, digital frequency resolution, input transients, or aging.

The selected LLC schedule uses 91.2–139.6 kHz nominally within a 75–180 kHz band. In the tolerance population, the observed extremes are 85.5 and 153.5 kHz. The control band therefore retains visible reserve after component variation.

8.5. Adaptive Dead Time and Physical-Margin Symmetry

Here, adaptive means an operating corner-dependent schedule constructed offline from a declared uncertainty model. It is distinct from the body diode-detection-based adaptation reported by Lange et al. [22]. No detector, cycle-by-cycle timing feedback or associated hardware performance is claimed. Deployment must also respect the finite commutation window analyzed in parasitic-aware timing work [21], including measurement/driver delays and an upper admissible dead time boundary.

The locked schedule increases the command at 360 V/full load and decreases it at the other corners. This is a corner-dependent timing allocation, not evidence that the switching loss is minimized. A real implementation must also check the upper admissible dead time limit, current reversal, body diode conduction and driver behavior; those are not resolved by the FHA quantile calculation [21].

The schedule should be implemented as a function of measurable or commanded states, for example;

$$t_d^* = \mathcal{L}(V_{in}, I_o, f_s, T_j), \quad (45)$$

where the calligraphic map denotes a calibrated discrete or interpolated lookup table, the output current is measured or estimated, and the junction temperature is estimated for the semiconductor devices. The present table uses only input voltage and load fraction; temperature and device-specific nonlinear charge data must be added during hardware closure.

8.6. Reproducibility and Auditability

Supplementary Materials S1–S3 provide the complete code, deterministic seed, benchmark configuration, aggregate and run-level CSV files, and both PNG and SVG figures. The code records not only a selected design but also rejected family candidates, feasible-grid points, active constraints, and sensitivity statistics. This is important because reproducibility in converter design is not limited to reproducing a final waveform. It should also reproduce the path by which alternative families and parameter regions were rejected.

9. Limitations and Validation Roadmap

The experimental stages are not being declared unnecessary: Wei et al., Zaikin et al. and Leone et al. report prototype-based assessments for their respective designs [17,19,20]. Those results establish a distinct evidence level. The present study identifies and evaluates candidate regions and regimes and uses them for pre-synthesis; its planned measurements will test the predictions and update device, magnetic and timing models rather than assume their confirmation.

The present study is intended as an auditable analytical and numerical pre-synthesis methodology rather than as a complete hardware-validated converter design. Its limitations can be grouped into three categories: model fidelity, component representation, and uncertainty coverage.

Model fidelity: FHA remains the synthesis model, whereas Section 6.8 adds a separate generic switched-circuit check with finite conduction paths, nonlinear output charge, differential capacitance, output dynamics and added series leakage. The check is independently integrated but is not a full manufacturer SPICE model. Symmetric piecewise-linear rectifier paths and lumped junction capacitance do not reproduce calibrated reverse recovery or common-mode paths. Magnetic saturation, frequency-dependent winding loss, core loss, interwinding common-mode capacitance, gate-loop dynamics and thermal coupling remain outside both quantitative models. Flux estimates remain preliminary, not a completed magnetic design.

Device and loss representation: the FHA aggregate ranking proxy is distinct from the integrated dissipative terms in the new switched circuit. The latter are computed from explicit generic resistances, diode thresholds and imposed conductance commands, and satisfy the stated energy-balance check. Neither quantity is measured efficiency or a calibrated total converter loss. The nonlinear $Q(v)$ curve is charge-normalized to the stated envelope rather than fitted to a selected device. Hardware closure requires device-specific $Q_{oss}(v, T)$, reverse-conduction and recovery data, an actual gate circuit and measured parasitic parameters.

Uncertainty and validation status: independent clipped-normal variations and a locked holdout protocol quantify FHA-model coverage, not field reliability. The new circuit campaign evaluates nominal corners and declared parameter scenarios, not all 20,000 tolerance realizations. Effective turns-ratio variation is not fractional physical turns. Correlated component lots, nonlinear magnetics, temperature dependence, aging and untested distribution tails remain outside the evidence. No prototype measurements, measured efficiency or EMI compliance are reported. The new commutation figures are executed time-domain calculations and are not reconstructed FHA sinusoids.

The retained design should subsequently pass a four-stage validation ladder:

- Device-specific and external-simulator validation. Extend the common generic circuit check using actual device-charge/recovery curves, a selected integer-turn transformer, measured leakage and winding capacitance, and a gate-loop model. A separate established circuit simulator and device characterization should test these implementation-level assumptions; the current BDF2/Radau cross-check verifies numerical agreement for the declared equations, not their identity with hardware.
- Magnetic, thermal, and control closure. Complete the transformer and resonant inductor design using material-dependent core-loss, copper-loss, saturation, and temperature models, and validate the closed-loop frequency controller with quantization, saturation, startup, burst-mode entry, load steps, and line transients.
- Protection and EMI validation. Evaluate short-circuit and overload operation, startup stress, common- and differential-mode parasitic paths, conducted and radiated EMI,

insulation coordination, and the interaction between protection thresholds and the feasible operating region.

- Experimental verification and model updating. Construct a laboratory prototype and acquire synchronized switch-node voltage, gate voltage, resonant-current, output, and thermal measurements. The measured component, timing, charge, loss, and temperature distributions should then be used to recalibrate the tolerance model and the adaptive dead time schedule.

CLLC and bidirectional resonant conversion remain intentionally outside the scope of the present paper. Their extension requires direction-dependent equivalent loads, reverse-power operating modes, bidirectional device-conduction models, and a separate symmetry-aware synthesis framework.

10. Conclusions

ResoSym-RD organizes normalized family screening, physical-unit LLC margins, selected rounded targets and timing statistics as an auditable pre-synthesis sequence. Its contribution is the visibility of assumptions and competing criteria, not the invention of FHA, optimization or adaptive dead time.

For the 400 V/48 V, 1 kW benchmark, nested-domain screening expands SRC coverage from two to three corners and PLRC coverage from eight to all nine. LLC remains preferred under the declared frequency-headroom priority, but its expanded winner carries more reactive burden and does not universally dominate the other families. The retained physical LLC targets, $L_r = 20 \mu\text{H}$, $C_r = 88 \text{ nF}$ and $L_m = 106 \mu\text{H}$, provide a nominal minimum normalized margin of 1.441. The prespecified rounded FHA comparator has a lower nominal margin and a higher loss-ranking proxy, but higher fixed-timing sampled feasibility.

With matched timing perturbations and an independent 20,000-realization test population, the locked continuous schedule gives 99.925% joint charge-only feasibility versus 98.860% for fixed 250 ns timing. Its mean command is 36.42% shorter. Ceiling quantization to 5 ns changes the mean reduction to 34.89% and test feasibility to 99.935%; requiring the additional 25 ns guard to survive perturbations is a stricter, separately reported test. None of these empirical model fractions is an experimental ZVS rate or a reliability guarantee.

The contribution is a pre-synthesis and design-screening tool, not a replacement for detailed engineering closure. Its value lies in the traceable chain:

specification → domain-aware family screening → simultaneous margins → rounded targets → independent tolerance assessment → locked control schedule.

The matched switched-circuit stage adds an explicit fidelity gate: the uncorrected FHA schedule can miss output by 5.61% and underestimate the RD peak current by 21.06% in the tested scenario. Frequency correction recovers the nine operating points, but the equal-output loss comparison is modest and non-dominating: there is a 1.42% lower uniform mean for RD, with a reversal at low-line/full load. The executed waveforms separate primary low-voltage turn-on from secondary current-extinction behavior. Generic circuit agreement supports targeted design refinement, not measured converter performance.

This chain provides a practical bridge from resonant converter symmetry theory to future automated, device-aware design environments.

Supplementary Materials: The following supporting information can be downloaded at: <https://www.mdpi.com/article/10.3390/sym18101608/s1>. The combined archive contains Supplementary Materials S1–S4. Supplementary Materials S1 and S2 contain the previously reported numerical and reproducibility records. Supplementary Material S3 contains the six-state circuit equations, declared generic parameters, principal comparison tables, native calculated wave-

form samples, numerical-convergence and separate-integrator checks, timing transfers, parameter scenarios, source code, execution logs, and an integrity manifest. S3 distinguishes executed circuit calculations from FHA statistics and from the still-unavailable hardware evidence. Supplementary Material S4 records the targeted literature update, source-inspection scope, study-to-claim mapping, and current reference-number crosswalk for the studies cited in the main manuscript [11–23]. All scholarly references discussed in S4 are included in the main manuscript reference list; S4 introduces no additional scientific references.

Funding: This work was supported by the European Regional Development Fund under the ‘Research Innovation and Digitization for Smart Transformation’ Program 2021–2027, Project BG16RFPR002-1.014-0006 ‘National Center of Excellence Mechatronics and Clean Technologies’. The APC was funded by the Project BG16RFPR002-1.014-0006.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Numerical data, source code, configurations, execution records and integrity manifests are supplied in Supplementary Materials S1–S3. Supplementary Material S3 labels the differential-circuit solver and generic assumptions; it contains no laboratory or external-SPICE measurement record. Native waveform samples and reported metrics can be regenerated with the supplied scripts.

Acknowledgments: The research was carried out within Project BG16RFPR002-1.014-0006 ‘National Center of Excellence Mechatronics and Clean Technologies’. The author thanks the reviewers for identifying the numerical-alignment and reproducibility issues addressed in the frozen revision workflow.

Conflicts of Interest: The author declares no conflicts of interest.

Appendix A Nomenclature

Symbols, units and conventions for normalized screening, physical LLC synthesis, robustness, timing and calculated commutation waveforms are summarized in Table A1.

Table A1. Symbols and conventions used in screening, physical LLC synthesis, statistical assessment and switched-circuit waveforms.

Modeling Level	Units or Type	Definition	Symbol/Operator
Normalized family screening quantities			
Screening	dimensionless; rad s ^{−1} for ω	Normalized operating angular frequency; ω is the operating angular frequency and ω_r is the reference resonant angular frequency. The screening assignments $\omega_r = 1$ and $Z_r = 1$ are per-unit bases, not physical values.	$F = \omega / \omega_r$
Screening/LLC	Ω or dimensionless	Characteristic impedance; normalized load resistance $R = Z_r / Q$; load quality factor; full-load quality factor; prescribed load fraction at regulated V_o .	$Z_r, R, Q, Q_{full}, \ell$
Screening	dimensionless	Topology identifier $\mathcal{T}$; topology-specific structural coordinate η ; LCC ratio $\alpha = C_p / C_s$; LLC magnetizing ratio $m = L_m / L_r$.	$\mathcal{T}, \eta, \alpha, m$
LCC structural quantities	F ; dimensionless ratio	Series and output-side shunt capacitances of the LCC tank before normalization; $\alpha = C_p / C_s$.	C_s, C_p
Screening	normalized complex impedance	Normalized series, output-side, and input impedances, with $Z_{in} = Z_s + Z_p$.	Z_s, Z_p, Z_{in}
Screening	complex; dimensionless	Complex normalized transfer $H_{\mathcal{T}}$ (abbreviated H in Section 3); reference $H_{ref} = H_{\mathcal{T}}(1, Q_{full}, \eta) $; normalized gain $G_{\mathcal{T}} = H_{\mathcal{T}} / H_{ref}$ (abbreviated G).	$H_{\mathcal{T}}, H, H_{ref}, G_{\mathcal{T}}, G$

Table A1. Cont.

Modeling Level	Units or Type	Definition	Symbol/Operator
Screening	normalized complex current	Complex normalized RMS phasors of the series/input, load, and topology-specific shunt currents; $I_{\text{load,ref}} = H_{\text{ref}} Q_{\text{full}}$ is the full-load reference current magnitude.	$I_{\text{in}}, I_{\text{load}}, I_{\text{sh}}, I_{\text{load,ref}}$
Screening	normalized complex voltage	Maximum normalized capacitor- and inductor-voltage phasors obtained from the native reduced model.	V_C, V_L
Screening	dimensionless	Normalized current burden, screening circulation burden, and voltage burden. The superscript “scr” distinguishes the reduced-model metric from the physical LLC circulation index.	$K_I, K_{\text{circ}}^{(\text{scr})}, K_V$
Screening	dimensionless	Resonance-centered control headroom, local normalized-gain slope $S_G = dG_{\mathcal{T}}/dF $, and root-selection cost.	H_C, S_G, J_{scr}
All stages	operator	Clipping operator $\min\{\max\{x, 0\}, 1\}$.	$\text{clip}(x, 0, 1)$
Physical LLC quantities			
Physical LLC	V, W , dimensionless	DC input and regulated output voltage; rated output power; prescribed power $P_o(\ell) = \ell P_{o,\text{rated}}$ at regulated V_o ; turns ratio $n = N_p/N_s$.	$V_{\text{in}}, V_o, P_{o,\text{rated}}, P_o(\ell), n$
Physical LLC	Hz; rad s^{-1}	Switching frequency, actual series-resonant frequency, target resonance, and angular frequencies $\omega = 2\pi f_s$, $\omega_r = 2\pi f_r$. All headroom frequencies use one common unit.	$f_s, f_r, f_r^*, \omega, \omega_r$
Physical LLC	H, F, Ω	Resonant inductance, resonant capacitance, magnetizing inductance, and characteristic impedance $Z_r = \sqrt{L_r/C_r}$.	L_r, C_r, L_m, Z_r
Physical LLC	Ω	Full-load DC reference $R_o = V_o^2/P_{o,\text{rated}}$; primary-referred FHA resistance at ℓ ; $R_{\text{ac,full}} = R_{\text{ac}(1)}$. The physical partial-load resistance is R_o/ℓ .	$R_o, R_{\text{ac}}(\ell), R_{\text{ac,full}}$
Physical LLC	Ω ; dimensionless H	Physical series, magnetizing, output-side and input impedances; $Z_m = j\omega L_m$. $H = Z_p/Z_{\text{in}}$; $H(f_s)$ is evaluated at $\omega = 2\pi f_s$.	$Z_s, Z_m, Z_p, Z_{\text{in}}, H$
Physical LLC	V rms, A rms	First harmonic RMS bridge voltage and complex RMS phasors of the resonant, reflected-load, and magnetizing currents.	$V_{1,\text{rms}}, I_r, I_{\text{load}}, I_m$
Physical LLC	rad; degrees	Non-negative input-impedance phase. φ is used in radians in trigonometric functions; $\varphi_{\text{deg}} = 180\varphi/\pi$ is used in degree-based margins.	$\varphi, \varphi_{\text{deg}}$
Physical LLC/control	Hz; dimensionless indices	Lower/upper allowed switching frequencies; physical frequency headroom; relative gain sensitivity from Equations (20) and (21). Distinct from screening H_c and S_G .	$f_{\text{min}}, f_{\text{max}}, H_f, S_F$
Physical LLC/control	C , dimensionless, s	Aggregate commutated device output charge, charge safety factor, applied dead time, and added implementation guard time.	$Q_{\text{oss},\Sigma}, k_Q, t_d, t_{\text{guard}}$
Physical LLC/control	A ; dimensionless; s	FHA peak commutation-current estimate; commutation-charge margin; charge-transfer time plus scheduling guard t_{guard} .	$I_{\text{com,pk}}, M_Q, t_{d,\text{req}}$
Physical LLC	A, V, T	Peak resonant current, peak resonant capacitor voltage, peak resonant inductor voltage, and preliminary transformer flux-density estimate.	$I_{r,\text{pk}}, V_{C_r,\text{pk}}, V_{L_r,\text{pk}}, B_{\text{pk}}$

Table A1. Cont.

Modeling Level	Units or Type	Definition	Symbol/Operator
Magnetic screening	turns; m ² ; T	Primary and secondary turns; effective core area; preliminary flux-density limit. The stated idealized turns reference is not a completed winding design.	N_p, N_s, A_e, B_{max}
Physical LLC	dimensionless	Physical LLC circulation index $ I_r / I_{load} $. It is distinct from $K_{circ}^{(scr)}$.	$K_{tank}^{(LLC)}$
Physical LLC	Ω, W , averaging operator	Equivalent primary-path resistance, conduction-loss proxy, aggregate ranking proxy, and arithmetic mean over the nine nominal operating corners.	$R_{path}, P_{cond}^{proxy}, P_{\Sigma}^{proxy}, overbar$
All circuit models	operator	Parallel combination $AB/(A+B)$.	$A//B$
Robustness, feasibility, and control quantities			
Robust synthesis	dimensionless	Normalized margins for commutation charge, control headroom, inductive angle, peak current, resonant capacitor voltage, flux density, and gain sensitivity, respectively.	$M_1 \dots M_7$
Robust synthesis	sets/dimensionless	Design vector $x = (Q_{full}, m)$; corner $c = (V_{in}, \ell)$; required set $\mathcal{C}$; feasible region Ω ; worst-corner minimum reserve ρ .	$x, c, \mathcal{C}, \Omega, \rho$
Robust synthesis	vector; index; operator	Design vector maximizing ρ in Ω ; constraint index $j = 1, \dots, 7$ in Equation (33). The latter differs from $j = \sqrt{-1}$ in circuit impedances.	$x_\rho, j, argmax$
Tolerance study	dimensionless; count; %	Minimum reserve per realization; population size; number passing all stated corner conditions; $Y = 100N_{feasible}/N_{MC}$. fixed/locked/test identify the timing scheme and population.	$\rho_{MC}, N_{MC}, N_{feasible}, Y$
Tolerance study	dimensionless	Signed physical gain-magnitude deviation at corner c . Its maximum absolute value over $\mathcal{C}$ is the stored maximum gain error; not the screening $G_{\mathcal{T}}$.	$\Delta G(c), \max_{c \in \mathcal{C}} \Delta G(c) $
Control scheduling	operator; s	Empirical 99.5th percentile over calibration realizations at fixed corner c ; selected, then locked, command. $\star$ does not certify loss optimality.	$Quant_{0.995}\{\cdot\}, t_d^*(c)$
Implementation	lookup function	Calibrated discrete or interpolated dead time lookup map; I_o is measured/estimated output current and T_j is estimated junction temperature.	$\mathcal{L}(V_{in}, I_o, f_s, T_j)$
Switched-circuit and waveform quantities			
Switched circuit	C; F; V	Per-device output charge and differential output capacitance versus device drain-source voltage v . Charge $Q(v)$ is not the tank quality factor Q .	$Q(v), C_{oss}(v), v$
Switched circuit	A	Instantaneous resonant current, positive from switch node into tank; magnetizing current, positive from the primary port to its return. Upper-case I_r, I_m denote FHA RMS phasors.	i_r, i_m
Switched circuit	V	Switch node relative to primary return; physical resonant capacitor voltage including DC bias; primary-port voltage; output voltage.	v_{sw}, v_{Cr}, v_p, v_o
Primary commutation	V; A	Drain-to-source voltage: $v_{DS,1} = V_{in} - v_{sw}$. Upper body diode current is positive from switch node to positive DC rail.	$v_{DS,1}, i_{DB1}$
Primary commutation	dimensionless	Imposed upper/lower channel-conductance commands, from 0 (OFF) to 1 (fully enabled); not gate-source voltages.	u_1, u_2
Secondary commutation	A; V	D1 forward anode-to-cathode conduction current, excluding displacement current; diode voltage $v_{AK,D1} = v_{A,D1} - v_{K,D1}$, negative in reverse bias.	$i_{D1}, v_{AK,D1}$

Table A1. Cont.

Modeling Level	Units or Type	Definition	Symbol/Operator
Diode-drop model	A	Forward conduction current in the particular diode in Table 11; not a shared resonant or primary-referred current.	i
Circuit comparison	W; labels	Integrated modeled dissipation in Table 12. Subscripts RD and H identify the ResoSym-RD and hand-calculated FHA designs; H here is a design label, not a transfer function.	P_{dis}, RD, H

The symbols ℓ and l denote the same prescribed load fraction. Unless stated otherwise, vertical bars denote complex magnitude or scalar absolute value, overbars denote arithmetic means over the stated corner set, and unity is the normalized-margin feasibility boundary. Subscripts nom, rated, full, min, max, rms, pk, com, req and fix denote nominal, rated, full-load, minimum, maximum, RMS, peak, commutation, required and fixed-command quantities. The superscripts scr and LLC identify the screening and physical circulation measures. A star denotes a declared target or selected value according to context, not a guarantee of experimental optimality.

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