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# The Development and Progress of Multi-Physics Simulation Design for TSV-Based 3D Integrated System

**Xianglong Wang [1], Dongdong Chen [1,*], Di Li [1,*], Chen Kou [2] and Yintang Yang [1]**

[1] School of Microelectronics, Xidian University, Xi'an 710071, China
[2] Business School, Xijing University, Xi'an 710123, China
* Correspondence: ddchen@xidian.edu.cn (D.C.); lidi2004@126.com (D.L.); Tel.: +86-183-9099-9143 (D.C.); +86-137-0925-0163 (D.L.)

**Abstract:** In order to meet the requirements of high performance, miniaturization, low cost, low power consumption and multi-function, three-dimensional (3D) integrated technology has gradually become a core technology. With the development of 3D integrated technology, it has been used in imaging sensors, optical integrated microsystems, inertial sensor microsystems, radio-frequency microsystems, biological microsystems and logic microsystems, etc. Through silicon via (TSV) is the core technology of a 3D integrated system, which can achieve vertical interconnection between stacked chips. In this paper, the development and progress of multi-physics simulation design for TSV-based 3D integrated systems are reviewed. Firstly, the electrical simulation design of TSV in a 3D integrated system is presented, including the lumped parameters model-based design and numerical computation model-based design. Secondly, the thermal simulation design of TSV in a 3D integrated system is presented based on the analytical model or numerical computation model. Thirdly, the multi-physics co-simulation design of TSV in a 3D integrated system is presented, including the thermal stress and electron thermal coupling simulation design. Finally, this paper is concluded, and the future perspectives of 3D integrated systems are presented, including the advanced integrated microsystems, the crossed and reconfigurable architecture design technology and the standardized and intelligent design technology.

**Keywords:** 3D integrated system; through silicon via; simulation design; multi-physics



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## 1. Introduction

With the feature size of integrated circuits shrinking down toward the limits of the conventional nanometer scale, three-dimensional (3D) integrated technology is a promising approach for extending Moore's law [1]. Three-dimensional integrated technology can alleviate the interconnection bottleneck that currently exists at the nanoscale. Three-dimensional integration technologies can be divided into 3D System-in-Package (SiP), 3D Wafer-Level-Packaging (WLP) and 3D Stacked-Integrated-Circuit (SIC). The common scaling denominator of these 3D integration technologies is the stacking of multiple layers of CMOS chips. The difference between these technologies is whether the electrical interconnect is achieved by using package-level lead bonding or 3D vertical interconnects and whether the interconnect is achieved at the package level or at the chip level. The 3D SiP technology is used to achieve the connection of multi-layer stacked CMOS chips at the package level based on the wire bonding and flip chip technology. The 3D WLP technology is a wafer-level packaging technology based on the rewiring and TSV to transfer the electrical signal. Based on the chip fabrication equipment, 3D SIC technology is referred to as using TSV to penetrate the substrate to realize the global and intermediate interconnect of multi-layer stacked chips. Due to increase clocking speed, reduced transmission losses, power consumption and footprint area [2], 3D integrated technology is promising for multiple cores [3], memory [4], radio-frequency (RF) systems [5], logic units [6] and 3D

integrated circuit [7–9]. Based on the vertical stacking of chips, 3D integrated technology can effectively increase the integration degree, reduce the interconnection length and realize heterogeneous integration. Since the thickness of each silicon layer can be reduced to 20–100 μm, the length of TSV (typically about 30–100 μm) is substantially reduced by two to three orders of magnitude compared to the length of on-chip global interconnects (1 $mm^{-1}$ cm). Due to the advantages of low delay, small parasitic parameters and high data communication speed, through silicon via (TSV) [10–12] is the critical technology of 3D integrated systems. Due to the good conductivity and compatibility with CMOS processes of Cu material, TSV conductive filling is currently generally achieved by copper plating. The goals of electroplating are low stress, no holes and voids during the manufacturing of TSV. In the manufacturing of TSV, the critical material property deviation can make experiments deviate from the simulation and optimization. The electrical interconnection is realized by TSV in a 3D integrated system.

The major technical challenges of 3D integration are manufacturing, cost, performance and reliability. In terms of manufacturing, new materials, equipment and processes are introduced into 3D integration, which has a significant impact on existing integrated circuits manufacturing technologies. The CMOS process-compatible TSV manufacturing and 3D integration processes are the focus of research and development. In terms of equipment and materials, the aim is focused on developing greater efficiency and meeting the requirements of new equipment and materials for deep etching, high-precision alignment bonding, copper plating, etc. In terms of performance and reliability, 3D integration changes the structure of traditional integrated circuits, which has a significant impact on electrical performance, thermal stress reliability, yield and test methods. For different applications, the major concern is addressing the manufacturing technology, yield and cost.

Due to the significant increases in power density per unit area, the thermal reliability problem of a 3D integrated system is more prominent. Meanwhile, because the coefficient of thermal expansion (CTE) between materials is mismatched during the fabrication of TSV, the thermal stress is introduced in a 3D integrated system, which will affect the charge carrier mobility of electron devices. When the integrated system is driven by voltage, Joule heat is produced. The temperature is increased by Joule heat, which affects the electrical parameters and thermal conductivity. The electric field distribution is further affected by the Joule heat, so the mutual coupling between the electric and thermal fields is iterated continuously until achieving a stable thermal distribution. The coupling relationships of electrical, thermal and stress are shown in Figure 1. The reliability of TSV is a multi-physics coupling problem, which requires that thermal, electrical and mechanical reliability be considered simultaneously. The computational complexity is depended on the size of the established model and the size of the computational grid.

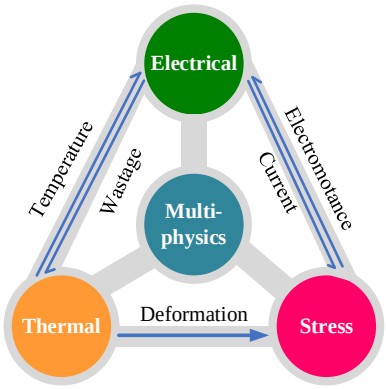



**Figure 1.** Multi-physical field coupling relationship.

In this paper, the development and progress of multi-physics simulation design for TSV-based 3D integrated systems are reviewed to provide a valuable reference for designing high-performance and reliable TSV-based 3D integrated systems. The electrical simulation

design of TSV in a 3D integrated system is introduced in Section 2. The thermal simulation design of TSV in a 3D integrated system is presented in Section 3. Section 4 presents the multi-physics co-simulation design of TSV in a 3D integrated system, including the thermal stress and electro-thermal coupling simulation design. Finally, the conclusions and perspectives of the TSV-based 3D integrated system are presented.

## 2. Electrical Simulation Design of TSV in 3D Integrated System

With the rapid development of modern chip technology, fast and accurate extraction of parasitic parameters of TSV is crucial to the design of 3D integrated systems. In order to extract the parasitic parameters of TSV accurately, the TSV lumped parameter models and numerical computation models have been investigated by many scholars.

### *2.1. Lumped Parameter Model-Based Design*

Generally, the closed-form expressions of the aggregate parameter model of the TSV are investigated based on the diameter of TSV, the height of TSV, the thickness of the insulation layer, the spacing from the ground TSV, the signal TSV, etc. Due to its simple structure, cylindrical TSV has been widely investigated. Savidis et al. [13] proposed the compute equations of the RLGC model of TSV based on the data fitting method. The numerical calculation results are compared with the simulation results, and the maximum errors of R, L and C are all less than 8%. The equivalent RLGC model of cylindrical TSV and the analytical equation of the lumped model parameter also has been proposed by Hu et al. [14], as shown in Figure 2a. The electrical characterization of TSV is analyzed in the frequency domain and time domain. In addition, the accurate electrical modeling of cylindrical TSV is proposed by Bandyopadhyay et al. [15] based on the metal-oxide-semiconductor (MOS) capacitance effects. Based on the Electroquasi-static theory and Bessel function, Xu et al. [16] established the RLGC model for TSVs valid from low- to high-frequency regimes, which consider the skin effect and MOS capacitance effect. Moreover, the coaxial TSV is proposed to decrease the crosstalk of the signal effectively. The outer metal layer of coaxial TSV has a shielding effect. Xu et al. [17] presented the RLGC empirical calculations expressions of coaxial TSV, which agree well with the full-wave extraction in coaxial TSV passive elements. Zhao et al. [18] proposed the equivalent lumped element circuit model of square and circular coaxial-TSV, as shown in Figure 2b. The parasitic capacitance, characteristic impedance and S parameters at different frequencies and temperatures are characterized and numerically compared. Lu et al. [19] proposed a wideband equivalent circuit model of coaxial annular TSV for 3D integrated circuits (ICs), as shown in Figure 2c. The closed-form expressions of RLGC are established based on the Bessel function, and the RLGC model is verified by a high-frequency simulator structure (HFSS). The maximum errors of R, L, G and C are 6.5%, 1.7%, 5.5% and 1.8%, respectively. Liang et al. [20] established the closed-form expression of resistance by solving the current continuity equation, and then the closed-form expression of inductance was established based on the Biot-Savart law. The maximum errors of resistance and inductance are 2% and 5%, respectively. Lu et al. [21] proposed the equivalent circuit model of shield differential TSVs in 3D IC, as shown in Figure 2d. The equivalent model is verified by 3D full-wave field solver HFSS, and the simulation results show that the equivalent model has a high accuracy during the range of 100 GHz. The high-frequency electromagnetic characteristics of differential impedance and insertion loss are analyzed. Salah et al. [22] proposed an equivalent lumped element model based on the physical size and material properties of TSV, as shown in Figure 2e. The closed-form expressions for R, L and C are introduced. The simulation results show that the maximum errors are all less than 6%. Qu et al. [23] established the equivalent model of differential TSV pair in 3D IC, as shown in Figure 2f. The computation results based on the equivalent are verified by HFSS in a wide frequency range. Fu et al. [24] proposed a shielded differential annular TSV and established the equivalent circuit model, as shown in Figure 2g. The simulation results show that the keep-out zone can be reduced without decreasing performance. Su et al. [25] propose a novel TSV that can be used to suppress the substrate noise. The equivalent RLGC model is

established, as shown in Figure 2h. The simulation results show that the errors of |S11| and |S21| are less than 3.3 dB and 0.05 dB, respectively. Furthermore, Hu et al. [26] proposed the differential multibit carbon nanotube (CNT) TSV and established the equivalent RLGC model, as presented in Figure 2i. Rao [27] investigated the electrical characteristics of taper TSV and established the equivalent circuit model of RLGC, as shown in Figure 2j. The return loss of tapered TSV displayed at 30 GHz is less than −20 dB, which is conducive to the high-frequency application of tapered TSV. Liu et al. [28] proposed the parasitic inductor model of ground–signal–ground taper TSV pair. The simulation results show that the error of the model is less than 8%. Alam et al. [29] assumed that the silicon substrate of TSV is a metal conductor to derive the closed-form expression of capacitance, but the effect of the depletion layer is not considered. Weerasekera et al. [30] established the RLC model of TSV based on the experiments fitting, which did not consider the thickness of the oxide layer and depletion zone. The simulation results show that the maximum error is less than 6%. Katti et al. [31] established a depletion layer capacitance model of TSV based on the depletion layer width and verified the model through numerical emulators. The maximum error is less than 3.52%. Cai et al. [32] derived the parasitic capacitance expression of TSV based on the depletion zone capacitance and oxide layer capacitance and analyzed the capacitance model in detail. The computation results are compared with the simulated results by Silvaco. The error between the mathematical model and the simulation results is 6.9%, while the error between the mathematical model and the measured results is 10.1%. The maximum errors of different RLGC models are presented in Table 1. and the lumped parameter closed-form expressions of different TSV for different conditions are shown in Table 2.

**Table 1.** Maximum errors of different RLGC model.

| Ref. | Maximum Errors | | | |
|---|---|---|---|---|
| | R | L | G | C |
| Savidis et al. [13] | 8% | 8% | 8% | 8% |
| Lu et al. [19] | 6.5% | 1.7% | 5.5% | 1.8% |
| Liang et al. [20] | 2% | 5% | - | - |
| Salah et al. [22] | 6% | 6% | - | 6% |
| Liu et al. [28] | - | 8% | - | - |
| Weerasekera et al. [30] | 2% | 3% | - | 6% |
| Katti et al. [31] | - | - | - | 3.52% |
| Cai et al. [32] | - | - | - | 10.1% |

**Table 2.** Closed-form expressions for different TSV.

| Closed-Form Expressions | Reference |
|---|---|
| $R_{\mathrm{DC}} = \frac{\rho H_{\mathrm{TSV}}}{\pi r_{\mathrm{TSV}}^2}$ | [32] |
| $R_{\mathrm{DC}} = \frac{\rho H_{\mathrm{TSV}}}{\pi(r_1 + H_{\mathrm{TSV}} r_2)}\left[1 + \frac{1}{2} r_2^2\right]$ | [20] |
| $R_{\mathrm{AC}} = \frac{\rho H_{\mathrm{TSV}}}{\pi(r_{\mathrm{TSV}}^2 - (r_{TSV} - \delta)^2)}$ | [33] |
| $R_{\mathrm{AC}} = \frac{\rho(2+r_2{}^2)}{4\pi r_2 \delta} \ln\left(1 + \frac{2 r_2 H_{\mathrm{TSV}}}{2 r_1 - \delta}\right)$ | [20] |
| $L = \frac{\mu_0}{4\pi}\left[2H_{\mathrm{TSV}} \ln\left((2H_{\mathrm{TSV}} + \sqrt{r_{TSV}^2 + (2H_{\mathrm{TSV}})^2})/r_{TSV}\right) + r_{TSV} - \sqrt{r_{TSV}^2 + (2H_{\mathrm{TSV}})^2}\right]$ | [31] |
| $L = \frac{\mu_0 \alpha}{2\pi}\left[H_{\mathrm{TSV}} \ln\left((H_{\mathrm{TSV}} + \sqrt{r_{TSV}^2 + H_{\mathrm{TSV}}^2})/r_{TSV}\right) + r_{TSV} - \sqrt{r_{TSV}^2 + H_{\mathrm{TSV}}^2} + \frac{H_{\mathrm{TSV}}}{4}\right]$ | [34] |
| $L = \frac{\mu_0}{4\pi}\left[\begin{array}{c} 2H_{\mathrm{TSV}}\left((H_{\mathrm{TSV}} + \sqrt{r_1^2 + H_{TSV}^2})/r_1\right) + 2r_1 - 2\sqrt{r_1^2 + H_{TSV}^2} + 0.5H_{\mathrm{TSV}} \\ + \frac{4\beta H_{\mathrm{TSV}}(H_{TSV}^2 - (H_{\mathrm{TSV}} + r_1)(\sqrt{r_1^2 + H_{TSV}^2} - r_1))}{(\sqrt{r_1^2 + H_{TSV}^2} - H_{\mathrm{TSV}})(4r_1 + \beta H_{\mathrm{TSV}})} \end{array}\right]$ | [20] |
| $L = \frac{\mu_0}{2\pi} H_{\mathrm{TSV}} \ln(1 + 2.84 H_{\mathrm{TSV}}/\pi r_{TSV})$ | [30] |
| $L_{21} = \frac{\mu_0 \alpha}{2\pi}\left[H_{\mathrm{TSV}} \ln\left((H_{\mathrm{TSV}} + \sqrt{p^2 + H_{\mathrm{TSV}}^2})/p\right) + p - \sqrt{p^2 + H_{\mathrm{TSV}}^2}\right]$ | [34] |

**Table 2.** *Cont.*

| Closed-Form Expressions | Reference |
| --- | --- |
| $L_{21} = \frac{\mu_0}{2\pi}\left[H_{\mathrm{TSV}} \ln\left(\frac{H_{\mathrm{TSV}}+\sqrt{p^2+H_{\mathrm{TSV}}^2}}{p}\right) + p - \sqrt{p^2+H_{\mathrm{TSV}}^2} + \frac{2\beta H_{\mathrm{TSV}}(H_{\mathrm{TSV}}^2-(H_{\mathrm{TSV}}+p)(\sqrt{p^2+H_{\mathrm{TSV}}^2}-p))}{(\sqrt{p^2+H_{\mathrm{TSV}}^2}-H_{\mathrm{TSV}})(4p+\beta H_{\mathrm{TSV}})}\right]$ | [20] |
| $C_{\mathrm{ox}} = (\varepsilon_0\varepsilon_{ox}/t_{ox})2\pi r_{\mathrm{TSV}} H_{\mathrm{TSV}}$ | [35] |
| $C_{\mathrm{ox}} = \frac{\varepsilon_0\varepsilon_{ox}}{\ln((r_{\mathrm{TSV}}+t_{ox})/r_{\mathrm{TSV}})} 2\pi H_{\mathrm{TSV}}$ | [36] |
| $C = \frac{63.34 H_{\mathrm{TSV}}\varepsilon_0}{\ln(1+5.26 H_{\mathrm{TSV}}/r_{\mathrm{TSV}})}$ | [30] |
| $C_{\mathrm{dep}} = \frac{2\pi H_{\mathrm{TSV}}\varepsilon_0\varepsilon_{si}}{\ln\left((r_{\mathrm{TSV}}+t_{ox}+W_{\mathrm{dep}})/r_{\mathrm{TSV}}\right)\sqrt{1-V/V_{th}}}$ | [22] |
| $C_{\mathrm{dep}} = \frac{2\pi H_{\mathrm{TSV}}\varepsilon_0\varepsilon_{si}}{\ln\left((r_{\mathrm{TSV}}+t_{ox}+W_{\mathrm{dep}})/(r_{\mathrm{TSV}}+t_{ox})\right)}$ | [31] |
| $C_{\mathrm{Si}} = \frac{0.5\pi H_{\mathrm{TSV}}\varepsilon_0\varepsilon_{si}\alpha(8n_{bc}+1)p}{r_{\mathrm{TSV}}\ln((r_{\mathrm{TSV}}+w_{bc})/r_{\mathrm{TSV}})}$ | [22] |
| $C_{\mathrm{Si}} = \varepsilon_0\varepsilon_{si}\frac{0.5p+2r_{\mathrm{TSV}}+\beta_1}{\alpha_1 p} H_{\mathrm{TSV}}$ | [37] |
| $G_{\mathrm{Si}} = \sigma_{si}\frac{0.5p+2r_{\mathrm{TSV}}+\beta_1}{\alpha_1 p} H_{\mathrm{TSV}}$ | [37] |
| $G_{\mathrm{Si}} = \frac{0.5\sigma_{si}(8n_{bc}+1)\pi H_{\mathrm{TSV}}}{(\alpha_1 p/r_{\mathrm{TSV}})\ln((r_{\mathrm{TSV}}+w_{\mathrm{bc}})/r_{\mathrm{TSV}})}$ | [37] |

$H_{\mathrm{TSV}}$ is the height of TSV, and $r_{\mathrm{TSV}}$ is the radius of TSV. $\rho$ represents the electrical resistivity. $r_1$ and $r_2$ are the bottom and top radius of taper TSV, respectively. $\delta$ represents the skin depth. $\mu_0$ is the magnetic conductivity. $\alpha$ represents the fit coefficient. $p$ is the spacing between the TSVs. $\varepsilon_0$, $\varepsilon_{ox}$ and $\varepsilon_{si}$ are the permittivity of vacuum, dielectric constant of oxide layer and dielectric constant of silicon, respectively. $t_{ox}$ is the thickness of oxide layer. $W_{\mathrm{dep}}$ is the width of depletion layer. $V$ is the impressed voltage, and $V_{\mathrm{th}}$ is the threshold voltage. $n_{bc}$ is the coefficient of body contact, and $w_{\mathrm{bc}}$ is the spacing of body contact. $\sigma_{si}$ is the electrical conductivity of silicon.

### *2.2. Numerical Computation Model-Based Design*

Currently, the finite-difference method (FDM) model, finite element method (FEM) model, and finite volume method (FVM) model are the commonly used numerical computation model for 3D integrated systems. Although these numerical computation models are different in solving the electrical simulation performance of TSV, the Maxwell equation is the basic solution mode.

Under the framework of FDM, the problem domain is divided into a difference grid, and the problem domain is replaced by a finite number of network nodes. The FDM is approximately solved by the difference quotient of the function values on the grid nodes through the Taylor series expansion method. It has the advantages of perfect theory, applicable to various precision and easy parallel calculations. The disadvantages are that it is very complicated to deal with irregular areas, and a little mistake will cause a great error. Based on the FDM, Dahl et al. [38] used the rectangular grid to conduct near-field modeling of cylindrical TSV, as shown in Figure 3a. The sparse matrix can be obtained by dispersing Maxwell's equations, and the impedance characteristics of TSV can be accurately further obtained through the sparse matrix. Xie et al. [39] proposed an efficient method for modeling signal paths with TSV in silicon interposer for a 3D integrated system, as shown in Figure 3b. The established model can accurately compute the parasitic effects of multiple transmission lines. Huang et al. [40] established the MOS capacitance model of TSV based on the FDM. The point distribution of the insulation layer and depletion layer can be obtained by only one iteration through the FDM.

The FEM is developed by the variational principle and weighted residual method. The basic strategy for solving the FEM is to divide the problem into a finite number of discretized elements. The appropriate nodes are selected as the interpolation points of the problem function to solve the differential equation in each element. Due to its high precision, the FEM has been widely used in the 3D integrated system. Whether the equivalent circuit model proposed by Kim et al. [21] or the cylindrical mode basis function proposed by Han et al. [41] is used to calculate the electrical characteristics of TSV, the R, C and L equations of TSV derived by Savidis et al. [13] are based on the FEM. The computation results of FEM are used as accurate solutions to validate these models and methods.

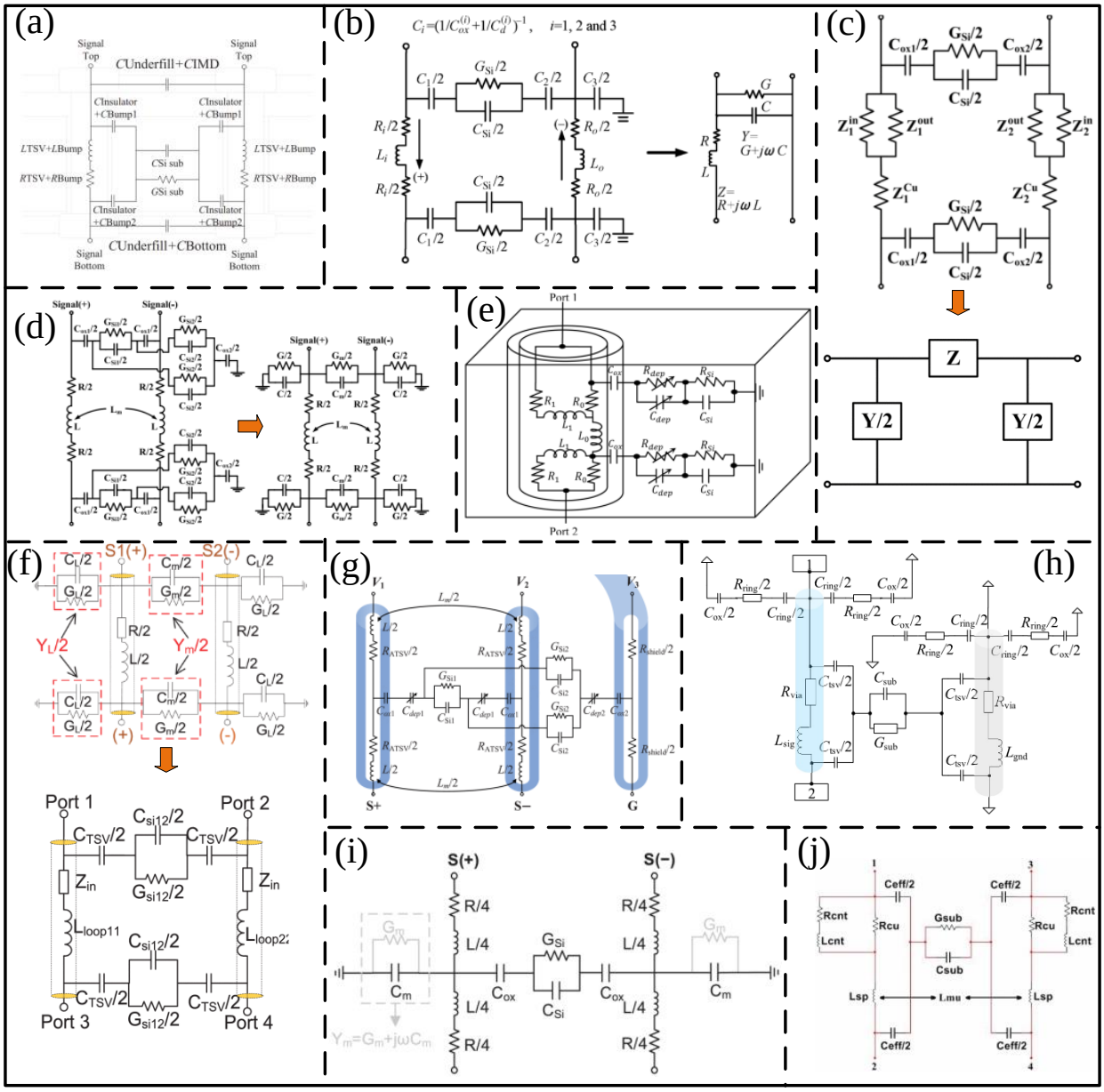



**Figure 2.** (**a**) Equivalent RLGC model of TSVs. (Reprinted from [14], Copyright 2012, with permission from IEEE); (**b**) Equivalent lumped-element circuit model and its simplified transmission-line model of the coaxial-TSV. (Reprinted from [18], Copyright 2011, with permission from IEEE); (**c**) Equivalent circuit model and its simplified model of coaxial annular TSVs. (Reprinted from [19], Copyright 2018, with permission from IEEE); (**d**) Equivalent circuit model and its simplified model of shield differential TSVs. (Reprinted from [21], Copyright 2015, with permission from IEEE); (**e**) The proposed lumped model for a TSV based on a single $\pi$ structure. (Reprinted from [22], Copyright 2011, with permission from IEEE); (**f**) Simplified equivalent circuit model of differential TSVs and Equivalent circuit model of two signal TSVs. (Reprinted from [23], Copyright 2017, with permission from IEEE); (**g**) Equivalent circuit model of the shielded differentia annular TSV. (Reprinted from [24], Copyright 2018, with permission from IEEE); (**h**) Schematic of partial coaxial TSV and its equivalent circuit model. (Reprinted from [25], Copyright 2019, with permission from IEEE); (**i**) Schematic of the differential multibit CNT TSVs and its Equivalent circuit model. (Reprinted from [26], Copyright 2020, with permission from IEEE); (**j**) Equivalent RLGC circuit of CU/SWNTS filled tapered TSVs. (Reprinted from [27], Copyright 2017, with permission from IEEE).

The FVM is used to divide the solution domain into a number of unrelated small volumes and connect them together through grid points. The interpolation function of the FVM is only used to compute the integral of a small volume, which makes it possible to use different interpolation functions for different terms in the differential equation. Based on the FVM, Xie et al. [42] proposed a non-uniform grid to calculate the voltage drop of a 3D power distribution network, as shown in Figure 3c. The effects of temperature on material properties and the relationship between resistivity and position are considered in the differential equation. Xu et al. [43] proposed an electromagnetic field semiconductor coupled solver for the investigation of 3D IC. Under the framework of the solver, the FVM is used to deal with the full wave effects and semiconductor effects of 3D IC.

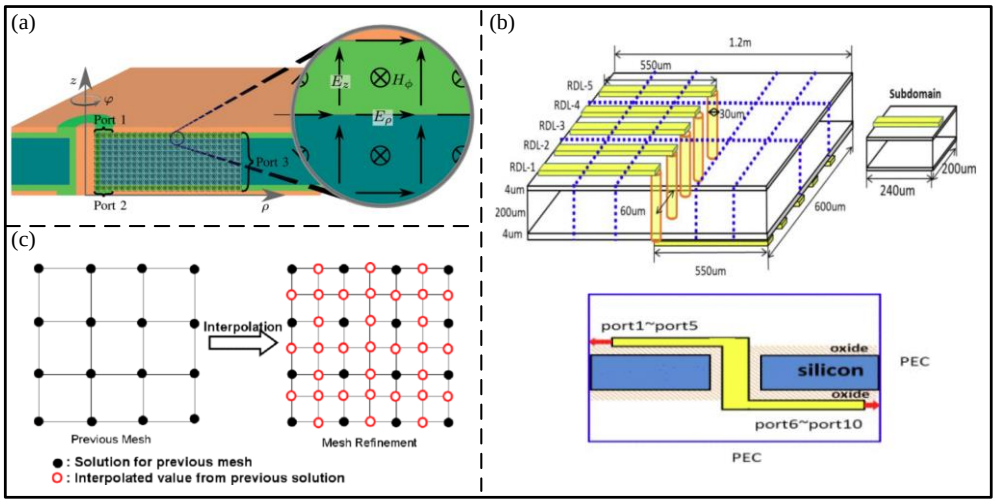



**Figure 3.** (**a**) Cut through the considered structure with finite-difference frequency domain grid for near-field modeling (Reprinted from [37], Copyright 2015, with permission from IEEE); (**b**) Five RDL–TSV–RDL transition structure and the cross-sectional view. (Reprinted from [38], Copyright 2014, with permission from IEEE); (**c**) Mesh refinement and interpolation. (Reprinted from [42], Copyright 2010, with permission from IEEE).

## 3. Thermal Simulation Design of TSV in 3D Integrated System

Because the stacking of multiple chips will increase the power density and reduce the cooling efficiency of the 3D integrated system, the thermal problem of the 3D integrated system becomes extremely serious [44–47]. In the thermal simulation design of TSV in a 3D integrated system, the critical design parameters based on the analytical model or numerical computation model are the design parameters of the TSV structure, the material parameters, the power consumption distribution between different layers, the operating frequency of the devices and circuits and the thermal impedance between chips. In addition, the key performance index for thermal simulation design is the peak temperature. In order to analyze the errors of the analytical model, the results of the analytical model are usually compared with the FEM-based numerical computation model. The path length and thermal resistance of the chips to the heat sink are increased. In addition, the local hot spots are aggregated to form volume hot spots by the stacked power density. With the increase in integration density, the temperature of the integrated system is constantly rising, and the performance, reliability and service life of the integrated system are greatly reduced. In order to predict and control the temperature of the 3D integrated system, the thermal performance of the 3D integrated is investigated and analyzed. The effective cooling method is very significant for the thermal management of 3D integrated systems. Currently, the analytical model and numerical computation model are mainly used to investigate the thermal problem of 3D integrated systems.

### *3.1. Analytical Model-Based Design*

Based on Green's function, Zhan et al. [48] proposed an analytical thermal algorithm for IC, which can compute the steady-state temperature of the whole chip according to different precision requirements. Huang et al. [49] improved the analytical thermal algorithm through generalized integral transformation, which has a faster computation speed than the algorithm derived by Green's function. The flowchart is shown in Figure 4a. The maximum error is 0.3576%. In addition, Jain et al. [50] simplified the 3D integrated system into a 1D thermal resistance model, as shown in Figure 4b. Although the developed method can quickly compute the heat distribution of a 3D integrated system, the temperature measurement of each layer is not particularly accurate. Based on the TSV structure, Pi et al. [51] proposed a simplified calculation method of thermal diffusion resistance, as shown in Figure 4c. The FEM simulation is adopted to verify its accuracy. Based on the thermal resistance model and graph theory, Zhao et al. [52] established an overall multi-modal theoretical model with minimum cost and calculated the optimal layout of TSV through multi-level algorithms, as shown in Figure 4d. Based on the longitudinal heat transfer characteristics of TSV, Ayala et al. [53] established the thermal resistance model in the 3D integrated system. Liu et al. [54] proposed a side thermal resistance model of TSV based on the copper structure and oxide layer, as shown in Figure 4e. Lan et al. [55] established a comprehensive thermal analytic flowchart based on the thermal resistance model and 3D encapsulated network model, as shown in Figure 4f. Although the analytical method is fast in calculation and simple in modeling, its constraint is too strong. Generally, it can solve the steady state and simple 3D thermal model, and its accuracy is relatively poor.

### *3.2. Numerical Computation Model-Based Design*

Compared with the analytical model, the applicability of the numerical computation model is more general. This is because the numerical computation model can accurately solve the thermal problem of each part of the 3D integrated system, and the temperature change over time in the integrated system can also be accurately reflected. However, greater memory consumption and computing time are required. Zhu et al. [56] computed the heat conduction equation by FDM. The temperature matrix is computed by the minimum residual method and symmetric continuous overrelaxation pretreatment. Based on the FDM, Kuo et al. [57] investigated the thermal characteristics of system-level packages TSV. Xie et al. [58] investigated the transient thermal characteristics of the 3D integrated system based on the FEM and non-conformal domain decomposition method, as shown in Figure 5a. Based on the alternating implicit characteristics of unconditional steady-state, Wang et al. [59,60] evaluated the transient thermal characteristics of 3D chips combined with FEM, as shown in Figure 5b.

Due to high simulation accuracy, FEM has been widely used for the computing of 3D integrated systems. Based on the FEM, Fu et al. [61] proposed a triangular layout method of TSV. The thermal dissipation capacity of the TSV array is improved without increasing the occupied area; thus, the thermal performance of a 3D integrated system can be improved. The simulation results show that the average temperature and peak temperature are reduced by 0.22% and 1.69%, respectively, during vertical heat dissipation. The temperature is reduced by 0.10% for lateral heat transfer. Based on the FEM, Hoe et al. [62] improved the thermal conductivity at the connection points by adjusting the physical size of TSV; thus, the thermal performance of the 3D integrated system can be optimized, as shown in Figure 5c. Todri et al. [63] improved the integrity of the power supply and reduced the peak temperature by changing the physical form of TSV. However, this has a very limited impact on the heat dissipation efficiency of 3D integrated systems by improving the physical performance of TSV and its arrangement rule. In order to improve the heat conduction ability between layers and reduce the temperature of hot spots as soon as possible, Chiang et al. [64] proposed the concept of thermal TSV (TTSV). The TTSV is only used for interlayer heat conduction, and the diameter is much larger than the signal TSV. Goplen et al. [65] applied TTSV in 3D IC, as shown in Figure 5d. The TTSV is added to a specific area to adjust the effective thermal conductivity of 3D IC. The simulation results show that the proposed method can reduce the peak temperature by more than 57%.

Singh et al. [66] performed a complete analysis of a single TTSV. When the TTSV is inserted at the hot spot of the chip, its temperature can be reduced by 62 °C. Wang et al. [67] proposed a high-efficiency design method of TSV array for thermal management of a 3D integrated system based on the FEM and equivalent thermal conductivity model. The simulation results show that the thermal distribution of the 3D integrated system is homogeneous. Based on the principle of the thermoelectric effect, Gagan et al. [68] proposed a novel TSV, as shown in Figure 5e. The novel TSV can be used to absorb heat and also serves to transport signals. In addition, Singh et al. [69] improved the heat dissipation performance by using CNT instead of traditional copper. Based on the FEM, Shi et al. [70] increased the thermal conductivity between the layers through combined the micro-channel with the TSV heat dissipation method, as shown in Figure 5f. The experiment results show that the developed method reduced the temperature by about 40% compared with the simple use of TSV, which made a great contribution to promoting the heat dissipation of the 3D integrated system by micro-channel.

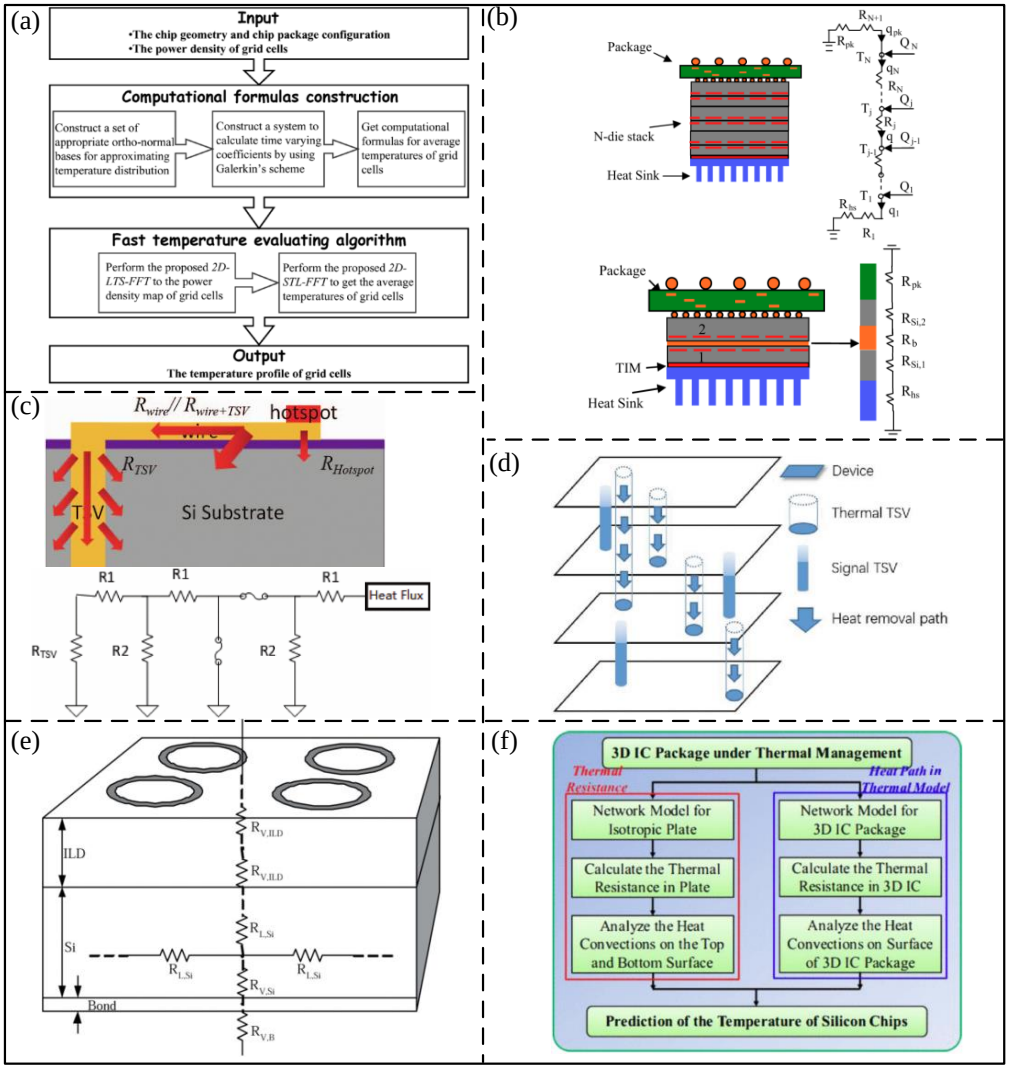



**Figure 4.** (**a**) Executing flow of the proposed generalized integral transform-based thermal simulator. (Reprinted from [49], Copyright 2009, with permission from IEEE); (**b**) Thermal resistance network with multiple heat-generating junctions. (Reprinted from [50], Copyright 2009, with permission from IEEE); (**c**) Equivalent thermal resistance network. (Reprinted from [51], Copyright 2017, with permission from IEEE); (**d**) Heat dissipation path. (Reprinted from [52], Copyright 2018, with permission from IEEE); (**e**) Extending the proposed lateral model into more complicated TSV structures. (Reprinted from [54], Copyright 2014, with permission from IEEE); (**f**) Thermal analytic flowchart based on the thermal resistance model and 3D encapsulated network model. (Reprinted from [55], Copyright 2014, with permission from IEEE).

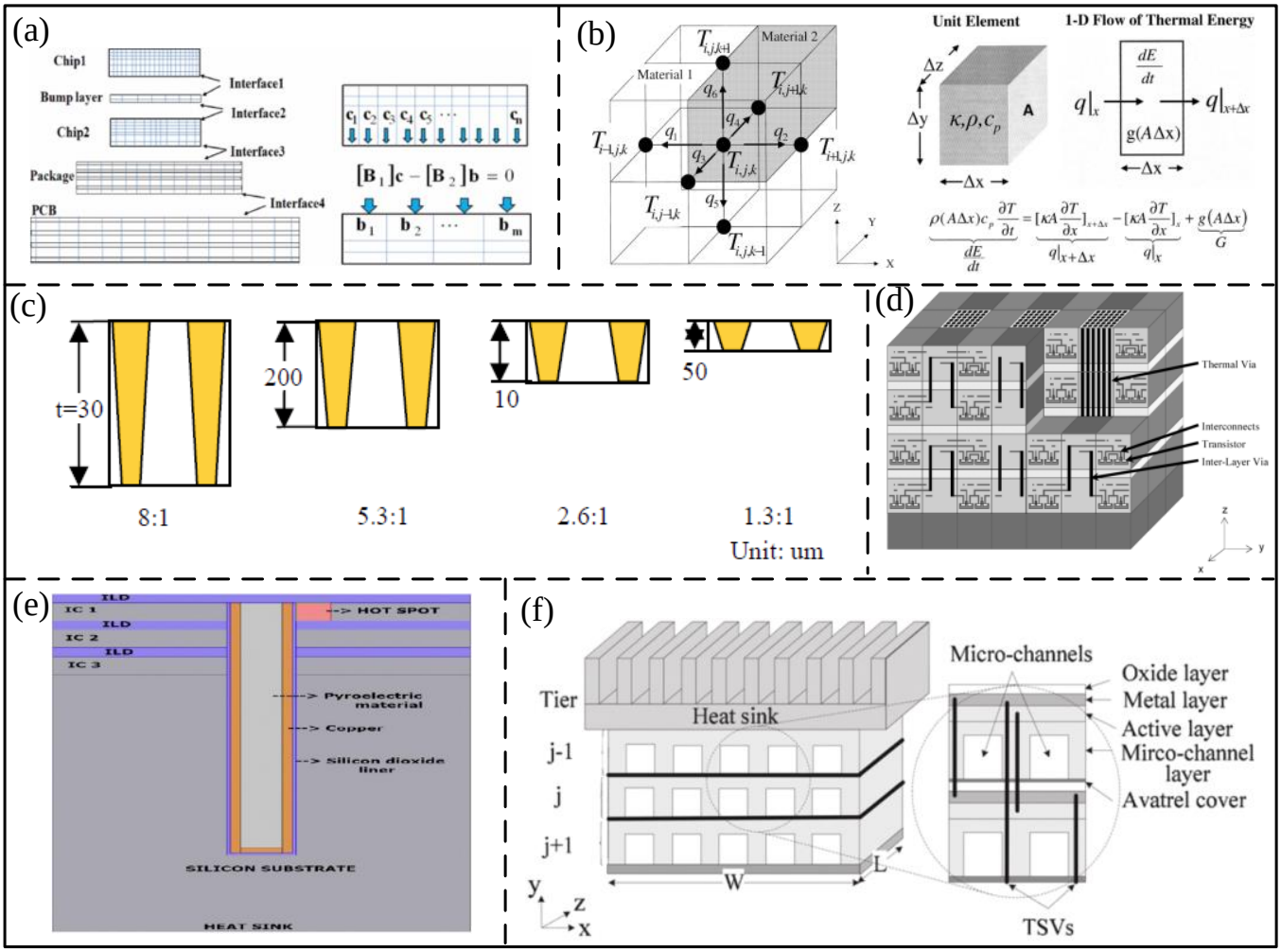



**Figure 5.** (**a**) Non-conformal gridding of 3D system into domains and heat flow continuity illustration. (Reprinted from [58], Copyright 2012, with permission from IEEE); (**b**) Conservation of energy and the heat conduction equation. (Reprinted from [60], Copyright 2003, with permission from IEEE); (**c**) TSV geometry for different aspect ratios. (Reprinted from [62], Copyright 2009, with permission from IEEE); (**d**) Cutaway showing transistors and interconnects based on TSV. (Reprinted from [63], Copyright 2006, with permission from IEEE); (**e**) The schematic of the simulated 3D stack with TTSV (Reprinted from [68], Copyright 2015, with permission from IEEE); (**f**) Stacked 3D integrated system with micro-channels and TSVs. (Reprinted from [70], Copyright 2012, with permission from IEEE).

## 4. Multi-Physics Co-Simulation Design of TSV in 3D Integrated System

The unification of computing, electrical, physical, thermal and reliability aspects of an integrated system is called co-simulation design. Due to the lack of understanding of cross-domain interactions and their impacts on the feasibility region of the architectural design space, the independent optimization and design of each aspect lead to sub-optimal designs. Although the cooperative design strategy is becoming more and more necessary for 3D integrated systems, the high reliability of 3D integrated systems is becoming even more critical. The interlayer coupling with the system architecture and a higher degree of connectivity between components increases the independence between physical design parameters, architectural parameters, performance, hotspot distribution, power and reliability. The embedded TSV greatly influences the former parameters. The 3D integrated system extends the design space by stacking integrated chips in the vertical direction. When the system is operated, the signal input generates Joule heat, which brings various temperatures and affects its electrical parameters, silicon conductivity, thermal conductiv-

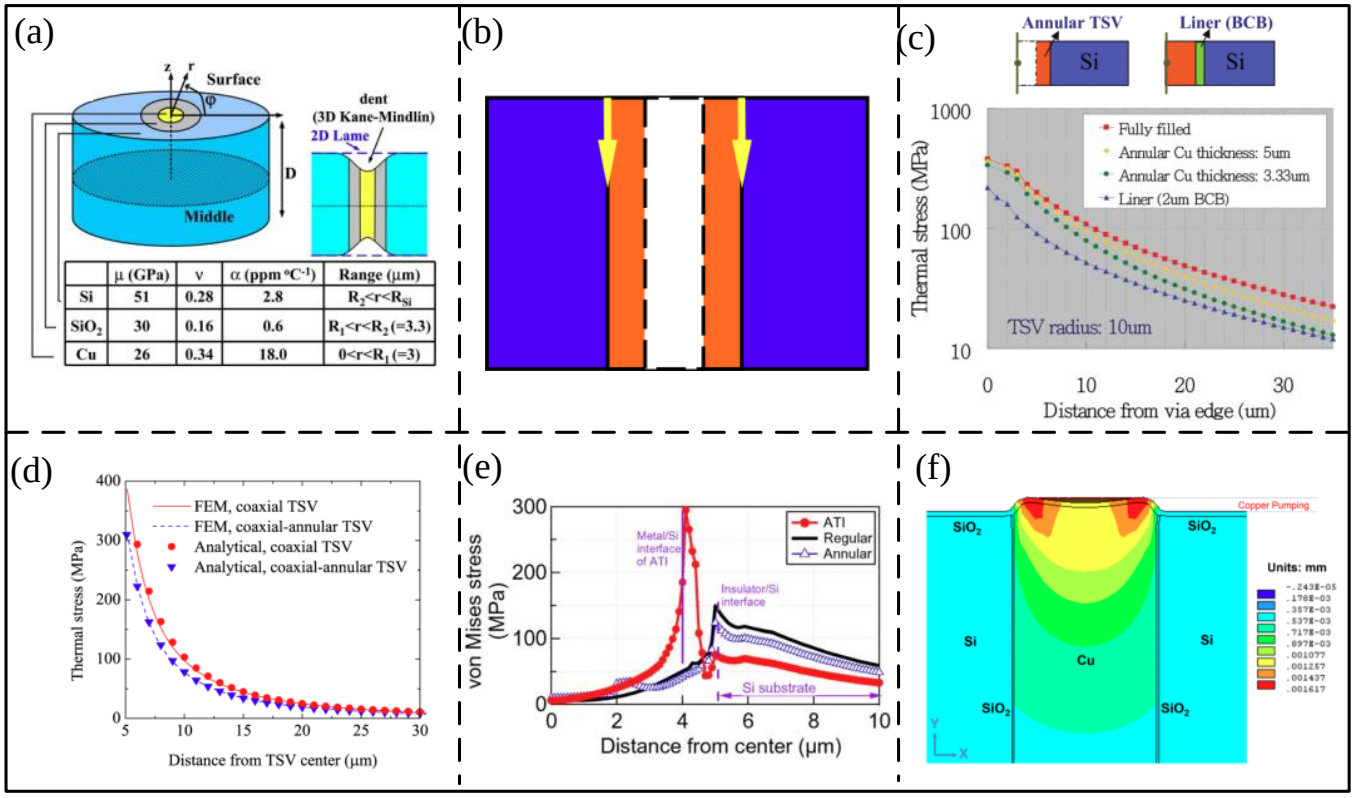
ity, etc. Meantime, due to the differences in CTE between materials, temperature changes generate thermal stress. The band gap width, carrier mobility and electrical parameters can be affected by the thermal stress. Therefore, it is necessary to develop the multi-physics co-simulation design of TSV in a 3D integrated system.

### *4.1. Thermal Stress Coupling Simulation Design*

Because of the difference in CTE between the metal-filled TSV and the materials of the nearby structure, the thermal stress is generated after annealing and other manufacturing processes. Under the effects of thermal stress, the TSV is extruded and leads to the protrusion at both ends of the filled metal and the separation of the filled metal from the side wall. When the thermal stress is too large, the device will be destroyed. The band gap width and carrier mobility can be affected by thermal stress. Based on the reported work, 100 MPa of stress can change more than 7% of carrier mobility. Therefore, it is necessary to investigate the stress distribution evolution of TSV structure under thermal load. The investigation on the thermo-stress properties of TSV-based 3D integrated systems mainly focuses on the establishment of a thermal stress model, stress damage prediction and detection.

Generally, the thermal stress of cylindrical TSV has been investigated in the early stage, and the analytical model of the thermal stress introduced in silicon wafers has been established [71]. As shown in Figure 6a, the TSV is filled with copper, which causes large thermal stress. Then, the thermal stress is optimized based on the various TSV structures. Because the copper ring is used in the annular TSV [72], the thermal stress is much smaller than the cylindrical TSV filled with copper, as shown in Figure 6b. Based on the FEM, Wang et al. [73] proposed an analytical model of strain and stress for annular TSV. The simulation results show that the maximum average errors of strain and stress analytical models are 6.6% and 6.8%, respectively. Based on the FEM and stress analytical method, Lu et al. [74] investigated the thermal stress of TSV interconnect. The stress distribution of a single TSV is investigated by analytical method, and the stress interaction between the TSV arrays is further deduced based on the principle of linear superposition. The stress intensity factor on a radial crack is computed for TSV lines under 175 °C of thermal load. The effects of the TSV pitch on thermal stress are also investigated, as shown in Figure 6c. Due to the complex structure and large radius, the thermal stress problem of coaxial TSV [75] is more serious while improving the electrical characteristics. However, the coaxial annular TSV [76] is combined the superior thermal–mechanical characteristic of the annular TSV with the excellent electrical characteristic of the coaxial TSV, which reduces the thermal stress introduced in the silicon wafer on the premise of ensuring the superior electrical characteristic. The architecture and simulation results are shown in Figure 6d. In addition, Feng et al. [77] proposed an annular trench isolated TSV by adding a layer of silicon annular between the copper and insulation layers. The thermal stress generation point is moved from the boundary of TSV to the boundary of the silicon annular, and the thermal stress in the silicon substrate is reduced, as shown in Figure 6e. Since thermal stress is the main reason for device failure, the investigation of the effect of permutation on failure has a guiding significance for the design of the TSV array. Ryu et al. [78] investigated the effects of thermal stress on carrier mobility and keep-out zone by focusing on the stress characteristics near the surface where the electronics are located. Liu et al. [79] investigated the effect of copper column expansion of TSV on the stress of the redistribution layer, as shown in Figure 6f. The results show that the copper column protrusion tends to occur at the top edge of the TSV orifice under high thermal load, which leads to dielectric layer cracking and interface separation. The further results show that reducing the diameter and height of TSV is beneficial to reduce the influence of stress on the redistribution layer. Dong et al. [80] established a thermal stress analysis model of TSV and investigated the effects of TSV radius, the thickness of Cu diffusion barrier and the material on the thermal stress based on the FEM. The simulation results show that the error between the FEM model and the analysis model is 2%. Dequivre et al. [81] analyzed the TSV model and obtained its stress distribution gradient. The analysis is verified by the X-ray diffraction

experiment, and the results show that the medium layer fracture is the main mechanism of device failure. Based on the internal stress distribution diagram of TSV under different thermal loads by using the electron backscattering diffraction method, Heryanto et al. [82] counted the height of TSV deformation at 250, 300, 350, 400 and 450 °C, which has reference significance for improving the high-temperature process. Based on the micro-infrared photoelasticity system with a thermal loading function, Su et al. [83] analyzed the stress of TSV. Yoo et al. [84] demonstrated the characterization of silicon stress near copper-filled TSV by using high-resolution micro-Raman spectroscopy and investigated the stress changes of TSV with different diameters, depth-to-width ratios and spacing distributions.




| | μ (GPa) | ν | α (ppm °C$^{-1}$) | Range (μm) |
|---|---|---|---|---|
| Si | 51 | 0.28 | 2.8 | $R_2$<r<$R_{Si}$ |
| $SiO_2$ | 30 | 0.16 | 0.6 | $R_1$<r<$R_2$ (=3.3) |
| Cu | 26 | 0.34 | 18.0 | 0<r<$R_1$ (=3) |

**Figure 6.** (**a**) Structure of the TSV filled with different materials, and the dent on TSV surface. (Reprinted from [71], Copyright 2012, with permission from IEEE); (**b**) The structure of annular TSV. (Reprinted from [72], Copyright 2010, with permission from IEEE); (**c**) Thermal stress around TSVs with various structures. (Reprinted from [74], Copyright 2009, with permission from IEEE); (**d**) Comparison of thermal stress results from analytical solution with FEM simulation for coaxial and coaxial annular TSVs. (Reprinted from [76], Copyright 2014, with permission from IEEE); (**e**) The von Mises stress distributions for annular-trench-isolated TSV, regular TSV and annular TSV at 125 °C. (Reprinted from [77], Copyright 2016, with permission from ELSEVIER). (**f**) CTE mismatch-induced stress in the TSV structure. (Reprinted from [79], Copyright 2016, with permission from IEEE).

Based on the different heating rates, Zhao et al. [85] investigated the copper deformation behaviors of TSV, such as the invasion and protrusion of TSV copper. The results of Raman spectrums show that the changes in stress distribution are related to the copper deformation behavior. In the area near the Cu via, Cu protrusion behavior might aggravate the stress in Si obtained from the Raman measurement, while Cu intrusion might alleviate the stress. Based on the FEM, Zhang et al. [86] proposed a general method to predict the thermal distribution and stress distribution of the TSV array in a 3D integrated system. The individual and comprehensive effects of the parameters of the TSV array (TSV height, diameter and spacing etc.) on the thermal and stress of a 3D integrated system are predicted by the proposed method.

The thermal stress reliability of TSV is the main factor of device failure. Due to the large difference in the CTE between materials, the thermal stress is relatively high. Therefore, the effective way to reduce the thermal stress of a 3D integrated system is reducing the difference of CTE between materials to achieve the improvement of reliability.

### *4.2. Electro-Thermal Coupling Simulation Design*

With the increase of integration density, the self-heating effect of interconnect has become an inevitable problem in 3D integrated systems. Therefore, a unified, standardized and systematic study on the electro-thermal coupling problem of TSV in a 3D integrated system was conducted. Wang et al. [87] investigated the effects of temperature on the parasitic resistance and capacitance of TSV through combined the properties of copper with the equivalent circuit model. Subsequently, Zhao et al. [88] extended the theory to coaxial TSV on this basis and analyzed the parasitic effect in detail. In addition, Katti et al. [89] verified the effects of temperature on TSV parasitic parameters based on experiments, and the results are shown in Figure 7a. Wang et al. [90] analyzed the thermal distribution and electric field distribution based on the FEM, and the electro-thermal characteristic is investigated by changing the amplitude of voltage and the thickness of the TSV oxide layer, as shown in Figure 7b. Based on the FEM, Lu et al. [91–93] investigated the influence of steady-state temperature distribution, DC voltage drop and high-frequency S parameter in electro-thermal coupling TSV array and power transmission networks. The instantaneous process is obtained, as shown in Figure 7c. Sai et al. [94] established a nonlinear electro-thermal delay model to investigate the TSV-based 3D integrated system, as shown in Figure 7d. The concept of virtual TSV is proposed to balance the temperature and stress gradient, and it is demonstrated that the clock shift is reduced by an average of 61.3% based on the proposed model. Based on the principle of heat–electricity analogy, Jiang et al. [95] analogized thermal to electrical to realize the steady-state thermal analysis of large-scale interconnect structures by using electrical simulation software, as shown in Figure 7e. In addition, the advantages and limitations of the analytical model, FDM, FEM and FVM are presented in Table 3.

**Table 3.** Advantages and limitations of analytical model, FDM, FEM and FVM.

| Models | Advantages | Limitations |
| --- | --- | --- |
| Analytical model | Simple and easy;<br>Low computational complexity;<br>High computing efficiency. | Limited parameters for analysis;<br>Low precision. |
| FDM | Theoretical perfection;<br>Applicable to various accuracies;<br>Easy to compute in parallel. | Complicated dealing with irregular areas;<br>Poor adaptability to grids. |
| FEM | High precision;<br>Multiple parameters for analysis;<br>Easier to handle irregular areas;<br>Easy to compute boundaries;<br>Good adaptability to grids. | Low computing efficiency;<br>High computational complexity;<br>High computational memory consumption. |
| FVM | Good conservativeness;<br>Good adaptability to grids. | Complicated computing boundary;<br>High computational memory consumption;<br>Low simulation efficiency. |

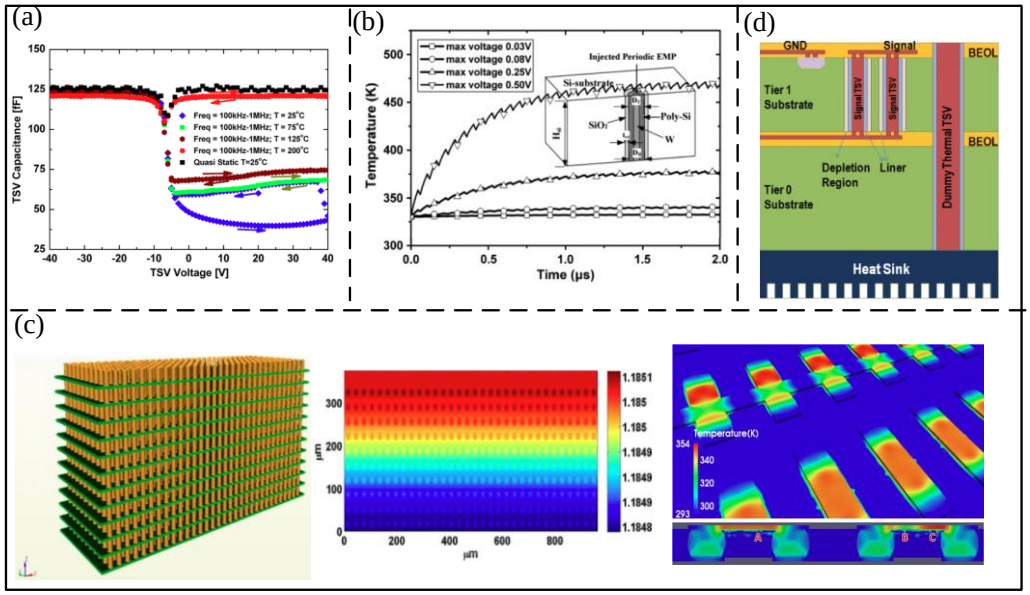



**Figure 7.** (**a**) C−V characteristics of TSV at higher operating temperatures. (Reprinted from [86], Copyright 2011, with permission from IEEE); (**b**) Transient temperature responses of two single-layered H-shaped TSVs with a trapezoidal voltage pulse applied. (Reprinted from [87], Copyright 2010, with permission from IEEE); (**c**) The 3D structure, DC voltage drop and temperature distribution of TSV. (Reprinted from [88–90], Copyright 2014, with permission from IEEE); (**d**) Signal TSV in 3D IC and the virtual TSV. (Reprinted from [91], Copyright 2013, with permission from IEEE).

## 5. Conclusions

The development and progress of multi-physics simulation design for TSV-based 3D integrated systems are reviewed in this paper. The highly reliable 3D integrated system is required to consider the electricity, thermal, stress and multi-physics coupling during the design and fabrication. With the development of 3D integrated systems, the application and innovation in many fields have made great progress, and the 3D integrated technology platforms with their own characteristics have been formed. The future development and perspectives of the 3D integrated system are summarized as follows:

(1) Advanced integrated microsystems. The 3D integrated technology of imaging sensing is based on the route of imaging sensing chip and CMOS chip integration, using high-density TSV or inter-chip bonding technology, which lays a technical foundation for the development of computational and intelligent imaging in the future. The RF 3D integrated system has been widely applied in aerospace, aviation, ships, weapons, information technology, biology, medicine, industrial control, consumer electronics, etc. In addition, the Chiplet-based 3D integration technologies will be widely used in high-performance computing systems, high-reliability MEMS systems, mass memory systems, etc.

(2) Crossed and reconfigurable architecture design technology. The 3D heterogeneous integration of the microsystem is focused on system-level packaging, and the crossed design from system to package is also required. In addition, the cost and lifetime of 3D wiring, multi-domain and multi-tools interactions are need to addressed for high-reliability 3D integrated microsystems. The reconfigurable technology can effectively improve the utilization efficiency of Chips and then improve the utilization range of 3D integrated microsystems. With the product development cycles continuing to shorten, collaborative design across multiple disciplines and domains such as circuit, structure, process and thermal design is required to achieve the 3D heterogeneous integrated microsystems.

(3) Standardized and intelligent design technology. Standardized and intelligence are the design direction of 3D integrated microsystems. The standardized interconnec-

tion protocols can achieve the normalization and modularization of circuits in 3D integrated microsystems. In addition, intelligence refers to the application of the system to more scenarios and environments so that the degree of autonomy of the system is greatly enhanced. The application field of the system is significantly expanded, and the continuous innovation of the platform is promoted. Moreover, the intelligent optimization method can be used to improve the design efficiency of a 3D integrated system.

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