symmetry

MDPI

Article

Research on Establishment and Application of Digital Twin for a Phase-Shift Full-Bridge Current Doubling Rectifier Converter

Guihua Liu *, Xinyang Wang, Mingyi Wang and Wei Wang

School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China
* Correspondence: liuguihua@hit.edu.cn

Abstract: In order to improve the safety and reliability of airborne power supply and distribution system, a digital twin of a phase-shift full-bridge current doubling rectifier converter based on gallium nitride metal-oxide-semiconductor field-effect transistor (GaN MOSFET) is built. The digital twin can be regarded as virtual symmetry of the real converter. The particle swarm optimization (PSO) algorithm is applied to compare the voltage and current waveforms of the real converter with relative waveforms of its digital model established in simulation software, and the interior parameters of the model are constantly updated until the waveforms of the digital twin coincide with that of the converter. Applications of this digital twin are discussed through experimental verification, and the results show that the digital twin can deduce the parameter value of key components of the converter in the case of soft faults. In the case of hard faults, a back propagating artificial neural net (BP ANN) is trained by data collected from the digital twin, and the BP ANN is able to identify different running states of the converter. The outcomes of this paper present a non-intrusive and high real-time method of condition monitoring and fault diagnosis, which is beneficial to improve the reliability of airborne HVDC power supply system.

Keywords: digital twin; converter; GaN MOSFET; PSO algorithm; condition monitoring

check for updates

Citation: Liu, G.; Wang, X.; Wang, M.; Wang, W. Research on Establishment and Application of Digital Twin for a Phase-Shift Full-Bridge Current Doubling Rectifier Converter. *Symmetry* **2023**, *15*, 292. https://doi.org/10.3390/sym15020292

Academic Editor: Dumitru Baleanu

Received: 4 December 2022
Revised: 12 January 2023
Accepted: 17 January 2023
Published: 20 January 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

With the advance of research on the more-electric aircraft (MEA) and the all-electric aircraft (AEA), the electrification level of aircrafts has been constantly improving. The main architectures of onboard power supply systems in MEAs and AEAs include low voltage direct current (LVDC), variable frequency alternating current (AC), constant frequency AC as well as high voltage direct current (HVDC). Because of its large capacity, light weight, high efficiency, and high reliability, HVDC becomes the most promising structure of airborne power supply systems. In order to promote the application of HVDC in the power supply and distribution systems of aircrafts, a robust and reliable method of condition monitoring and fault diagnosis is required to prevent the loss of propulsion and critical flight functions due to power failures. In the future, as the complexity of airborne power supply and distribution systems increase, the fault types will also increase, and it would be a great challenge to carry out panoramic analysis and simulation in the whole life-cycle.

The architecture of the airborne HVDC power supply system is shown in Figure 1 [1]. The alternating current generated by generators is rectified by AC-DC converters and conveyed to the HVDC bus, which is connected to the LVDC bus by DC-DC converters. HVDC loads are powered directly by HVDC buses while a few AC loads are powered by HVDC buses through DC-AC inverters. Research on the control strategy of these power electronic converters is nearly mature. For example, with regard to the AC-DC rectifier, Reference [2] proposed a model predictive control strategy to predict supply current of the rectifier; in [3], an improved harmonic suppression control strategy is put forward to reduce the harmonic distortion of the rectifier and in [4], disturbance observer-based finite-time control is proposed to estimate the disturbance of the rectifier. In the field of

the DC-AC inverter, a nonlinear control method is raised in [5], while in reference [6], a virtual oscillator control is promoted, with both strategies improving the performance of the inverter. As for the DC-DC converter in [7], several advanced control strategies are put forward and discussed under various application requirements to seek the best control method. However, there is still much room for improvement in condition monitoring and fault diagnosis of the power electronical converters.

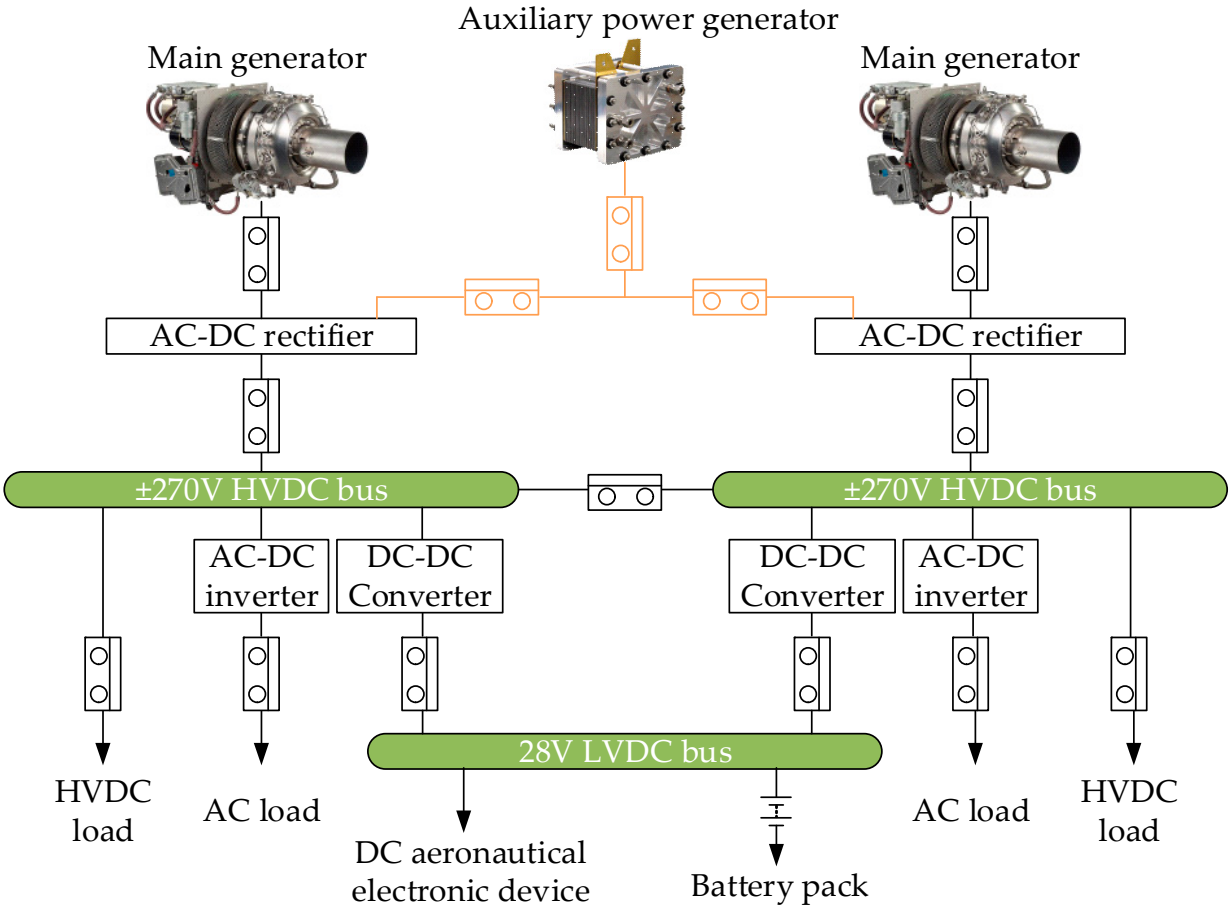


Figure 1. Architecture of airborne HVDC power supply system.

The common voltage level of the airborne HVDC bus is 270 V, while nominal voltage of power loads onboard is mostly 28 V. The DC-DC converter connects the two buses and converts 270 V DC to 28 V DC, which is required by electrical equipment, with its performance directly affecting the safety of the aircraft. Therefore, the DC-DC converter plays a significant role in the onboard power supply and distribution system, and therefore, implementing its effective condition monitoring would be an important breakthrough point of enhancing the robustness of the airborne HVDC system.

Traditional condition monitoring methods of the power electronic system can be divided into the component-level and the system-level. Component-level methods mainly focus on the power semiconductors [8] and capacitors [9], which require additional circuits to measure the electrical and thermal indicators. These methods will increase the complexity of the system, and the failure of additional circuits might cause the failure of the monitored system. System level methods focus on the frequency response [10] and harmonics [11] of the system, which require invasive setups to detect and analyse system signals. These methods require additional setups, and lack the sensitivity during the degeneration of components.

Recently, digital twin (DT) has attracted the attention of researchers as a new condition monitoring method. A digital twin is a virtual replica of the physical equipment, which can

self-update through data interaction with the physical world, in order to reflect the running states of the corresponding devices on the whole life. Digital twin technology integrates artificial intelligence, machine learning, and sensor technology to create a model that can be updated in real time, underlying the process of condition monitoring and decision making. Thus, combining digital twin technology with health condition monitoring and fault diagnosis of power electronic systems would be a significant breakthrough to improve the reliability of onboard HVDC systems.

In the field of electrical engineering, digital twin has been applied to microgrid security [12], aerospace integrated vehicle health management (IVHM) [13], fault diagnosis in distributed photovoltaic systems [14], as well as state estimation for inverter dominated grid [15], etc. Specific to power electronics, in [16], the author proposed a digital twin for modular multilevel converter (MMC) based on real-time simulation (RTS), but, as a method of semi-physical simulation, requires multiple hardware-in-the-loop (HIL) units, so the cost is high. In [17], a digital twin for SiC MOSFET power-electronics switching cells is presented to improve printed circuit board (PCB) layout, however, modelling techniques with higher accuracy and standardization are still demanded. Both [18] and [19] put forward embeddable digital twins for power electronic converters, with the former being based on dynamic neural networks, which has the drawback of high computational expense, and the latter defines the digital twin as a real-time, probabilistic simulation model with stochastic random variables, and applies it to diagnostic analysis of converters. With that said, there exists a contradiction between the complexity and fidelity of the model.

Latest works have proposed simpler methods of establishing a digital twin for power electronic converters, and applied the digital twin in parameter identification as well as condition monitoring. In [20,21], an estimation method for health indicators of a converter is presented and is verified on a buck converter. The PSO algorithm is utilized to analyse and compare experimental data from a digital twin and real converter, in order to update the estimated value of each of the health indicators of the buck converter. The experiment is conducted under different conditions, in order to simulate the degradation trend of key components in the converter. In [22], the author builds the digital twin from a single-phase DC/AC inverter with same method and applies it to detect the degeneration of the filter capacitor. In [23], the digital twin of a two-phase interleaved boost converter is built, and the Genetic Algorithm (GA) is compared with the PSO algorithm in the process of optimization, the result of which shows that GA has a better convergence rate. However, methods, above all, require mathematical modelling of the converter, which means complex state analysis should be done and a large number of differential equations have to be solved, Therefore, in sophisticated systems, the precision and practicability of this method might be lower. To solve the problem, in [24], the method is promoted, and the model of the digital twin is based on simulation software rather than mathematical model, and this method is validated on a buck converter. In [25], a digital twin of the boost converter, based on simulation, is built and Bayesian optimization is used to update parameters. In [26], the arithmetic optimization algorithm (AOA) is applied in the digital-twin-based identification of degradation parameters for a buck converter, compared to the PSO algorithm, with AOA having a better global search ability and faster convergence on this issue.

In this paper, we promote a digital twin for a phase-shift full-bridge current doubling rectifier DC-DC converter based on GaN MOSFET, and discuss its application in condition monitoring. The digital twin has the following characteristics:

(1) The digital twin can accurately reflect the internal structure and external performance of the real converter.

(2) The digital twin can deduce the internal parameters and status of the converter by analysing its external behaviours, so non-invasive condition monitoring can be implemented.

Compared to traditional methods, on the one hand, the utilization of a digital twin upon monitoring the converter can avoid invasive tests or extra hardware, thereby reducing the complexity and cost of product testing. On the other hand, running data can be collected from the digital twin rather than the real converter, so there's no need to put on damaging

experiments. For airborne DC-DC converters, the application of a digital twin lays a foundation for fault diagnosis, auxiliary decision-making, and intelligent control of the DC microgrid onboard, improving the safety of the whole flight system.

The rest of this paper is organized as follows. The construction method of the proposed digital twin is established in Section 2. The test results of the digital twin are presented in Section 3. The application of the digital twin in condition monitoring, including soft faults and hard faults, is discussed in Section 4. Finally, the conclusion is presented in Section 5.

2. Establishment of Digital Twin

Figure 2 shows the three-layer digital twin model, including the physical layer, digital layer, and computational layer. A sensor is used for collecting running data from the physical layer, a solver is used for solving the simulation model in the digital layer, and database is used for gathering data generated by all three layers.

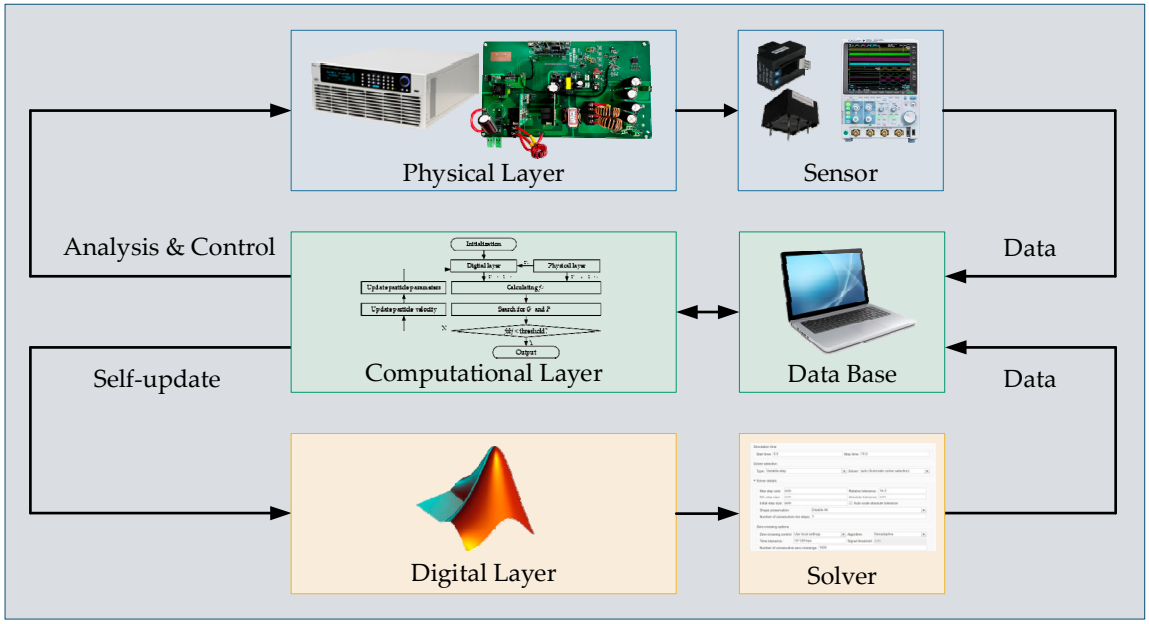


Figure 2. Schematic diagram of the three-layer digital twin model.

As shown in Figure 2, the physical layer is the phase-shift full-bridge current doubling rectifier DC-DC converter. The digital layer is a digital copy of the physical layer, which refers to a converter with the same structure built in the simulation software. The computational layer is the bridge between the physical layer and digital layer. In the computational layer, running data collected from the other two layers is comprehensively analyzed, with the analysis results driving the digital layer to update itself, while the condition of the physical layer is disclosed, and the related control method is proposed. The establishment of these three layers is described in detail as follows.

2.1. Physical Layer

The main technical indicators of the phase-shift full-bridge current doubling rectifier DC-DC converter are shown in Table 1. The converter is designed based on these indicators.

Table 1. Technical indicators of the converter.

Parameter	Indicators	Parameter	Indicators
V_{in}	270 V (250 V–280 V)	Maximum V_{in} ripple	6 V
V_{out}	28 V (22 V–29 V)	Maximum V_{out} ripple	1.5 V
P_o	1 kW	f_t	200 kHz

Figure 3 shows the topology and the control strategy of the converter, while the value of key components is listed in Table 2. The primary side of the converter is a phase shift full bridge, where the MOSFET gate drive signals on the same bridge arm are complementary, and the duty ratio is 50%. There is a phase-shift angle between the gate drive signals of the MOSFET on different bridge arms, and the output voltage can be controlled by adjusting the phase-shift angle. Due to its simple and controllable dynamic characteristics, as well as high precision output voltage control, peak-current control is selected to generate the pulse width modulation (PWM) waveform for driving the MOSFETs. A digital signal processing (DSP) chip is applied to implement the control strategy, where the digital compensator is realized by the control code, and a 2-pole 2-zero (2P2Z) compensator is chosen. the voltage of sampling and reference voltage to the compensator are input, allowing the reference value of the peak current to be generated through calculation, in order to realize the peak-current control. The PWM waveforms of the phase-shift control are shown in Figure 4.

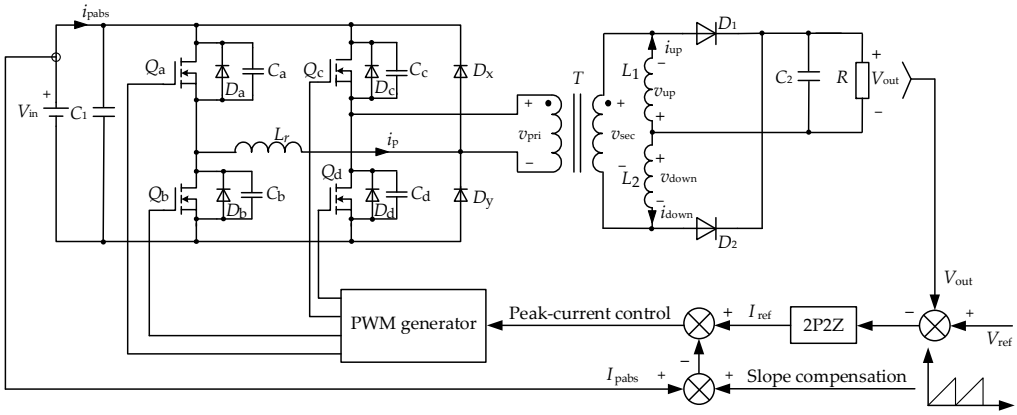


Figure 3. Topology and control strategy of the DC-DC converter.

Table 2. Key parameters of the DC-DC converter.

Parameter	Value	Parameter	Value
C_1	100 µF	L_r	5 µH
C_2	684 µF	L_1, L_2	47 µH
C_a, C_b, C_c, C_d	150 pF	R	>0.7 Ω [1]

[1] The follow-up experiments are conducted under a relatively low power, where load resistance is set to 5 Ω.

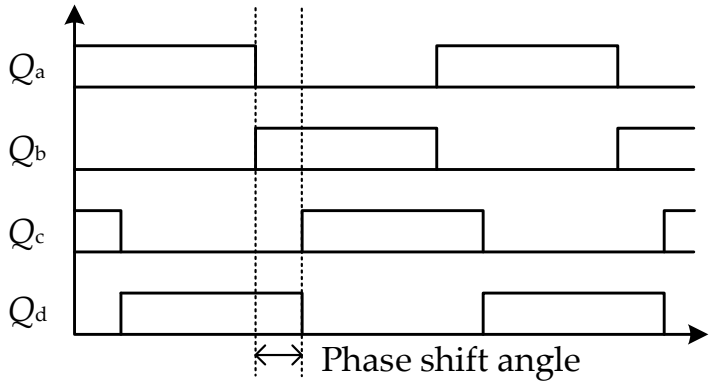


Figure 4. Schematic diagram of PWM waveform of the phase-shift control.

As a third generation semiconductor material, GaN is of a wide bandgap, with a high thermal conductivity, and has good chemical stability, thereby having the characteristics of high operating temperature, high breakdown voltage, as well as strong anti-radiation

ability [27]. Thus, GaN MOSFET is chosen as the switch on the primary side of the converter. The hardware experimental platform is shown in Figure 5.

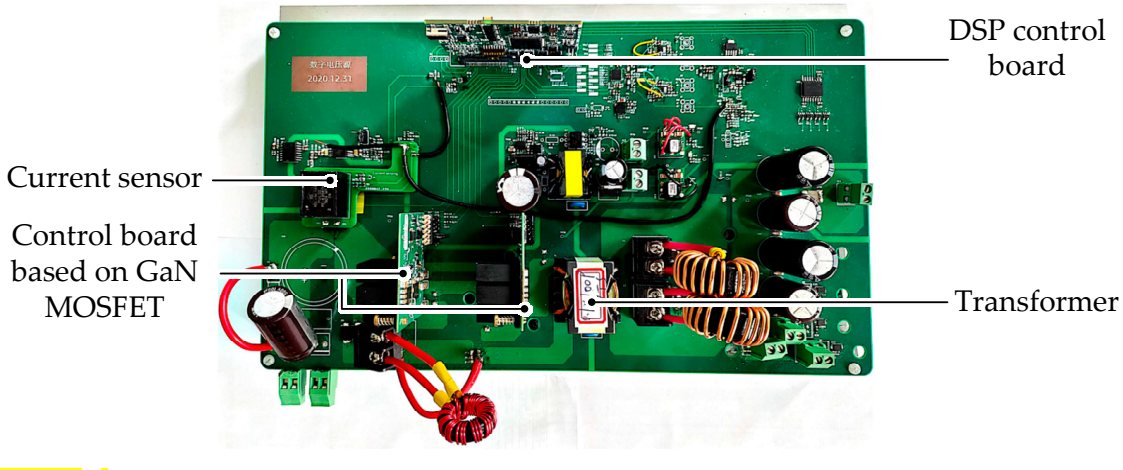
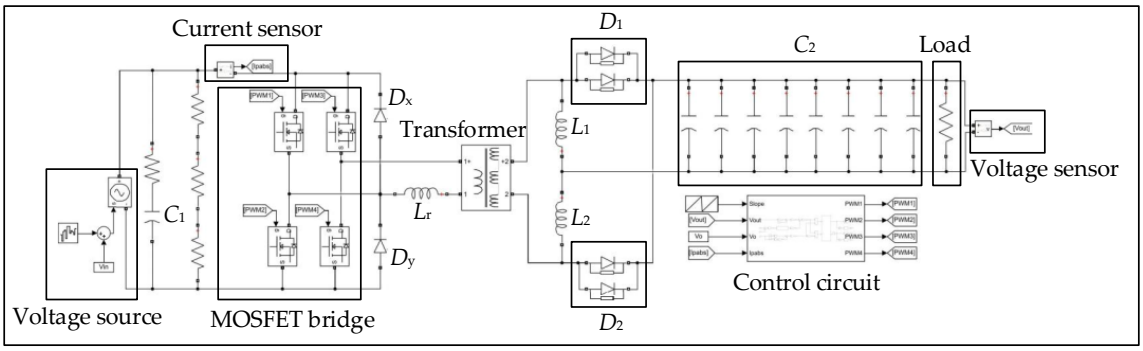


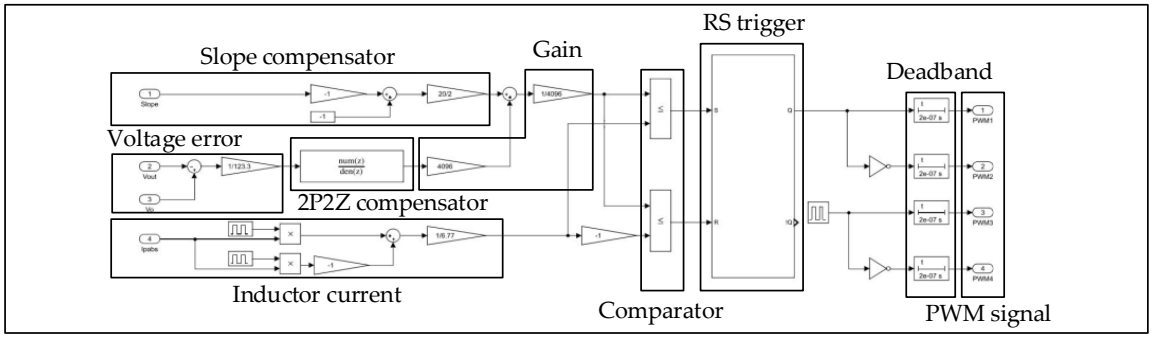
Figure 5. Hardware experimental platform of the converter.

2.2. Digital Layer

In the digital layer, the digital model of the phase-shift full-bridge current doubling rectifier converter is built in the simulation software as a virtual copy of the physical layer. The digital layer has the same structure, control strategy, and technical indicators as the physical layer. Figure 6 shows the digital model of the converter.



(**a**)



(**b**)

Figure 6. Digital model of the converter. (**a**) The main circuit; (**b**) The control circuit.

As shown in the Figure 6, the digital layer is divided into two parts: the main circuit and the control circuit. The main circuit corresponds to the main circuit of the converter in the physical layer, and the control circuit corresponds to the DSP chip. The control circuit includes gain modules that correspond to the 12-bit ADC module, comparators that correspond to the comparator subsystem (CMPSS) module, as well as a reset-set (RS) trigger that corresponds to the enhanced pulse width modulator (ePWM) module. To ensure accuracy, the 2P2Z compensator is adopted with the same coefficients as the physical layer.

2.3. Computational Layer

The computational layer is the pivot of the digital twin, connecting the physical layer and the digital layer. The goal of the computational layer is to make the output data of the digital layer and the physical layer as consistent as possible, so that the resistance, inductance, and capacitance values of the devices in the digital layer can approach the actual condition. The PSO algorithm is applied to realize this goal. It is an evolutionary algorithm that originates from the study of bird predation behavior. Its basic idea is to find the optimal solution through the cooperation and information sharing among individuals in the group. In this paper, a parameter set of devices in the digital layer is regarded as a particle, and a group of particles are initialized with random parameter values (the resistance, capacitance, and inductance value of each device in the circuit) as a population. The difference between the output waveform of the digital layer and physical layer is taken as the objective function. The objective function is used for evaluating each particle in the population, with the particle with the smallest objective function value is regarded as the optimal particle, which refers to the global optimal solution. If the value of the objective function is lower than the threshold, then the parameter set represented by the optimal particle will be output. Otherwise, each particle in the population will self-update according to the global optimal solution shared by the whole population and the current individual optimal solution found by the particle itself. The updated population will keep repeating the above process until the specified number of iterations is reached or the objective function is below the threshold. At that time, the parameter value of the digital layer corresponding to the global optimal particle is very close to the actual value in the physical system. Consequently, the digital twin can be used to indicate the actual condition of the converter in the physical world.

In the computational layer, the waveform signals from the physical layer and digital layer are collected and processed. A total of 25 points are sampled at equal intervals in each period during the steady-state. Three consecutive periods are investigated in order to avoid the possible influence of special circumstances on the calculation results. The objective function is calculated according to the difference between the sampling points. The formula is as follows:

$$f_{\mathrm{obj}} = \frac{\sum_{k=1}^{N}\left\{\sum\left[p\cdot\left(v_{\mathrm{physical,k}}-v_{\mathrm{digital,k}}\right)^2\right]+\sum\left[p\cdot\left(i_{\mathrm{physical,k}}-i_{\mathrm{digital,k}}\right)^2\right]\right\}}{N} \tag{1}$$

where, N is the total number of sampling points, in this paper, the value of N is 75, k is the serial number of sampling points, and p is the weight factor of each term. v_{physical} and v_{digital} refer to voltage data collected from the physical layer and the digital layer, respectively, while i_{physical} and i_{digital} refer to current data collected from the physical layer and the digital layer, respectively. It is worth noting that the voltage and current values in the formula should be normalized due to the different values.

The global optimal particle G_{b} and individual optimal particle P_{b} are selected according to the result of the objective function, then the renewal process of particles is conducted on the basis of Formulas (2) and (3):

$$v_{\mathrm{i+1,j,d}} = w\cdot v_{\mathrm{i,j,d}} + c_1\cdot r_1\cdot\left(G_{\mathrm{b,d}}-P_{\mathrm{i,j,d}}\right)+c_2\cdot r_2\cdot\left(P_{\mathrm{b,j,d}}-P_{\mathrm{i,j,d}}\right) \tag{2}$$

$$P_{i+1,j,d} = P_{i,j,d} + v_{i+1,j,d} \quad (3)$$

where, v is the particle velocity, i, j, and d refer to number of iterations, serial number of particles, and serial number of device parameters, respectively. r_1 and r_2 are random numbers between 0 and 1, c_1 and c_2 are the social weighting factor and individual weighting factor, while w refers to the learning factor, which is related to the global and local search ability [28]. All the learning factors and the weighting factors are empirical values. In this paper, w is set to 0.6, and c_1 and c_2 are both set to 1.5. Once the number of iterations reaches the maximum value, or f_{obj} is below the threshold value, then the algorithm is terminated and the optimal parameter set is output. Figure 7 shows the algorithm flow chart of the computational layer.

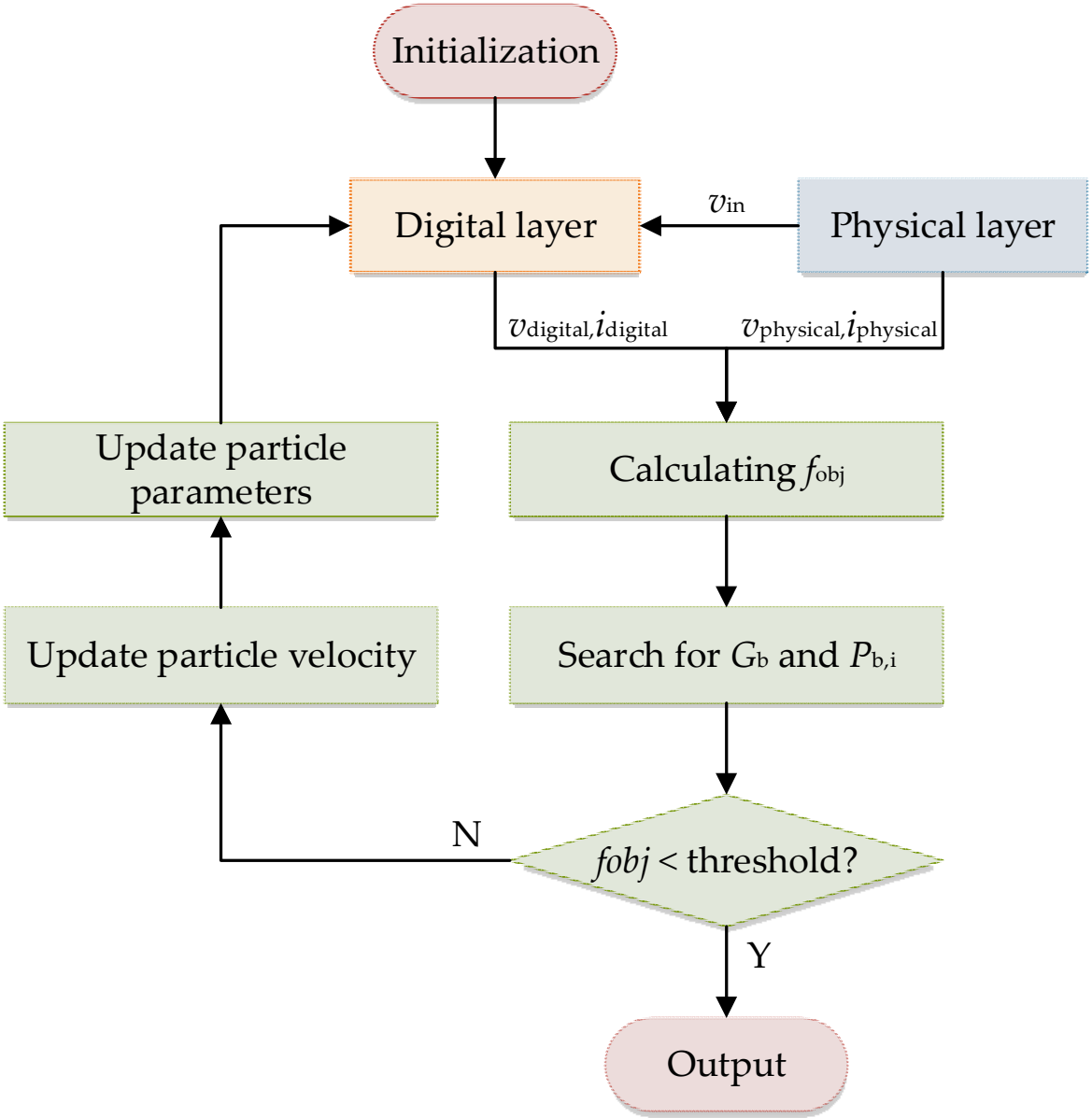


Figure 7. Algorithm flow chart of computational layer.

3. Experiment of Digital Twin

Firstly, voltage and current waveform data during the steady state is collected from the DC-DC converter in the physical layer, using sensor. The waveforms are shown in Figure 8.

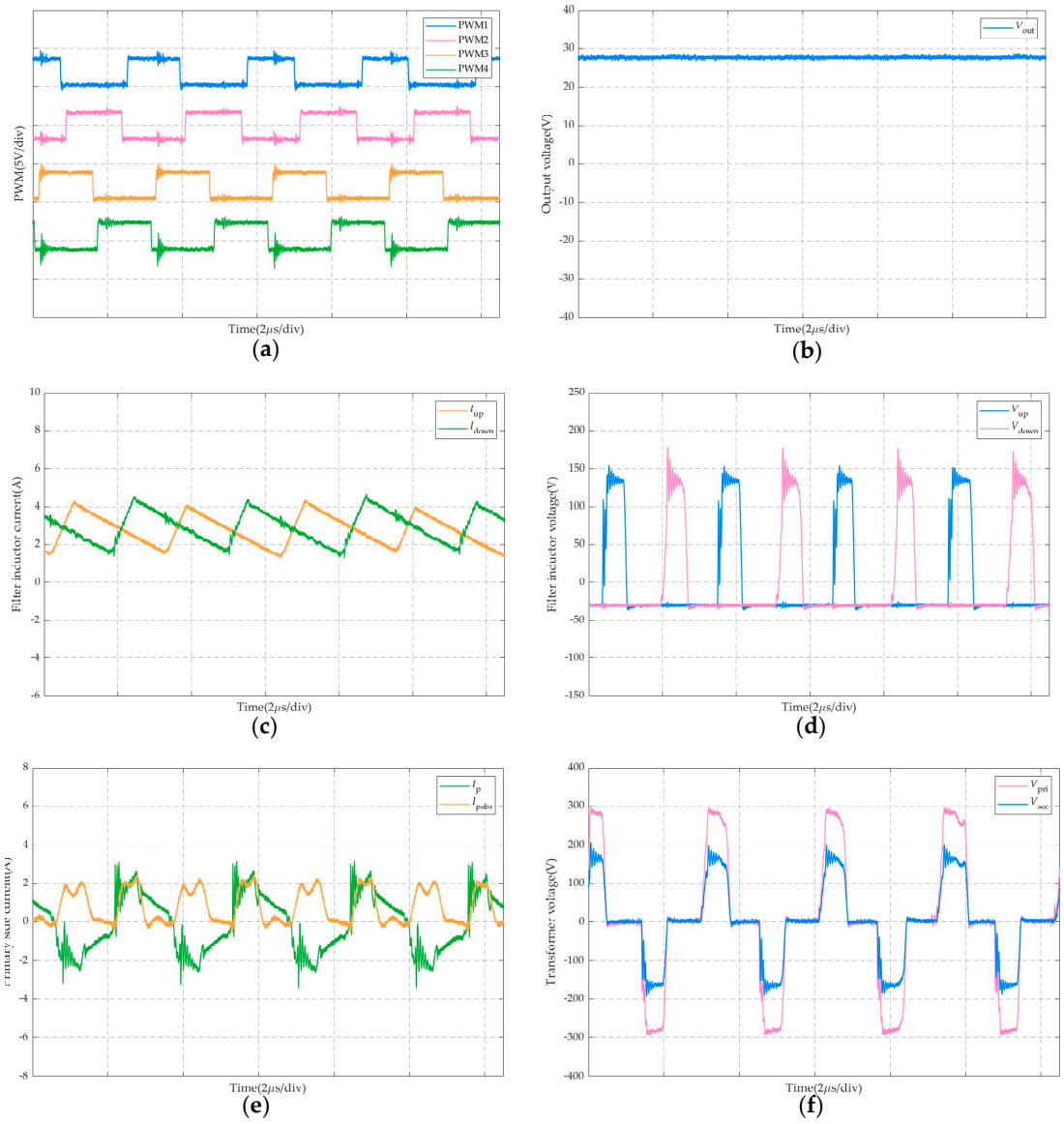


Figure 8. Voltage and current waveforms collected from the physical layer. (**a**) PWM waveforms; (**b**) Output voltage waveform; (**c**) Secondary side current waveforms; (**d**) Secondary side voltage waveforms; (**e**) Primary side current waveforms; (**f**) Transformer voltage waveforms.

Secondly, the data is processed by extracting data points from the waveforms above. Meanwhile, the converter model in the digital layer is set to output the same number of data points from corresponding waveforms, during the steady state.

Finally, data collected from both the physical layer and digital layer is imported to the computational layer. The population size is set to 24 and the maximum number of iterations to 100, then the code of the algorithm mentioned in Section 2.3 is run. The result is shown below.

Figure 9 shows the process of decline of the objective function. As shown in Figure 9, as the number of iterations increases, f_{obj} reduces exponentially. After nearly 80 iterations, the value of f_{obj} tends to be stable, and remains at a very low value. At that time, the difference between the output waveforms at the physical and digital layers has reached the minimal level. The main voltage and current waveforms of the digital layer and the physical layer under steady state are compared, with part of the results demonstrated in Figure 10.

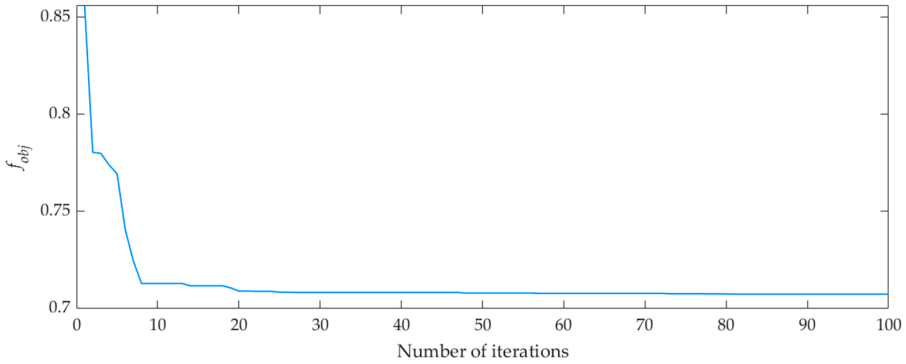


Figure 9. Iterative process of the objective function.

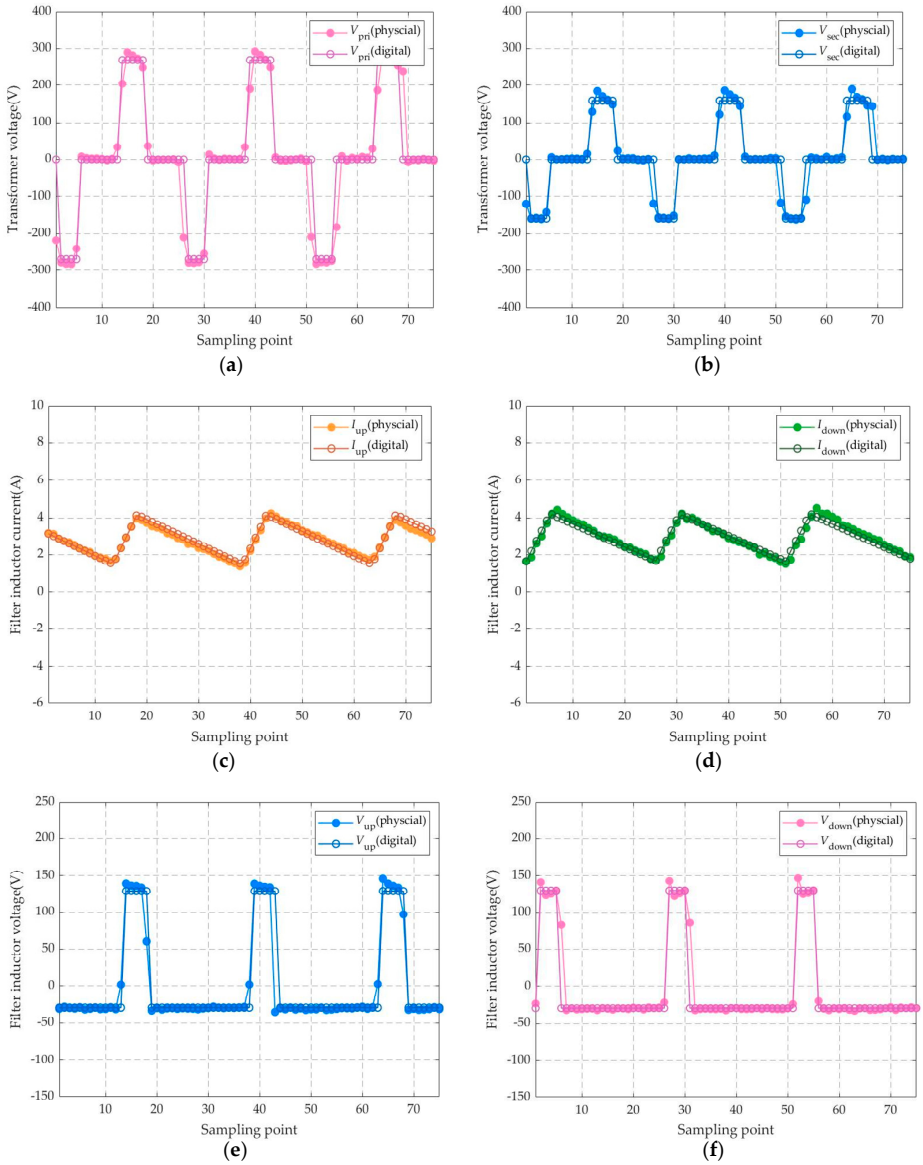


Figure 10. Comparison of steady-state waveforms between physical layer and digital layer. (**a**) Primary side voltage of transformer; (**b**) Secondary side voltage of transformer; (**c**) Current across L_1; (**d**) Current across L_2; (**e**) Voltage of L_1; (**f**) Voltage of L_2.

It can be seen from the comparison results that the waveforms of the physical layer generally coincide with that of the digital layer during the steady state, which indicates

that the digital twin can reflect well the running state of the DC-DC converter in the real physical world. There exists slight errors due to the environmental disturbance, the error of the sensor, and different processing ways between the digital twin and the real converter.

4. Application of the Digital Twin

Soft faults and hard faults are two types of faults in the DC-DC converter. A soft fault refers to the performance degeneration of components after long-term running, and is unnoticeable at early stages in the life-cycle but will lead to the abnormal operation or the eventual collapse of the whole DC-DC system. A hard fault refers to the function loss of the converter caused by the damage of the components. Both types of faults have a severe influence on the safety of the converter as well as the relative power of the system, thus, it is of great importance to monitor the condition of the converter. In order to verify the application value of the established digital twin on the condition monitoring of the DC-DC converter, experiments are conducted as follows.

4.1. Application of Digital Twin on Soft Faults

Electrolytic capacitors and inductors are typical components that are prone to performance changes [29]. The DC-DC converter in this paper has five electrolytic capacitors (including one voltage stabilized capacitor C_1 and four filter capacitors, the four filter capacitors are paralleled and can be seen as capacitor C_2) and three inductors (including one resonance inductor L_r and two filter inductors, L_1 and L_2), under long-term environmental stress, the capacitance of the electrolytic capacitors and the inductance of the inductors will decrease [30,31]. Once the value is below the threshold, serious faults may occur.

Figure 11 shows the distribution of the parameters of the main components at the beginning and the end of the iteration, by boxplot. The value of load resistance usually remains unknown, in order to deduce its actual value. R is also included in the experiment.

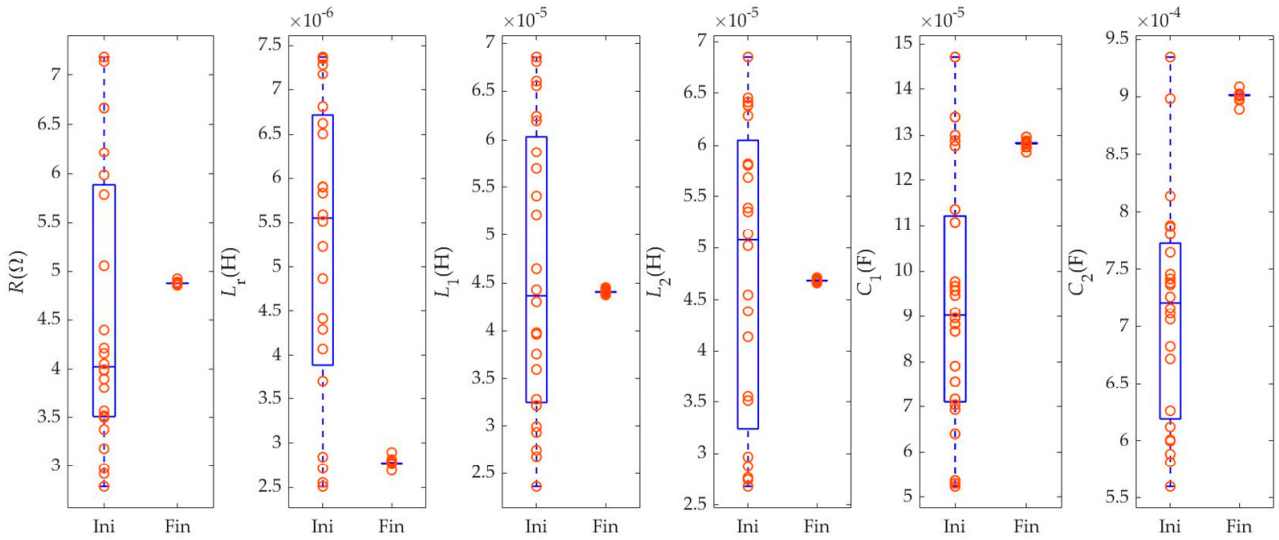
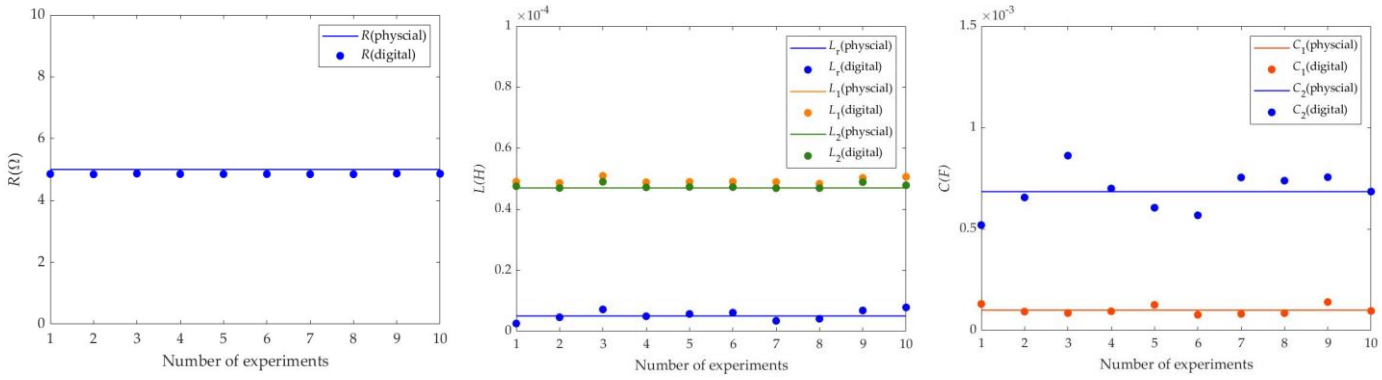


Figure 11. Boxplot of distribution of device parameters.

As shown in Figure 11, after the random initialization, the parameter values are distributed over a wide range, but after 100 iterations, the device parameter values converge at specific values, which refer to the actual value of the device parameters.

Due to the randomness of the PSO algorithm, the experiment demonstrated in Section 3 is repeated ten times, in order to observe the ability of the digital twin to identify the parameter values of the converter. The results are compared with actual parameter values tested by digital bridge. Comparative results of main components are shown in Figure 12.



(**a**) (**b**) (**c**)

Figure 12. Comparison of parameter values between physical converter and digital twin. (**a**) Load resistance; (**b**) Inductance of the inductors; (**c**) Capacitance of the electrolytic capacitors.

It can be seen in Figure 12 that, although there are slight differences among the results of the experiments, the parameter values of the digital twin are always around the actual values. The fluctuation range of C_2 is larger than other parameters, resulting from the inadequate measurement accuracy of the sensors in hardware experimental platform, where the ripple of output voltage is not measured precisely.

The results above show that, in spite of random initialization of the PSO algorithm, the digital twin can well identify the value of electrolytic capacitors, inductors, and resistance through self-updating. Thereby, in the case of soft faults, the digital twin can infer the variation tendency of key components in the converter by observing its external running condition. Thus, it is possible to know the internal condition of the converter without needing to stop it running or enforcing invasive testing. In addition, maintenance can be conducted depending on the condition of the converter in real time, instead of regularly.

4.2. Application of Digital Twin on Hard Faults

A digital twin can be combined with data-drive methods, in order to detect hard faults. Hard faults usually include short-circuit faults and open-circuit faults in the circuit. When short-circuit faults occur, overcurrent and overheating occur, which leads to converter failure and serious consequences. Thus, short-circuit faults are usually detected and proceeded by hardware protection in order to cut down the faults quickly. However, when open-circuit faults occur, the converter can continue running in a steady but abnormal state, and under long-term abnormal running states, can fail irreversibly. Therefore, it is meaningful to monitor the open-circuit faults of the converter.

In this paper, four open-circuit faults are simulated by the digital twin of the phase-shift full-bridge current doubling rectifier converter, leading arm open-circuit, lagging arm open-circuit, load open-circuit, and a resonance inductor open-circuit, respectively. There is data loss in the primary-side currents, output voltage as well as output current due to the existence of filter capacitors and filter inductors, but the primary voltage of the transformer V_{pri} is determined by the on-off of the switch directly [32]. So, V_{pri} can provide sufficient and concise information about the running states of the converter. Therefore, V_{pri} of the converter under different running conditions is detected, of which the results are shown in Figure 13. It is noteworthy that there exists a fluctuation of input voltage in the real converter, so white noises are added into the input voltage of the digital twin for the sake of precision.

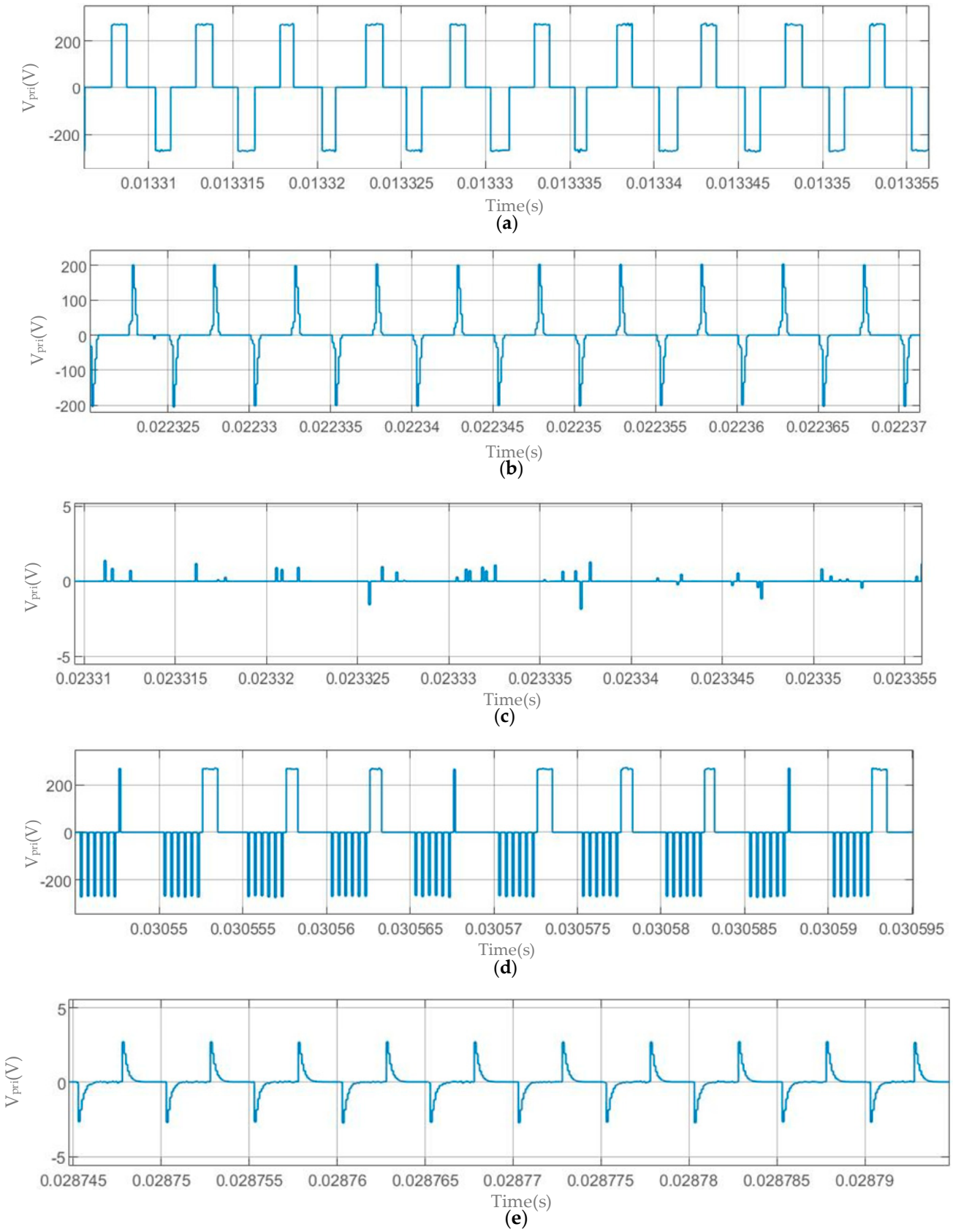


Figure 13. Vpri waveforms of digital twin under different running conditions. (**a**) Normal; (**b**) Leading arm open-circuit; (**c**) Lagging arm open-circuit; (**d**) Load open-circuit; (**e**) Resonance inductor open-circuit.

V_{pri} data of 4000 periods are collected from the normal state and four abnormal states respectively, and 25 data points are sampled with the same interval from each period. In order to extract the characteristics of waveform under each condition, 12 typical time domain features are calculated from each period by using formulas proposed in [33]. Table 3 shows processed data of 10 periods under normal state.

Table 3. Typical time domain features of V_{pri} under normal state.

Period	Maximum	Minimum	*p-p* Value	Mean	Variance	Standard Deviation	Kurtosis	Skewness	Waveform	Peak	Pulse	Margin
1	273.444	−270.566	544.010	0.296	29,164.897	170.777	2.500	0.008	1.581	1.601	2.532	6.289
2	270.920	−272.933	543.853	10.487	26,137.145	161.670	2.759	−0.025	1.667	1.672	2.787	7.683
3	272.259	−275.883	548.142	0.002	29,296.096	171.161	2.501	0.000	1.581	1.591	2.515	6.248
4	271.100	−276.002	547.102	−11.084	26,056.404	161.420	2.752	0.004	1.667	1.676	2.793	7.702
5	271.087	−272.283	543.370	21.474	28,835.378	169.810	2.439	−0.064	1.581	1.584	2.504	6.218
6	273.019	−271.854	544.873	−0.011	23,295.633	152.629	3.126	0.000	1.768	1.789	3.162	9.797
7	273.887	−271.892	545.779	0.153	29,228.823	170.964	2.500	0.004	1.581	1.602	2.533	6.293
8	273.851	−271.120	544.971	21.663	28,715.446	169.456	2.435	−0.057	1.581	1.603	2.535	6.293
9	273.356	−273.796	547.152	−10.830	26,034.891	161.353	2.756	0.013	1.667	1.690	2.817	7.770
10	274.347	−270.990	545.337	11.143	26,149.781	161.709	2.751	−0.003	1.667	1.693	2.821	7.777

In order to implement classification of the running states by data-drive methods, each state is numbered by a sequence of zeros and ones, which is listed in Table 4.

Table 4. Classification label of each state.

State	Serial Number
Normal	10000
Leading arm open circuit	01000
Lagging arm open circuit	00100
R open circuit	00010
L_r open circuit	00001

A BP ANN is established to classify different running conditions of the converter. BP ANN is a multilayer feedforward network trained by error back propagation, it learns certain rules through training and gets the result closest to the expected output when given the input. BP ANN has the ability of complex pattern classification as well as excellent multi-dimensional function mapping. The established BP ANN has three layers, including one input layer, one output layer and one hidden layer with 10 neurons. The logsig function is selected as the transfer function of the hidden layer, the purelin function is selected as the transfer function of the output layer, while the traingdx function is selected as the function of backpropagation. The structure of the BP ANN is shown in Figure 14.

Half of the processed V_{pri} data is used as a training set, while the other half is used as a test set. The training goal is set to 0.0001, learning rate to 0.01, and maximum number of training sets to 10000. The test result shows that the recognition rate of the BP ANN is 99.29%. Figure 15 shows a confusion matrix that depicts the classification result.

It can be seen from the Figure 15 that the diagonal squares are very dark in colour, which means the BP ANN can classify different running states with high accuracy. There are a few very light blue squares, which means only a small number of data in the test set is mis-classified. Thus, the BP ANN can identify different running states of the DC-DC converter within one single period.

Actual V_{pri} data under different states is collected from the hardware experimental platform to validate the practicability of the BP ANN, including normal state and the state of leading arm open circuit. The state of leading arm open circuit is simulated by grounding the drive signal of MOSFET. The experimental waveforms are shown in Figure 16.

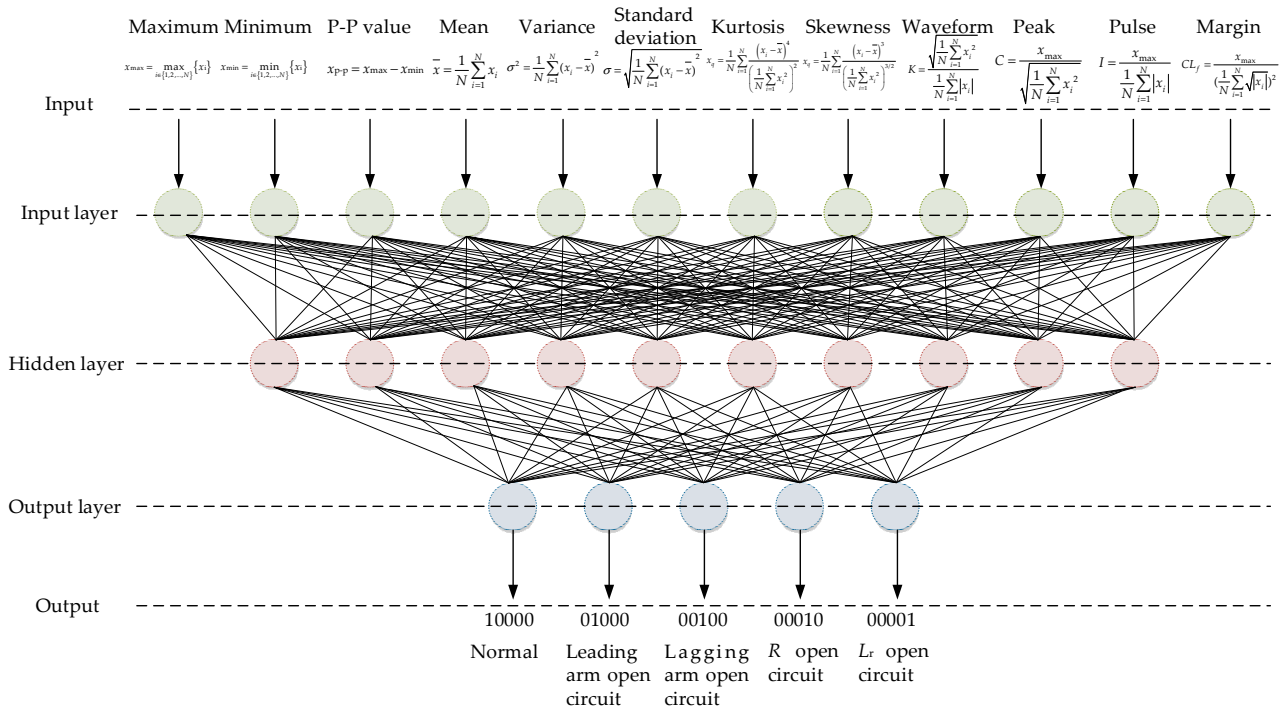


Figure 14. Three-layer BP ANN.

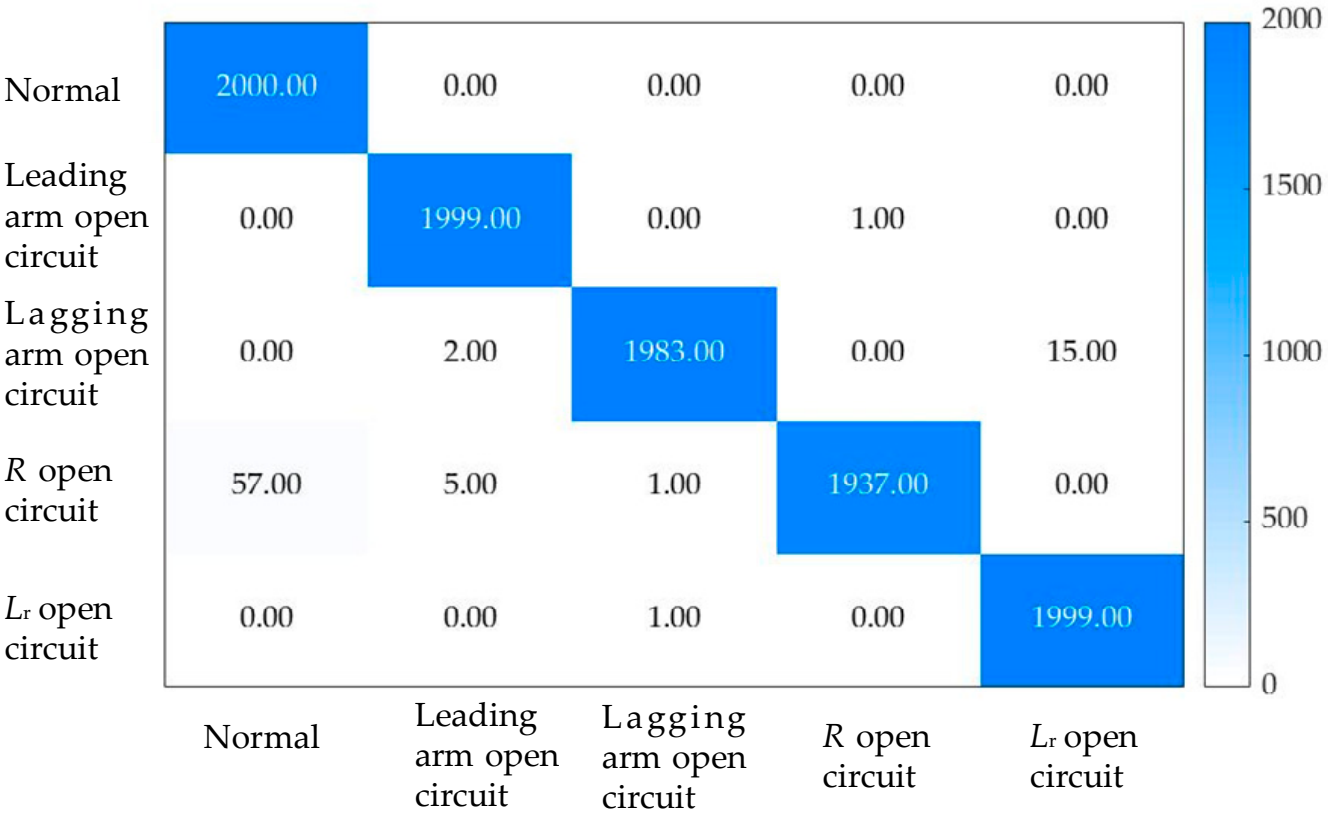


Figure 15. Confusion matrix of classification result.

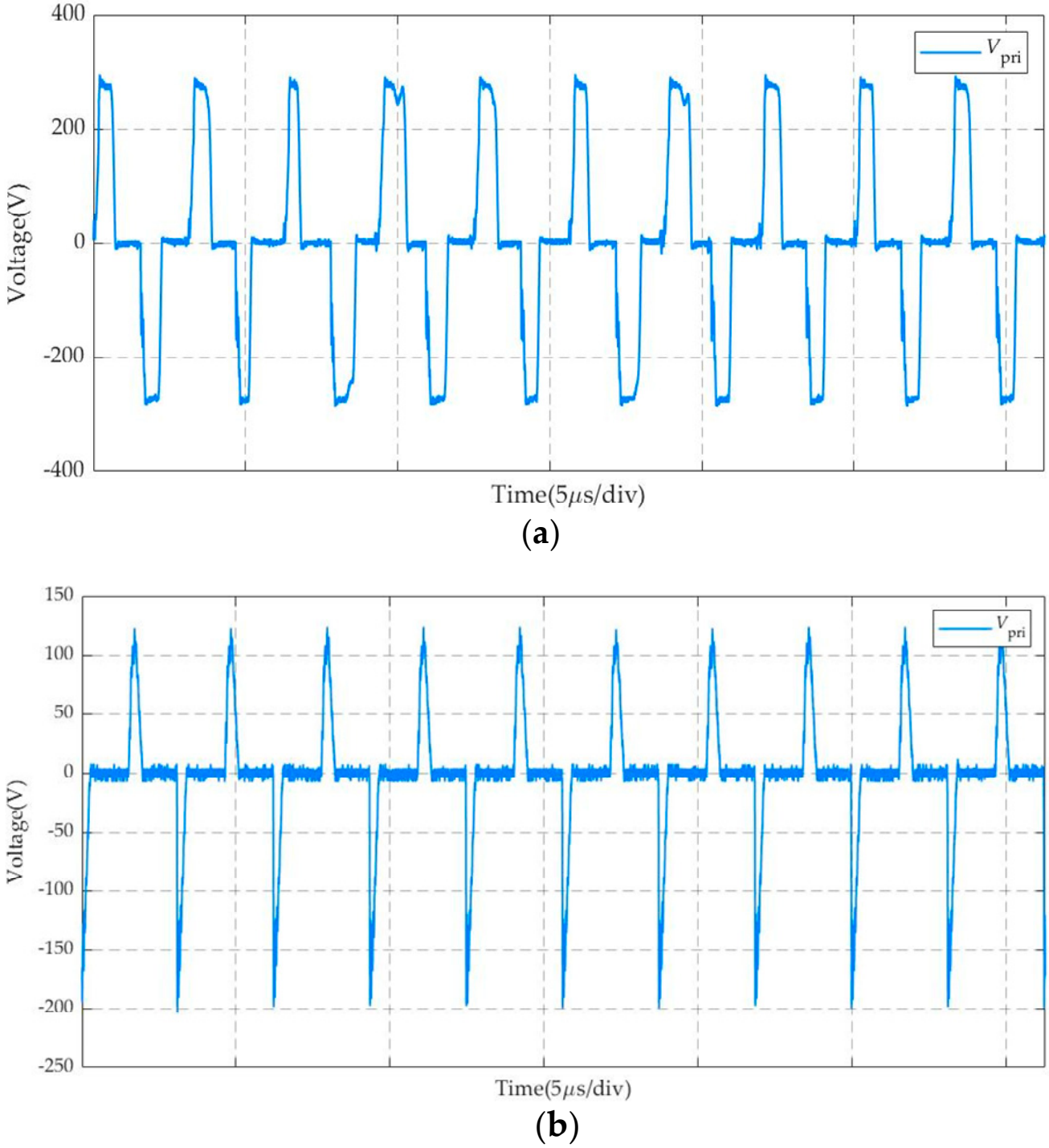


Figure 16. Actual V_{pri} data. (**a**) Normal; (**b**) Leading arm open-circuit.

The data is processed and is input into the trained BP ANN. The classification results are shown in Table 5, where the maximum number in each column is regarded as 1, and other numbers in this column are regarded as 0. It can be seen in Table 5 that the classification results agree with the actual running condition.

Table 5. Classification results of 10 periods of the real converter under different states.

State	Number of Periods									
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Experimental condition: normal										
Normal	1.002→1	0.961→1	0.948→1	0.955→1	0.870→1	0.919→1	0.568→1	0.868→1	1.025→1	0.824→1
Leading arm open circuit	−0.063→0	−0.019→0	−0.035→0	−0.039→0	−0.021→0	−0.023→0	−0.037→0	−0.078→0	−0.051→0	−0.036→0
Lagging arm open circuit	−0.011→0	−0.010→0	−0.028→0	−0.007→0	−0.016→0	−0.014→0	0.006→0	0.004→0	0.002→0	−0.006→0
R open circuit	0.017→0	0.033→0	0.053→0	0.039→0	0.116→0	0.074→0	0.433→0	0.143→0	0.002→0	0.160→0
L_r open circuit	0.047→0	0.027→0	0.044→0	0.045→0	0.041→0	0.030→0	0.038→0	0.033→0	0.027→0	0.054→0
Experimental condition: leading arm open circuit										
Normal	−0.046→0	−0.043→0	−0.049→0	−0.062→0	−0.069→0	−0.063→0	−0.054→0	−0.056→0	−0.063→0	−0.061→0
Leading arm open circuit	1.027→1	1.011→1	1.028→1	1.030→1	1.039→1	1.040→1	1.028→1	1.016→1	1.019→1	1.012→1
Lagging arm open circuit	0.065→0	0.060→0	0.076→0	0.078→0	0.080→0	0.090→0	0.074→0	0.079→0	0.085→0	0.089→0
R open circuit	−0.222→0	−0.201→0	−0.204→0	−0.197→0	−0.208→0	−0.196→0	−0.205→0	−0.178→0	−0.171→0	−0.158→0
L_r open circuit	0.176→0	0.174→0	0.150→0	0.151→0	0.157→0	0.130→0	0.157→0	0.139→0	0.129→0	0.117→0

This method is simple and fast due to the consistency of the digital twin and the real converter. The analysis and process of data are based on time domain, and the state of the converter can be identified within a single period.

5. Conclusions

In this paper, a digital twin for phase-shift full-bridge current doubling rectifier DC-DC converter is established. Firstly, the prototype of the converter is built, then its digital twin is built in a simulation software. The PSO algorithm is used to update the interior parameters of the digital twin by examining the difference of waveforms between the converter and digital twin, so that the digital twin can reflect the operation state of the real converter. Then, the application of the digital twin on condition monitoring is discussed through corresponding experiments. In the case of soft faults, the digital twin can infer the parameter values of key components in the converter by updating itself, then the degeneration process can be detected through observing external performance instead of invasive tests. In the case of hard faults, a BP ANN is trained by data collected from the digital twin, and the experimental results show the BP ANN can distinguish the converter state under different test conditions. The proposed digital twin can update itself in real time and implement monitoring of DC-DC converter in its whole life. Compared to traditional methods, the proposed digital twin realizes the non-invasive monitoring of converter at the system level, and can monitor the health condition of components in real time without extra hardware circuit. This method provides a practical solution for the condition monitoring and fault diagnosis of power electronic converters, thereby being a workable way of improving the reliability of airborne power supply system.

Author Contributions: Conceptualization, G.L.; methodology, G.L. and X.W.; software, X.W.; validation, X.W., G.L. and M.W.; formal analysis, W.W. and M.W.; investigation, G.L. and W.W.; resources, G.L.; data curation, X.W.; writing—original draft preparation, X.W. and G.L.; writing—review and editing, X.W., G.L. and M.W.; visualization, X.W.; supervision, G.L. and W.W.; project administration, W.W.; funding acquisition, G.L. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Key Laboratory of Special Machine and High Voltage Apparatus (Shenyang University of Technology), Ministry of Education under Grant KFKT202108, in part by the Fundamental Research Funds for the Central Universities, in part by the National Natural Science Foundation of China under Grants 52077041.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chen, J.; Wang, C.; Chen, J. Investigation on the selection of electric power system architecture for future more electric aircraft. *IEEE Trans. Transp. Electrif.* **2018**, *4*, 563–576. [CrossRef]
2. Gokdag, M.; Gulbudak, O. Model predictive control of AC-DC matrix converter with unity input power factor. In Proceedings of the 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), Doha, Qatar, 10–12 April 2018.
3. Wang, G.; Wang, X.; Lv, J. An improved harmonic suppression control strategy for the hybrid microgrid bidirectional AC/DC converter. *IEEE Access* **2020**, *8*, 220422–220436. [CrossRef]
4. Fu, C.; Zhang, C.; Zhang, G.; Song, J.; Zhang, C.; Duan, B. Disturbance Observer-Based Finite-Time Control for Three-Phase AC–DC Converter. *IEEE Trans. Ind. Electron.* **2021**, *69*, 5637–5647. [CrossRef]
5. Jorge, S.G.; Solsona, J.A.; Busada, C.A. Nonlinear Control of a Two-Stage Single-Phase DC–AC Converter. *IEEE J. Emerg. Sel. Top. Ind. Electron.* **2022**, *3*, 1038–1045. [CrossRef]
6. Luo, S.; Wu, W.; Koutroulis, E.; Chung, H.S.-H.; Blaabjerg, F. A new virtual oscillator control without third-harmonics injection for DC/AC inverter. *IEEE Trans. Power Electron.* **2021**, *36*, 10879–10888. [CrossRef]
7. Yin, Y.; Liu, J.; Marquez, A.; Lin, X.; Leon, J.I.; Vazquez, S.; Franquelo, L.G.; Wu, L. Advanced control strategies for DC–DC buck converters with parametric uncertainties via experimental evaluation. *IEEE Trans. Circuits Syst. I: Regul. Pap.* **2020**, *67*, 5257–5267. [CrossRef]
8. Lai, W.; Chen, M.; Ran, L.; Alatise, O.; Xu, S.; Mawby, P. Low ΔT_j Stress Cycle Effect in IGBT Power Module Die-Attach Lifetime Modeling. *IEEE Trans. Power Electron.* **2015**, *31*, 6575–6585. [CrossRef]
9. Wu, Y.; Du, X. A VEN condition monitoring method of DC-link capacitors for power converters. *IEEE Trans. Ind. Electron.* **2018**, *66*, 1296–1306. [CrossRef]
10. Dusmez, S.; Bhardwaj, M.; Sun, L.; Akin, B. In situ condition monitoring of high-voltage discrete power MOSFET in boost converter through software frequency response analysis. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7693–7702. [CrossRef]
11. Xiang, D.; Ran, L.; Tavner, P.; Yang, S.; Bryant, A.; Mawby, P. Condition monitoring power module solder fatigue using inverter harmonic identification. *IEEE Trans. Power Electron.* **2011**, *27*, 235–247. [CrossRef]
12. Danilczyk, W.; Sun, Y.; He, H. Angel: An intelligent digital twin framework for microgrid security. In Proceedings of the 2019 North American Power Symposium (NAPS), Wichita, KS, USA, 13–15 October 2019.
13. Ezhilarasu, C.M.; Skaf, Z.; Jennions, I.K. Understanding the role of a digital twin in integrated vehicle health management (IVHM). In Proceedings of the 2019 IEEE International Conference on Systems, Man and Cybernetics (SMC), Bari, Italy, 6–9 October 2019.
14. Jain, P.; Poon, J.; Singh, J.P.; Spanos, C.; Sanders, S.R.; Panda, S.K. A digital twin approach for fault diagnosis in distributed photovoltaic systems. *IEEE Trans. Power Electron.* **2019**, *35*, 940–956. [CrossRef]
15. Song, X.; Cai, H.; Kircheis, J.; Jiang, T.; Schlegel, S.; Westermann, D. Application of digital twin assistant-system in state estimation for inverter dominated grid. In Proceedings of the 2020 55th International Universities Power Engineering Conference (UPEC), Turin, Italy, 1–4 September 2020.
16. Milovanovic, S.; Polanco, I.; Utvic, M.; Dujic, D. Flexible and efficient mmc digital twin realized with small-scale real-time simulators. *IEEE Power Electron. Mag.* **2021**, *8*, 24–33. [CrossRef]
17. Race, S.; Nagel, M.; Kovacevic-Badstuebner, I.; Ziemann, T.; Grossner, U. Towards digital twins for the optimization of power electronic switching cells with discrete SiC power MOSFETs. In Proceedings of the PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 10–12 May 2022.
18. Wunderlich, A.; Santi, E. Digital twin models of power electronic converters using dynamic neural networks. In Proceedings of the 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 14–17 June 2021.
19. Milton, M.; De La O, C.; Ginn, H.L.; Benigni, A. Controller-embeddable probabilistic real-time digital twins for power electronic converter diagnostics. *IEEE Trans. Power Electron.* **2020**, *35*, 9850–9864. [CrossRef]
20. Peng, Y.; Wang, H. Application of digital twin concept in condition monitoring for dc-dc converter. In Proceedings of the 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 29 September–3 October 2019.
21. Peng, Y.; Zhao, S.; Wang, H. A digital twin based estimation method for health indicators of DC–DC converters. *IEEE Trans. Power Electron.* **2020**, *36*, 2105–2118. [CrossRef]
22. Wu, Q.; Wang, W.; Wang, Q.; Xiao, L.; Hu, B. Digital Twin Approach for Degradation Parameters Identification of a Single-Phase DC-AC Inverter. In Proceedings of the 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 20–24 March 2022.
23. Mirza, A.B.; Choksi, K.; Vala, S.S.; Radha, K.M.; Chinthavali, M.S.; Luo, F. Cognitive Insights into Metaheuristic Digital Twin based Health Monitoring of DC-DC Converters. In Proceedings of the 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 5–9 September 2022.
24. Liu, Y.; Chen, G.; Liu, Y.; Mo, L.; Qing, X. Condition Monitoring of Power Electronics Converters Based on Digital Twin. In Proceedings of the 2021 IEEE 3rd International Conference on Circuits and Systems (ICCS), Chengdu, China, 29–31 October 2021.
25. Chen, S.; Wang, S.; Wen, P.; Zhao, S. Digital Twin for Degradation Parameters Identification of DC-DC Converters Based on Bayesian Optimization. In Proceedings of the 2021 IEEE International Conference on Prognostics and Health Management (ICPHM), Detroit (Romulus), MI, USA, 7–9 June 2021.

26. Rajendran, S.; Devi, V.K.; Diaz, M. Digital twin based identification of degradation parameters of DC-DC converters using an Arithmetic Optimization Algorithm. In Proceedings of the 2022 3rd International Conference for Emerging Technology (INCET), Belgaum, India, 27–29 May 2022.
27. Millan, J.; Godignon, P.; Perpiñà, X.; Pérez-Tomás, A.; Rebollo, J. A survey of wide bandgap power semiconductor devices. *IEEE Trans. Power Electron.* **2013**, *29*, 2155–2163. [CrossRef]
28. Shi, Y. Particle swarm optimization: Developments, applications and resources. In Proceedings of the 2001 Congress on Evolutionary Computation (IEEE Cat. No. 01TH8546), Seoul, Republic of Korea, 27–30 May 2001.
29. Peyghami, S.; Palensky, P.; Blaabjerg, F. An overview on the reliability of modern power electronic based power systems. *IEEE Open J. Power Electron.* **2020**, *1*, 34–50. [CrossRef]
30. Soliman, H.; Wang, H.; Blaabjerg, F. A review of the condition monitoring of capacitors in power electronic converters. *IEEE Trans. Ind. Appl.* **2016**, *52*, 4976–4989. [CrossRef]
31. Scirè, D.; Rosato, S.; Lullo, G.; Vitale, G. A temperature dependent non-linear inductor model for a DC/DC boost converter. In Proceedings of the 2018 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Prague, Czech Republic, 2–5 July 2018.
32. Pei, X.; Nie, S.; Chen, Y.; Kang, Y. Open-circuit fault diagnosis and fault-tolerant strategies for full-bridge DC–DC converters. *IEEE Trans. Power Electron.* **2011**, *27*, 2550–2565. [CrossRef]
33. Xu, H.; Peng, Y.; Su, L. Research on Open Circuit Fault Diagnosis of Inverter Circuit Switching tube Based on Machine Learning Algorithm. *IOP Conf. Ser. Mater. Sci. Eng.* **2018**, *452*, 042015. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.