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A Symmetric Novel 8T3R Non-Volatile SRAM Cell for Embedded Applications

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Abstract: This paper proposes a symmetric eight transistor-three-memristor (8T3R) non-volatile static random-access memory (NVSRAM) cell. Non-volatile operation is achieved through the use of a memristor element, which stores data in the form of its resistive state and is referred to as RRAM. This cell is able to store the information after power-off mode and provides fast power-on/power-off speeds. The proposed symmetric 8T3R NVSRAM cell performs better instant-on operation compared to existing NVSRAMs at different technology nodes. The simulation results show that resistance of RAM-based 8T3R SRAM cell consumes less power in standby mode and has excellent switching performance during power on/off speed. It also has better read and write stability and significantly improves noise tolerance than the conventional asymmetrical 6T SRAM and other NVSRAM cells. The power dissipation is evaluated at different technology nodes. Hence, our proposed symmetric 8T3R NVSRAM cell is suitable to use at low power and embedded applications.

Keywords: non-volatile; symmetric NVSRAM; memristor; RRAM; instant-on; SRAM

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1. Introduction

Over the past decades, metal oxide-based memories such as SRAM, DRAM, and flash memory have been generally used to meet the capacity prerequisites of any data handling unit [1]. The expanse of mobile devices has prompted the need to plan storage devices with fast switching characteristics longer and battery life [2]. Despite the fact that it is fast, the volatile nature of SRAM can cause stored data to be lost when the power supply is removed [3]. Moreover, under the deep submicron range, SRAM cells encounter high leakage power consumption [4]. The CMOS technology is also moving toward the fundamental limit of size scaling [5] because of the expanded short-channel effect, seriously weakening device performance [6]. Therefore, to address the issues of normally-off applications, non-volatile memory (NVM) is generally used to back up the information in the SRAM when the power is off [7]. It is recommended that non-volatile memory (NVM) devices can further suppress standby power consumption by turning off the power of infrequently used SRAMs without loss of information. Before turning off the power of the SRAM cell, first store the SRAM data in the NVM device. After power-up, the data are restored again. Hence, Such SRAM cells can be called non-volatile SRAM (NVSRAM). Compared with the use of high threshold voltage (High Vth) to maintain the latch, this design dissipates much less leakage power to hold the data of the SRAM cell [8]. Among the different types of NVM devices, memristors (also called resistive random-access memory,

RRAM) based devices have certain benefits, including a small size (with dimensions 10 nm× 10 nm as described in [9]); high-speed operation, approximately 10 ns [10,11]; low programming voltage, approximately 1 V programming voltage as described in [12]; and compatible with CMOS manufacturing process.

Memristor was discovered by Leon Chua in the early 1970s, which established the relation between flux (Φm) and charge (q) and was able to maintain its resistive state even after removing the power supply [2]. The internal state variable (x_m) performs the role of the memristance (M) of the memristors, i.e., $x_m \equiv M$ [13]. The state of the memristor is defined by the following equation

$$i(t) = x_m - (v(t))$$

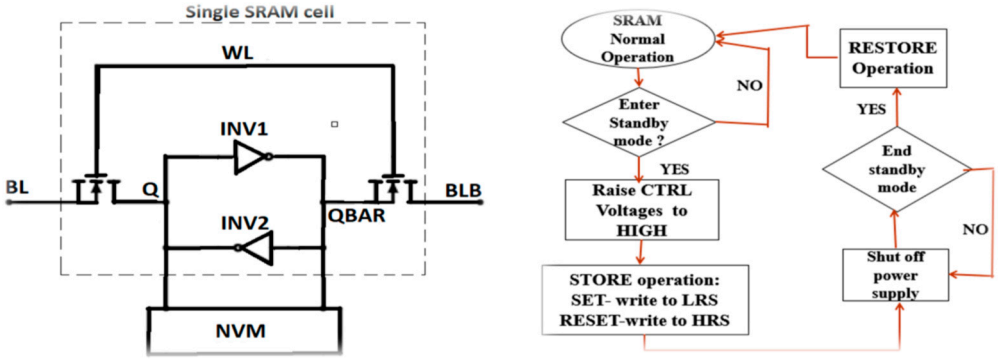
The memristor is a two-terminal device, originally considered to be the fourth passive element after the capacitor (C), inductor (L), and resistor (R) [14]. It is a non-linear switching mechanism of memristor that involves the operation of forming conductive filaments with oxide layers between the metal terminals to achieve a low-resistance state and high-resistance state of the device [15]. The magnitudes of these resistance states can have a different values. The external voltage applied determines the resistances states of the device. In addition, the use of memristors was proven to consume less power and high packaging density. Memristors can be used in many fields, such as the design of chaotic circuits [15–17], analog circuits [18], neural networks [19–21], logic arrays [22,23], and flip-flop [24]. In this article, a novel 8T3R NVSRAM is proposed that has dominance energy, noise immunity, and delay in terms of read and write operations than the traditional 6T SRAM cell design. The main features of this work are:

- Symmetric NVSRAM has shown improvements in standby power consumption and static noise margin when compared with standard 6T SRAM (S6T) cell;
- Using a memristor ensures that the circuit is inherently non-volatile.

The other sections of this paper discuss the following: In Section 2, a brief overview of NVM structure and operation flow is provided. Section 3 discusses the operation of the proposed symmetric 8T3R NVSRAM cell design at different operating modes, such as the store, power down, and restore operations, which are explained. The simulation results obtained were discussed in Section 4 and compared with other conventional CMOS 6T SRAM cells and NVSRAM cells. Finally, Section 5 concludes the paper.

2. NVSRAM Cell Design

The NVM with SRAM makes symmetric NVSRAM. The performance factors used for the NVM and SRAM are symmetrical in nature. Figure 1a shows the structure of symmetric NVSRAM with a combination of a single symmetric SRAM cell and NVM device. The NVM device is connected to data nodes Q and QBAR, which access the information from it and stores it for future purpose. Figure 1b shows the operational flow of the symmetric NVSRAM. In normal mode, the NVSRAM cell acts as an SRAM and performs functions similar to the SRAM cell and performs read/write operations [25]. In standby mode, symmetric NVSRAM enters the storage operation by pushing the SRAM cell data into the memristor devices with raise of control voltages [26]. The memristor is set to High-Resistance State (HRS)/Low-Resistance State (LRS) depending on the data present at nodes. The LRS represents the SET state, and HRS represents the RESET state [27,28]. After successfully backing up the data, the standby leakage power is reduced by shutting into power-down mode [29,30]. The previous data from the memristor to the data nodes are restored again whenever the NVSRAM cell is powered up [31–34]. After RESTORE operation, symmetric NVSRAM can be used as normal SRAM for read/write operations [34–37].



(**a**) (**b**)

Figure 1. (**a**) Structure for NVM with 6T SRAM cell as core. (**b**) Flow chart for operational flow of NVSRAM cell.

2.1. Existing NVSRAM Cells

The existing structures of non-volatile SRAM cells are depicted in Figure 2.

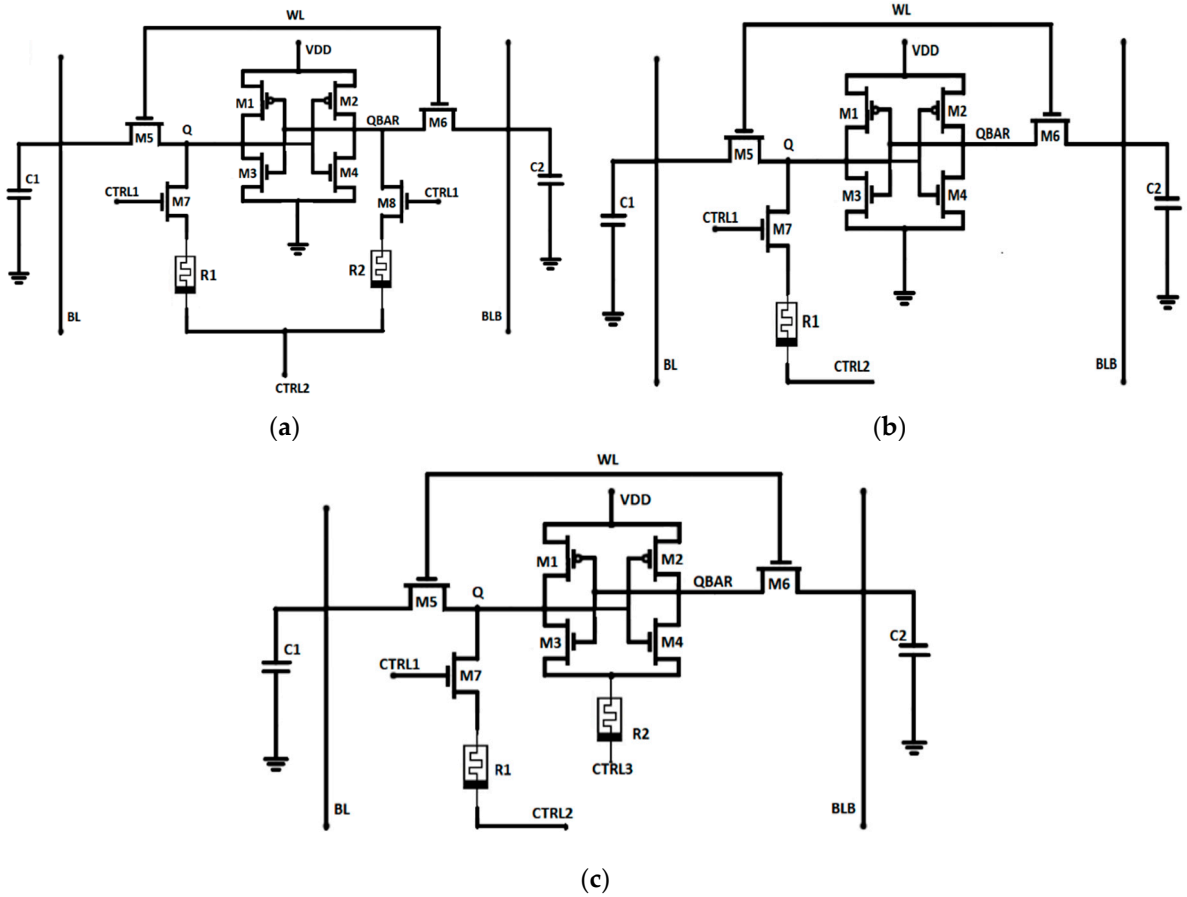


Figure 2. (**a**) Existing 7T1R NVSRAM 2. (**b**) Existing 7T2R NVSRAM 2. (**c**) Existing 8T2R NVSRAM.

2.1.1. 8T2R

The 8T2R based NVSRAM is shown in Figure 2a. RRAMs can be accessed by passing a CTRL1 signal to two transistors, M7 and M8, which are used to perform SET and RESET, respectively. Assuming that the SET signal is received, CTRL1 is set to high, while CTRL2 is grounded, and, depending on the data stored in the NVSRAM cell, either R1 or R2 is set to LRS (low-level read-write). During the RESET process, CTRL2 is set to VDD, and either R1 or R2 is set to HRS, depending on the data stored in the NVSRAM cell. The current

drive capability of the F-MOSFET is improved for the NVSRAM application, but the mode of operation dissipates more power in write and power-down mode.

2.1.2. 7T1R

Figure 2b shows the structure of the 7T1R NVSRAM cell [32]. The cell consists of seven Transistors and one RRAM comprised of 6TSRAM cells and 1T1R. The STORE operation is controlled by control transistor M7, which is connected between the RRAM device and memory node Q, which stores the logic states "0" and "1". The RRAM device's LRS and HRS are determined by the data stored at nodes Q and QBAR. Because there is only one RRAM device, the FORMING state is performed using BL at the start of the storing operation.

During the power-down stage, all voltage sources are switched off. During the RESTORE procedure, the current from CTRL2 passes through the RRAM device depending on the resistive state. When the RRAM is in LRS, for example, Q stays at "1", and Qb is discharged through M2. When CTRL1 and WL are set to high during READ, the amount of current flow is determined by the potential difference between the top and bottom electrodes of the RRAM device. Node Q is linked to BL to check the status of the memory cell. This design shows a significant reduction in energy for its operations required for "Instant-on" operation and is capable of storing and operating under multiple sets of configuration data for FPGA operation. However, a low restore yield degraded with stability margins tried to enhance the stability of the cell, but they used an additional source switch transistor that acquires extra area and increases the threshold value of voltage transfer characteristics (VTCs), which introduces a delay in the circuit.

2.1.3. 7T2R

The structure of 7T2R [31] is shown in Figure 2c, with RRAMs R1 and R2. R1 is connected to M7, and R2 is connected to common sources of M3 and M4. STORE/RESTORE actions are controlled by the M5 transistor. It should be noted that the FORMING procedure for R1 is carried out by a single BL. RRAM resistance varies from LRS to HRS or HRS to LRS during STORE, depending on the Q and Qb node voltages, as long as the CTRL1 signal is set high. WL and CTRL1 are set high during the read operation. The WRITE "0" and "1" commands are programmed into Nodes Q. BL is high to SET R1 during the STORE operation and low to RESET. If the RRAM device is in LRS mode, Node Q retains "1" during RESTORE and "0" if it is in HRS mode. Stability was improved, but with this model, the power dissipation rises ten times for the increase of every 100 K temperature.

One key challenge to RRAM cells is the write endurance. Endurance is usually defined as the number of set-reset operations (i.e., endurance cycles) after which the cell experiences a permanent-write failure. Several papers [38,39] demonstrated up to 10^6 endurance cycles at the array level.

3. Proposed Symmetric 8T3R NVSRAM Cell

This section may be divided into subheadings. It should provide a concise and precise description of the experimental results, their interpretation, as well as the experimental conclusions that can be drawn.

3.1. Structure

The proposed structure of the symmetric 8T3RNVSRAM cell is shown in Figure 3. The cell is comprised of a core 6T-SRAM cell (M1–M6), NMOS control transistors (M7, M8) and memristors R1, R2 (connected to data nodes through control transistors), and memristor R3 is connected to the common sources of pull-down transistors M3 and M4 with control signal CTRL3. This memristor R3 avoids direct connection between SRAM cell core and ground Vss. The CTRL3 makes the cell in a stable state by providing low voltage in the read mode. The data are stored in R1 and R2 by enabling the M7 and M8 with control signals CTRL1 and CTRL2. The logic state of memristor "1" represents STORE, and logic "0"

represents the RESET state. The operation of the 8T3R NVSRAM cell follows the following sequence: normal SRAM operation (READ/WRITE), RESET, STORE, POWER-DOWN, and POWER-UP/RESTORE.

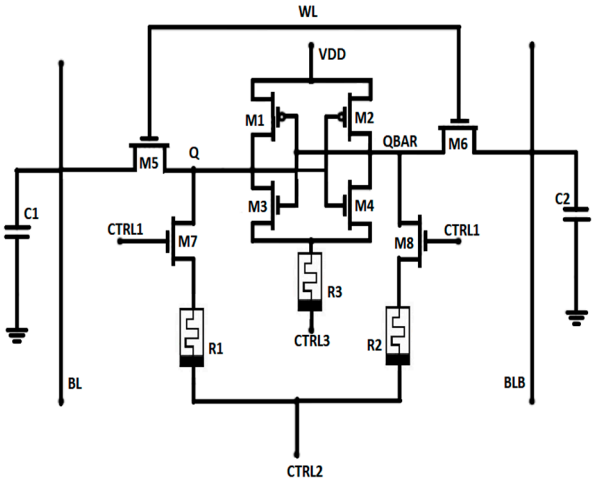


Figure 3. Symmetric 8T3R NVSRAM Cell.

The following subsections illustrate the complete sequence of NVSRAM operation-the bias conditions for the different operating modes of the RESTORE cycle. The bias conditions used for the memristor device with the control signals are summarized in Table 1.

Table 1. Condition for the control signals.

Parameter	WL (V)	VDD (V)	CTRL1 (V)	CTRL2 (V)
RESET	0	1	0	1
STORE	1	1	1	1
POWER DOWN	0	0	0	0
RESTORE	1	1	1	1

The text continues here (Figure 2 and Table 2).

Table 2. Parameters for NVSRAM Simulation.

Parameter	16 nm	20 nm	22 nm	32 nm
VDD	0.9 V	0.9 V	0.95 V	1 V
CTRL1, CTRL2, CTRL3	0.9 V	0.9 V	0.95 V	1 V
RSET (LRS)		100 Ω		
RRESET (HRS)		16 KΩ		
Temperature		25 °C		

3.2. Normal SRAM Operation

During normal SRAM operation, read/write operations are not affected by the presence of memristors R1 and R2 as they are separated from the core SRAM cell by M7 and M8, which are turned OFF with CTRL1 = CTRL2 = 0 V, and memristor R3 is also used to stabilize the read and write operations with CTRL3 = 0 V in write mode and −1 V in the read mode.

3.3. RESET Operation

A RESET operation is performed before storing the data into the memristors in order to ensure no logic state has been set in the memristors previously. R1/R2 can be made to RESET by closing the control transistors M7 and M8 with CTRL1 and enabling CTRL2 to 1 V.

3.4. STORE Operation

After the RESET operation, the STORE operation is performed by enabling the control transistors M7 and M8 through CTRL1. The memristors R1 and R2 store the values of data nodes Q and QBAR. The logic is stored in R1, and R2 is in the form resistance state. For instance, if Q = 1, a positive potential difference is generated at the top and bottom electrodes and sets the memristor in LRS; when Q = 0, it creates a negative potential difference that sets it in HRS. The LRS state represents the logic "1", and HRS represents logic "0".

3.5. POWER DOWN Operation

The condition for POWER-DOWN operation is obtained by making all the control signals and supply to the ground.

3.6. RESTORE Operation

The RESTORE operation is performed by enabling the controls signals at NMOS transistors. The nodes Q and QBAR retrieve the data by accessing the potential voltage drop created at memristors. If Q stored logic "0", then it is set in the LRS state; this makes the node voltage Q to HIGH, which is enough to turn ON pull-down transistor M4. Thus, the node QBAR is pulled down to logic "0", which in turn makes the Q to logic "1". In this way, the data are restored in the SRAM core cell, which constitutes an NVSRAM cell.

3.7. Evaluation of Non-Volatility

The conventional symmetry-based SRAM cell (Figure 1) is inherently volatile because it cannot store information when the supply is removed, so 8T2R NVSRAM [30] was introduced to store the data node information in RRAM and restores it again when the supply is turned ON. Even though this cell is non-volatile but it has less stability. Hence, the proposed design symmetric 8T3R NVSRAM cell overcomes stability issues as well as non-volatile properties. This RRAM-based NVSRAM acquires the properties of non-volatile and is able to store the information contained in the core SRAM cell when the power is OFF with the aid of control transistors and retains the data back whenever the supply is ON.

In order to assess SRAM as symmetric NVSRAM, the following four basic working operation principles of R1, R2, and R3 are explained: (i) initial state or the normal state of SRAM, (ii) store state (NVM state), (iii) power down (VDD = 0 V), and (iv) restore state (VDD = HIGH) with the control signals (CTRL). CTRL1 = 0, CTRL2 = 0 shows that there is no connection between the RRAM's R1, R2, and the output nodes of the back-to-back inverters of the core 6T SRAM cell. Therefore, making control signals to shut down normal SRAM operation is achieved. In order to store the information or to make SRAM as NVSRAM, the control signals CTRL1 and CTRL2 are enabled high. The data are stored in a memristor or RRAM in the form of resistance states. For instance, if node Q stores the logic "0", then R1 is in HRS and R2 is in LRS (QBAR = 1), and vice versa.

The advantage of Q = 0 is that in both operations, such as store and restore, there is no need to change the state of the memristor, which already stays in HRS. If the power and all the control signals are shut down, the information is stored in the memristor with its HRS and LRS states. The original data are restored by enabling the CTRL1, CTRL2, and VDD. After all operations such as store, power down, and restore, the memristor at the data node storing logic "0" comes into HRS. Therefore, it does not require additional reset after successful restore, 0, which was required for 8T2R [30] and 7T1R [32]. The non-volatility operation of 8T3R NVSRAM was studied by using HSPICE simulation. The timing diagram

(Figure 4) explains the steps involved in the store and restore operations. After successfully writing data into the nodes Q and QBAR, the data are stored from Q into R1 and QBAR into R2. From the timing diagram, the first cycle shows the write enable signal given to write circuitry.

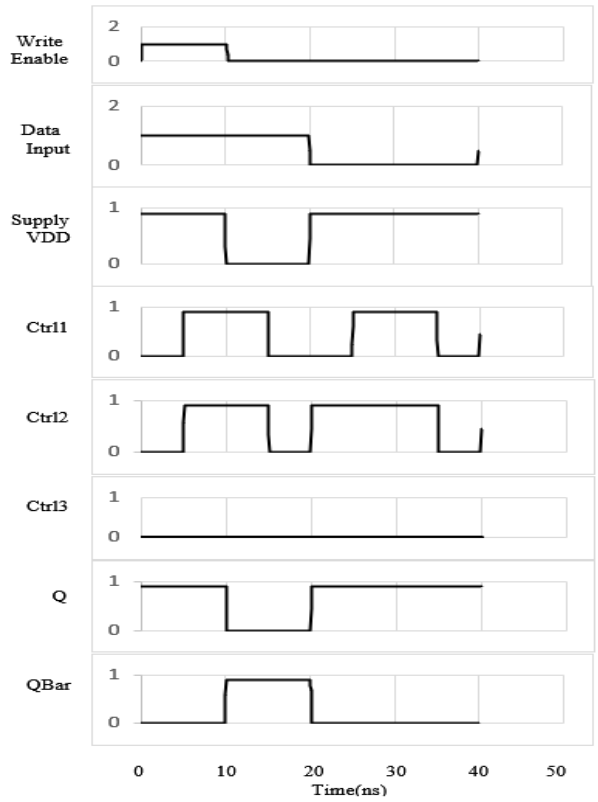


Figure 4. Non-volatile timing waveform of proposed 8T3R NVSRAM cell.

In writing "Q = 1," VDD, WL, and BL are enabled high, while BLB, CTRL1, CTRL2, and CTRL3 are maintained low. The seventh and eighth cycles show the data written into the cell for the first 10 ns with Q at logic HIGH and QBAR at logic LOW. After 10 ns, the power supply is removed, and all the control signals WL, CTRL1, and CTRL2 are changed to LOW, shown in the third, fourth and fifth cycles. After power down, the memristor R1 is SET to LRS, and R2 is RESET to HRS. During a restore operation, VDD, CTRL1, and CTRL2 are enabled after 20 ns. CTRL1 and CTRL2 again setups a connection between the R1–R2 and the cell nodes, which forces R1, R2 to retrieve the lost data into nodes Q and QBAR. This can be observed in the last cycles after 20 ns. After all cycles of operation, the 8T3R NVSRAM cell comes to its initial mode or its normal mode. Therefore, the SRAM cell becomes NVSRAM by storing the lost data. The read operation of restored data NVSRAM cell is similar to normal SRAM cell operation. After restoring the data to the nodes, the cell data value is called through pre charge and sense amplifier circuits, which show the timing, as demonstrated in the diagram (Figure 5).

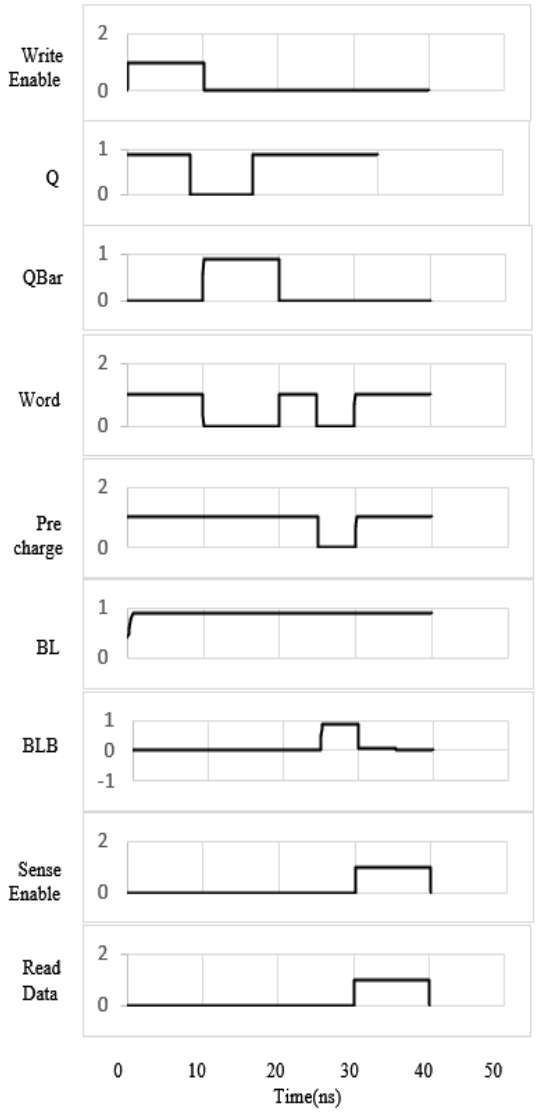


Figure 5. Read operation timing waveforms of proposed 8T3R NVSRAM.

4. Simulation Results and Discussion

Performance Parameters of Proposed Symmetric 8T3R NVSRAM

This paper proposed a novel 8T3R NVSRAM cell, which is designed and simulated by using the SYNOPSYS HSPICE tool, and evaluated various cell parameters, such as read delay, write delay, read SNM (RSNM) and write SNM (WSNM), static and dynamic power dissipation at different technology nodes of [19], and the spice memristor model [3]. The formation of a conductive oxygen layer between two terminals determines the HRS and LRS of the memristor [26]. The condition parameters of memristor HRS (ROFF), LRS (RON), and mobility μv are chosen as 16 KΩ, 100 Ω, and 10^{-14} m^2 v^{-1} S^{-1}, respectively. The length "D" of the semiconductor film is taken as 10 nm. The linear charge control memristor can be modeled as two resistors in series according to the following formula:

$$R(w) = R_{ON} \times \frac{w}{D} + R_{OFF}\left(1 - \frac{w}{D}\right) \quad (1)$$

$$M(q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON} q(t)}{D^2}\right) \quad (2)$$

where M(q) is the overall memristance of the memristor, RON and ROFF are the ON state and OFF state resistances, D is the device length, and μv is the mobility of oxygen ions. The

static noise margin (SNM) is calculated from butterfly curves by plotting Q and QB VTC characteristics under DC conditions. For proper comparison, the technology is scaled up to 16 nm Predictive Technology Model. The condition parameters for symmetric NVSRAM simulation at different technology nodes are tabulated in Table 2.

The simulation results of power dissipation in terms of static and dynamic and delays in terms of read and write are summarized in Table 3. It can be seen that compared with the traditional 6TSRAM, the read and write SNM of the proposed 8T3R NVSRAM structure has been improved by 10% and 20%, respectively. It is found that the total power dissipation of 8T3R is 22.65% less than 6T SRAM cells.

Table 3. Simulation Results of symmetric 8T3R NVSRAM at different technology nodes.

Parameters	16 nm	20 nm	22 nm	32 nm
Write Delay (ps)	33.87	53.89	57.81	66.84
Read Delay (ps)	145.7	155.3	172	92.41
Static Power (nW)	2.78	2.78	0.34	5.17
Dynamic Power	14.16	17.52	9.54	18.06
RSNM (mv)	170	148	166	220
WSNM (mv)	554	536	560	636

Table 4 shows the performance parameters comparison results of 6T, 7T1R [32], 7T2R [23], 8T2R [30], and proposed 8T3R at 16 nm. The SNM graphs are in terms of hold, read, and write (Figure 6). The comparison graphs for 6T SRAM, NVSRAMs, and proposed 8T3R NVSRAM are compared at technology nodes 32 nm, 22 nm, 20 nm, and 16 nm, as shown in Figures 7–12.

Table 4. Comparison results of proposed symmetric NVSRAM with other NVSRAM's at 16 nm Technology.

Parameters	6T	7T1R	7T2R	8T2R	Proposed NVSRAM
Write Delay (ps)	50.53	52.2	52.19	53.16	53.14
Read Delay (ps)	61.52	62.63	86.52	87.98	89.8
Static Power (nW)	57.62	51.65	51.55	52.64	52.08
Dynamic Power (nW)	111	77.18	93.08	80.48	78.34
Total Power Dissipation (nW)	168.62	128.83	144.63	133.12	130.42
RSNM (mV)	139	119	153	140	162
WSNM (mV)	462	491	539	501	539

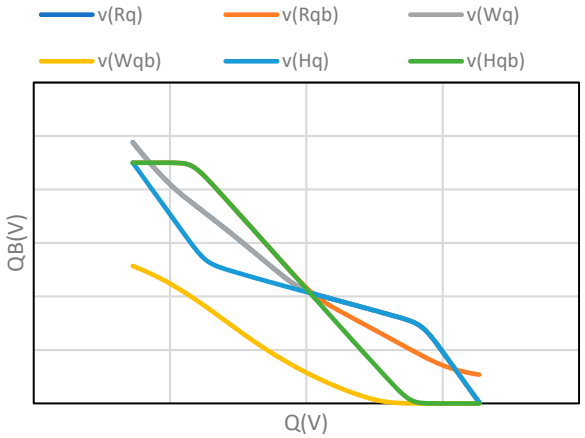


Figure 6. SNM curves of hold, read, and write of proposed symmetric NVSRAM cell.

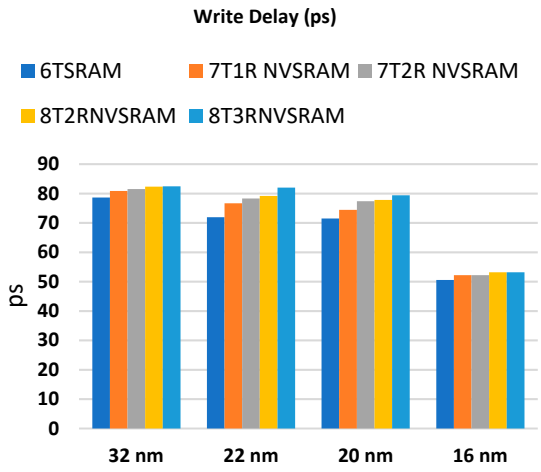


Figure 7. Write delay of different NVSRAMS and proposed NVSRAM cells.

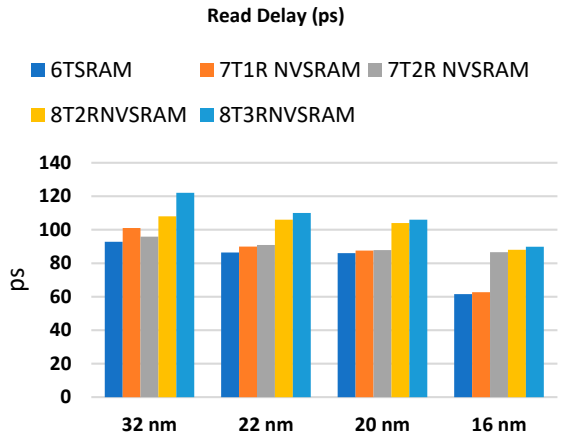


Figure 8. Read delay of different NVSRAMS and proposed NVSRAM cells.

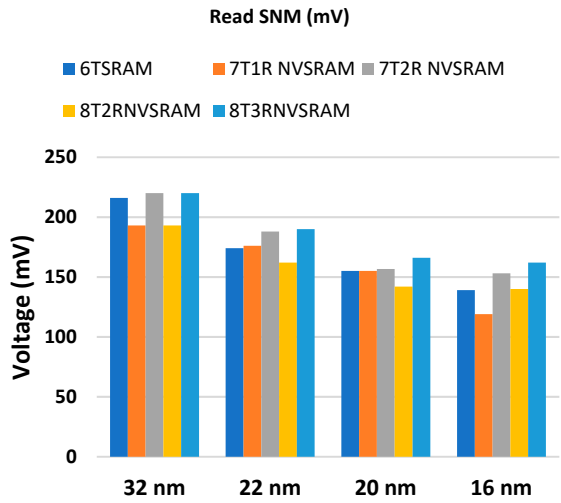


Figure 9. Read SNM of different NVSRAMS and proposed NVSRAM cells.

The clear observation is made by plotting the graphs of parameters such as delays, static and dynamic powers, read and write stability margins of NVSRAMs, and proposed 8T3R NVSRAM cells at 16 nm node. Even though the proposed cell takes compatible delays shown in Figures 13 and 14, the static or standby power dissipation of the proposed 8T3R NVSRAM is significantly reduced with respect to 6T SRAM. The other parameter, such as dynamic power, is greatly reduced. The proposed cell consumes less power than

all other NVSRAMs and as well as conventional 6T SRAM cell (Figures 11 and 12). It is decreased by an average of 28%. The static and dynamic power at 16 nm technology is represented in Figures 15 and 16. This design improved both the stability margins, read and write (Figures 9 and 10). The additional memristor used at NMOS transistors M3 and M4 improved read stability (Figure 17), with respect to 6T, 7T1R [32], 7T2R [23], and 8T2R [30], by 21%, 42%, 5%, 15%, respectively. From Figure 18, the WSNM over 6T, 7T1R [32], and 8T2R [30] is improved by 16%, 10%, and 7%, respectively.

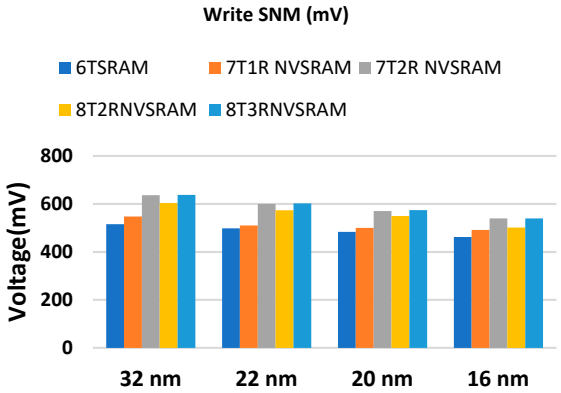


Figure 10. Write SNM of different NVSRAMS and proposed NVSRAM cells.

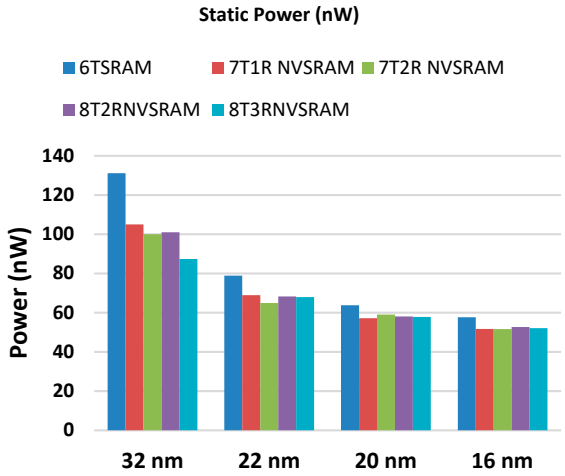


Figure 11. Static power dissipation of different NVSRAM cell.

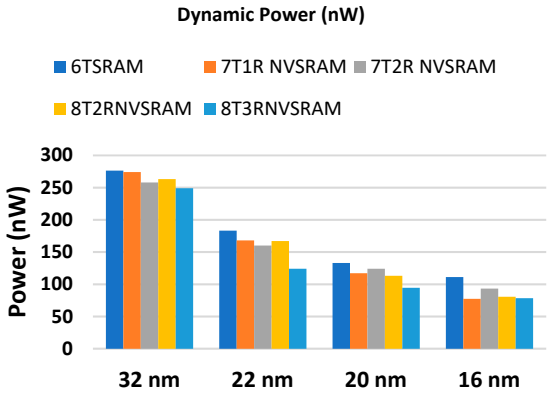


Figure 12. Dynamic power dissipation of different NVSRAMS and Proposed NVSRAM cells.

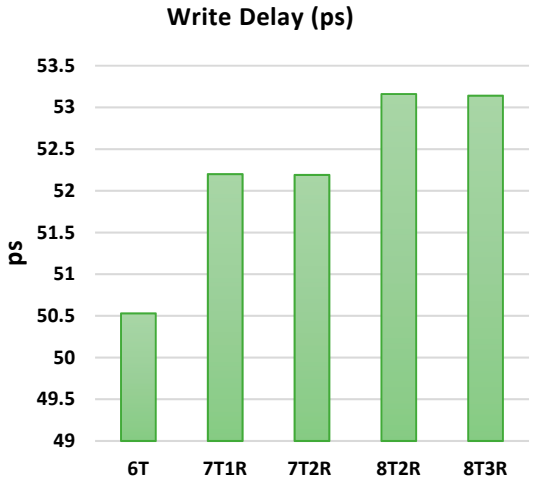


Figure 13. Write Delay of 6T SRAM, NVSRAMs, and proposed NVSRAM cells.

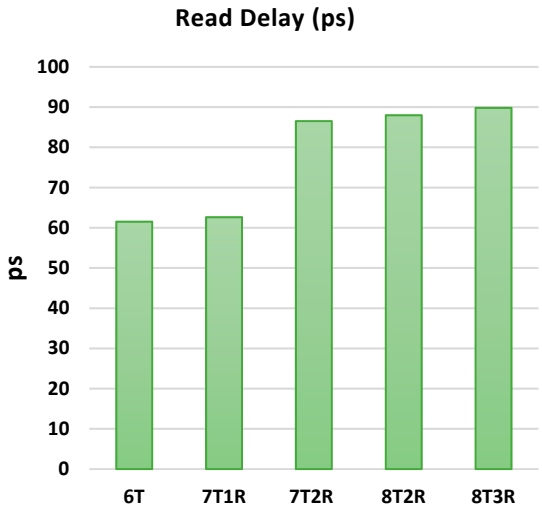


Figure 14. Read Delay of 6T SRAM, NVSRAMs, and proposed NVSRAM cells.

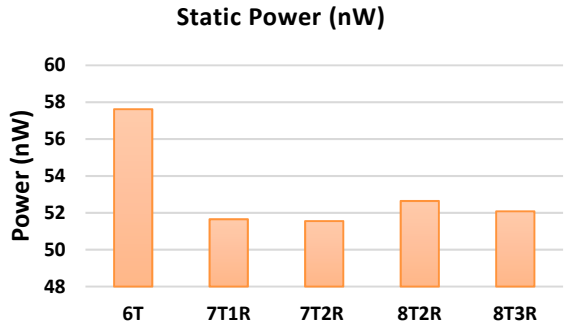


Figure 15. Static power dissipation of 6T SRAM, NVSRAMs, and proposed NVSRAM cells.

In summary, the proposed 8T3R design shows better performance than the 6T SRAM cell in terms of stability and power consumption and achieves non-volatile properties by using memristors. It also marks superior among the other NVSRAMs in terms of stability and power consumption.

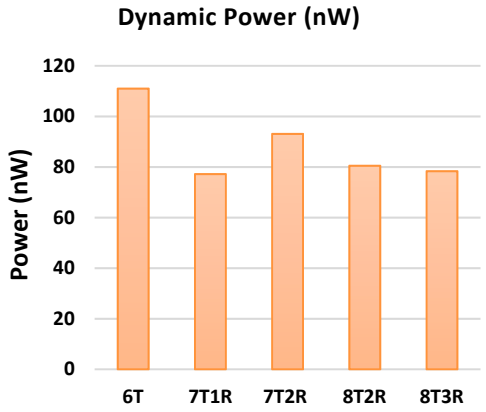


Figure 16. Dynamic power dissipation of 6T SRAM, NVSRAMs, and proposed NVSRAM cells.

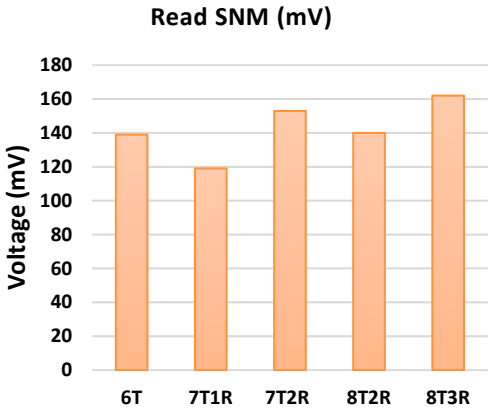


Figure 17. RSNM SNM of 6T SRAM, NVSRAMs, and proposed NVSRAM cells.

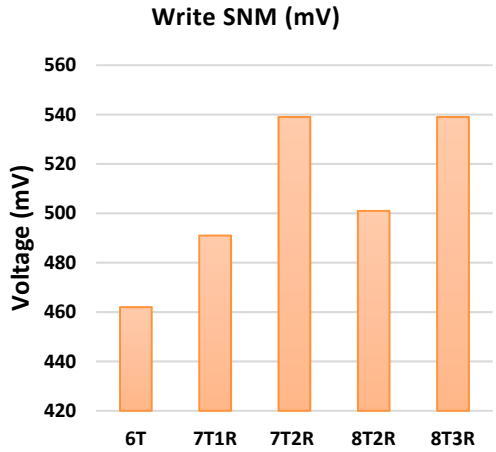


Figure 18. WSNM SNM of 6T SRAM, NVSRAMs, and proposed NVSRAM cells.

5. Conclusions

In this paper, a memristor-based symmetric 8T3R NVSRAM cell is designed and analyzed its performance at different technology nodes and compared with conventional 6T SRAM cells and other existing NVSRAM cells. The memristor R3 is connected at the source terminals of the NMOS transistors M3 and M4 and is used to stabilize read/write SNM, and the other two are connected at the data node of the core SRAM cell, which assesses SRAM as NVSRAM. The symmetric 8T3R NVSRAM cell successfully performed "normal SRAM, RESET, STORE, POWER DOWN, and RESTORE" operations. The read and write stability are improved by 10% and 20%, respectively; the static and dynamic power are also reduced by 15% and 28%, respectively, to conventional 6T SRAM cells. Compared

with other NVSRAMs, this proposed cell consumes less dynamic power since no additional RESET operation is required. This design has lower power dissipation because leakage power is reduced by using the NMOS M3 and M4 source memristor. Moreover, it has greater read and write stability than all other NVSRAMs discussed above. Due to higher stability and less power consumption, and leakage power, this work may provide a design and optimization method for non-volatile SRAM with RRAM devices. The designed symmetric 8T3R NVSRAM is feasible to assist normally off-computing applications. Hence, the memristor-based 8T3RNVSRAM cell constitutes a better non-volatile memory cell.

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