Article

Low Power SAR ADC Design with Digital Background Calibration Algorithm

Shouping Li, Jianjun Chen, Bin Liang and Yang Guo *

Department of Microelectronics, College of Computer Science, National University of Defense Technology, Changsha 410073, China; lishouping12@nudt.edu.cn (S.L.); chenjianjun@nudt.edu.cn (J.C.); binliang@nudt.edu.cn (B.L.)

* Correspondence: guoyang@nudt.edu.cn

Received: 24 September 2020; Accepted: 21 October 2020; Published: 23 October 2020

Abstract: This paper proposed a digital background calibration algorithm with positive and negative symmetry error tolerance to remedy the capacitor mismatch for successive approximation register analog-to-digital converters (SAR ADCs). Compensate for the errors caused by capacitor mismatches and improve the ADC performance. Combination with a tri-level switching scheme based on the common-mode voltage V_{cm} to achieve capacitor reduction and high switching energy efficiency. The proposed calibration algorithm significantly improves capacitor mismatch without resorting to extensive computation or dedicated circuits. The active area is 0.046 mm^2 in 40 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology. The post-simulation results show the effective number of bits (ENOB) improves from 8.23 bits to 11.36 bits, signal-to-noise-and distortion ratio (SNDR) improves from 51.33 dB to 70.15 dB, respectively, before and after calibration. This improves the spurious-free dynamic range (SFDR) by 24.13 dB, from 61.50 dB up to 85.63 dB. The whole ADC's power consumption is only 0.3564 mW at sampling rate $f_s = 2 \text{ MS/s}$ and Nyquist input frequency, with a figure-of-merit (FOM) 67.8 fJ/conv.-step.

Keywords: SAR ADC; mismatch; background calibration; power efficiency

1. Introduction

In recent years, various applications extensively use analog-to-digital converters, successive approximation register analog-to-digital converter (SAR ADC) domain in low power and medium-speed systems. SAR ADCs are essential in different types of sensors. For example, to detect all kinds of vital sign data of patients using biomedical device sensors. Environmental monitoring and surveillance use various sensors, such as gas-sensitive, light-sensitive, noise sensitive, and water pollution monitoring sensors. The precision of the ADC directly determines the quality of the sensors. A traditional fully differential capacitive charge-redistribution SAR ADC consists of four fundamental components: sample and holds (S&H) circuits, capacitive digital-to-analog (CDAC) circuit, dynamic comparator, and SAR control logic circuit. In this architecture, the capacitor mismatch is the main reason for deteriorating the whole ADC performance. Ref. [1] adopted a bypass technique which allows the design to search the capacitors with a sub-binary ratio without complexity, combined with a redundancy algorithm. Still, the error tolerance windows becoming asymmetric due to the search steps asymmetric. Ref. [2] designed an innovative input switch using 1.8 V devices in 28 nm technology, which makes it support up to 3.6 V inputs, achieve high precision at the area costs and power consumption. Ref. [3] presented a dynamic element matching (DEM) technique through residue oversampling to reduce capacitor mismatch and noise without calibration. Ref. [4] adopted 4-way interleaved and hybrid architecture achieve high speed, but capacitor mismatch and channel mismatch limited the precision due to absence of calibration. Ref. [5] presented a histogram-based ratio mismatch (HBRM) calibration

method for the capacitive bridge DAC to improve conversion nonlinearity and realize a high-speed SAR ADC, it needs additional calibration time. To correct the capacitor mismatch, Ref. [6] proposed a dither-based background calibration technique with a data-weighted averaging method but required extra circuits. Ref. [7] proposed a new circuit applied the negative DAC side to reduce the dielectric relaxation effect and improve ADC performance. Some other ADC adapts the hybrid structure to improve the sampling rate [8–10]. Design different switching strategies to reduce quantization error and power consumption [11]. Engineers and researchers do much research and work about digital calibration techniques to improve the capacitor mismatch [12]. Each of these structures has its advantages, mainly depending on the requirements of the application domain.

This SAR ADC is designed based on common-mode voltage V_{cm} with a tri-level switching method. Compare with the traditional structure, it only uses half of the unit capacitors. It can save a large proportion of switching energy consumption, the most significant bit (MSB) conversion without drawing any energy, and tri-level switch changing from common-mode voltage V_{cm} to the reference voltage V_{ref} or physical ground GND in every bit of the decision subsequently. Adopt a digital background calibration with redundancy capacitor array to minimize capacitor mismatch. Improve the ADC's static performance, such as differential nonlinearity (DNL) and integral nonlinearity (INL). The digital calibration method can make sure it is high speed and does not impact original circuits, and it is compatible with device scaling.

This paper mainly consists of five parts: Section 2 introduces the architecture of charge redistribution SAR ADC based on the common voltage V_{cm} with the tri-level switching method. Section 3 shows the digital calibration theory and implementation method. Section 4 displays the simulation results of ADC performance. Finally, a brief conclusion is presented in Section 5.

2. ADC Architecture

A unit capacitor C_{Rd} ($C_{Rd} = C_u$) adds to the capacitor arrays for signal sampling completeness. The unit capacitor C_{Rd} participates in the sampling process and does not participate in the quantization process. The total number of unit capacitors of the full differential N-bit charge redistribution SAR ADC is $2^N \cdot C_u$; Figure 1 depicts the structure of binary-weighted error compensation SAR ADC where it inserts three compensative capacitors array C_{2c} , C_{5c} , and C_{8c} , and the weight equal with C_2 , C_5 , and C_8 , respectively. The digital error correction logic circuit is generated by the design compiler to execute the error compensation. The DAC switching method saves a large proportion of switching energy and half of the capacitors than the conventional structure. When the ADC system starts to work, the two capacitor arrays' bottom plates start sampling the input signal. Then, the full differential dynamic comparator starts the first comparison.

Figure 1. The architecture of 12-bit full differential successive approximation register analog-to-digital converters (SAR ADC).

2.1. Switching Method

This design adopts the strategy by using the bottom plates of the capacitor array sampling the input signal to get better linearity. Bottom plate switches changing from common-voltage V_{cm} to reference voltage V_{ref} or physical ground GND in every bit of conversion. Moreover, the most significant bit (MSB) can determine without any switching energy consumption; V_{cm} based tri-level switching method example, as shown in Figure 2 with 3 bits conversion. The stepping size is directly proportional to the capacitor array's sizing during the binary search with this method. The input signal compares with $(\pm 2/4) V_{ref}$ according to the first comparison, switch turning up or down, connect with the reference voltage V_{ref} or physical ground GND in the DAC. For 12-bit SAR ADC, V_{cm} based tri-level switch structure produces switching energy consumption of $681.83 CV_{ref}^2$, saving 87.51% of changing energy consumption than the traditional DAC switch structure.

Figure 2. 3 bits V_{cm} based switching method example.

2.2. SAR Control Logic

The SAR control logic circuit is necessary to control the tri-level switches and digital codes output. At the beginning of conversion, sample and hold circuits sample the input signal, and all Flip-Flops are reset by the global reset signal at the same time. When the clock's rising edge is coming, the Flip-Flops

load the results from the comparator. MSB output is one or zero depending on the MSB switch control signal of the control logic to the DAC. Then the shift register ring counter shifts one when a bit has been decided until least significant bit (LSB). This type of shift register ring counter designed $M+4$ clock cycles to convert each sample, four clock cycles sampling sufficiently and steadily, and ensure the sampling bandwidth is larger than the Nyquist frequency. M clock cycles determine the MSB to LSB successively, including redundant code. This architecture keeps many advantages: Firstly, it is low power consumption based on V_{cm} architecture with a tri-level switching method; Besides, since the shift register ring counter and SAR control logic is iterative, it is easily extended to higher resolutions by just extending the shift registers, using this similar method, assign different clock period to an individual bit decision step is possibly and easily. Figure 3 shows the schematic of the SAR control logic and its timing diagram. CLK14 to CLK0 load the digital output codes from the comparator to the output register. After that, the digital output code feedback as control signals for the tri-level switches of lower capacitor array to accomplish the switching procedure. The digital calibration circuit performs 15b redundancy code to 12 b digital output code conversion simultaneously.

(a) SAR control logic

(b) Timing diagram

Figure 3. SAR control logic and timing diagram.

3. Calibration Implementation

In the design of charge redistribution SAR ADC uses many capacitors. The process deviation and the parasitic capacitance will inevitably cause the capacitor mismatch. Capacitor mismatch is the main cause of voltage error in conversion, directly affecting the ADC's performance.

3.1. Capacitor Mismatch

This design considers the impacts of the parasitic capacitance on the top and bottom plates of the capacitor array, the channel capacitance of the MOS switch, and the parasitic capacitance on the comparator input gate in the case of non-ideal layout and wiring. The parasitic capacitance on the top plate of the capacitor array will cause the amplitude attenuation of the input signal, which will reduce the effective power of the input signal. This design adopts a bottom plate sampling strategy to improve the linearity. The parasitic capacitance of the bottom plate on the capacitor array will seriously affect the input signal's linearity. This paper presents a digital background calibration technique based on capacitance array redundancy, reducing the voltage difference caused by parasitic capacitance and capacitor mismatch, thus improving the ADC's performance. The calibration algorithm ensures to reduce or even eliminate the maximum voltage error caused by capacitor array mismatch. Figure 4 shows the histogram of the Metal-Oxide-Metal (MOM) unit capacitor mismatch in 2000 times Monte Carlo simulations.

Figure 4. Unit capacitor mismatch Monte Carlo simulation.

3.2. Calibration Theory

This paper proposed one kind of a redundant research background calibration algorithm based on code-density. It starts to work with ADC operation simultaneously, converting the 15b redundant codes to 12b binary codes. In a redundant SAR ADC with M-step translate to N-bit (in which $M > N$), the original output bits (B_i 's and B_{ic} 's) and the actual decision values (D_{out} 's) are a function of actual

capacitor values as given in Equation (1). The swing of input signal shrink with a factor of α due to the redundancy capacitors, α can calculate with Equation (2), in this design, α is equal to 0.876, so the peak-to-peak of the input signal equal to reference voltage multiply the factor α , which is approximate 1.05 V. Overflow occurs when the signal swing is over the range, the digital output codes will be a settlement to the value from 0 to 4095 to keep the function normal and prevent data from spilling up or down. Figure 5 shows an example of the digital background calibration process.

$$D_{out} = \sum_{i=0}^{N-1} (B_i \times 2^i) + \sum_{i=2,5,8} (B_{ic} - 0.5) \times 2^i \quad (1)$$

$$\alpha = \frac{\sum_{i=0}^{N-2} 2^i \cdot C_u + C_{Rd}}{(\sum_{i=0}^{N-2} 2^i \cdot C_u + C_{Rd}) + \sum_{i=2,5,8} 2^i \cdot C_{ic}} \quad (2)$$

Figure 5. Example of the digital background calibration process.

Previous research introduces a ditched-based background calibration algorithm to improve precision in exchange for extra power consumption and design complexity. In the non-binary weighted capacitor array design, the redundancy calibration algorithm may be ineffective in correcting dynamic switching errors as the asymmetry error tolerance windows. In this design, the redundancy capacitor array helps improve the conversion rate by symmetry error-tolerance windows, especially at the first few MSBs because of massive voltage change during transitions. The redundancy capacitor array combines with the common voltage V_{cm} based tri-level switching method, as shown in Figure 2. In the binary-weighted search method, the stepping size is equal to the corresponding capacitor array proportion in the overall capacitor array. Around each decision level, the stepping sizes and the error-tolerance windows are symmetric. Combine the redundant capacitors array digital background calibration algorithm with the tri-level switching method. The complexity of circuit design is reduced, but also achieves symmetric error tolerance windows with ± 292 LSB.

4. Simulation Results

To test and verification the static and dynamic performance, ADC operates at a sampling rate of 2 Million Samples Per Second (MSPs) and Nyquist full-scale sine wave input signal. Figure 6 displays the differential nonlinearity (DNL) and integral nonlinearity (INL) before and after the calibration. Before calibration, the maximum DNL is $+1.2/-1.1$ LSB, and the maximum INL is $+13.1/-13$ least

significant bit (LSB). After calibration, the maximum DNL reduce to $+0.7/-0.6$ LSB, and the maximum INL reduce to $+1.1/-1.0$ LSB. Figure 7 shows a 4096-points Fast Fourier Transform (FFT) simulation results of the dynamic performance. Before calibration, the signal-to-noise-and-distortion ratio (SNDR) is 51.33 dB, and the spurious-free dynamic range (SFDR) is 61.50 dB, and the effective number of bits (ENOB) is 8.23 bits. After calibration, the SNDR up to 70.15 dB, SFDR up to 85.63 dB, and ENOB up to 11.36 bits. The total power consumption is as low as 356.4 μ W, and a figure-of-merit (FoM) is 67.80 fJ/conv.-step.

Figure 6. Simulation results of DNL and INL before and after calibration.

Figure 7. 4096-point output FFT spectrum.

The differential nonlinearity and integral nonlinearity with 1000 times Monte Carlo simulations before and after calibration, respectively, as shown in Figure 8. The simulation results show that the digital background calibration algorithm improves the static performance significantly.

The effective number of bits with 1000 times Monte Carlo simulations before and after calibration, respectively, as shown in Figure 9. This indicates that the ENOB normalizes distribution with 8.23 bits mean and 0.43 bits standard deviation before calibration improves to 11.36 bits mean and 0.21 bits standard deviation after calibration. The simulation results show that the digital background calibration algorithm improves dynamic performance significantly.

Figure 10 shows the SNDR and SFDR vary with the input frequency at a constant sampling rate of $f_s = 2$ MS/s. Both the SNDR and SFDR are decreasing slightly with the input frequency increase before and after calibrations. Both SNDR and SFDR improved significantly after calibration.

The breakdown of the power consumption of the SAR ADC test chip is shown in Figure 11. The comparator, capacitor digital-to-analog converter (CDAC), and sample and hold circuits are the main proportion of power consumption. The digital background calibration circuitsonly account for 6% of overall power consumption.

Figure 8. DNL and INL Monte Carlo simulation.

Figure 9. The effective number bits (ENOB) Monte Carlo simulation.

Figure 10. Dynamic performance before and after calibration.

Figure 11. SAR ADC power consumption breakdown.

The performance comparison and summary of the prototype ADC display in Table 1 shows that previous research is all 12 bits SAR ADC. Our design has excellent advantages in SNDR, SFDR, ENOB, and power consumption.

Table 1. Performance comparison with other published SAR ADC.

Specifications	Ref. [2]	Ref. [3]	Ref. [4]	This Work
Architecture	SAR	SAR	SAR	SAR
Technology(nm)	28	40	28	40
Supply(V)	1.8	1.0	1.2/1.5	1.2
Sampling Rate(MS/s)	4	40	600	2
Resolution(bit)	12	12	12	12
SNDR(dB)	70.1	63.46	60.7	70.15
SFDR(dB)	84.3	73.72	—	85.63
ENOB(bit)	11.35	10.25	9.79	11.36
DNL(LSB)	+0.2/−0.2	+0.51/−0.49	—	+0.7/−0.6
INL(LSB)	+0.6/−0.6	+1.95/−1.44	—	+1.1/−1.0
Power(mW)	1.73	1.25	26.5	0.3564
FOM(fj/conv.-step)	165.5	25.7	68	67.80
Active Area(mm ²)	0.13	0.04	0.076	0.046

The test chip of this SAR ADC is the implementation in standard 1P8M 40 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology with Metal-Oxide-Metal (MOM) capacitors and 1.2 V core power supply. The active die area is 0.046 mm². The whole test chip micrograph, as shown in Figure 12.

Figure 12. Test Chip Micrograph.

5. Conclusions

This paper proposed a digital background calibration algorithm, combined with the common voltage V_{cm} based switching method and redundancy capacitors to correct the decision errors due to incomplete setting and capacitor arrays mismatch. Applied to a 12-bit full differential SAR ADC, the test chip implemented in standard 40 nm CMOS technology, at Nyquist full-scale sine wave input and 2 MSPs sampling rate reached SNDR 70.15 dB, SFDR up to 85.63 dB, ENOB is 11.36 bits. DNL and INL are +0.7/−0.6 LSB and +1.2/−1.1 LSB, respectively.

Author Contributions: S.L. designed the circuits, analyzed the measurement data, and wrote the manuscript. J.C. assisted the circuits analysis and implementation, gave some valuable guidance, confirmed the manuscript's final version. Contributed to the technical discussions, and reviewed the manuscript. B.L. responsible for project administration. Y.G. performed supervision and funding acquisition. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Natural Science Foundation of China Program, under Grant 61772540 and Grant 61974163.

Acknowledgments: This research was supported by the Graduate Innovation Center for Microelectronics and Microprocessors and funded by the National Natural Science Foundation of China Program.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Liu, W.; Huang, P.; Chiu, Y. A 12b 22.5/45MS/s 3.0 mW 0.059 mm² CMOS SAR ADC Achieving over 90dB SFDR. In Proceedings of the 2010 IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 7–11 February 2010; pp. 380–381.
2. Berens, M.; Mai, K.; Feddeler, J.; Pietri, S. A General Purpose 1.8-V 12-b 4-MS/s Fully Differential SAR ADC With 7.2-Vpp Input Range in 28-nm FDSOI. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1785–1789. [\[CrossRef\]](#)
3. Hsu, C.; Chang, S.-J.; Huang, C.-P.; Chang, L.-J.; Shyu, Y.-T.; Hou, C.-H.; Tseng, H.-A.; Kung, C.-Y.; Hu, H.-J. A 12-b 40-MS/s Calibration-Free SAR ADC. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2018**, *65*, 881–890. [\[CrossRef\]](#)
4. Venca, A.; Ghittori, N.; Bosi, A.; Nani, C. A 0.076 mm² 12 b 26.5 mW 600 MS/s 4-Way Interleaved Subranging SAR-ΔΣ ADC With On-Chip Buffer in 28 nm CMOS. *IEEE J. Solid-State Circuits* **2016**, *51*, 2951–2962. [\[CrossRef\]](#)
5. Zhu, Y.; Chan, C.; Wong, S.; Seng-Pan, U.; Martins, R.P. Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC. *IEEE Trans. Large Scale Integr. (VLSI) Syst.* **2016**, *24*, 1203–1207. [\[CrossRef\]](#)

6. Wang, P.; Sun, J.; Wu, J. Dither-based background calibration of capacitor mismatch and gain error in pipelined noise shaping successive approximation register ADCs. *Electron. Lett.* **2019**, *55*, 984–986. [[CrossRef](#)]
7. Matsui, T.; Sento, K.; Ebata, T.; Ishibashi, A. A Capacitor Dielectric Relaxation Effect Cancellation Circuit in a 12-Bit, 1-MSps, 5.0-V SAR ADC on a 28-nm Embedded Flash Memory Microcontroller. *IEEE Solid-State Circuits Lett.* **2019**, *2*, 95–98. [[CrossRef](#)]
8. Liu, C.-C.; Huang, M.-C.; Tu, Y.-H. A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC. *IEEE J. Solid-State Circuits* **2016**, *51*, 2941–2950. [[CrossRef](#)]
9. Chung, Y.; Yen, C.; Tsai, P.; Chen, B. A 12-bit 40-MS/s SAR ADC with a Fast-Binary-Window DAC Switching Scheme. *IEEE Trans. Large Scale Integr. (VLSI) Syst.* **2018**, *26*, 1989–1998. [[CrossRef](#)]
10. Zhong, J.; Zhu, Y.; Chan, C.; Sin, S.; Seng-Pan, U.; Martins, R.P. A 12b 180MS/s 0.068mm² With Full-Calibration-Integrated Pipelined-SAR ADC. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 1684–1695. [[CrossRef](#)]
11. Chung, Y.; Zeng, Q.; Lin, Y. A 12-bit SAR ADC With a DAC-Configurable Window Switching Scheme. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 358–368. [[CrossRef](#)]
12. Collins, N.; Tamez, A.; Jie, L.; Pernillo, J.; Flynn, M.P. A Mismatch-Immune 12-Bit SAR ADC with Completely Reconfigurable Capacitor DAC. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 1589–1593. [[CrossRef](#)]

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).