

Review

# Van der Waals Heterostructure Based Field Effect Transistor Application

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**Abstract:** Van der Waals heterostructure is formed by two-dimensional materials, which applications have become hot topics and received intensive exploration for fabricating without lattice mismatch. With the sustained decrease in dimensions of field effect transistors, van der Waals heterostructure plays an important role in improving the performance of devices because of its prominent electronic and optoelectronic behavior. In this review, we discuss the process of assembling van der Waals heterostructures and thoroughly illustrate the applications based on van der Waals heterostructures. We also present recent innovation in field effect transistors and van der Waals stacks, and offer an outlook of the development in improving the performance of devices based on van der Waals heterostructures.

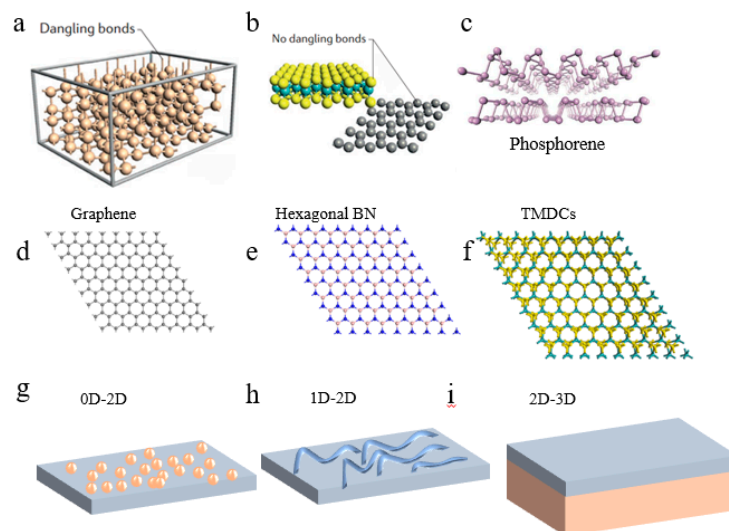
**Keywords:** van der Waals heterostructure; field effect transistor; two-dimensional material

## 1. Introduction

In the past few decades, graphene, which exhibits extraordinary electronic and optoelectronic properties in exploring low-dimensional materials, has become the most advanced research in the field of two-dimensional layered material (2DLM) science, solid-state physics and engineering [1–3]. Because graphene originally has excellent parameters, such as mechanical stiffness, strength and elasticity, very high electrical and thermal conductivity, graphene-based transistor preforms better than conventional Si-based transistors [1] in fabricating high-frequency transistors with the possible cut-off frequency  $f_T = 1\text{THz}$  at a channel length of about 100 nm [4] and photodetectors with a wide spectral from ultraviolet to infrared [1]. Therefore, the discovery of graphene creates a new generation of electronic devices with atomically thin geometry and unprecedented combination of speed and flexibility. Except for the advantages and merits of graphene-based transistor mentioned above, there are some shortcomings, such as the unique zero bandgap, hindering the graphene's application in electronic industry [3]. To overcome the defect brought by graphene device, this extensive library of 2DLMs, such as graphene, phosphorene, hexagonal boron nitride and transition metal dichalcogenide mentioned in this article with selected properties opens up the possibility of heterogeneous integration at the atomic scale, creating novel hybrid structures that display totally new physics and enable unique functionality [5]. Because 2DLMs have various bandgap, the different material shows different property. For example, black phosphorus shows the characteristic of conductor; molybdenum disulfide ( $\text{MoS}_2$ ) and tungsten selenide ( $\text{WSe}_2$ ) are semiconductors; and boron nitride (BN) performs as insulator. 2DLMs with various properties make it possible to form special combination of heterogeneous integration at atom scale, such as van der Waals heterostructures (vdWHs).

In general, heterostructures formed by 2DLM monolayers are assembled by covalent bond force within layers and stacked together by van der Waals force between layers. Thus, there is no free dangling bond between 2DLM layers. In contrast to typical nanostructures persecuted by dangling

bond and trap state on the surfaces [6], monolayer are free of these disadvantages (Figure 1a,b) and exhibit extraordinary electronic and optoelectronic properties. Additionally, without free dangling bonds, the interface between neighbor 2DLM layers are assembled by van der Waals forces, which is much weaker than chemical bond force. Therefore, the van der Waals heterostructure can be easily isolated by exfoliation with the help of taps [7]. Although some highly disparate materials have a great lattice mismatch in creating heterostructure, those can be assembled together by van der Waals force. This allows diverse 2DLMs to construct various van der Waals heterostructures (vdWHs) with completely novel properties and functions.



**Figure 1.** Two-dimensional layered materials and van der Waals heterostructures: (a,b) materials with and without dangling bond; (c) anisotropic transport behavior of phosphorene in different direction; (d–f) monolayer graphene, hexagonal boron nitride and transition metal dichalcogenides, graphene shows semimetal characteristic, hexagonal boron nitride behaves as insulator and transition metal dichalcogenides act as semiconductor; (g–i) van der Waals heterostructure formed with free dangling bond materials; (g) 0D (particles or quantum dots) and 2D layered materials stack; (h) 1D (nanowires) and 2D layered materials stack; and (i) 2D layered materials and 3D bulk materials stack. (a–e) are reproduced with permission from Nature Publishing Group, Ref [6,8].

The early study in vdWHs focus on the combination of 2DLMs with 0D (for example, plasmonic nanoparticles and quantum dots) and 1D (for example, nanowires and nanoribbons) nanostructures [9–12]. These novel 0D–2D (Figure 1f) and 1D–2D (Figure 1g) vdWHs structures have fabricated many highly performed devices, such as photodetectors with highly optical response [10] and transistors with high speed and flexibility [12]. In recent years, most efforts have been taken to form 2D–2D integration vdWHs by vertically stacking various 2DLMs; for example, Dean fabricated a graphene–BN heterostructure transistor which Hall mobility reached  $\sim 25,000 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  at high density [13], and Withers stacked metallic graphene, insulating hexagonal boron nitride and various semiconducting monolayers into complex but carefully designed sequences, which exhibited an extrinsic quantum efficiency of nearly 10% and the emission can be tuned over a wide range of frequencies by appropriately choosing and combining 2D semiconductors [14]. 2D–2D vdWHs with diverse 2DLMs make it possible to accurately control and modulate the transport of charge carriers, excitons and photons within the atomic surface, and greatly promote the new generation of unique devices. Apart from 2D–2D vdWHs, 2DLMs can also be integrated with 3D bulk materials to form 2D–3D structures [8,15] (Figure 1f–h), which attract some interest. Hot electron transistors based on 2D–3D heterojunctions have been reported [16]. Gate tunable p–n junctions based on 2D–3D

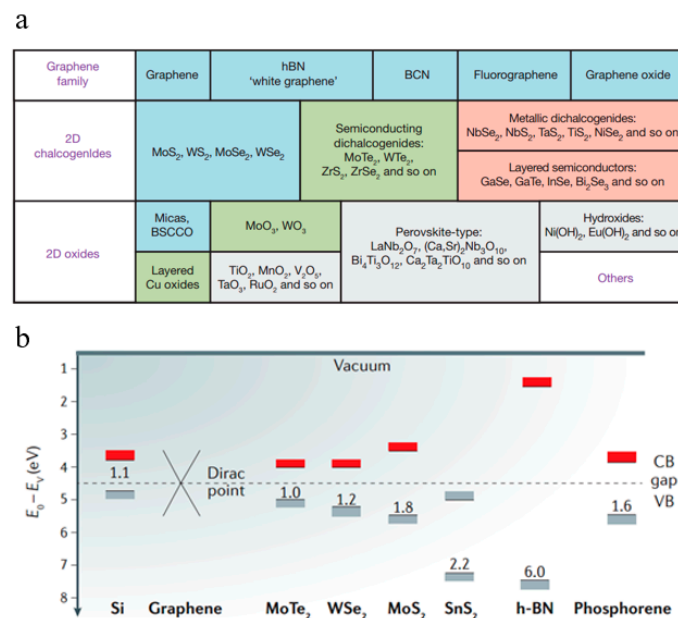
heterojunctions have been reported [17,18]. Heterojunction formed with MoS<sub>2</sub> and p type Ge can fabricate high performance tunneling field transistor [18].

Recently, most vdWHs are formed by mechanically stacking different monolayers together. Although this method allows great flexibility, it is slow and inconvenient. Thus, some simple and high-quality techniques are being developed, for example, large-area 2DLMs grown by chemical vapor deposition (CVD) and direct growth of heterostructure by CVD or physical epitaxy, which improves the growth quality of monolayers and the properties of heterostructure exhibited [19–21].

In this review, we mainly concentrate on the integration, properties, application and technology of vdWHs. First, we give a brief introduction of typical materials, which got highly unprecedented attention in the field of materials science and solid-state physics in the past few years, and discuss the electronic properties about them. Then, we focus on the applications of field effect transistors based on vdWHs, including elevating mobility, decreasing the contract resistance and conventional transistors like tunneling field effect transistor. Except for traditional FETs, we investigated some late-model structure, namely the vertical thin film transistor. Finally, we analyze the process of mechanically and chemically stacking van der Waals heterostructures. Meanwhile, we discuss the process of fabricating the field effect transistors (FETs) by van der Waals stacking methods.

## 2. Two Dimensional Materials

Two-dimensional materials, which constitute van der Waals heterostructures (vdWHs), have been explored to exhibit entirely different characteristics (Figure 2a), including conductors, semimetals, semiconductors, and insulators. Large group of two-dimensional materials provide various band gap and different electronic and optical performance, which offers the theoretical possibility of different device application requirement. With different 2D materials to form heterostructure, not only novel properties can be observed but also highly reliable nano-device can be achieved as well.



**Figure 2.** Different 2D layered materials and electronic properties. (a) Classified 2D layered materials based on different conductive characteristic. Monolayers proved to be stable in air condition are marked as blue. Those probably stable in air are shaded green. Those monolayers stable in inert atmosphere are shaded pink. Grey shading shows that monolayer can be successfully exfoliated from bulk materials. Reproduced with permission from Nature Publishing Group, Ref [22] (b) Band gaps of 2D layered materials compared with Dirac point. Reproduced with the permission from IEEE in Ref [23].

### 2.1. Graphene

With a honeycomb lattice structure assembled by strong covalent bond force, crystal structure shown in Figure 1d, graphene only has a single atomic carbon layer, which can be manufactured via mechanically exfoliating from bulk graphite. Due to bulk graphite has weak interlayer connection formed by van der Waals force, the large-area monolayer graphene can be easily and successfully exfoliated from bulk material with the help of a scotch tape. Owing to the unique lattice structure and atom combination, graphene has zero band gap which means charge carriers move in a ultrahigh speed about  $25,000 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  at room temperature [24]. In other words, with high conductivity in 2DLMs family, graphene behaves like metal, which is the significant component of forming vdWHs. Transistors with graphene electrodes will have a lower contact resistance compared to transistors without graphene electrodes [25]. In flash memory devices, graphene also acts as charge trap layers [26]. Due to the single-atom thickness and specific density of state (DOS), it exhibits partial optical and electrostatic transparency under tunable work function. For possessing this characteristic, graphene serves as contact material integrated with other two-dimensional semiconductors in vdHW transistors, which achieves an appropriate contact resistance and admirable electrical performance [27].

Bilayer graphene, which is constituted of two atomic carbon-layers stacked by van der Waals interaction under specific direction, does not exhibit the same properties as monolayer graphene. That is because the interaction between two neighboring layers provides extra van der Waals electric field, which inducts bilayer's bandgap [28] and forms four pseudospin flavors [29]. Although bilayer graphene has a band gap up to 250 mV under gate controlling, it is still smaller than other 2DLM like transition metal dichalcogenide, and even bulk Si (the band gap is about 1.2 eV). Even though monolayer graphene has zero band gap, it can be used in other ways such as graphene electrode in transistor, charge trap layer in flash memory and metal-graphene interfaces which can provide photo-generated carriers in photodetectors [30,31]. Moreover, bilayer graphene transistors also have a degradation of the carrier mobility compared with monolayer graphene [2].

### 2.2. Transition Metal Dichalcogenide

Transition metal dichalcogenide (TMDC) is the group of two-dimensional materials with chemical form  $\text{MX}_2$ , where M stands for transition metal (molybdenum and tungsten) and X represents for the chalcogenide (sulfur, selenium or tellurium). The arrangement of atomic layered TMDC is X-M-X form. The crystal structure is shown in Figure 1f. Considering the same reason that adjacent layers of TMDC are weakly held together by van der Waals force, monolayers of TMDC can also be directly split from bulk crystals (regardless of artificiality or natural mineral) by scotch tape, called mechanical exfoliation, and it can also be fabricated by chemical vapor deposition (CVD) processes [32,33]. From bulk structure to two-dimensional layered structure, the most frequently studied TMDCs, such as  $\text{MoS}_2$ ,  $\text{MoSe}_2$ ,  $\text{WS}_2$  and  $\text{WSe}_2$ , show various band gaps (Figure 2b) and tunable electronic properties with its volume changing from bulk material to monolayer [16]. At room temperature, as the thickness of TMDC decreases from bulk to monolayer, its band gap ranges from 1 eV to 2 eV and carrier mobility reaches over  $100 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ . Owing to the varied bandgap resulting in tunable electrical characteristics, there are some distinctive properties observed in TMDC, for example, valley Hall effect [34], valley polarization [35], superconductivity [36] and photoelectric characteristic [37,38]. TMDC's lack of dangling bands is another reason that makes it attractive for use in FET channel material. This means the lattice mismatching is out of consideration during the formation of TMDC-TMDC van der Waals interconnection.

### 2.3. Phosphorene

Phosphorene is a monolayer material constituted of phosphorus, with a vertically interlaced hexagonal lattice that looks like armchairs. Phosphorene's bandgap varies from 0.33 eV to 1.5 eV depending on the number of layers stacked [39]. Notably, an individual property is observed

in few layers of phosphorene, i.e., anisotropic transportation in different phosphorene's crystal orientations [40]. Specifically, transporting in the armchair direction (x direction) is much more efficient than in zigzag direction (Figure 1c). In addition, a p-type semiconductor characteristic emerges in phosphorene. When the hole mobility exceeds  $1000 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  in certain direction [41], the phosphorene becomes the significant 2D material for electronic device. Later report shows that the drain current of FETs based on phosphorene can be modulated to  $10^5$ , which means the  $I_{\text{on}}/I_{\text{off}}$  ratio reaches  $10^5$  [42]. The tunable bandgap of phosphorene make it possible to react with different spectral regime from visible to infrared, which can be applied in fabricating multispectral photodetector [43].

The main challenge for phosphorene's extensive application is the environmental stability, which means it can be easily oxidized [44]. To prevent the surface oxidation which leads to the decrease of device performance, some solutions have been adopted, for example, using h-BN [45], atomic layer of  $\text{Al}_2\text{O}_3$  [46,47] and hydrophobic fluoropolymer [48] as encapsulating materials during process of van der Waals stacking.

#### 2.4. Hexagonal Boron Nitride

Hexagonal boron nitride (h-BN), also called white graphite, has the same lattice structure as graphite. (Figure 1e) For boron and nitrogen are combined together by the strong covalent  $\text{sp}^2$  hybridized chemical bond, h-BN exists as insulator with a large bandgap of 6 eV [49]. Mechanical exfoliation can provide an atomically smooth surface without dangling bond and carrier traps, so a few layers of h-BN can be used as ultra-flat insulating substrates, the gate dielectrics [50] and ideal encapsulate material [24] in heterostructure transistors [13]. Besides, ultrathin h-BN can be served as great tunneling barrier material in tunneling devices [51,52].

#### 2.5. Other Various 2D Materials for vdWHs

In the past few years, novel 2D TMDCs draw a lot of concentration on creating new types of devices; meanwhile, traditional 2D materials such as  $\text{MoS}_2$  and  $\text{WSe}_2$  have been considered once more. In virtue of doping technology, high-k amorphous titanium suboxide (ATO) is used as an n-type charge transfer dopant on the monolayer  $\text{MoS}_2$ , which decreases the contact resistance to  $180 \Omega \cdot \mu\text{m}$  [53]. Utilizing  $\text{AlO}_x$ , another method of n-type doping in  $\text{MoS}_2$  is demonstrated, which can also reduce the contact resistance to  $480 \Omega \cdot \mu\text{m}$  [54]. After confirming operational parameters of chemical vapor deposition, ultrathin  $\text{MoS}_{2(1-x)}\text{Se}_{2x}$  alloy nano-flakes with atomic or few-layer thickness can be obtained and it have high activity and durability during the hydrogen evolution reaction [55]. These various 2D materials show variable bandgaps, tunable optical and electronic properties [56,57].

### 3. Techniques

Two-dimensional materials can be assembled or grown directly into heterostructures, where the monolayers are held together by van der Waals forces. Although variety of 2D materials have been found, the assembly techniques currently used allow only certain types to build up the heterojunction. At the same time, the alternative technique, called sequential growth of monolayers, potentially do well in large scale production. Actually, the growth method has some limitations, such as slow growth and hard to control, and is still in early stages. Nevertheless, a great number of experiments with van der Waals heterostructure indicate that 2D materials are versatile and practical for further applications [58].

#### 3.1. Assembly

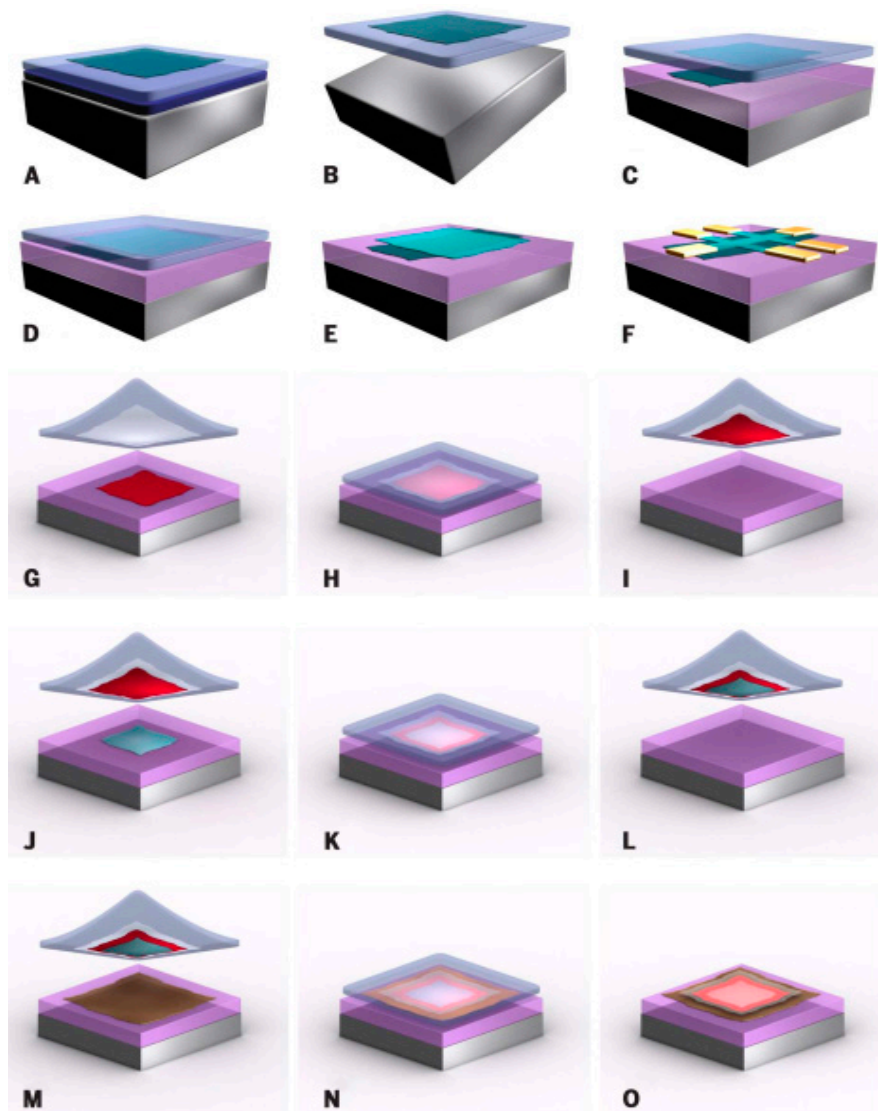
Direct mechanical assembly is the most commonly used techniques of assembling heterostructures at present. This techniques was been put forward in 2010 by Dean et al., who demonstrated a very high level of performance provided by graphene and h-BN [13].

In early works, the technique is only used in preparing a flake of 2D material on a sacrificial membrane, such as PDMS, aligning and placing it on the substrate, and then remove or dissolve the membrane (Figure 3A–G). Then, the progress is repeated to deposit the other 2D material on the top of



the former layer. Because the materials have close contact with the sacrificial layer, which is dissolved finally, the interface between TMDC and sacrificial layer will be contaminated. However, annealing can remove this contamination and achieve high interface quality, so the mobility of graphene device can reach  $10^6 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  [13].

The other substantially cleaner method has the same principle that van der Waals interaction exist between layers. After sticking the first layer onto membrane, the second layer is directly stuck on the first layer, instead of dissolving the membrane (Figure 3G–O). Then, the process is repeated several times to get expected multilayer. This method leads to cleaner interface over large areas, and higher electron mobility.



**Figure 3.** Assemble van der Waals heterostructures techniques: wet-transfer and pick-and-lift. (A–F) Wet-transfer technique: (A) A 2D crystal prepared on a sacrificial layer. (B) Pick up the sacrificial layer with 2D material. The layer is then placed on (C) and the second layer is transferred the same way (D). Then, it is placed on top of the first layer (E). Deposited metal on the proper location (F). (G–O). Pick-and-lift technique: A 2D material on a membrane is aligned (G) and then placed on top of another 2D crystal (H). The process is repeated to lift additional crystals (I–L). Finally, the whole multilayer is placed on the substrate (M–O), and the membraned is dissolved. Reused with the permission from American Association for the Advancement of Science in the Ref [58].

### 3.2. Growth Methods

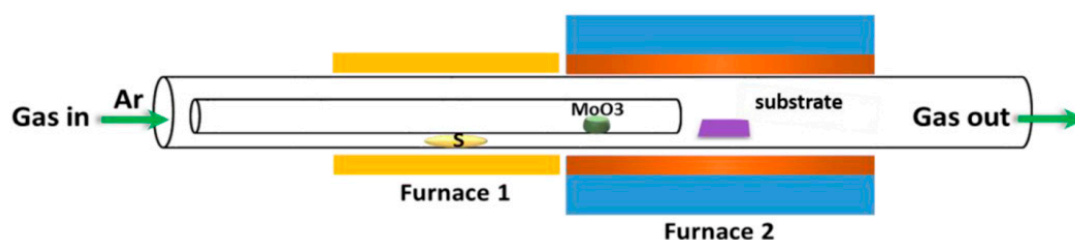
Although the assembly methods can stack the layers and achieve a clean interface, it still has some disadvantages, for example, the stacking position cannot be accurately controlled, which affects the device properties [22]. The direct growth of vertical layered heterostructures via chemical vapor deposition (CVD) is much more promising in terms of being controllable and scalable.

The direct growth of heterostructures can be divided into two parts: (1) sequential CVD growth of 2D materials layered; and (2) molecular beam epitaxy (MBE). The detailed information is presented in the following.

#### 3.2.1. CVD

For the CVD system of  $\text{MoS}_2$  growth, as depicted in Figure 4, two separated furnaces are used to precisely control temperature applied on both precursors and substrate. Sulfur powder and the substrate are in the same pipe while different furnaces, where the interaction temperature can be independently controlled. Twenty milligrams of  $\text{MoO}_3$  powder, which temperature is dominated by furnace 2, is loaded between sulfur powder and the substrate and has an independent mini-pipe (diameter 1 cm). This is to prevent any cross-contamination and reaction between sulfur and  $\text{MoO}_3$ , resulting in the decrease amount of  $\text{MoO}_3$  and unstable precursor supply in the vapor phase. Typical growth temperatures used for sulfur,  $\text{MoO}_3$ , and the substrate are  $\sim 180^\circ\text{C}$ ,  $\sim 300^\circ\text{C}$ , and  $\sim 800^\circ\text{C}$ , respectively. To ensure the sufficient supply of sulfur vapor in the system, it is preheated before increasing the temperature of  $\text{MoO}_3$ .

This simple but scalable CVD growth approach can realize the direct fabrication of large-area  $\text{MoS}_2/\text{h-BN}$  heterostructures with cleaner interface and better contact, compared with mechanical transfer method or assembly methods [59].



**Figure 4.** Schematic illustration of CVD growth methods for  $\text{MoS}_2$  growth. Reproduced with permission from American Chemical Society Publishing Group in Ref [59].

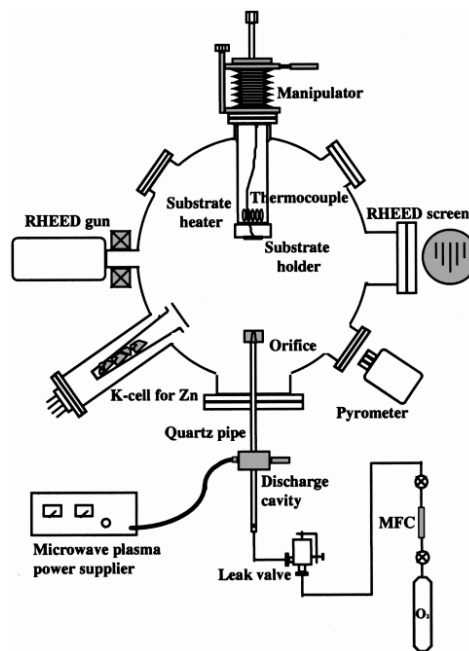
#### 3.2.2. MBE

As one of the most commonly used growth methods of heterostructures, CVD has successfully accomplished several two-dimensional layered materials [60]. Although it is almost theoretically perfect, the reaction condition of CVD is hard to control at present and the results reported publicly can only form a few well-defined islands over the entire wafer. Considering the defects, MBE is an alternative approach for CVD in some ways [61].

As the name suggests, MBE is a kind of physical deposition method that takes place in ultrahigh vacuum. Figure 5 shows a typical MBE system. The required components are heated into vapor and sprayed on the substrate through a small hole. At the same time, a controlling molecule beam is used to scan the substrate line by line, and the molecules or atoms are arranged layer by layer in lattice structure. The ultra-high vacuum (UHV) environment minimizes the contamination of the interface between substrate and growing flake. Because there are few particles in UHV environment, the ionized atoms and molecules traveled in nearly collision-free path until hitting the substrate or the chilled oven walls, where atoms condense immediately, and thus are effectively cleaned up from the reacting system without extra contamination. Because the components are sprayed onto substrate through a

small hole, it can be turned off almost instantly and changed into another reactant whenever necessary. Most importantly, MBE growth can be simplistically described as “spray painting” the substrate crystal with layers of atoms, changing the composition or impurity in each layer until a desired structure is obtained [62].

Compared with CVD, MBE can potentially grow products overspread the whole wafer, precisely control the rate of interaction by means of regulating the rate of spraying and easily change the reactant as requirement. In this sense, MBE is almost the ideal method of vdWHs fabrication since the composition can be precisely controlled layer by layer.



**Figure 5.** Schematic diagram of the MBE system. Reproduced with the permission from American Institute of Physics in the Ref [63].

#### 4. FETs Based on Heterostructures Applications

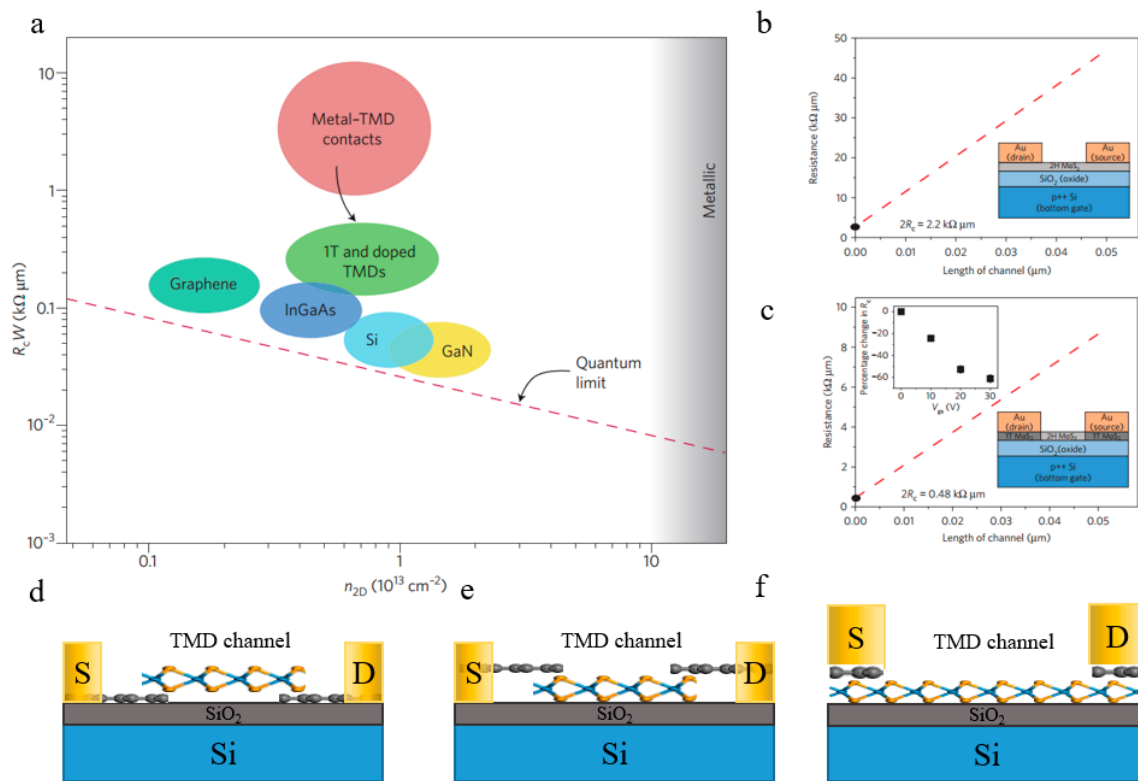
Various 2D materials provide diverse electronic properties from conductors to insulators which benefits new devices creation. Van der Waals heterostructures exhibit ultrathin thickness and special properties that give a chance to build transistors at nanoscale size compared to bulk materials. Thus, novel field effect transistors based on van der Waals heterostructures have developed.

##### 4.1. Decrease the Contact Resistance

Two-dimensional semiconductors (2DSCs), especially TMDCs, have sparked immense interest in the electronic devices since the MoS<sub>2</sub>-based transistor was first reported [64]. Source and drain are often made of Metal-TMD directly contact, which induce a high contact resistance  $R_c$ . Even the contact resistance is larger than Si based transistors. The excessive contact resistance  $R_c$  on the source and drain interface is a great challenge for 2DSCs devices.

The high contact resistance, induced by a high Schottky barrier [65], prevent the charge carriers moving through the metal-semiconductor contacts. While the typical 2DLMS contact resistance currently achieved is 100 times higher than Si-based electronics ( $<20 \Omega \cdot \mu\text{m}$ ) [66], there is still much work to do to decrease the actual contact resistance (Figure 6a). Some strategies have been used to reduce the contact resistance with the help of graphene/metal heterostructures. Schematics are shown in Figure 6d–f.





**Figure 6.** Contact resistance for different two-dimensional materials: (a) various contact resistance of materials against quantum limits; Reused with the permission from Nature publishing Group in the Ref [65] (b) contact resistance with traditional 2H-MoS<sub>2</sub> material; (c) contact resistance with 1T-MoS<sub>2</sub> and 2H MoS<sub>2</sub> as channel material; (d) coplanar contacts of graphene electrodes; (e) staggered contacts of graphene electrodes; and (f) hybrid contacts of graphene electrodes. (b,c) are reproduced with the permission from Nature publishing Group in the Ref [67]. (d–f) are adapted with the permission from Nature publishing Group Ref [5].

In silicon-based transistor, doping is conventionally used in traditional process of decreasing contact resistance at the source and drain interface, which is not reliable in TMDC-based transistor. That is because a highly doped silicon-based transistor can provide more carriers to fill valence band [65]. However, injecting other elements into TMDC seriously damages the covalent bonds between the atoms and breaks TMDC's unique lattice structure, thus a great deal of defects are generated into layers resulting in Fermi-level pinning, which causes undesired contact resistance [68,69]. Besides TMDC, graphene is another 2DLM drawing extensive concern. The greatest contribution of graphene is forming van der Waals stacks with metal and 2DLM, which commendably decreases the contact resistance due to its special band structure. Because graphene is single-element 2DLM, it can be doped similar to silicon. Compared with intrinsic graphene, the highly-doped graphene decreases the height of Schottky barrier formed by the connection of graphene and metal, which means the contact resistance is greatly reduced [70]. A typical TMDC-based transistor, which uses monolayer graphene as metal electrodes, 2DLMs such as tungsten diselenide (WSe<sub>2</sub>) as semiconductor channel, and hexagonal boron nitride (h-BN) as gate dielectric, exhibits very high performance, such as high current on/off ratio, remarkable temperature stability, low contact resistance and low subthreshold slop [71]. Even though the Schottky barriers is still high (0.22 eV) at the graphene–WSe<sub>2</sub> contact, the on-state current is dominated by tunneling through the barriers which makes the barriers almost transparent to the charge carriers. After using 3 nm h-BN as gate dielectric and 1.5 nm WSe<sub>2</sub> flake as channel material, the tunneling distance is only 1.6 nm [72]. There are

three types of interface of graphene–2DSCs contact: coplanar contacts (Figure 6d), staggered contacts (Figure 6e) and hybrid contacts (Figure 6f).

The coplanar structure is that the TMD channel materials and source/drain electrodes are on the same side of graphene. With the bottom graphene contact for 2DSCs transistors, nearly perfect work function matching lead to a barrier-free contact, which can significantly decrease  $R_c$ .  $\text{MoS}_2$  and  $\text{WSe}_2$  transistors using this strategy have been demonstrated [25,70,73,74]. Staggered contacts mean that TMD channel and source/drain electrodes are on different sides of graphene. With this strategy, transistors can be less susceptible to lithographic contamination, because the polymer residue did not touch TMD channel directly. Otherwise the residue will affect the charge transport at the interface. With this method, high performance  $\text{MoS}_2$  transistors [75–78] and air stable black phosphorus transistors [45] have been reported. Metal–graphene hybrid structure as a unique contact to reach minimized  $R_c$  ( $300 \Omega \cdot \mu\text{m}$ ) compared to metal–TMD structure. With graphene inserted as the interlayer buffer, the carrier injection was enhanced at metal–graphene–TMD channel interfaces. For example, nickel–etched–graphene electrodes have achieved a relatively low resistance [79]; Ti–graphene– $\text{MoS}_2$  stacks can reduce  $R_c$  from  $12.1 \pm 1.2 \Omega \cdot \text{mm}$  to  $3.7 \pm 0.3 \Omega \cdot \text{mm}$  to some degree compared with stacking Ti onto  $\text{MoS}_2$  directly [80].

When integrating two-dimensional transition metal dichalcogenides with metal, the valence band shows unusual Fermi level pinning. Compared with chemical doping, which will destroy the covalent bond of TMDs within layers, the stacking of graphene can create a undamaged van der Waals contact and a ultraclean interface, which prevents Fermi level pinning [25,75]. There are some other reports demonstrate a stacking structure formed by  $\text{MoS}_2$  and graphene to reduce the connect resistance [73,77,81]. In this structure, graphene and metal are connected together to form electrodes and molybdenum disulfide ( $\text{MoS}_2$ ) is used as channel. The tunability of doping graphene's work function can significantly improve the ohmic contact to  $\text{MoS}_2$  [77].

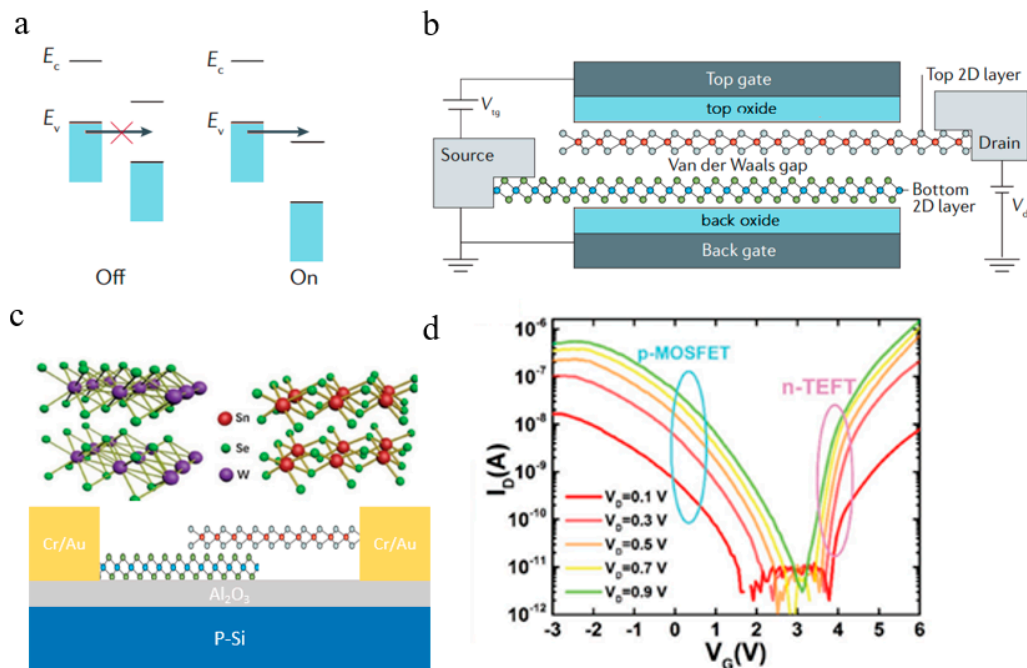
Besides graphene, other 2DLMs such as  $\text{MoS}_2$  can also be doped with element to improve the mobility of charge carriers which leads to low contact resistance, for example, physisorbing chloride molecule into  $\text{WS}_2$  or  $\text{MoS}_2$  [82]. With the method of physisorbed molecules, contact resistance can be obviously decreased [83]. Other efforts of contacting electrode metal materials with TMDs create the low Schottky barrier. For example, the connection between molybdenum (Mo) and  $\text{MoS}_2$  forms perfect interface, leading to ultralow Schottky barrier about 0.1 eV [84]. Other methods based on van der Waals heterostructure to decrease  $R_c$  have include phase-engineering. With the organolithium chemical method,  $\text{MoS}_2$  changes from 1T phase to 2H phase. 2H phase  $\text{MoS}_2$  behaves as electronic channel, as shown in Figure 6b. This 1T–2H–1T structure can receive relatively low  $R_c$  [67] (Figure 6c). To create stable homojunction contact of  $\text{MoTe}_2$ , some reports use laser to achieve two phase interconversion. Stacking semiconducting hexagonal (2H) and metallic monoclinic (1T)  $\text{MoTe}_2$  together can fabricate an ohmic heterophase homojunction, which is necessary in lowering contact resistance [67]. Phase engineering, therefore, provide a way of creating lateral heterostructures with low resistance, but additional work is needed to achieve values comparable to state-of-art materials and close to the quantum limit.

#### 4.2. Tunneling Field Effect Transistor and Barrister

The principle of tunneling field effect transistors (TFETs) is band-to-band tunneling [85]. The barriers induce by van der Waals gap narrow because the width of van der Waals gap is below 1 nm, which will lead to charge carriers tunneling [86]. For width of barriers narrowing at the contact interface, the tunneling current between source and drain increases rapidly in silicon-based transistor. However, vertical tunneling transistor based on vdWHs is different from conventional TEFTs. In vertical structure, two separate monolayers of graphene serve as electrodes, and ultrathin dielectric material are stuck between them. Based on gate-voltage tunability of the DOS in graphene, the height of Schottky barrier reduces and realizes the charge carriers' transportation.

Transistors based on that principle use very thin BN (1.4 nm) and MoS<sub>2</sub> as vertical transport barrier, making devices have the switching ratio of  $\sim 10,000$  at room temperature [87]. Further study of this type of heterostructure is the resonant tunneling and gate voltage-tunable negative differential conductance [88]. Other studies have put forward how to achieve the resonant tunneling with the help of crystallographic orientation alignment of the graphene-BN-graphene heterostructure [89,90].

In addition of graphene, two dimensional TMDs have sharp band edges and ultra-narrow channel length, which has been the suitable candidates for TFETs. By correctly choosing two 2D layers of semiconductors to make up a suitable heterojunction (one layer is n-type and the other layer is p-type), it can achieve both large tunneling current and low subthreshold swing (SS). Subthreshold swing (SS) shows the current transformation with the change of voltage, when the device works in subthreshold state. With the proper heterojunction band offsets between the two 2D semiconductor layers (Figure 7a,b), the tunneling current will be significantly increased because of the band alignments. TFETs with SnSe<sub>2</sub>/WSe<sub>2</sub> van der Waals heterostructure (Figure 7c) have achieved the SS of 80 mV/dec at room temperature and  $I_{ON}/I_{OFF}$  ratio exceeding  $10^6$  [91] (Figure 7d). In addition, dual-gated MoS<sub>2</sub>/WSe<sub>2</sub> van der Waals heterostructures were demonstrated and carrier concentration of MoS<sub>2</sub> and WSe<sub>2</sub> can be independently controlled by up and down symmetric gates, which achieved a high efficiency of 80% due to the weak electrostatic barrier through atomic layers [92].



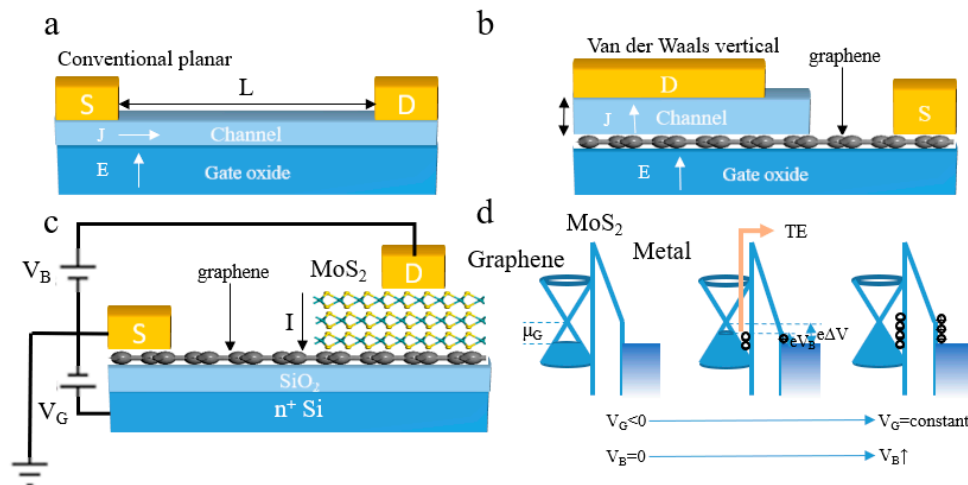
**Figure 7.** Tunneling field effect transistors structure and transfer curve (a) Band offset of p-type semiconductor and n-type semiconductor. (b) A schematic illustration of TFETs. The devices consist of ultrathin p-type layer and n-type layer connected to source and drain, respectively.  $V_{tg}$  is the gate tunable voltage and  $V_{ds}$  is the drain voltage. (c) WSe<sub>2</sub>/SnSe<sub>2</sub> heterostructure based TFET schematic diagram. (d) Transfer curve of WSe<sub>2</sub>/SnSe<sub>2</sub> TFET with the gate voltage of 0.1 V, 0.3 V, 0.5 V, 0.7 V, 0.9 V. (a,b) are adapted with the permission of Nature publishing Group in ref [6] (c,d) are adapted with the permission of John Wiley & Sons, Inc. in Ref [91].

#### 4.3. Van der Waals Heterostructure Based Vertical Transistors (VFETs)

With ultrathin structure and suitable band structure, 2DLMs can create totally new devices such as vertical transistors. Compared with conventional planar field effect transistors, which consist of a source and a drain plate electrode with a conducting channel located between them, vertical transistors often use graphene and metal as source and drain electrodes, respectively. In planar transistors

(Figure 8a), the gate electrical field ( $E$ ) controls the channel carriers to influx. Thus, the channel current density ( $J$ ) is always perpendicular to the gate electrical field ( $E$ ) ( $J \perp E$ ). The channel length is decided by the area of 2DSCs. In other word, the lithographic accuracy which decides the distance of source and drain would influence the channel length. In particular, the tunable work function and partial electrostatic transparency make graphene become the appropriate candidate of interconnecting with semiconductor to fabricate vertical transistors, in which graphene acts as the active contact. In this fundamentally different geometry, as shown in Figure 8b, the channel carriers transport direction is parallel to the gate electrical field ( $J \parallel E$ ). The channel length is decided by the thickness of 2DSCs which can be prominently shorter than the planar transistors. With effectively modulating the work function of graphene by introducing the gate voltage, the Schottky barrier between graphene and semiconductor changed and result in large current injection, which brings a large on/off ratio that cannot be achieved in planar transistors.

Different kinds of transistors based on vertical vdWHs have been reported according to its special device structure. N-channel vertical FET created by sandwiching multilayered  $\text{MoS}_2$  between graphene and metal panel (Figure 8c), has the on/off ratio  $>10^3$  at room temperature [93]. Due to van der Waals interface between  $\text{MoS}_2$  and graphene, the Schottky barrier restrains current injection. Introducing an external electric field can strongly modulate the height of Schottky barrier owing to the small density of states of graphene [94]. The band structure of graphene/ $\text{MoS}_2$ /metal heterostructure is shown in Figure 8d. The source/drain voltage ( $V_B$ ) drives current follow vertically into multilayered  $\text{MoS}_2$  channel. The carriers transport is dominated by thermionic-emission (TE). The application of  $V_B$  changes the Fermi level in graphene due to the capacitive coupling through  $\text{MoS}_2$ . With the increasing  $V_B$ , the Fermi level will reach the Dirac point at some point, as shown in the right panel of Figure 8d [95,96]. Other 2DLMs such as  $\text{WS}_2$  possessing the same geometrical structure of  $\text{MoS}_2$  VFETs have been reported, achieving extremely large on-state current [97].



**Figure 8.** Van der Waals vertical stack structure and devices: (a) conventional planar transistor, channel current exists in planar area; (b) van der Waals vertical stack and channel current follow in vertical direction; (a,b) are adapted with the permission of Nature Publishing Group in Ref [5] (c) schematic of metal/ $\text{MoS}_2$ /graphene vertical stack and measurement circuit; Adapted with the permission of AIP Publishing LLC in Ref [94] (d) band alignment of metal/ $\text{MoS}_2$ /graphene vertical stack with a constant  $V_G$  and changing with the increase of  $V_B$ . Adapted with the permission of American Institute of Physics Publishing LLC in Ref [95].

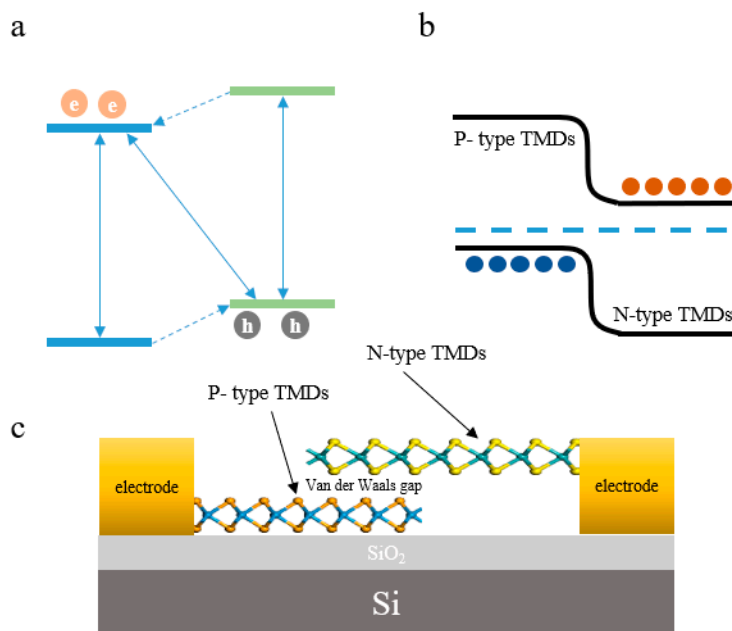
As graphene has attracted increasing attention among researchers, other carbon-based materials such as fullerene also draw attention to be assembled with graphene or 2DLMs to create organic vertical field effect transistors (OVFETs). In other words, the work function of fullerene ( $\text{C}_{60}$ ) is closed to graphene. Thus, the graphene/ $\text{C}_{60}$ /metal VFET with a measured current on/off ratio up to  $10^5$

has been reported [98] and the logic inverter based on this structure also has been reported yet [99]. Some types of organic or molecular crystals can act as semiconductor. After stacking on graphene to form 2D–3D heterojunction, which is an excellent vertical channel for VFETs, new opportunities in developing novel OVFTs exist. At the same time, organic transistors such as 2D quasi-freestanding molecular based graphene transistors which had the mobility up to  $10 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  have been achieved [100].

#### 4.4. Photodetector and Diodes Based on van der Waals Heterostructure

Based on fine optical characteristic of two-dimensional TMDCs, photovoltaic applications about van der Waals heterostructure combined with such materials have been explored. The typical application is the photodetectors made of graphene act as channel material and  $\text{MoS}_2$  act as light sensitive material [101]. Under the combination of two kinds of 2D materials which have different tunable work functions, photoexcited electrons and holes can be accumulated in conductor layers. Shown in Figure 9a, photoexcited pairs have been observed in the heterostructure of  $\text{MoS}_2/\text{WSe}_2$  [102] and  $\text{MoSe}_2/\text{WSe}_2$  [103]. Most photovoltaic devices can be created by combining few layers of TMDCs with graphene. Using graphene as electrodes and TMDCs sandwiched between two graphene electrodes, one can create efficient photoexcited carriers inject into graphene electrodes [104,105]. In other words, graphene can form a typical ohmic contacts which will significantly decrease the resistance and serve as a transparent electrode.

If p-type and n-type 2D semiconductors stack together with van der Waals force, then atomic layers of p-n junctions can be acquired. Gate tunable diode based on TMDCs have been abundantly created. Various combinations of 2D semiconductors were used to construct p-n junction for photodetectors (typical p-n structure and band structure shown in Figure 9b) to realize the excellent performance of responsivity and detectivity [106–112]. Heterostructures such as  $\text{MoS}_2/\text{WSe}_2$  [107], black phosphorus/ $\text{MoS}_2$  [109], and  $\text{MoS}_2/\text{WS}_2$  [110] p-n junctions are widely used in photodetectors.  $\text{GaTe}/\text{MoS}_2$  heterostructure received a high photovoltaic performance whose photoresponsivity can reach  $21.83 \text{ AW}^{-1}$  [112].

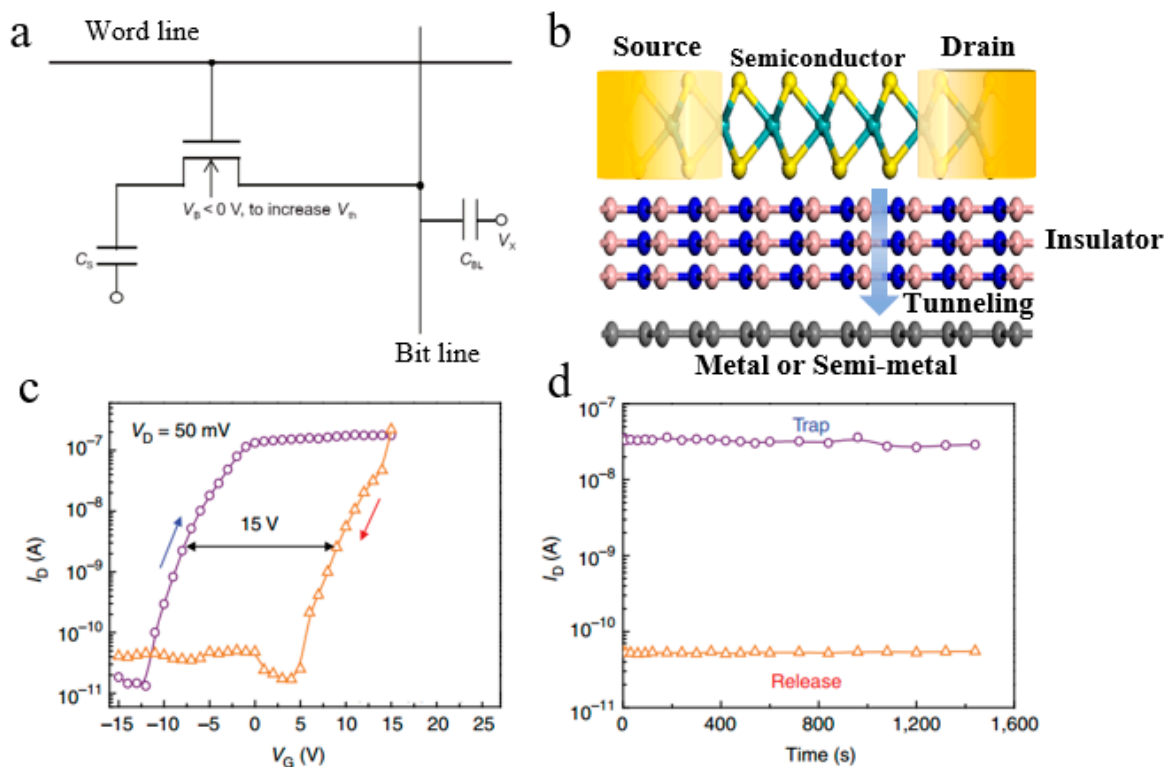


**Figure 9.** Photodetector and diodes schematic diagram: (a) photoexcited pairs generate in  $\text{MoS}_2/\text{WSe}_2$  heterostructure; (b) band structure of n- $\text{MoS}_2$  and p- $\text{WSe}_2$  p-n junction; and (c) schematic illustration of vertical stack p-n diode based on two-dimensional TMDCs.



#### 4.5. Memory

There are many types of memory devices which include dynamic random access memory (DRAM), static random access memory (SRAM), resistive random access memory (RRAM) and flash memory. The memory cells of DRAM and SRAM are based on the one-transistor and one-capacitance (1T1C) structure and six transistors (6T), respectively. The 1T1C DRAM cell is shown in Figure 10a. The capacitance charging and discharging controlled by the transistor on-state and off-state. When the word line voltage reaches the transistor on-state voltage, the current will follow through transistor and charge the capacitance when the bit line voltage is at high potential. This operation is called the programming process. When the bit line voltage is at low potential, the charged capacitance will discharge and the current will follow through the transistor into bit line, which is called erasing process. When the word line voltage controls transistor at the off-state, the charge carriers will be held in capacitance. After setting bit line at half of the high potential, the voltage will rise if the capacitance is charged and will decline if the capacitance is discharged. This is called the reading operation of DRAM. However, DRAM is a typical volatile memory, which means that the storage performance will disappear under the power-down state.



**Figure 10.** Schematic diagram of different type of memory and performance curve: (a) 1T1C structure of dynamic random access memory; (b) semiconductor–insulator–metal heterostructure of flash memory; (c) gate hysteresis curve of flash memory; (d) stability and endurance of flash memory. (c,d) are reproduced with permission from Nature Publishing Group, Ref [113].

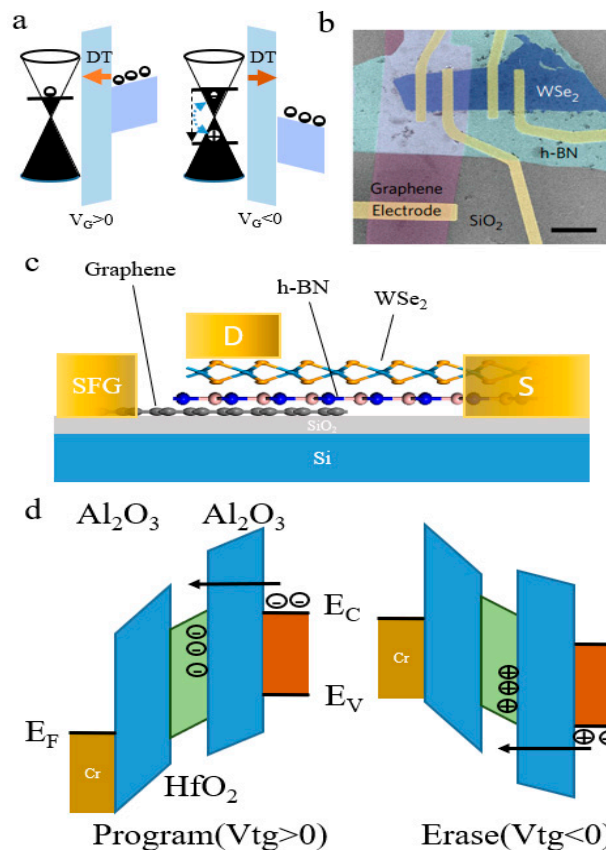
A new concept of constructing memory is based on the domain wall motion which means that crystalline particles with the same polarization direction as the external electric or magnetic field inside the crystal become larger. This process is done by the movement of domain wall. Current driven domain wall motion and electrically controlling the magnetization switching by spin orbit torque have been proposed for information storage. Decreasing the current density to realize the domain wall motion plays an important role in practical applications [114]. Basically, the external magnetic field is necessary to control the current-induced magnetization switching direction by spin

orbit torque [115,116]. Later research has reported that the electric field definitively control the current induced ferromagnet switching at room temperature with the polarized ferroelectric substrate [117]. Piezo voltage solely controlling the magnetization switching at room temperature without external magnetic field has been realized, which can largely decrease the energy consumption compared with the electric current switching magnetization [118]. This concept offers an idea to develop ferroelectric random access memory, magnetic random access memory and phase change random access memory.

Another block of memory is flash, a kind of non-volatile memory. Flash memory is based on 2D material stacks established on a semiconductor–insulator–metal (SIM) structure (Figure 10b). MoS<sub>2</sub>/BN/Graphene heterostructure for use in flash memory has been widely explored [113,119]. Graphene and MoS<sub>2</sub> were utilized as charge trapping layers and channel layers and h-BN acted as a tunnel barrier, respectively. Under a considerable voltage positive bias, the tunneling current exponentially increases with the decreasing of BN thickness, which will lead to the increasing charge injection into the trap layer. Thus, the thickness of insulator becomes especially important in SIM structure. The critical thickness of tunneling barrier is 7 nm. Tunneling current cannot be formed in the thick layers (>10 nm), while leakage current will exist in the thinner layers (3.5 nm), which will cause charging process failure [113]. When gate voltage becomes negative in releasing process, charge carriers trapped in the graphene layer will be transferred into MoS<sub>2</sub>. Thus, the charge retention and gate hysteresis that contains a memory window can be observed (Figure 10c). Retention time of trapping and releasing current shows the endurance of charge trapping flash device (Figure 10d). Detailed band structure is shown in Figure 11a with the charging and releasing process.

Nonvolatile floating gate flash memory based on black phosphorus/BN/MoS<sub>2</sub> stacks have been reported, where MoS<sub>2</sub> behaves as charge trapping layer and black phosphorus acts as channel [120]. Charge trap memory with high *k* dielectric materials can greatly improve the storage performance. Few-layer MoS<sub>2</sub> channel and three-dimensional Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> stack together to form a charge trap flash memory device, exhibiting an unprecedented gate window of 20 V and a program/erase current ratio of 10<sup>4</sup> [121]. Band diagram of program/erase state of device under different top gate bias (*V*<sub>tg</sub>) is shown in Figure 11d. Positive *V*<sub>tg</sub> carry out the programming process. Electrons tunneling from MoS<sub>2</sub> channel are accumulated in HfO<sub>2</sub> charge-trap layer. Negative *V*<sub>tg</sub> carry out the erasing process. Holes tunnel from MoS<sub>2</sub> channel to HfO<sub>2</sub> charge-trap layer. The charge-trap layer holds different charges, causing the threshold shifting. Thus, memory window exists. Besides MoS<sub>2</sub> channel based charge-trap memory, Ambipolar WSe<sub>2</sub> channel based charge-trap memory devices have also been reported [122]. Subsequently, black phosphorus based charge-trap memory devices with a Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> charge trap stack have been demonstrated, where the long data retention with only 30% charge loss after 10 years were obtained [123]. Beside floating gate memory, novel structure based on vertically stacked 2D materials (WSe<sub>2</sub>/h-BN/graphene) has the gate metal stack directly on the graphene, thus we call it semi-floating gate (SFG) flash memory [124]. The structure is shown in Figure 11b,c. When a positive voltage is applied on Si, electrons are accumulated in the WSe<sub>2</sub>. These electrons tunnel through BN and begin to be accumulated in graphene due to the different potential between WSe<sub>2</sub> and graphene which is considered as programming process. When the positive bias is removed, electrons are still trapped in graphene due to the potential barriers of h-BN. When applying a small negative voltage bias on Si, the electrons tunnel through BN and are injected into WSe<sub>2</sub> channel as an erasing process. Similar behaviors can be observed for holes when a negative voltage is applied on Si. When treated with plasmas, multilayer MoS<sub>2</sub> transistors can serve as nonvolatile, highly durable flash memory with multibit data storage capability. This novel multibit flash memory is desirable for improving data storage density in order to reach manufacturing process [125].

Memory have made significant progress due to the multiduty van der Waals heterostructures. New type of memory devices structure began to spring up. However, effort still needs to be made to improve the memory performance such as stability, reliability and time of memory operation. 2D van der Waals heterostructures offer a new route of building novel memory.



**Figure 11.** Semi-floating gate flash memory and band structure diagram of SIM heterostructure: (a) band structure with different gate voltage and charge carriers following direction; (b) SEM image of semi-floating gate memory based on WSe<sub>2</sub>/h-BN/Graphene stack; (c) schematic diagram of SFG device; and (d) band structure of charge trap memory operations. (a–c) are reproduced with permission from Nature Publishing Group, Ref [124]. (d) is reproduced with permission from American Chemical Society Publishing Group in Ref [121].

## 5. Perspective

The inherent absolute advantages of 2D materials—exhibiting free of dangling bond and gate tunable electronic properties—make them promising candidates for van der Waals stacks, which are widely used in novel device design. However, the burgeoning van der Waals heterostructures applied to electronic devices remain in their infancy. Technical improvement still needs to be explored in the following effort.

Conventional laboratory-stage process of assembling van der Waals stack is mechanical exfoliation and transfer methods. The shape of exfoliated 2D materials is irregular and the size can only reach micron order. It is hard to acquire monolayer materials and most are few layers. Large area 2D materials are still needed in some cases during transfer process. Although with the utilize of chemical vapor deposition, large-scale synthesizing 2D materials and van der Waals heterostructures is developed, it still cannot be applied in integrated technique and lacks controllability of the relative orientation, size, shape and interlayer spacing with increasing vdWH layers. Furthermore, the electrical performance of chemically synthesized 2DLMs is inferior to their exfoliated counterpart. Thus, there is still much room to improve the process of assembling van der Waals heterostructure.

FETs based on van der Waals heterostructures have largely focused on attaining high performance with certain parameter to measure. However, parameters such as low SS at extensive range of gate voltage biases, which will lead to large on/off ratios with low input voltage biases, have become important criteria for measuring the performance of the devices. Besides, contact resistance is still a

big deal for limiting the improvement of devices. There is still plenty of room to lower the contact resistance, as it is still above theoretical minimum, even larger than Si based transistors. The contact resistance must be lower by at least an order of magnitude to  $<100 \Omega \cdot \mu\text{m}$ . In 2D TMDCs, based on phase engineering, changing semiconductor to metal phases is a promising route of creating an ohmic contact which can greatly lower the contact resistance. In addition, the majority of TMDCs are unipolar, n-type or p-type. Controllable and stable doping process is still a major challenge to overcome the achievement of bipolar—both n-type and p-type—semiconductors or van der Waals stack of homogenous material, which will enable the next generation of high speed and low power devices. Direct growth of homogenous 2D semiconductor with stable doping process to form different types of heterostructures and phase engineering to decrease contact resistance are topics for future research. Scalable fabrication of van der Waals stacks also need to be explored. Creating new structure of semiconductor devices based on van der Waals heterostructures still has a long way to go.

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