

Review

Epitaxial Graphene on SiC: A Review of Growth and Characterization

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Abstract: This review is devoted to one of the most promising two-dimensional (2D) materials, graphene. Graphene can be prepared by different methods and the one discussed here is fabricated by the thermal decomposition of SiC. The aim of the paper is to overview the fabrication aspects, growth mechanisms, and structural and electronic properties of graphene on SiC and the means of their assessment. Starting from historical aspects, it is shown that the most optimal conditions resulting in a large area of one ML graphene comprise high temperature and argon ambience, which allow better controllability and reproducibility of the graphene quality. Elemental intercalation as a means to overcome the problem of substrate influence on graphene carrier mobility has been described. The most common characterization techniques used are low-energy electron microscopy (LEEM), angle-resolved photoelectron spectroscopy (ARPES), Raman spectroscopy, atomic force microscopy (AFM) in different modes, Hall measurements, *etc.* The main results point to the applicability of graphene on SiC in quantum metrology, and the understanding of new physics and growth phenomena of 2D materials and devices.

Keywords: graphene; epitaxial; SiC; sublimation

1. Introduction

A single layer of carbon atoms, bonded together in a hexagonal honeycomb lattice, that has been isolated from graphite is commonly referred to as graphene. A precise definition of this material has been available since 1986; about 11 years later (1997), the International Union of Pure and Applied Chemistry (IUPAC) formalized these definitions by incorporating them into their Compendium of Chemical Technology. Historically, the word graphene is derived from the Greek word *graphein*, which means “to write”; this was one of the earliest uses of graphene. In 1800, Wagner, a German chemist, used the word graphite for the bulk material in pencils. However, graphite was thought to be a form of lead at that time, due to which graphite pencils were mistakenly named lead pencils.

For the first time, in 1840, the German scientist Schafhaeutl decoupled individual flakes of graphite through intercalation (insertion of a small-molecule species, such as an acid or alkali metal, in between the carbon sheets) and exfoliation (with sulphuric and nitric acids). These flakes comprised extraordinary electrical properties which were later demonstrated in freestanding graphene [1–3]. B. C. Brodie, in 1859, claimed the discovery of the new carbon form “graphon”; he obtained it by intercalation of graphite and named it carbonic acid. When graphite is exposed to strong sulphuric and nitric acids, it results in the intercalation of graphite and the formation of graphite oxide (GO) [4,5]. Boehm *et al.*, in 1962, produced thin lamellar carbon after the chemical reduction of GO. In this process, dilute alkaline media with hydrazine, hydrogen sulphide or iron salts are used as reducing agents [1,6]. In 1975, van Bommel *et al.* sublimed silicon atoms from silicon carbide (SiC (0001)) crystal under high vacuum ($<10^{-10}$ Torr) at elevated temperature to form thin sheets of graphene [7]. An attempt was made to form monolayer flakes of graphene through a micromechanical approach in 1999 but

this process failed at that time [8]. In 2004, Geim and Novoselov used the same micromechanical approach and obtained thin flakes of carbon from highly ordered pyrolytic graphite (HOPG) [9]. Geim and Novoselov were awarded the Noble Prize in physics for the demonstration of graphene in 2010; indeed, 2010 is called “the year of graphene”. The history of graphene is summarized in Figure 1.

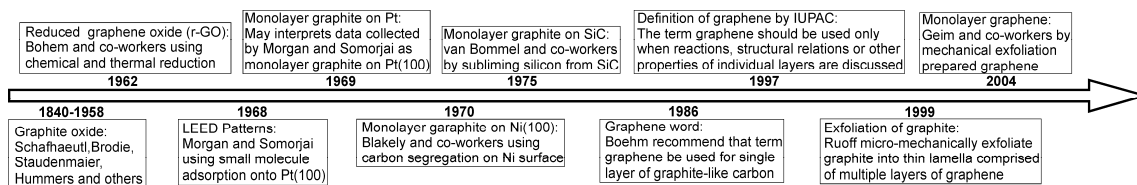


Figure 1. History of graphene.

The unconventional two-dimensional (2D) electron gas properties of graphene have attracted remarkable interest for condensed matter physics and material science as well as advanced technologies. Graphene is a two-dimensional crystal with a honeycomb structure of sp^2 -bonded carbon atoms; the carbon-carbon distance is 1.42 Å and the lattice constant is 2.46 Å (Figure 2a,b). It can exist in a free-standing state. The definition “graphene” is not only used for single layers, but also for bilayer and few-layer graphene (three to <10 layers) [10]. Graphene has an extremely high optical transparency, high electric and thermal conductivity, single-molecule gas detection sensitivity, mechanical toughness, and high electron mobility [11]. It is a semi-metal with linear energy dispersion around the Dirac point (Figure 2c) due to its two-dimensional honeycomb structure [11,12]. This makes the material behave differently from the conventional semiconductors and therefore opens new avenues for revolutionary applications, such as RF devices [13], sensors [14], and high precision metrology [15].

Lang *et al.*, in 1975, performed one of the earliest efforts of fabricating monolayer graphite (graphene) [16]. They produced mono- and multi-layered graphite by thermal decomposition of carbon on single-crystal Pt substrates. After demonstrating graphene, several methods have been developed for the fabrication of monolayer (ML) and multilayer graphene. One of the methods is mechanical exfoliation of graphite, which is basically a repeated peeling process. Andre Geim and Konstantin Novoselov, in 2004, extracted a single graphene sheet by rubbing or by scratching the graphite surface with scotch tape until they found a thin flake of graphene. The largest flakes obtained by this way are about 10–100 µm, which is only useful for fundamental laboratory research and is not large enough for industrial purposes [9]. Chemical exfoliation can be introduced as a two-stage process; the first stage is increasing the space between layers in graphite, which results in reducing the interlayer van der Waals forces. This can be done by intercalating graphite to make graphite-intercalated compounds (GICs) [17]. In the second stage, these GICs are exfoliated to a single- or few-layer graphene by ultra-sonication or rapid heating. This process is a promising method to synthesize large-scale graphene, but the structure has a lot of defects due to the oxidation and reduction processes. An alternative technique is the chemical vapor deposition (CVD) of graphene on transition metal substrates, such as Cu, Ni, Pd, Au, or Ru [18,19]. The first report on few-layer graphene synthesized by CVD was found in 2006 [20]. This method is based on the saturation of transition metal by carbon in a hydrocarbon gas ambient at high temperature. In this process, the metal substrate works as a reaction catalyst and determines the deposition mechanism of graphene which has an effect on the graphene quality. Since some of the transition metals can be etched by acid solutions, graphene on these materials can be transferred to other substrates. Synthesis of large graphene domains is an advantage of this method, but it requires transfer to an insulating substrate with methods that have yet to be developed.

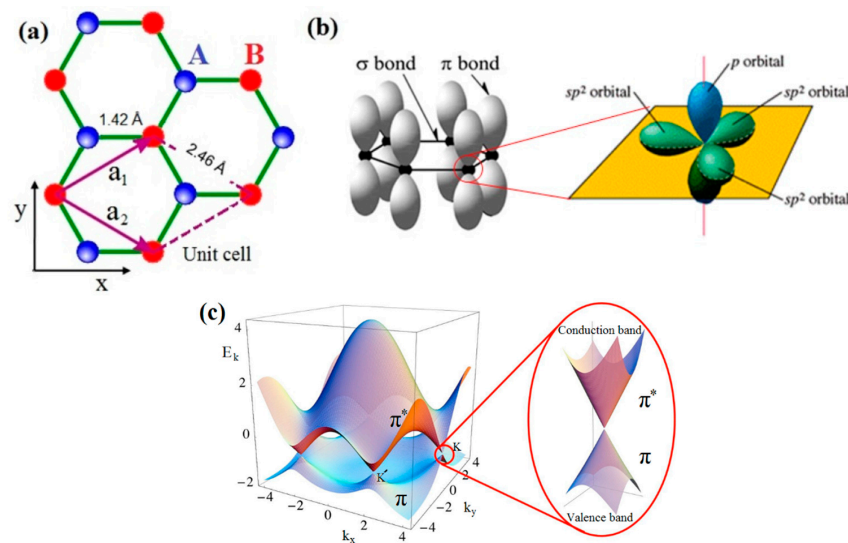


Figure 2. (a) Bravais lattice of the graphene; (b) σ and π bonds in graphene; (c) graphene π - and π^* -band structure [12].

Sublimation of SiC in comparison with other methods is a technique that has been developed for the simple fabrication of large-area, low-defect-density graphene films directly on a semiconducting substrate [13,21–26]. In 1970, the basic principles of a modified seeded sublimation growth process for the growth of 6H-SiC were established by Tairov and Tzvetkov [27,28], which was a breakthrough for SiC growth. This process is also known as the modified Lely process. Some principles of the sublimation growth of SiC are useful to develop the sublimation growth of graphene. Later on, van Bommel *et al.*, in 1975, described the sublimation of silicon from single crystals of SiC(0001). At elevated temperatures under ultrahigh vacuum (UHV; $<10^{-10}$ Torr), monolayer flakes of carbon consistent with the structure of graphene were obtained, as determined by LEED and Auger electron spectroscopy [7].

Growth of graphene by the sublimation method is nowadays typically performed in a furnace with an Ar overpressure to improve the uniformity of the epitaxial graphene (EG) layer. The main advantages of epitaxial graphene on SiC are that no transfer is needed for device processing and the size of the graphene sheet can be as large as the substrate, which is another benefit for device processing. SiC as a polar material has two inequivalent terminations, called the Si face, corresponding to the (0001) polar surface, and the C face (000 $\bar{1}$). For both the Si face and C face, the growth mechanism of graphene layers is driven by the same physical process: sublimation of Si at elevated temperatures at a rate much faster than C due to its higher vapor pressure [29]. The remaining C forms a graphene film on the surface. The surface reconstructions and growth kinetics for Si and C faces are different, resulting in different graphene growth rates, growth morphologies and electronic properties [7,30]. The underlying SiC substrate, having the space group $P6_3mc$ with a hexagonal lattice, provides excellent symmetry matching for graphene epitaxy. Graphene grown in this manner is referred to as “epitaxial graphene” [31]. Epitaxial graphene growth on SiC by the sublimation method is a promising technique for quality graphene growth and shows interesting physical characteristics such as ballistic transport in nanoribbons [32], high frequency transistors [13,33], quantum Hall resistance standard for metrology [15], and half-eV bandgap structures [34].

2. Main Methods for Graphene Characterization

Graphene is a material of atomic thickness which implies that the characterization methods should meet certain requirements in terms of resolution and source energy. In the following, few most common characterization techniques (also in our group at Linköping University (LiU)) for graphene layers are introduced briefly.

2.1. Low-Energy and Photoemission Electron Microscopy

Low-energy electron microscopy (LEEM) and photoemission electron microscopy (PEEM) are techniques suited to performing dynamic observations of surfaces with nanometer resolution in a vacuum. In 1966 [35] and 1985 [36,37], the first photoemission electron microscopy and low-energy electron microscopy images were published, respectively. PEEM is based on the extraction of photoelectrons from the sample, which is usually achieved with an ultraviolet source (e.g., laser), while LEEM relies on secondary or reflected electrons, which are created by a low-energy electron beam. For imaging in both methods, low-energy electrons, below 100 eV, are used to obtain a great surface sensitivity for the few highest layers of the sample. LEEM images reveal the electron reflectivity which is related to the density of states, and PEEM images disclose work function contrasts. Adding an energy analyzer in PEEM allows us to make a cross-section of angle-resolved photoemission spectroscopy with a constant energy [38]. With LEEM, the performance of low-energy electron diffraction (LEED) and micro-LEED experiments is possible. LEED is a standard method for studying the surface structure of a crystalline material—low-energy electrons (20–200 eV) impact the surface and elastically backscattered electrons illuminate a diffraction pattern on a florescent screen. The LEED method is a surface-sensitive technique as electrons have low energy and are not able to penetrate deep into the sample.

In 2008, Ohta *et al.* and Vinojanadara *et al.* monitored the evolution of graphene layers on SiC(0001) using LEEM measurements [39,40]. Figure 3 shows a LEEM image of graphene with different thicknesses grown on 6H-SiC. The method of graphene thickness determination is shown. The LEED technique also has been used by researchers to study graphene formation on SiC [7,25,40,41]. A micro-sized LEED revealed the presence of rotational variations of graphene on SiC substrate. Riedl *et al.* and our group at LiU have used this method for graphene thickness measurements by the intensity ratio at 126 eV and 53.3 eV of the graphene LEED spot compared to that of its neighboring ($6\sqrt{3} \times 6\sqrt{3}$)R 30° satellite spots, respectively [40]. A quantitative relationship between the intensity ratio and the graphene thickness was established by Fisher *et al.* in 2010 [42].

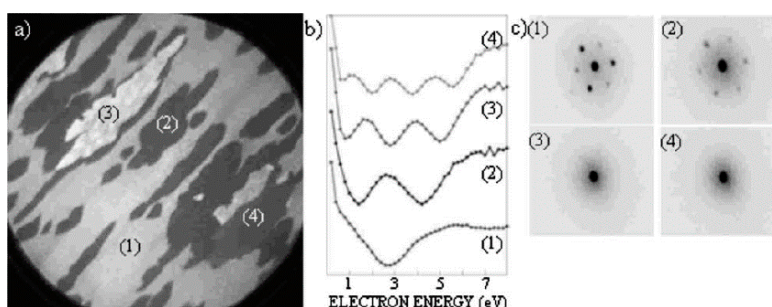


Figure 3. (a) LEEM image of graphene layers (FOV is 20 μm); (b) Electron reflectivity spectra extracted from the four representative areas 1–4 corresponding to graphene of 1–4 ML thick, respectively; (c) Micro-LEED collected from the four different areas [40].

2.2. Raman Spectroscopy and Microscopy

C.V. Raman first observed Raman scattering in 1928 by means of sunlight [43,44], and this technique has been used for material science since 1940s. In this method, photons of an incident laser beam are unelastically scattered in the solid or in molecules and information about the photon properties of the crystal or the vibrational properties of the molecule will be obtained.

Raman spectroscopy is a useful technique to characterize graphene. It provides information about the number of layers in graphene stacks, the atomic structure of graphene edges, disorder and defects, the stacking order between different layers, the effect of strain, and charge transfer. Graphene has three main features in its Raman spectrum, called the D, G, and 2D (also called G') modes. As shown in Figure 4, they appear at about 1350, 1583 and 2700 cm^{-1} [45]. The D peak appears just in samples

with disorder in the graphene layer. The presence of defects in sp^2 carbon systems results in resonance Raman spectra and, for this reason, Raman spectroscopy is one of the most sensitive techniques to characterize defects in the graphene layer. The G mode is a first-order Raman scattering process involving in-plane transverse optical and longitudinal optical excitations at the middle of the Brillouin zone [46]. The G peak is highly sensitive to doping and strain effects in the sp^2 system and can be used for studying modifications on the graphene surface. Impurities or surface charges in the graphene layer ultimately split the G peak into two peaks, G (1583 cm^{-1}) and D' (1620 cm^{-1}). The relative intensity and width of the 2D mode involve information about the number of layers in the graphene stacks. Righi *et al.* show that the orientation of graphene layers in graphene stacks can be studied by specific Raman peaks [47]. The type of graphene edges of flakes can be recognized by using polarized light [48]. Raman modes are strongly affected by strains of C–C bonds occurring under stress [49], and this can be used to characterize the nature of the interaction between graphene and its substrate. Reflectance mapping is another method to determine the number of graphene layers on SiC [50], and this technique is based on monitoring the power of the laser beam reflected from the sample in a slightly modified micro-Raman setup.

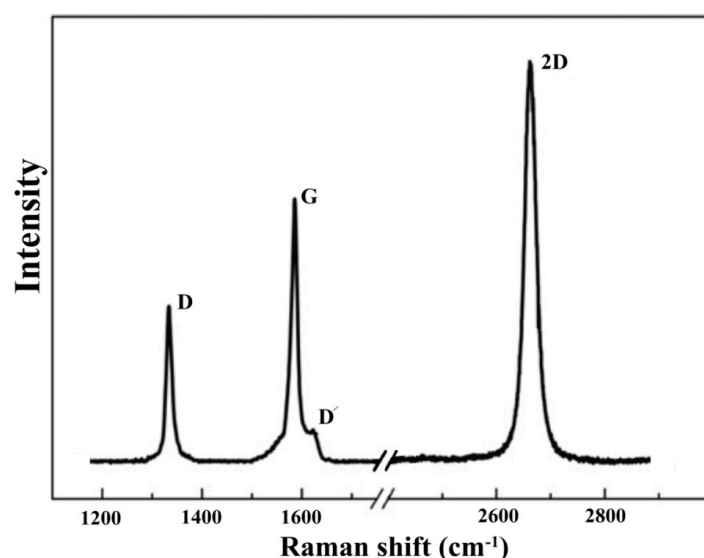


Figure 4. Main Raman peaks: D, G and 2D bands of graphene layer.

2.3. Scanning Tunneling Microscopy

Scanning tunneling microscopy (STM) is a technique for imaging surfaces at the atomic level. STM was invented by G. Binnig, H. Rohrer, and C. Gerber in 1982 [51]. STM provides information about structural and electronic properties of conducting surfaces, and it can be used in a variety of environments: UHV, air, and liquids [52]. In this technique, a sharp tip scans the surface of a sample in a regime of such tip-sample distances that electrons can tunnel from the tip to the sample surface or *vice versa*. STM can be performed in a constant current or constant height mode. The low temperature STM measurements provide thermal stability which is a requirement for high resolution imaging and spectroscopic analysis.

In 1990s, the first atomically resolved images of graphene/Pt were obtained with this method [53]. STM is a powerful technique to study the structure of epitaxial graphene, and can reveal the presence of defects in the graphene layer on substrates [54]. It can show the superstructures in graphene on SiC (Figure 5) and metals.

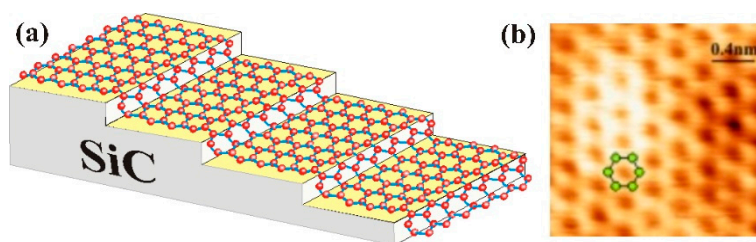


Figure 5. (a) A sketch of graphene layer on SiC substrate; (b) STM image of graphene layer grown on SiC; the size is $2 \times 2 \text{ nm}^2$ [22,55].

2.4. Atomic and Electrostatic Force Microscopy

G. Binnig *et al.*, in 1986, developed atomic force microscopy (AFM) in order to investigate the surfaces of insulators, while such materials could not be studied with the scanning tunneling microscope (STM) which needs conducting or semiconducting surfaces [56]. In AFM, the force between atoms located at the sharp point of the tip (located on the cantilever) and atoms at the sample surface, varying substantially during the scan, is measured. The interaction between tip and sample is transduced into changes of the motion of the cantilever which is a macro-scale phenomenon. The detector of AFM measures the deflection of the cantilever (by optical detection of the cantilever movement) and converts it into an electrical signal. AFM is widely used under atmospheric conditions and room temperature for a fast characterization of graphene surfaces and thickness uniformity. It was found that the phase signal shows strong contrast (Figure 6) from a ML graphene to few-layer graphene [57] due to sensitivity of the phase signals to the dissipation properties of materials.

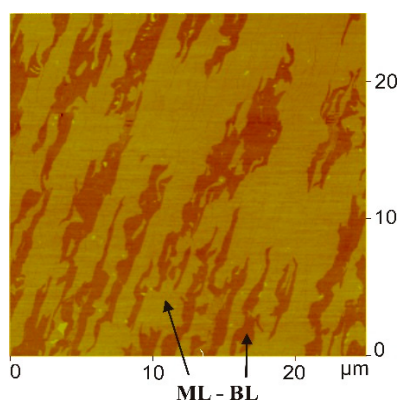


Figure 6. AFM phase image of monolayer and bilayer graphene on SiC (not published results).

The electrostatic force microscopy (EFM) mode of AFM has been used to probe variations of the surface potential of graphene layers as its thickness varies. The EFM phase forms in a two-pass mode; in the first pass, the AFM tip traces the sample topography, and in the second (interleave) pass along the same scan line, the electrical DC bias is applied either to the probe or graphene sample and retraces the topography at a fixed lift height above the surface. The EFM study in our samples (Figure 7) operated both in ambient conditions and at elevated temperatures to obtain potential difference maps of epitaxial graphene on 4H-SiC(0001). Quantification of the potential difference maps allowed for an explicit distinction between graphene layers with different thicknesses [58].

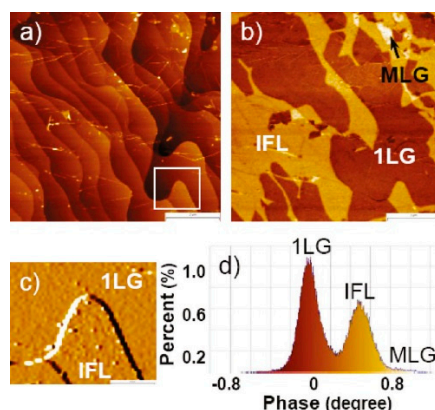


Figure 7. Typical area of epitaxial graphene on 4H-SiC(0001): (a) topography (z-range is 13 nm); (b) corresponding EFM phase image (z-range is 2°); (c) topography deflection error signal highlighting the adsorbates found on the interfacial layer (IFL) compared to the clean 1LG; (d) histogram for the EFM phase image clearly showing 1LG (40% of the total area) and IFL areas. MLG constitutes less than 2% of the total area [58].

Conductive atomic force microscopy (C-AFM) is a scanning probe technique which measures the current flowing between the sample and metal-coated tip when applying a voltage. In contrast to STM, which cannot detect forces and thus needs the current as a feedback signal, C-AFM is able to act on insulators as it can use the cantilever deflection signal as a feedback signal and measure the current signal independent of the feedback loop. The C-AFM can be used for imaging and spectroscopy; for imaging C-AFM is driven in contact mode, and for spectroscopy the tip is stationary while the voltage is being swept.

For graphene sheets torsion resonance conductive atomic force microscopy (TR-CAFM) is usually used. This method is another mode of C-AFM which allows nondestructive electrical measurements from a tip oscillation in a torsional or twisting mode close to the sample surface. This noncontact technique has an advantage over C-AFM performed in contact mode because of the absence of shear force which can damage the graphene layers.

2.5. Transmission Electron Microscopy

The invention of the transmission electron microscope (TEM) by Max Knoll and Ernst Ruska at the Berlin Technische Hochschule goes back to the 1930s [59]. They overcame the barrier of higher resolution which is imposed by the limitations of visible light wavelengths. In this technique, an electron gun generates electrons and injects them into a column; then, by using the electromagnetic field (lenses), electrons focus to shape a high energy electron beam (10 to few 100 keV). Electrons then pass through a thin sample (less than 50 nm thick), and the sample plane is imaged through another set of electromagnetic lenses. By using aberration-corrected instruments, it is possible to increase the resolutions to less than 1 Å [60].

TEM on graphene should be done with electron energy less than 80 keV to induce a smaller amount of defects, because this energy is the threshold electron energy for damaging a single-wall carbon nano-tube [61]. There are some other difficulties in the study of graphene by TEM, e.g., in a plane-view geometry (top-view graphene) the substrate causes strong electron scattering, and a thick substrate makes it impossible to detect the graphene layer. For a cross-section view, detecting a ML graphene is a difficult task as it needs simulation of the TEM images.

2.6. Scanning Electron Microscopy

The development of the scanning electron microscopy (SEM) is the same as TEM, dating back to the 1930s. Actually, it was Manfred von Ardenne who in 1938 invented a true microscope with

high magnification [62]. In SEM, a high-energy electron beam (ranging a few 100 eVs to a few keVs) is used to generate a variety of signals at the surface of a sample. These signals which come from the electron-sample interactions expose information about the sample, including surface morphology, crystalline structure, and chemical composition. These signals are secondary electrons which are used for SEM images, backscattered electrons and diffracted backscattered electrons. These modes are used to study crystal structures, X-rays are used for determining chemical composition, and visible light with a monochromator can be used for cathodoluminescence (CL).

SEM is also used for characterizations of the growth of graphene on SiC [63]. Because of its atomic thickness, graphene is usually detected with secondary electrons which probe only a sample surface. With SEM imaging, different contrast can be observed, such as thickness, roughness, and edge contrast; the brighter area shows the thinner part of the graphene layers [63]. The roughness contrast of a graphene layer is due to the different numbers of secondary electrons detected. The defects such as wrinkles, ruptures, and folds can be studied by different contrast in SEM images (Figure 8).

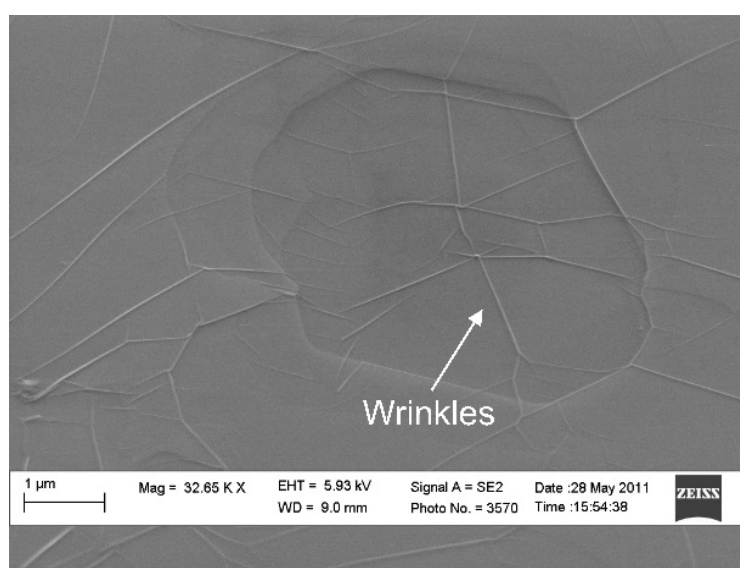


Figure 8. SEM image of graphene layers on SiC (not published results).

3. Epitaxial Graphene on SiC Polytypes

The word *epitaxy* comes from the Greek roots *epi*, which means “above”, and *taxis*, meaning “an ordered manner”. It means growth of a crystalline layer on a crystalline substrate which follows the structure of the substrate. The deposited layer is called the epitaxial layer. The growth of epitaxial graphene on SiC substrates by surface Si depletion is a promising method to produce a large area with uniform thickness and high quality graphene. One of the advantages of this technique is that it does not need the transfer of the graphene layer to another substrate, which allows electronic devices to be fabricated directly on semi-insulating SiC. For this method, SiCs up to 6 inch are commercially available, providing epitaxial conditions and existing as semiconducting (p- and n-type), semi-insulating, and in different polytypes which make different device designs possible. The growth of epitaxial graphene by the sublimation method is based on annealing the SiC crystal at high temperature; during sample annealing, primarily Si leaves the SiC crystal [64], leaving a carbon-rich surface behind. As silicon has a higher vapor pressure than carbon in the SiC substrate [31], the Si atoms therefore desorb first from the sample surface during the annealing process, leaving the C atoms behind, and allow a carbon-rich surface to emerge until the final graphene is formed. The high temperature ensures ordered and clean graphene in this technique. In 2004, de Heer *et al.* utilized the sublimation process to produce graphene layers [31], although surface graphitization of SiC had been observed before [41]. The process was

first performed in a vacuum, not in an Ar atmosphere, but growth is typically performed in an Ar overpressure atmosphere to improve the uniformity of the epitaxial graphene film [40].

3.1. SiC as a Substrate

SiC is a wide-bandgap (2.3–3.3 eV) semiconductor composed of silicon and carbon in an equal stoichiometric ratio. Naturally developed SiC can be found very rarely, either in some inclusions in minerals and diamond or in meteorites. SiC has superior material properties such as high thermal conductivity and chemical stability, and it is able to operate at high temperature and in a high radiation environment. These have led SiC to be used in many applications, especially high power devices, high temperature controllers and sensors, high voltage switching, and microwave components.

The first SiC was synthesized in 1824 by the Swedish scientist Jöns Jacob Berzelius [65]. In the following decades, only non-systematic studies of SiC synthesis in small quantities on a laboratory scale have been reported. The process of SiC powder production was introduced in 1892 by E.G. Acheson [66]. The first SiC production on an industrial scale was started by Acheson in 1893 [67]. In this process, SiC was manufactured by the electrochemical reaction of sand and carbon at high temperatures (up to 2550 °C). Because of its extreme hardness, the resulting material was used in polishing applications. The first electrical property (electroluminescence of SiC light emitting diodes (LEDs)) of SiC was measured in 1907 [68]. As the production of high quality SiC crystals is necessary for application in electronics, in 1955 Lely used a new method for the growth of high quality SiC, which was based on sublimation and enabled the growth of SiC platelets [69]. Tairov and Tsvetkov improved this process in 1978 when they introduced a SiC seed crystal on which the vapor species were deposited, resulting in a boule of the material [27]. This method is called sublimation growth and is based on physical vapor transport (PVT). It reduces the problems with polytype control and yield. Nowadays, the interest in silicon carbide is high and several corporations have formed to produce large boules having a particular crystal structure and controlled concentrations of impurities that determine the electrical and optical properties. There are commercially available 6 inch single-crystal wafers of 4H-SiC with micropipe densities less than 1 cm^{-2} . The common method for growing SiC epitaxial layers is CVD, and the advantages of this method are good structural quality and excellent doping control.

Silicon carbide never reached the importance that Si has for device technology, and this can mainly be attributed to difficulties in growing the crystal. However, SiC has found its place in some specific areas in the markets, where Si reaches its limits. For example, SiC is used in high power, high frequency and high temperature device applications. It is already used as a substrate for LEDs made from GaN, which actually is the largest market for commercial SiC products. Further applications are abrasive and cutting tools, break discs in cars and gemstones in jewelry. It is also used as a base material for medical implants. Since high quality epitaxial graphene can be formed on the SiC surface by the thermal decomposition of SiC [31,40], one of the future commercial application areas could be the epitaxial growth of graphene on SiC wafers.

Silicon carbide is a semiconductor material compound of group IV-IV with the chemical formula SiC and mainly covalent Si-C bonds (88% covalent and 12% ionic). The crystallography and polytypism in SiC are important to have control regarding the properties and the nature of the surfaces available for the epitaxial growth of III-nitride semiconductors. SiC is the only chemically stable compound containing only Si and C. Its crystalline structure consists of the close-packed stacking of double layers of Si and C atoms. The fundamental unit in the SiC structure is a covalently bonded tetrahedron with four-fold symmetry, consisting of either SiC₄ or CSi₄, as shown in Figure 9. The distance between the two neighboring silicon or carbon atoms is about 3.08 Å, while the very strong sp³ bond between carbon and silicon atoms is because of the very short distance between them, approximately 1.89 Å [70].

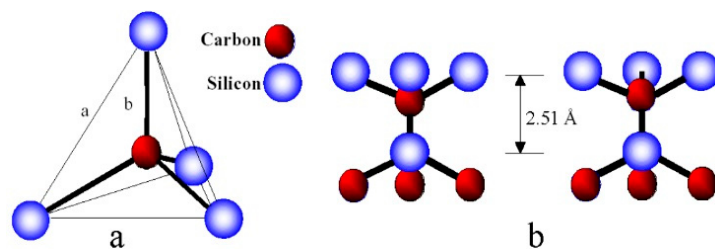


Figure 9. (a) Basic unit cell of silicon carbide. The distance between Si-Si or C-C atoms, a , is about 3.08 Å, and between C-Si atoms, b , is approximately 1.89 Å. (b) The two configurations of silicon and carbons atoms, rotated 180° [70].

Figure 9b shows the spacing between the silicon layers is approximately 2.51 Å. The unit cell is bonded through the corner atoms of the tetrahedron; as shown in Figure 9b there are two possible orientations of adjacent tetrahedrons (by 60° rotation). The various rotations and translations lead to the many different stacking arrangements (or polytypes) of the Si-C bilayers along the c -axis.

The possible atomic arrangements of the atoms in the hexagonal wurtzite unit cell are shown in Figure 10. One can denote the first layer of atoms with position A, and then the atoms in the next layer may sit at either position B or position C. Thus, the simplest polytype is 2H (... ABAB...). The cubic (zinc-blende) structure of 3C-SiC has a stacking sequence of ... ABCABC... (or ... ACBACB...). The most common forms of SiC are the 6H and the 4H polytypes with the ... ABCACBABCACB... and the ... ABCBABC... stacking, respectively. Here we use Ramsdell notation, which is common for describing the polytypes [71]. The number in the name of the polytype refers to the number of layers needed to repeat the pattern and the letter in a polytype's name corresponds to the first letter of the crystal system (C for Cubic, H for Hexagonal, and R for Rhombohedral) [70].

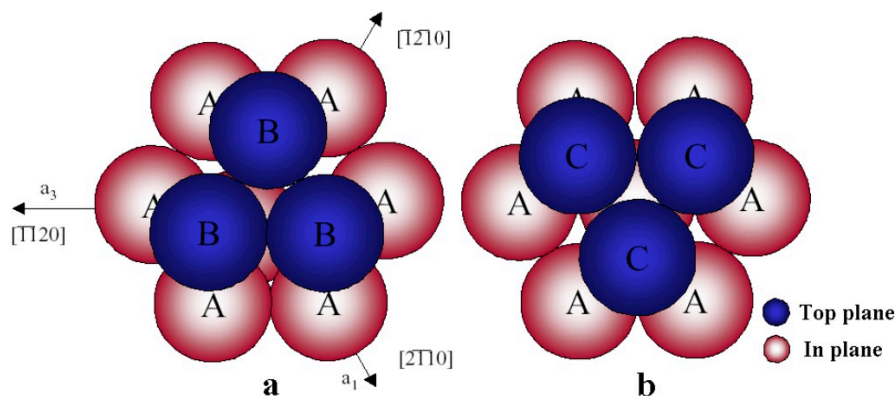


Figure 10. Possible stacking orientations of atoms in a close packed hexagonal structure [70].

The stacking sequence for 3C-, 4H-, and 6H-SiC polytypes are shown in Figure 11. Since there is no rotation in the stacking sequence of cubic polytype compared with the hexagonal polytypes, the 3C structure proceeds in a straight line and hexagonal structures proceed in a zigzag pattern. The A position in 4H-SiC is a cubic site, and the B position is a hexagonal site. In 6H-SiC, the A position is a hexagonal site, and B and C are cubic. More than 200 SiC polytypes have been found, some with a stacking period of several hundred bilayers [72]. The properties of SiC depend on the polytypes and also the atom position and its surroundings in the polytype.

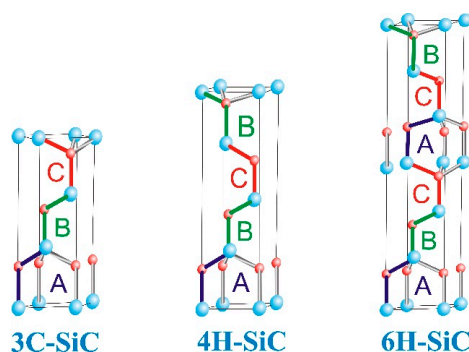


Figure 11. Stacking sequence of SiC polytypes.

Both wurtzite and zinc-blende structures have polar axes due to the lack of inversion symmetry. The polarity of SiC can be defined with respect to the position of the Si atom in the $\{0001\}$ bilayer. In the Si face of SiC, the Si atom occupies the top position in the bilayer, while in the C face of SiC, the top position is occupied by the C atom (Figure 12).

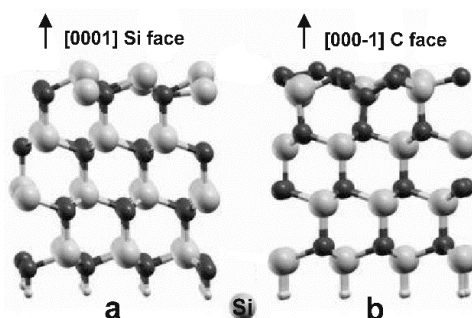


Figure 12. Schematic drawing of the SiC polar structures: (a) Si face; (b) C face.

3.2. Graphitization Process of SiC Polytypes

The growth of graphene on SiC surfaces, which is in principle a graphitization process under controlled conditions, can be made in different growth arrangements. Here we show an example of a vertical RF-heated furnace consisting of a quartz tube, porous graphite insulation and graphite crucible (Figure 13).

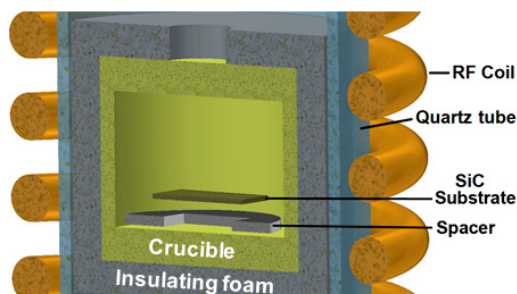


Figure 13. Sketch of a vertical RF-heated furnace in cross-section.

The growth mechanism of epitaxial graphene for both the Si face and C face graphene layers is driven by the same physical process: sublimation of Si at high temperatures with a rate faster than C due to its higher vapor pressure (more details in the following section). The remaining C forms a graphene film on the surface. However, the surface reconstructions and growth kinetics for each

polar surface are different, resulting in different graphene growth rates, growth morphologies and electronic properties [30,73–75]. Yakimova *et al.* have analyzed the conditions for large-area graphene formation on SiC substrate [21]. Characteristic features related to step bunching in SiC upon heating have been reported by Yazdi *et al.* [22].

As illustrated in Figure 14a, the 4H-SiC polytype has two kinds of decomposition energies, terraces 4H1 (−2.34 meV) and 4H2 (6.56 meV), respectively, and the 6H-SiC (Figure 14b) has three distinct terraces, −6H1 (−1.33 meV), 6H2 (6.56 meV) and 6H3 (2.34 meV), while 3C-SiC (Figure 14c) has only one kind of terrace, 3C1 (−1.33 meV) [76].

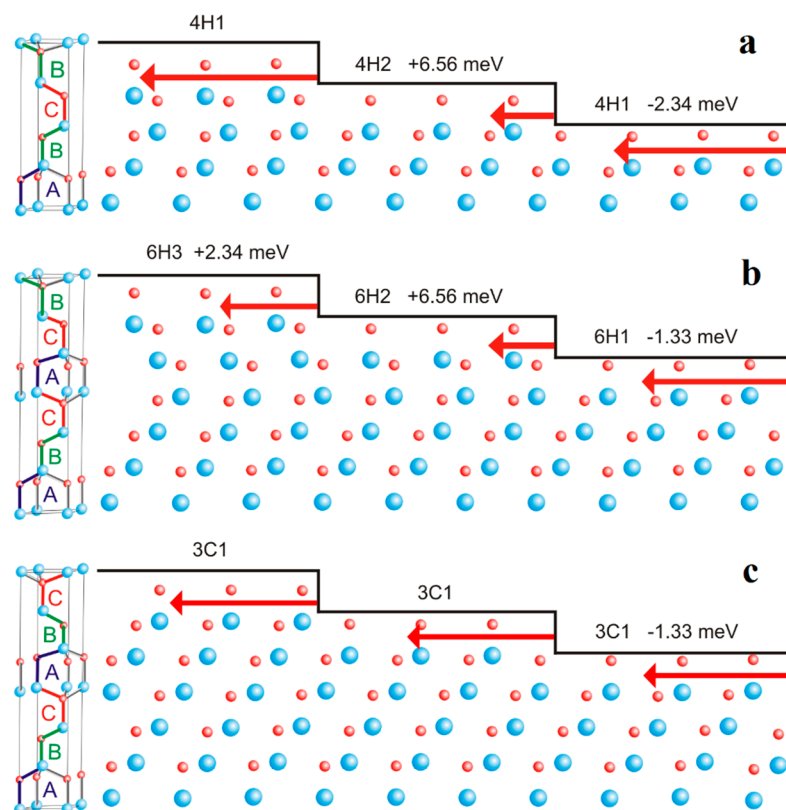


Figure 14. Stacking sequences and possible terraces on (a) 4H-SiC; (b) 6H-SiC; and (c) 3C-SiC surfaces. Large (blue) and small (red) circles represent Si and C atoms, respectively. Length of arrows indicates different step decomposition velocities. The surface energies needed to remove a particular terrace are demarcated [22].

The growth process is schematically shown for 4H-SiC in Figure 15. The growth of the epitaxial graphene is not equally distributed over the SiC substrate surface. Since the Si and C atoms are bonded more weakly in the vicinity of step edges, Si desorbs from these areas faster in comparison with the terraces. It is worth noting that the C contained in about three Si-C bilayers of the SiC substrate is sufficient to feed the formation of one layer of graphene.

Based on the mentioned terrace energies for 4H-SiC, it will cost less energy to remove a 4H1 terrace. Thus, for the 4H1 terrace the step decomposition velocity will be faster (Figure 14a). As shown in Figure 15, from the edge of the 4H1 terrace on the graphene-free surface, C atoms are emitted onto the terrace as Si atoms leave the surface (stage 1). The C atoms coalesce and nucleate into graphene islands (stages 1 and 2), which act as a sink for subsequently emitted C atoms [77]. After the 4H1 terrace step catches the 4H2 step, the newly formed two-SiC bilayer height step provides more C atoms as compared to the one-bilayer height step and the first graphene layer extends along the step edge (stage 2). The large percentage of bunched steps with four Si-C bilayers, *i.e.*, an increased source

of carbon, will impose the formation of a second layer of graphene (Figure 15, stage 3) since some extra C will be released. Therefore, a full coverage of the 4H-SiC substrate surface by just one layer of graphene may be an issue.

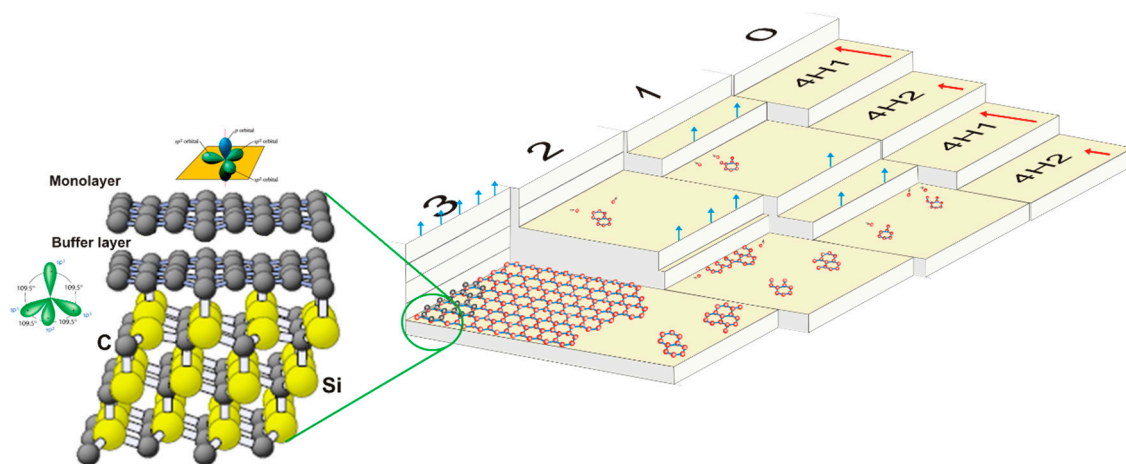


Figure 15. Schematic depiction of the formation process of epitaxial graphene via sublimation of Si from the SiC surface [22].

A similar mechanism of energy minimization is expected in the 6H-SiC polytype (Figure 14b). As a result, first the step 6H1 will catch step 6H2 and form two Si-C bilayers. Then step 6H3 will advance and merge with the two-bilayer step. The growth process for 6H-SiC is the same as the 4H-SiC as explained above. Most outstandingly, significant step bunching occurs; the initial steps flow over the surface while graphene is forming, bunch together, and form higher steps with larger terraces in between [22,78–80]. However, on 3C-SiC all terraces have the same decomposition energy (Figure 14c) and no energetically driven step bunching should be expected. In this polytype, a non-uniformity of sublimation may be induced by the presence of extended defects such as stacking faults which are characteristic of this material (see Section 3.4).

Structural and electronic properties of graphene grown on SiC are strongly affected by the substrate polytype and polarity. As mentioned above, the surface reconstructions and growth kinetics for Si and C faces of the SiC substrate surface are different. The first C-rich layer grown on the Si face of SiC polytypes, known as a zero layer or buffer layer, includes sp^3 bonds of C atoms to Si atoms of the substrate while the next layer of graphene grown on the first layer is known as a monolayer (ML) graphene, and the C atoms just have sp^2 bonds with the C atoms around (inset left side in Figure 15) as well as weak van der Waals bonding with the buffer layer. However, for the C face the buffer layer has not been confirmed. In the following we will focus on the differences of the growth mechanism, structural properties (stacking, morphology, step bunching, bilayer inclusions, domains, decoupling, orientational disorder), and electrical properties on 4H-, 6H- and 3C-SiC polar faces.

3.3. Growth of Graphene on SiC Polar Faces

Epitaxial growth of graphene by high temperature annealing of SiC wafers is a promising method for large-area production of graphene [7,21,22,40,41,81–83]. The most commonly used SiC polytype structures for growing epitaxial graphene are 4H-SiC and 6H-SiC. Both of these SiC polytypes have either Si- or C-terminated surfaces. There is an epitaxial match for these facets and hexagonal graphene lattice. It is important for an epitaxial system to be familiar with the substrate bulk and surface crystal structure, especially when we have a thin layer on the top and an interface structure in between.

In terms of the history of epitaxial graphene on SiC, the first experimental works with respect to graphitization of SiC crystals at temperatures around 2050–2150 °C in a vacuum (10^{-5} Torr) date back to 1962 and were conducted by D.V. Badami [84]. He studied the samples with X-ray diffraction and found

that the c-axis of graphite runs along the c-axis of the hexagonal SiC crystal [85]. Van Bommel *et al.*, in 1975, used low-energy electron diffraction (LEED) experiments to show that the graphite structure was formed on a hexagonal SiC(0001) surface via a $(6\sqrt{3} \times 6\sqrt{3})R 30^\circ$ structure [7]. He found that the carbon formation rate was greater on the SiC(000 $\bar{1}$) polar face than on the SiC(0001) face. In 1998, Forbeaux *et al.* [41] studied the evolution of a SiC surface as it becomes more graphite-like (Figure 16) by LEED and angle-resolved photoemission spectroscopy (ARPES) measurements. They showed that with the increase of annealing temperatures, the concentration of the Si vacancy in the top layers increases so that there is a larger number of C atoms surrounded by Si vacancies. In 2002, Charrier and coworkers used grazing-incidence X-ray diffraction and scanning tunneling microscopy to show that the thermal decomposition of 6H-SiC after annealing at increasing temperatures between 1080 and 1320 °C leads to the layer-by-layer growth of unconstrained, heteroepitaxial single-crystalline graphite. They could control the Si sublimation rate to form single- or a few-layer graphene on 6H-SiC(0001) [86]. In the same year (2004), Novoselov *et al.* reported the electric field effect on exfoliated graphene [9], and De Heer's group, on their highly ordered graphene samples grown in vacuum, showed Shubnikov-de Haas oscillations that corresponded to nonlinearities in the Hall resistance, indicating the potential of a new quantum Hall system. They also showed the Dirac nature of the charge carriers exceeding the carrier mobility of $25,000 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ in graphene on SiC [23,31]. In all the above-described research works, the growth of epitaxial graphene on SiC was done in ultrahigh vacuum (UHV) conditions, which resulted in an inhomogeneous graphene thickness.

G.R. Yazdi and colleagues studied the growth of graphene on 3C-, 6H-, and 4H-SiC and, for the first time, the influence of crystal structure at an atomic level for each polytype on the graphene formation was reflected [22]. Growth of graphene on SiC has progressed further, and recently large-area homogeneous monolayer, bilayer, and few-layer graphene on SiC(0001) and SiC(000 $\bar{1}$) have been obtained.

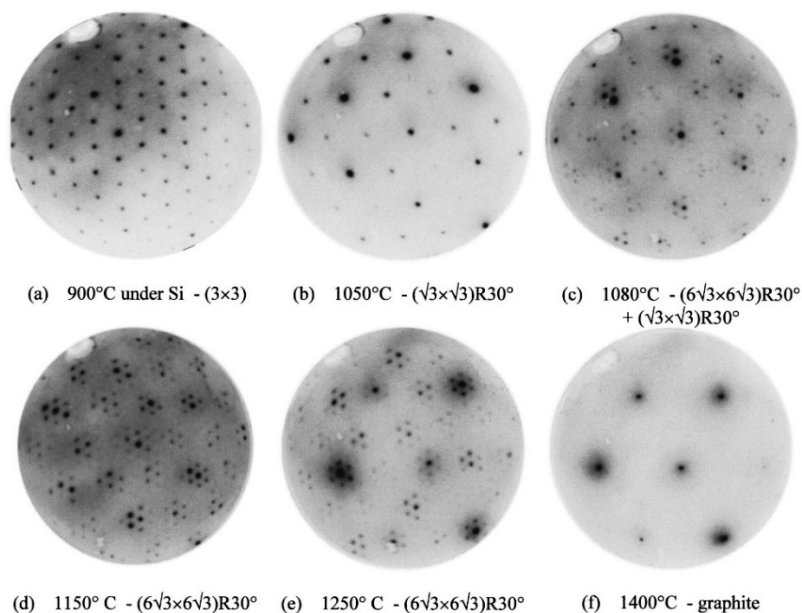


Figure 16. LEED patterns from 6H-SiC(0001) with a primary energy of 130 eV obtained on (a) (1×1) ; (b) $(\sqrt{3} \times \sqrt{3})R 30^\circ$; (c) $(\sqrt{3} \times \sqrt{3})R 30^\circ + (6\sqrt{3} \times 6\sqrt{3})R 30^\circ$; (d,e) $(6\sqrt{3} \times 6\sqrt{3})R 30^\circ$; and (f) graphite (1×1) [41].

3.3.1. Effect of Ambient Conditions

Graphene on SiC is expected as a thermodynamically stable phase which means high structural quality can be produced by choosing proper growth conditions. Thermodynamic study shows the existence of equilibrium or near-equilibrium chemical potential ranges (corresponding to specific

temperature and pressure conditions) for buffer layer, ML, and bilayer (BL) graphene grown on SiC. This result proves the potential for much better growth control than what could be expected if each phase was just a required kinetic intermediate [87].

The ambient conditions at which epitaxial graphene formation is performed have a strong influence on the graphene quality in both polar faces of SiC polytypes. For example, the growth of epitaxial graphene on SiC(0001) in ultrahigh vacuum (UHV) yields graphene layers with low quality and small grains [39,88]. Upon SiC annealing, silicon atoms leave the surface at a high sublimation rate, and carbon atoms stay on the surface. This is a process far from equilibrium, which leads to the SiC substrate roughening. It has been shown that a more homogeneous graphene layer can be produced by using a short period of high temperature annealing in comparison with a longer period of heating at a lower temperature [89,90]. By using a higher annealing temperature, the kinetic energy and mobility of C and Si atoms will be increased, thus making surface restructuring easier. However, this should be complete before the graphene layer is formed, and to avoid complete graphitization the Si sublimation should be suppressed. This can be done by having a controlled Si background pressure, and there are several methods to reach this goal.

In 2008, the group of R. Yakimova at LiU proposed a novel method for epitaxial graphene growth on SiC substrates. The method is based on high temperature (2000 °C) sublimation at 1 atm of Ar ambient, which yields ML graphene on a large area (up to $20 \times 20 \text{ mm}^2$) and allows good control over the thickness uniformity [21,40]. The role of Ar is to slow down the emission of Si atoms and to make the process of Si depletion more uniform. Figure 17 shows LEEM images of the graphene layers grown in vacuum and Ar ambient, and the results show an obvious better thickness uniformity and quality for the graphene grown in Ar pressure [40].

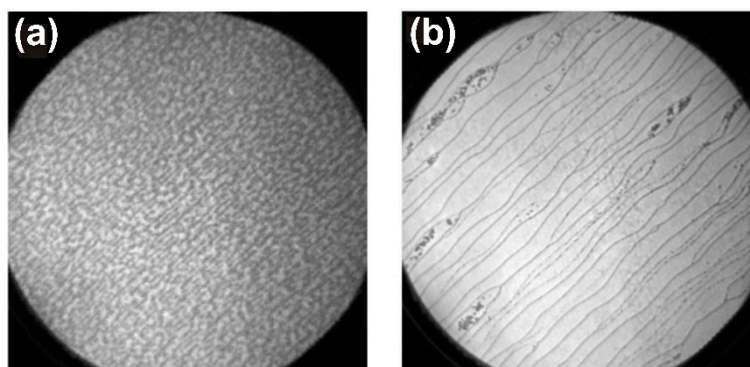


Figure 17. Graphene layers grown in (a) vacuum; (b) Ar [40].

In 2009, Emtsev *et al.* also used Ar buffer gas around 1000 mbar to suppress the evaporation of Si atoms [26]. This allowed them to use temperatures around 1650 °C, and no pit formation was observed when the terraces retracted upon Si sublimation. The interface layer and graphene actually started to grow at the step edge in contrast to the UHV preparation technique. Eventually, homogeneous terraces with a length of several tens of micrometers and a width of a few micrometers were observed, both for the interface layer and monolayer graphene. This is a huge improvement of the graphene thickness uniformity in comparison to the UHV preparation technique with terraces of around $100 \text{ nm} \times 100 \text{ nm}$. Transport measurements of the graphene layer indicated higher mobilities ($2000 \text{ cm}^2/\text{Vs}$) in comparison to UHV-grown epitaxial graphene ($700 \text{ cm}^2/\text{Vs}$) [81].

Tromp, Hannon, and other researchers controlled the Si background pressure using disilane gas [83,91]; the presence of extra Si flux allows the surface to be equilibrated in a pressure-temperature phase diagram. Due to the external Si background pressure of 10^{-6} mbar, the Si atoms that evaporate from the surface are reflected back to the surface. As a consequence, the phase transformation temperatures can be shifted up by several hundred degrees. The result is a strongly improved morphology of the graphene.

De Heer *et al.* controlled the sublimation (CCS) method by confinement, using a confined cavity which could retain a finite Si background pressure as Si evaporates from the SiC substrate [82]. The near-equilibrium CCS method has been demonstrated to be a useful method for producing high quality, uniform graphene layers on both the Si face and the C face of 4H- and 6H-SiC. It provides controlled and constant silicon vapor density over the surface and near-thermodynamic equilibrium, which is essential for uniform growth. The method allows good control of the graphitization temperatures, which is important, because growth at low temperatures (as in the case of sublimation in unconfined ultrahigh vacuum) produces defective graphene layers. In this method the graphitization temperature increases by approximately 300 °C in comparison with the UHV method. Further control of the graphitization rates can be obtained in this method by introducing inert gases, which can essentially inhibit the graphene growth even at temperatures exceeding 1600 °C [82].

To date, the majority of research on epitaxial graphene growth has focused on graphene grown on the Si and C polar faces; the growth mechanism for both faces is driven by the same physical process as explained in Section 3.2. The growth of epitaxial graphene and its final structure, growth morphologies, and electronic properties are strongly dependent on which SiC polar face is initially exposed. For homogeneous growth of graphene, the Si face is a better choice. In the following, we will focus with more detail on the growth of graphene in Ar ambient on these two polar faces.

3.3.2. Growth of Graphene on Si Face

The most outstanding advantage of graphene on the Si face is that it is easily possible to control the thickness of graphene at the wafer-scale SiC substrates. This control can be reached by optimizing the growth temperature and Ar pressure. Growth of ML graphene on the Si face occurs via a step-flow process, as shown in Figure 15. However, in this case the charge carrier mobility at room temperature is extremely reduced in comparison to freestanding graphene layers. This is due to an interaction between the monolayer graphene and the substrate. On this face, Si sublimation initially results in a C-rich ($6\sqrt{3} \times 6\sqrt{3}$)R 30° structure (shortly $6\sqrt{3}$) which nucleates at the step edges and has the same honeycomb structure of graphene. It is known as the buffer layer or zero-layer graphene [25,40,89,92–94]. This reconstructed surface loses its distinct graphene electronic properties because of sp^3 hybridization of about 30% of the carbon atoms which are covalently bonded with the Si atoms of the SiC interface (left inset in Figure 15) [40,95,96]. Because of this strong coupling with the substrate, a buffer layer does not show graphene-like π bands and is electronically inactive [97]. After formation of the buffer layer, further heating leads to decomposition of the SiC bilayers underneath the buffer layer, resulting in nucleation of a new carbon layer (left inset in Figure 15) [98]. It is believed that: (i) the $6\sqrt{3}$ layer acts as a template layer for graphene on the Si face, ensuring well-ordered graphene on that surface [99], and (ii) by further Si sublimation, a second $6\sqrt{3}$ reconstructed surface forms under the first one which decouples from the substrate and forms monolayer graphene [98].

TEM and STM studies showed that the buffer layer is located at 1.97 Å [100], 2.0 Å [101], 2.3 Å [102], or 2.5 Å [92] distance from the Si-terminated SiC surface which is less than the graphite inter-plane spacing of 3.35 Å. The spacing between the first and the second graphene layer is about 3.5 Å, which is very close to the average spacing between subsequent layers of 3.35 Å. Theoretical calculations also predicted that the first carbon layer is separated by 2.0 Å from the SiC surface [97]. This short bond length is due to covalently bound C atoms of the buffer layer with Si atoms from the SiC surface. For the Si face, theoretical calculations show that the average graphene separation is 2.58 Å from the SiC [97].

Graphene layers on the Si face are stacked with a 30° rotation, and the orientation relation is $[1\bar{1}00]_{\text{SiC}} \parallel [11\bar{2}0]_{\text{graphene}}$ and $(0001)_{\text{SiC}} \parallel (0002)_{\text{graphene}}$ [41]. In few-layer graphene (FLG), the crystallographic stacking of the individual graphene sheets provides an additional degree of freedom. From experimental and theoretical studies, it is recognized that the multilayer graphene electronic properties are strongly dependent on the stacking sequence. The distinct lattice symmetries associated with different stacking orders of FLG have been predicted to strongly influence the electronic properties of FLG including the band structure, interlayer screening, magnetic state, and spin-orbit coupling.

For bilayer graphene, Bernal AB stacking graphene which is more stable than AA stacking graphene shows a metallic behavior (zero gap) with chiral parabolic dispersions near the K point [103]. In AA stacking, all carbon atoms are above each other, while in a Bernal structure, carbon atoms in layer B are directly above the center of a carbon hexagon in layer A (Figure 18a,b). The description of the AA structure was often overlooked because it is energetically unfavorable [104]. However, there are reports of the existence of the AA stacking sequence of epitaxial graphene on the Si face of SiC [103]. When a perpendicular electric field is applied, the symmetry along the c-axis is broken and the two layers are no longer equivalent. Thus, an energy gap of about 30 meV is induced between the conduction band and the valence band in an external electric field of 77.94 mV/Å [105].

For trilayer graphene, the two stable crystallographic configurations are an ABA and ABC (rhombohedral) stacking order (Figure 18b–e). In a rhombohedral structure, the center of a carbon hexagon in layer A is directly below a corner of a hexagon in layer B, which is in turn directly below a nonequivalent corner of a hexagon in layer C (Figure 18c,e). These stackings are semi-metallic but their band structures are different and depend on the stacking sequence. The ABC trilayer opens a gap at the K point under an electric field. Both the Bernal (AB) and rhombohedral (ABC) stacking sequences are described theoretically [106,107] and experimentally [108,109]. For tetralayer graphene, four crystallographic configurations are predicted: an ABAB, ABCA, ABAC, and ABCB stacking order.

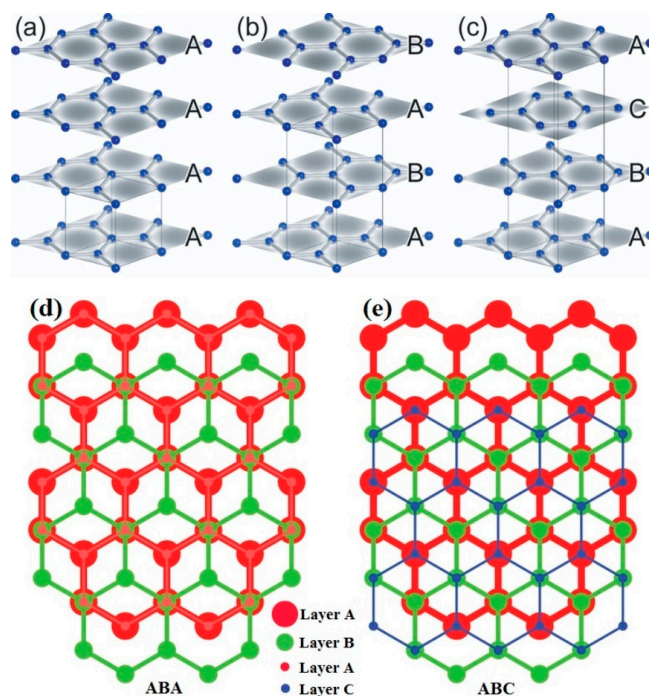


Figure 18. (a) AA; (b) AB and ABA; (c) ABC sketch.

For the growth of FLG, Daas *et al.* believe that, after a perfect crystal of graphene is nucleated on the SiC, no further growth is expected, and to grow multilayer EG, subsequent Si loss through a grown ML graphene must take place through defects in the EG. This can be seen geometrically, as the free space between carbon atoms in graphene is $\sim 1.4 \text{ \AA} < 2.3 \text{ \AA}$, and the Si atom diameter and graphene lattice are so tight that no Si can diffuse through the grown graphene layer [110].

It has been shown that the buffer layer exhibits a large band-gap and a Fermi level is pinned by a state having a small dispersion, related to the dangling bonds in between the bulk SiC and this buffer layer [111]. The existence of this buffer layer is an obstacle for the development of future electronic devices from graphene on the Si face of SiC, because it may affect the transport properties. However, hydrogen, sodium [96,112,113], oxygen [114], lithium [115], Si [116], gold [117], fluorine [118], and

germanium [119] intercalation at high temperatures can transform the buffer layer into a graphene layer with improved electrical properties compared to normal ML graphene which exists on the buffer layer [120]. With this treatment, the covalent bonds between the buffer layer and Si atoms on the SiC surface are broken and the buffer layer converts into a new graphene layer with graphene symmetry and its electronic structure. Non-metallic (fluorine, oxygen, and hydrogen) intercalations are more special as they make strong covalent bonds with the Si atoms of the SiC (Figure 19).

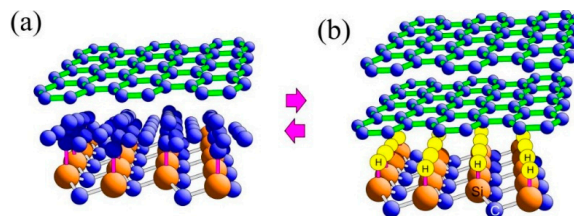


Figure 19. (a) A sketch of monolayer graphene on the SiC(0001) substrate including a strongly bound buffer layer at the interface. (b) The structural model of new phase formed, having a hydrogen intercalated layer in between the SiC substrate and the initial buffer layer which has now become the second graphene layer [112].

At LiU, different elements for intercalation are used; some of them are hydrogen, Li, Na, and Si [112–116]. Hydrogen intercalation studies by ARPES and energy-dispersive XPEEM measurements confirm that the buffer layer is converted to a graphene layer [96]. A model of hydrogen intercalation between the SiC substrate and the carbon layers is suggested (Figure 19) to explain the formation of this new phase [112]. It has been shown that H intercalation is a reversible process and the initial monolayer graphene plus carbon buffer layer situation is recreated after annealing at a temperature of about 950 °C [113], and also the charge carrier mobility of H-intercalated quasi-free-standing monolayer graphene is independent of the temperature. At room temperature, this mobility is about 3.5 times larger than that of monolayer graphene on top of the buffer layer.

For Si intercalation it is observed that Si is not able to penetrate through monolayer graphene when the sample is kept at room temperature. Intercalation is revealed to occur at an elevated temperature of about 800 °C and then the Si atoms are found to migrate through the graphene at domain boundaries and likely other defect areas. This is different from the findings on the Li intercalation of ML graphene on SiC [115]. For Li intercalation, Li-based compounds were formed and created defects/cracks on the surface which allowed Li to penetrate into the carbon layer already at room temperature. Intercalation of Si is also found to increase with time and to shift the Dirac point closer to the Fermi level.

For Na intercalation the results show that partial intercalation between carbon layers and at the interface occurred directly after deposition, but most of the Na initially remained on the surface and formed Na droplets. Intercalation was inhomogeneous and occurred on the ML and bilayer areas. The intercalation was found to be a dynamic process, increasing with time and electron/photon beam exposure, and was shown to be strongly promoted by annealing at about 100 °C. Annealing at higher temperatures resulted in Na de-intercalation and that Na started to desorb from the sample, but it was still possible to detect Na on the sample after annealing at 240 °C [113].

So far, only one element, hydrogen, has been identified as a promising candidate. We show, using first-principles density functional calculations, that nitrogen intercalation is another promising route to access charge-neutral graphene on SiC(0001). An atomically thin silicon nitride layer succeeds in satisfying all the surface Si dangling bonds, thereby eliminating charge transfer across the buffer layer to the subsequent graphene layers. These layers then display all the hallmarks of charge-neutral mono- and bilayer graphene. Achieving charge neutrality in the epitaxial graphene layer on SiC(0001) would be hugely beneficial for device performance, in particular for charge sensors and electronic devices dependent on high carrier mobilities [121]. The experimental nitrogen intercalation of graphene based on our theoretical results is in progress.

We have studied the effect of SiC substrate orientation on the graphene morphology as well as on the electron states [55]. We have grown large sheets of monolayer graphene on two 6H-SiC(0001) substrates with 0.03° and 0.25° mis-orientations from on-axis. The sample with 0.03° mis-orientations shows a continuous graphene sheet, covering also the $<15 \text{ \AA}$ high steps, with a size larger than $50 \mu\text{m}^2$. However, for the sample with 0.25° mis-orientations, higher steps (more step bunching) and smaller terrace widths (about $2 \mu\text{m}$) are revealed. The graphene layers on the terraces show mainly one type of domain. The continuation of graphene on the steps $40\text{--}50 \text{ \AA}$ in height could not be determined; therefore, graphene is either in the form of long ribbons or large sheets in this sample. STM images of ML graphene reveal two different types of carbon atom networks: honeycomb and three-for-six arrangement (Figure 20c). Since LEEM results showed only one ML graphene on our samples, the reports [122,123] which claim that two to three ML of graphene are required for the existence of the three-for-six arrangement cannot be valid.

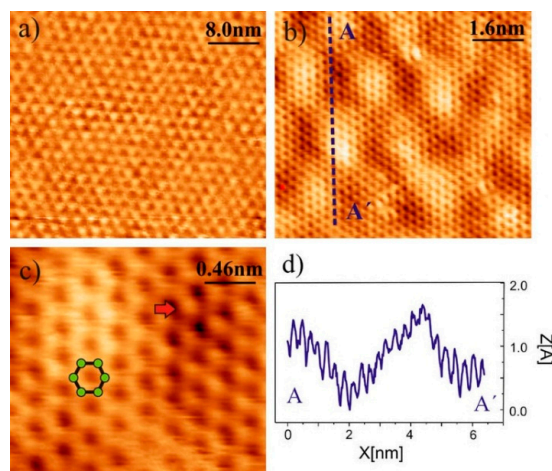


Figure 20. STM images recorded from the same region at the size of (a) $40 \times 40 \text{ nm}^2$; (b) $8 \times 8 \text{ nm}^2$; (c) $2 \times 2 \text{ nm}^2$; honeycomb and three-for-six arrangement showed by hexagonal and red arrow, respectively; and (d) a line profile extracted from image (b) [55].

Figure 21 shows the thickness dependence of graphene grown on 4H-SiC at a temperature in the range of $1700\text{--}2000^\circ\text{C}$, face polarity and orientation (on-axis and 8° off-orientation). The thickness was determined from the intensity ratio between the graphene/graphite and silicon carbide C 1s peaks, extracted from the XPS data. The process thermodynamics are not expected to change significantly for the two polytypes (6H or 4H) because the enthalpy of sublimation and the surface-free energy do not differ much.

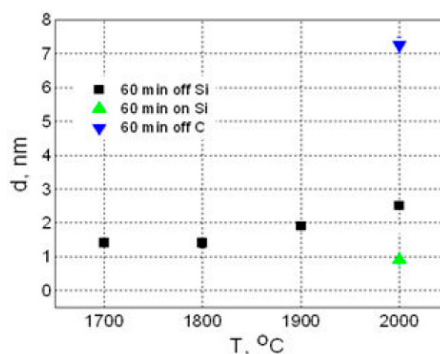


Figure 21. Graphene/graphite thickness *vs.* temperature for different faces of 8° off-oriented 4H-SiC samples and identical deposition time of 60 min. An on-axis sample is shown for comparison [21].

The corresponding torsion-resonant conductive atomic force microscopy (TRCAFM) current map and torsional morphology of graphene (grown at 2000 °C and in Ar ambient) on-axis (6H-SiC(0001)) and 8° off-axis 4H-SiC(0001) are shown in Figures 22 and 23 respectively. Comparing the morphological maps in these two images shows that while on the off-axis sample a significant step bunching was observed, a flatter surface (RMS = 2.4 nm) is obtained in the on-axis sample. The current maps are also distinctly different. A comparison of Figures 22b and 23b shows that the graphene layer on an on-axis substrate shows a uniform current all over the scanned area, suggesting a nanoscale uniformity [124]. The bright lines in the morphological map are the wrinkles on the epitaxial graphene [125]. They form due to the thermal expansion mismatch between graphene and SiC during the sample cooling, and carry a higher current density.

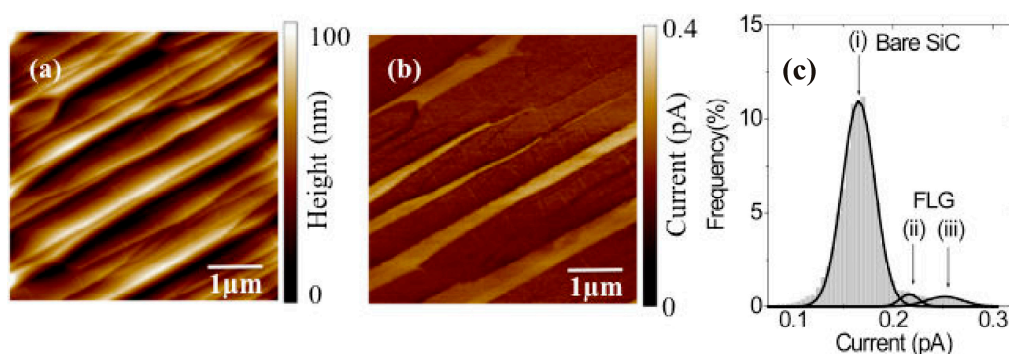


Figure 22. An AFM image (a) conductive atomic force microscopy map in (b). (c) Histograms extracted from the current map in (b). Three evaluated regions (region with graphene coverage (curves (ii) and (iii)) and region devoid of graphene (curve (i)) are indicated distinctly [124].

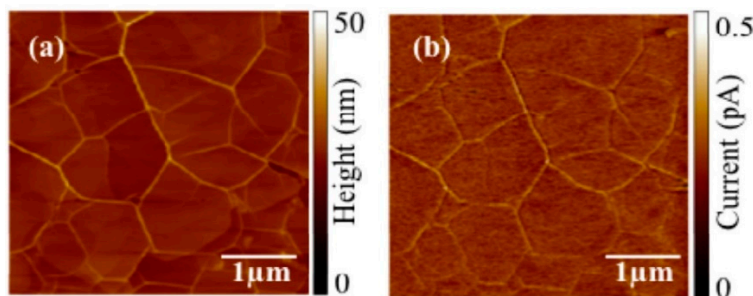


Figure 23. TR morphology (a) and current map (b) collected on an on-axis sample [124].

The off-cut angle influences the growth of graphene by multilayer graphene due to the high density of step edges on which growth nucleates. The few layers of graphene grown on 8° off-axis 4H-SiC(0001) in Ar ambient and a temperature range of 1600–2000 °C have been characterized by AFM and HR-XTEM [126]. The results show that FLG are covering the 100- to 200-nm-wide terraces of the SiC surface for all the growth temperatures (Figure 24). Wrinkles 1–2 nm high and 10–20 nm wide are preferentially oriented in the direction perpendicular to the step edges. This parallel orientation of wrinkles appears on the off-axis SiC surface, while for epitaxial graphene grown on on-axis 4H-SiC, an isotropic mesh-like network of wrinkles forms. The observed phenomenon deserves further investigations. Both the density of wrinkles and the number of graphene layers are found to increase almost linearly as a function of the growth temperature in the considered temperature range.

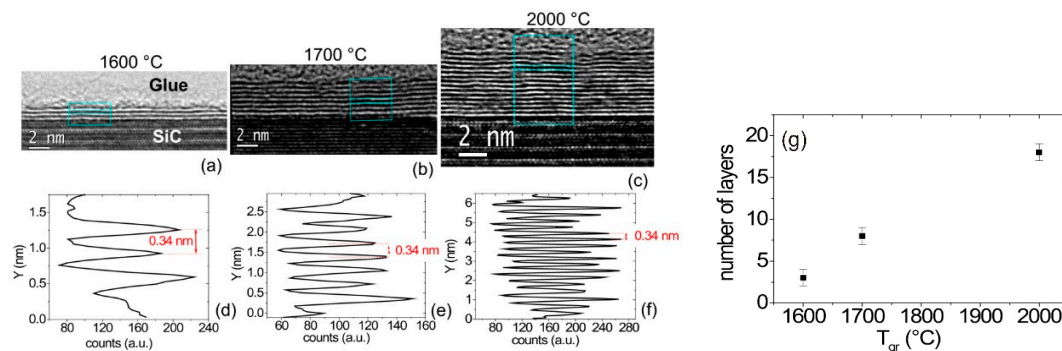


Figure 24. HRXTEM analyses on the samples annealed at different temperatures. Images on the samples annealed at 1600 (a), 1700 (b) and 2000 °C (c), and corresponding line scans ((d), (e) and (f)), showing three, eight and 18 layers grown on the surface of 4H-SiC, respectively; (g) number of graphene layers *vs.* growth temperature [126].

Two-dimensional nanoscale conductance maps (Figure 25) have been done to study the local resistance enhancement due to characteristic features in epitaxial graphene grown on 4H-SiC (0001), including substrate-related steps and the lateral variation of the number of layers, in particular the monolayer/bilayer junction [127]. The relationship between morphological and electrical maps revealed the local conductance degradation in epitaxial graphene on substrate steps or at the junction between ML and bilayer graphene regions. By conductance mapping on graphene layer coverage of 10 SiC steps with different heights, we found that the local resistance of ML graphene on steps decreases with decreasing step height. The effect of these steps strongly depends on the charge transfer phenomena between the step sidewall and graphene, while increasing resistance at the ML/bilayer junction is a purely quantum-mechanical effect. This is due to the weak wave-function coupling between the monolayer and bilayer bands, as demonstrated by *ab initio* calculations.

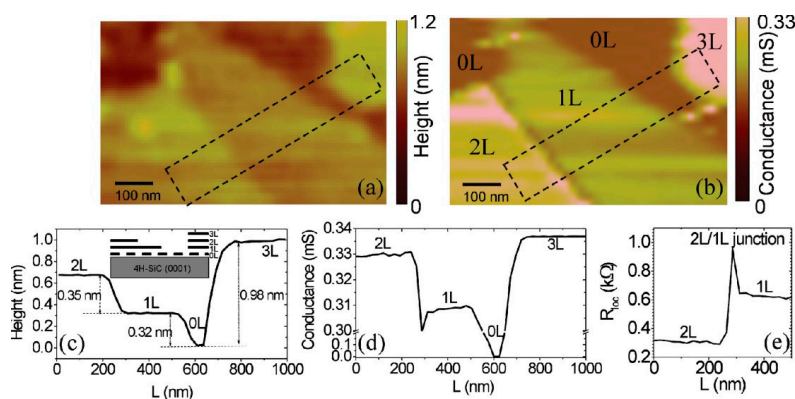


Figure 25. (a) AFM morphology and (b) conductance map on an epitaxial graphene with lateral variations in the number of layers. (c) Height profile extracted from the selected area on the morphology map, with the layer structure schematically represented in the insert. (d) Conductance profile extracted from the selected area in the conductance map. (e) Local sheet resistance of graphene calculated from the conductance profile in the region close to the monolayer/bilayer junction [127].

The above group in CNR-IMM (Nicotra *et al.*) also reported atomic resolution structural and spectroscopic characterization (STEM, and EELS) combined with nanoscale electrical measurements (conductive AFM) on a few layers of epitaxial graphene grown on an 8° off-axis, Si face of 4H-SiC [128]. The STEM analysis (carried out at an energy below the knock-on threshold for carbon) demonstrates that the buffer layer present on the planar SiC(0001) face delaminates from it on the (112n) facets of SiC surface steps. In addition, EELS reveals that the delaminated layer has a similar electronic

configuration to purely sp^2 -hybridized graphene. These observations can be used to explain the local increase of the graphene sheet resistance measured around the surface steps by conductive AFM, which suggests it is due to significantly lower substrate-induced doping and a resonant scattering mechanism at the step regions [128].

The energy structure in the density of occupied states of graphene grown on n-type 6H-SiC(0001) has been study recently. As shown in Figure 26, a quantum well (QW) and quantum well levels can be created [129]. Photoelectron spectroscopy shows that the energy structure in the valence band close to the Fermi level is described by quantum well states ($E_1 = 0.3$ eV, $E_2 = 1.2$ eV, $E_3 = 2.6$ eV). These results coincide with the calculated results for a deep ($V = 2.9$ eV) and narrow (QW width = 2.15 Å) quantum well, which forms by the potential relief of the valence bands in the structure graphene/n-SiC. It can be expected that this property is an attribute not only of graphene (or few-layer graphene) on the wide-bandgap semiconductor substrate (e.g., SiC) but also of graphene on dielectric and of suspended graphene. Based on the findings of this study, an n-type substrate results in the formation of a QW in an occupied VB, whereas the creation of a QW in an unoccupied CB is expected for a p-type substrate. The QW state formation is due to a large electron/hole mass in the direction perpendicular to the graphene plane.

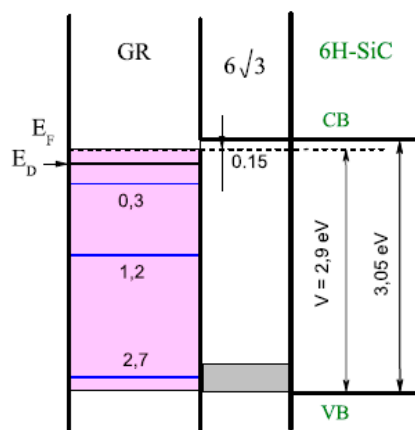


Figure 26. Scheme of the hole quantum well formed by graphene on SiC with a $6\sqrt{3}$ interface carbon monolayer (buffer layer) [129].

Epitaxial graphene on silicon carbide is a promising material for the next generation of quantum Hall resistance standards. Quantum Hall resistance standards based on epitaxial graphene on SiC have already surpassed the current state-of-the-art GaAs-based standards, with high precision and a better breakdown current density. To evaluate the quality of the available material, arrays of 100 Hall bars (Figure 27) connected in parallel on epitaxial graphene were fabricated. One out of four devices has shown quantized resistance that matched the correct value of $R_K/200$ within the measurement precision of 10^{-4} at magnetic fields between 7 and 9 T. The defective behavior of other arrays is attributed mainly to non-uniform doping. This result confirms the acceptable quality of epitaxial graphene, pointing towards the feasibility of well above 90% yield of working Hall bars [130]. Quantum Hall resistance measurements with metrological accuracy in a small cryogen-free system operating at a temperature of around 3.8 K and magnetic fields below 5 T, using a system that does not require an advanced skill set or infrastructure and so can proliferate easily, has been demonstrated [131].

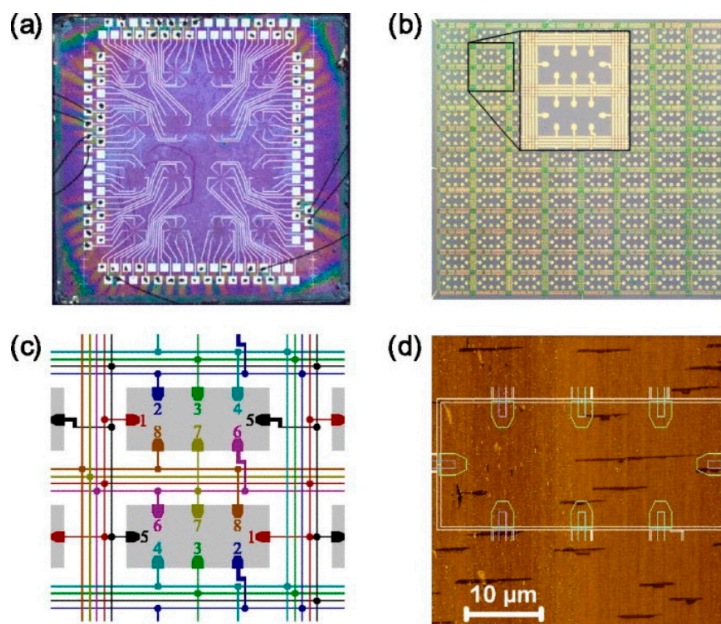


Figure 27. (a) A microphotograph of the entire chip. (b) A microphotograph of an array of 100 Hall bars. (c) A part of the schematics of the array. The interconnecting wires are arranged with a significant redundancy. (d) A typical AFM phase image of the graphene substrate with the drawing of a Hall bar on top of it. Dark areas are the bilayer patches [130].

3.3.3. Growth of Graphene on C Face

The growth mechanism of epitaxial graphene on the C face of SiC is significantly different from the one on the Si face, as the surface energy of the C face (300 erg/cm^2) is much less in comparison with the surface energy of the Si face (2220 erg/cm^2) of SiC [132]. Growth of graphene on the C face is faster and less controllable in comparison with the Si face. Graphene synthesized at this SiC surface seems to be relatively weakly attached to the underlying surface. No buffer layer (covalently bound carbon layer on the SiC surface) was detected and the first graphene layer is located at a distance of about 3.2 \AA from the SiC surface, which is too far to form covalent bonding between carbon atoms [133]. Low-energy electron diffraction [134] and scanning tunneling microscopy [54] results indicate a significant degree of rotational disorder in the graphene films. Due to the rotational disorder, the electronic properties of the graphene on the C face become similar to freestanding monolayer graphene. The band structure of each layer is linear and not parabolic as it is for bilayer graphene on the Si face of SiC [135,136]. Sprinkle *et al.* also show, based on ARPES measurements, that the band structure of multilayer graphene grown on the C face of SiC consists of multiple linearly dispersing graphene bands originating from individual rotated layers in the multilayer graphene. The observed Dirac cones show that most of the graphene sheets in the multilayer epitaxial graphene can be considered as electronically ideal isolated graphene sheets. The unique stacking order in multilayer graphene is the origin of this unique behavior. This is found out by introducing a relative rotation angle between two adjacent sheets that is not 60° as it is in graphite stacking [134]. It seems that as the C face graphene films grow, the substrate forces a relative rotation of $\sim 30^\circ \pm 7^\circ$ graphene layers in the film. The significance of this result is that uniform mono- or bilayer graphene are not necessarily a requirement for graphene electronics, since even multilayer films have the required electronic properties [135,136]. The measurements experimentally confirm that the electronic structure of each individual sheet in multilayer graphene is essentially that of an isolated graphene sheet as theoretically predicted [134] and indicated in previous experiments [23].

It has been shown that transport in thin epitaxial graphene is basically a single carrier type regardless of the SiC face. However, in thick multilayer graphene grown on the C face, electrical transport involves several groups of carriers with different mobilities in different graphene layers.

High mobilities are present in the graphene layers sandwiched between the underlying and overlaying conducting layers [137].

Therefore, using graphene layers grown on the C face, one can improve the electronic quality of graphene on the SiC. On this face graphene film likely grows following a 2×2 reconstruction, and does not have an ordered interfacial layer that causes increased carrier scattering [7].

Experimental results of graphene growth on the C face of on-axis 4H-SiC substrates using a high temperature (1800–2000 C) in Ar ambient clearly showed the existence of distinct graphene grains with different azimuthal orientations (Figure 28), indicating that the adjacent graphene layers are rotationally disordered. The results indicate that the electron carrier concentration induced in the second and third graphene layers on the C face is less than $\sim 4 \times 10^{11} \text{ cm}^{-2}$ [138]. Rotational disorder was observed, which was concluded from the sharp (1×1) μ -LEED patterns. Additionally, only six Dirac cones centered around the K-points in the Brillouin zone appeared in the constant energy photoelectron angular distribution patterns $E_i(k_x, k_y)$, recorded from grains with two, three and four graphene monolayers grown at lower temperatures (1400–1500C) [139].

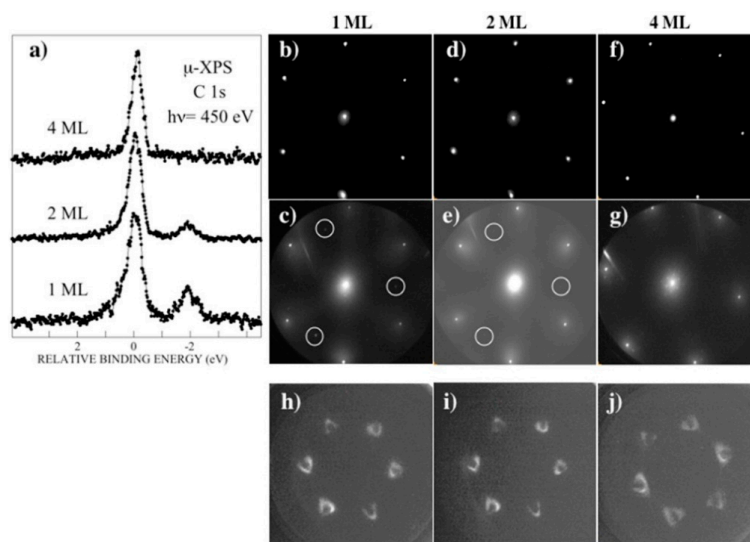


Figure 28. (a) C 1s spectra collected, using a probing area of $4 \mu\text{m}$, from domains with different graphene thickness; (b–g) show $1.5 \mu\text{m}$ selected area LEED patterns; (b,c) the one ML domain at 45 and 145 eV; (d,e) the two ML domain at 45 and 145 eV; and (f,g) the four ML domain at 45 and 130 eV, respectively. In (h–j) the photoelectron angular distribution pattern (PAD) collected from, respectively, the one ML, two ML and four ML domains are shown. The PADs were collected at an energy of 1.5 eV below the Fermi level, using a probing area of 800 nm [139].

The surface potential, chemical composition, and morphology of graphene grown on the C face of 4H-SiC have been explored [140]. By matching the same nanoscale features on the surface potential and Raman spectroscopy maps (Figure 29), individual domains and bare SiC substrate have been assigned to graphene patches one to five monolayers thick. It is shown that the growth proceeds in an island-like fashion, consistent with the Volmer-Weber growth mode, rather than in a layer-by-layer manner as established on the Si-terminated face of SiC. Raman spectroscopy data show evidence of large-area crystallites (up to 620 nm) and high quality graphene on the C face of SiC. X-ray photoelectron spectroscopy has been used for chemical analysis and surface potential mapping for thickness measurement of graphene layers. With the growth conditions used in this study, a continuous layer was not possible to form with five-monolayer-thick graphene. With the particular conditions used for graphene growth in the current study, and considering that the Volmer-Weber mode is dominant, synthesizing large-scale monolayer graphene on the C face of SiC remains a challenge, and for growth

of uniform ML graphene, the optimization of growth conditions by using different gas atmosphere or/and crucible design is needed.

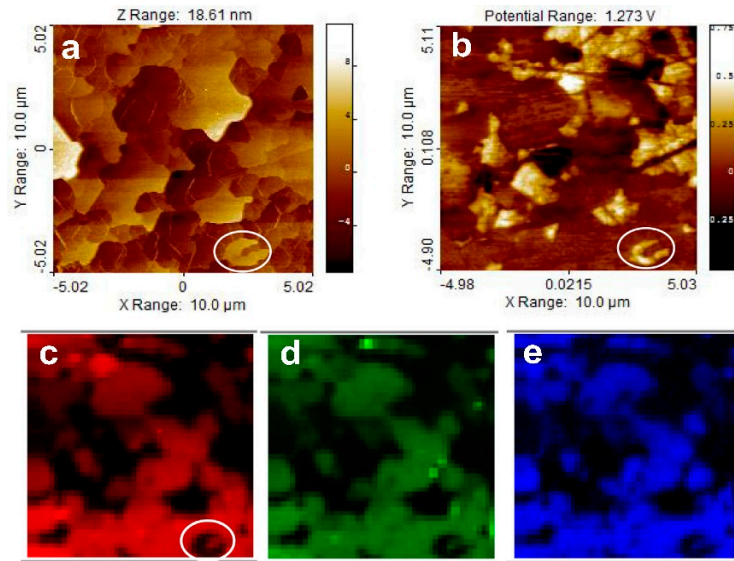


Figure 29. Topography (a) and surface potential maps (b) of a $10 \times 10 \mu\text{m}^2$ area of the sample. Spatially resolved Raman spectroscopy maps of the area depicted in (a) and (b) corresponding to 2D, G and D peak intensities are shown in (c–e), respectively. As a guide to the eye, A-like feature highlighted by the white circle in (a) and (b) can be correspondingly identified on the Raman spectroscopy maps [140].

The present study was done on the structural, vibrational, and dielectric function properties of graphene grown on the C face 4H-SiC at temperatures of 1800, 1900, and 2000 °C [141]. The results show that with increasing the temperature, the average number of layers and the size of the domains with uniform thickness increases. Enhanced sublimation of Si from the SiC results in improved graphene coverage and homogeneity. The improvement of graphene quality with the increase in growth temperature (Figure 30) is demonstrated further in an increased crystallite size (A domain of solid-state matter that has the same structure as a single crystal). This can be related to the elimination of SiC surface defects by surface restructuring during the sublimation growth. The in-plane crystallite size (L_a) is estimated from the ratio $A(D)/A(G)$ of the integrated intensities of the D band $A(D)$ and G band $A(G)$.

$$L_a = 2.4 \times 10^{-10} \lambda_{laser, nm}^4 \left(\frac{A_D}{A_G} \right)^{-1}$$

Micro-Raman spectroscopy imaging (μRSI ; Figure 30a–c) analysis has indicated that the graphene grown at 1800 °C exhibits decoupled graphene layers, while at higher temperatures the graphene stack consists mostly of graphitic layers. The transition from decoupled to Bernal stacked graphene layers with the increase in growth temperature is attributed to a competition between growth mechanisms and defect-assisted growth. At high temperatures, the increase of the amount of C atoms leads to the formation of Bernal stacked graphene layers around the extended surface defects (e.g., scratches). With increasing the thickness, a redshift of the critical point transition energy was observed at 4.5 eV in the dielectric function of graphene, which is accompanied by an increased polarizability. The graphene grown at 1800 °C shows graphene-like behavior, while the graphene grown at 2000 °C has a dielectric function closer to the one reported for graphite in accordance with the μRSI results. Both SE analysis and TEM results demonstrated the presence of an interface layer between the graphene layer and the SiC substrate. It was found that this interface layer is amorphous and consists of a mix of C and Si which is trapped during the sublimation process, and its thickness increases with the increase in growth temperature. Moreover, at the interface an enhanced restructuring of the SiC was observed.

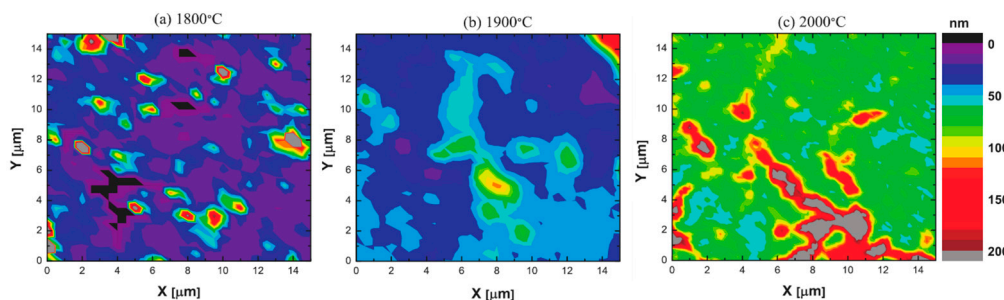


Figure 30. Three $15\ \mu\text{m}^2$ color-coded maps of in-plane crystallite size for the graphene grown at: (a) $1800\ ^\circ\text{C}$; (b) $1900\ ^\circ\text{C}$; (c) $2000\ ^\circ\text{C}$. The color bar represents the crystallite size in nm. The gray color in the bar represents a defect free area. The step is $0.5\ \mu\text{m}$ for the maps in (a) and (b) and $0.25\ \mu\text{m}$ for the map in (c) [141].

Recently, a deeper study on the nature and composition of this interfacial amorphous layer on the C face of SiC was provided by Nicotra *et al.* using aberration-corrected STEM, electron energy-loss spectroscopy (EELS), AFM, and the density functional theory [142]. They have shown that for high growth temperatures, the graphene/SiC(000 $\bar{1}$) interface is dominated by a thin amorphous film which strongly suppresses the epitaxy of graphene on the SiC. This film has almost a uniform thickness regardless of the number of the overlying graphene layers. The chemical analysis shows the presence of C, Si, and O in this amorphous film. Figure 31 shows three high-angle, annular dark-field and bright-field STEM images from different locations. The common characteristic of all three snapshots is the presence of an amorphous film on top of the SiC substrate, independent of the presence or absence of graphene. From the dark-field images as well as from EELS measurements it is possible to distinguish this amorphous region from the epoxy glue used for specimen preparation [142].

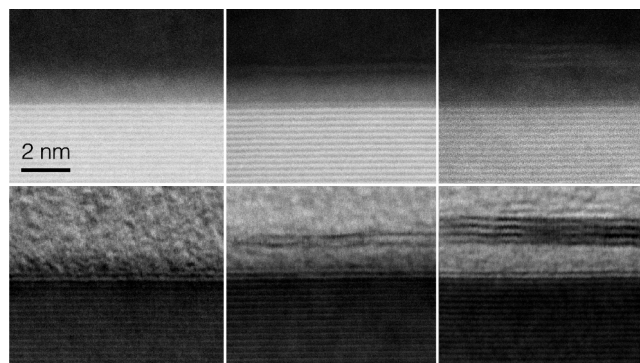


Figure 31. High-angle annular dark-field (above) and bright-field (below) STEM images at three different areas of the graphene/SiC(000 $\bar{1}$) system, showing zero (left), one (center), and three graphene layers (right) on top of an amorphous thin film. The acquisition took place at a 60 keV primary beam energy in order to prevent beam-induced damage [142].

3.4. Growth of Graphene on SiC Nonpolar Faces

As mentioned in the previous sections, during the graphitization of polar faces of SiC(0001) by thermal decomposition, a strongly bound carbon-rich layer (buffer layer) forms at the graphene/SiC interface. The existence of this buffer layer introduces donor states that effectively dope graphene, and it is also an obstacle for the development of future electronic devices as it affects the transport properties of the graphene layer. Buffer layer intercalation and the subsequent formation of quasi-free-standing graphene is a promising approach (as mentioned Section 3.3.2) for solving this problem.

It has been shown that there is a method to directly grow a quasi-free-standing graphene layer without using intercalation by the growth of graphene on the low-index a(11 $\bar{2}$ 0) and m(11 $\bar{1}$ 0) planes

of SiC as substrates [110,143,144]. Figure 32 shows the c-, m-, and a-planes on a 6H-SiC unit cell. The difference in the atomic arrangement on the surfaces can be quantified by the surface lattice site packing density values (as shown in Figure 32c,d), defined as the number of lattice sites per unit area on a given plane [110]. The growth of EG on the nonpolar $(11\bar{2}0)$ and $(11\bar{1}0)$ planes is different from the c-plane in terms of surface morphology, quality, and thickness, as the surface crystallographic structure and therefore surface energies are significantly different.

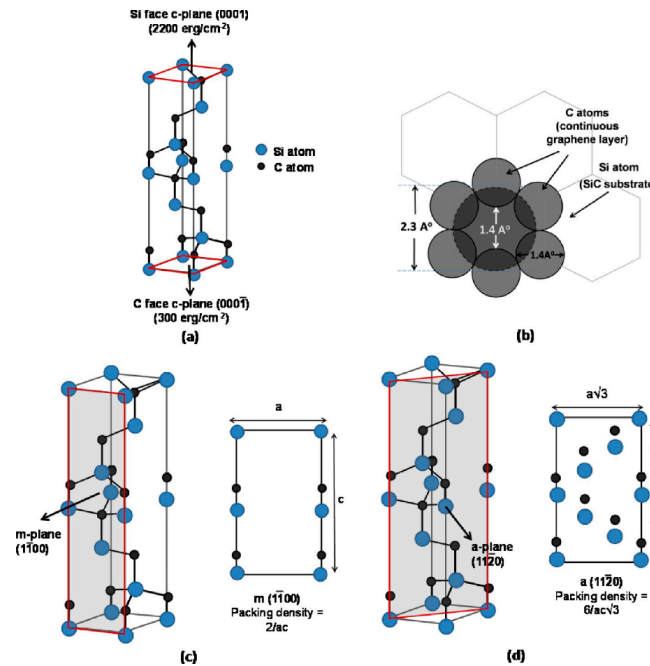


Figure 32. (a) Unit cell of 6H-SiC. (b) Continuous EG formation on the Si face. Packing density calculation on (c) m-plane, (d) a-plane of the 6H-SiC crystal. The packing density on the a-plane is $\sqrt{3}$ times as high as that on the m-plane, which translates into slower sublimation of Si and, hence, lower EG thickness [110].

Jabakhanji *et al.* investigated the epitaxial growth of graphene on both polar $(000\bar{1})$ and nonpolar $(11\bar{2}0)$ planes in a confined atmosphere created by covering the SiC substrate with a graphitic cap during the growth. The AFM and SEM (Figure 33) results show that the materials grown on $(11\bar{2}0)$ planes of 6H-SiC are mainly ML graphene islands, and based on their Raman measurements results, graphene layers are lightly doped and almost freestanding, the same as the epitaxial graphene grown on $(000\bar{1})$. They have shown that in both cases, the quality of the graphene layer is good enough to observe half-integer quantum Hall effect patterns [143].

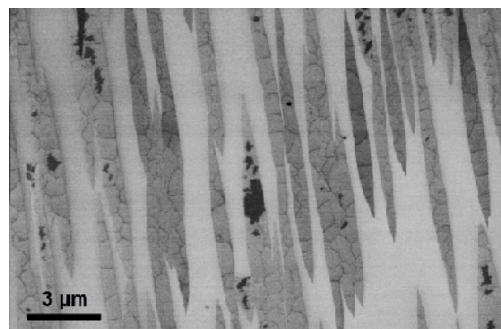


Figure 33. SEM image of ML graphene grown on 6H-SiC($11\bar{2}0$) [143].

Epitaxial graphene was grown on 4H-SiC($\bar{1}\bar{1}00$) and 4H-SiC($11\bar{2}0$) substrates using sublimation growth in an Ar atmosphere by Ostler *et al.* [144]. With the aid of XPS, ARPES, LEEM, LEED measurements, and the density functional theory, they have shown that quasi-free-standing graphene layers directly grow on the nonpolar ($11\bar{2}0$) and ($\bar{1}\bar{1}00$) surfaces. Both the experiment and theory results confirm the absence of a buffer layer for graphene on both planes. Based on the previous reports, they believe that the formation of tetrahedral bonds between the Si atom at the SiC surface and the C monolayer is the driving force for the formation of the strongly bound interface layer in epitaxial graphene on SiC(0001). In the case of nonpolar SiC surfaces, the formation of such bonds is not allowed, as weakly interacting configurations have been observed and calculated in reconstructed SiC(000 $\bar{1}$) surfaces [145]. Therefore, they associate the inhibition of tetrahedral bonds with the stability and the growth of the quasi-free-standing graphene configuration in the case of low-index ($11\bar{2}0$) and ($\bar{1}\bar{1}00$) planes. From an electrical view, the absence of a buffer layer should lower undesirably high doping levels and improve the overall electronic characteristics, without the need for post-annealing intercalation processes. By using LEEM data they have investigated the morphology and the thickness distribution of the graphene on the nonpolar surfaces. Figure 34a shows a bright-field image of graphene on 4H-SiC($\bar{1}\bar{1}00$); the growth on this plane is the same as the one on SiC(000 $\bar{1}$), exhibiting large rotational disorder. The graphene layer thickness distribution is difficult to control, yielding samples with small areas of monolayer graphene and uncovered areas alongside four ML graphene.

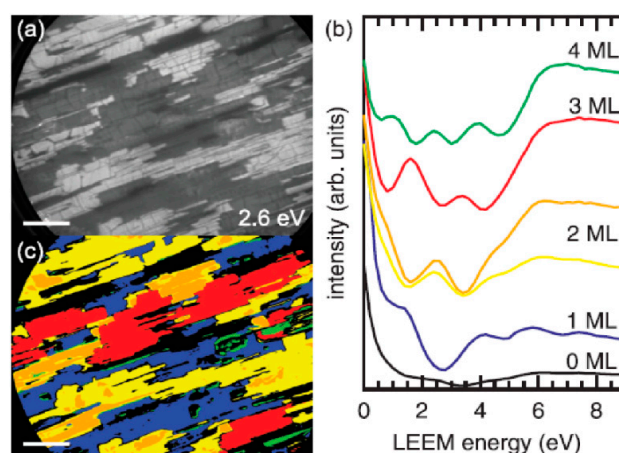


Figure 34. (a) LEEM bright-field image at $E_{\text{LEEM}} = 2.6 \text{ eV}$ of graphene on 4H-SiC($\bar{1}\bar{1}00$). (b) Typical reflectivity spectra offset from each other for clarity. (c) False color image of same area as in (a) colored corresponding to the spectra shown in (b). The length of the scale bar is $1 \mu\text{m}$ [144].

For growth of epitaxial graphene on SiC($11\bar{2}0$), they have shown that graphene grows without rotational disorder, even though no buffer layer is present. Figure 35a shows a bright-field image of graphene on ($11\bar{2}0$). The graphene coverage is more uniform in comparison with the ($\bar{1}\bar{1}00$) planes, with the larger area coverage of ML graphene. The results could indicate alternative ways of wafer-scale graphene production based on the EG/SiC technology.

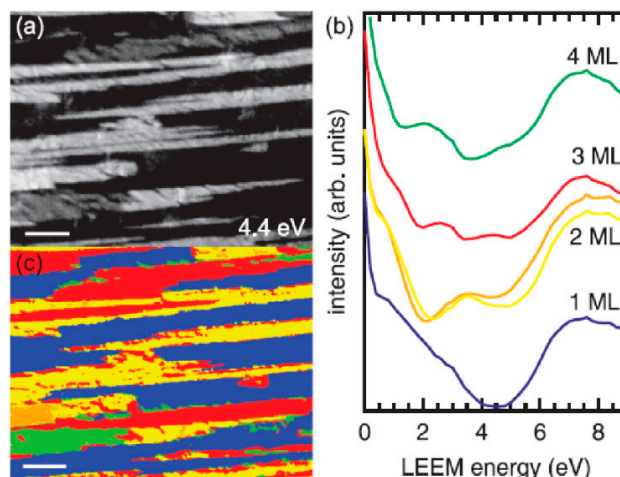


Figure 35. (a) LEEM bright-field image at $E_{\text{LEEM}} = 4.4$ eV of graphene on 4H-SiC(11 $\bar{2}$ 0). (b) Typical reflectivity spectra offset from each other for clarity. (c) False color image of same area as in (a) colored corresponding to the spectra shown in (b). The length of the scale bar is 1 μm [144].

Recently, a comparison between the growth of EG on polar and nonpolar planes of n-type 6H-SiC have been performed by Daas *et al.* [110]. They have studied the graphitization quality on polar Si and C faces and nonpolar (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) planes. Growth of EG was performed in an inductively heated RF furnace at high temperature and high vacuum. Figure 36 shows AFM images of EG-a, EG-m, and EG-c layers grown at the temperatures 1350, 1400, and 1450 $^{\circ}\text{C}$. Epitaxial graphene layers on the Si face show step-like morphology at all growth temperatures, and no grain boundaries are visible in the AFM images, suggesting a grain size >5 μm with a rms roughness <0.5 nm, while C face EG layers show clear grain boundaries. Surface morphology by AFM and LEEM shows significant differences between polar and nonpolar faces. Nonpolar faces display significantly smaller grain sizes in comparison with polar planes. The quality of EG layers is determined by Raman measurements, which agreed with the AFM measurements, except for the Si face. This difference was attributed to point defects in the Si face EG, as opposed to extended grain boundaries on the other faces [110].

The smaller grain sizes grown on the nonpolar faces are attributed to the lack of a hexagonal template (Figure 37), different surface energies, and step dynamics on the nonpolar faces. The Si face of the SiC substrate provides a hexagonal template for the EG growth by a $(6\sqrt{3} \times 6\sqrt{3})R 30^{\circ}$ surface reconstruction of the SiC surface which facilitates long-range order in the EG (Figure 37a). The greater coverage of grain boundaries allows greater Si desorption from the grain edge, resulting in thicker films on the nonpolar faces, as confirmed by XPS. Conversely, the Si and C faces, with larger crystals and a lower density of grain boundaries/defects, showed thinner layers. Thus, the growth of multilayer graphene, after the nucleation of the first layers, is shown to be limited by the density of defects/grain boundaries in the grown EG layers that allow the escape of Si from the SiC substrate [110].

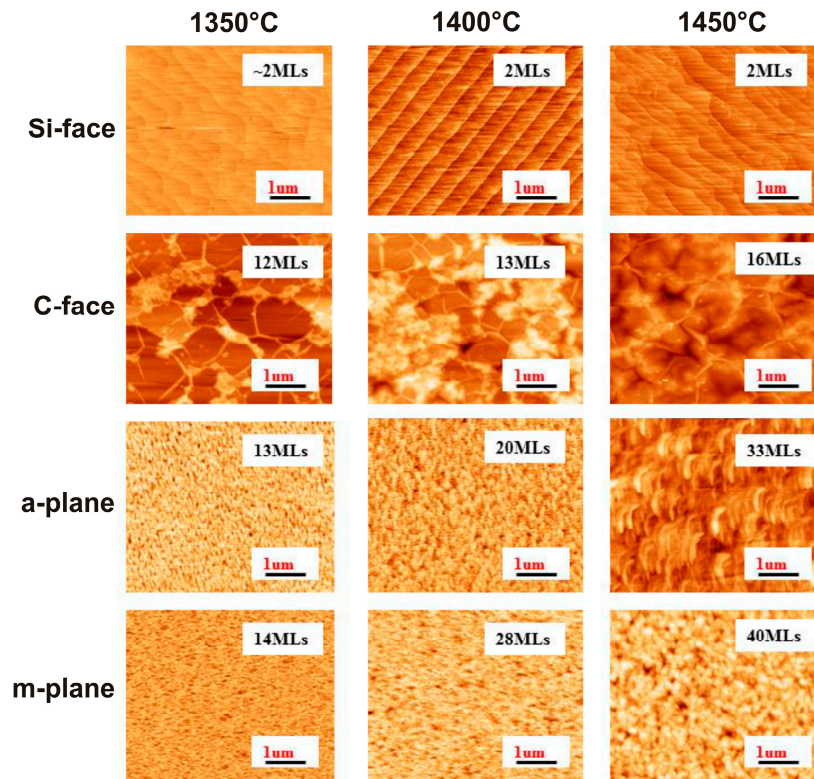


Figure 36. AFM images of epitaxial graphene grown on a-, m-, and c-plane 6H-SiC substrate at four different growth temperatures: 1300, 1350, 1400, and 1450 °C, respectively. Here the a- and m-planes show crystalline graphite-like features whereas the c-plane shows step-like features of EG on the silicon face [110].

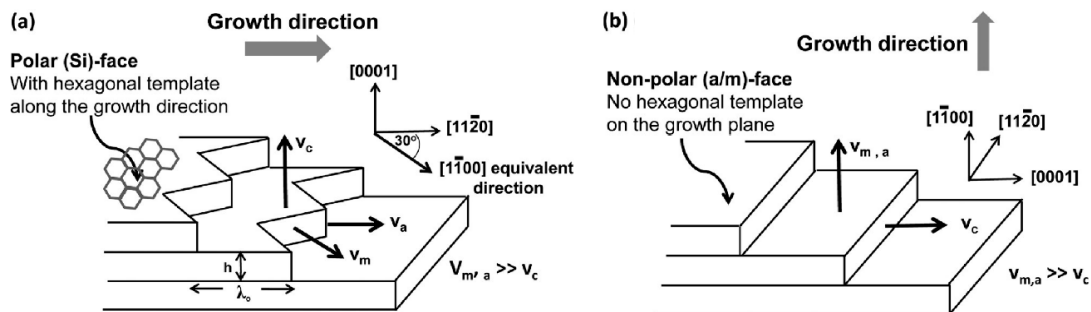


Figure 37. Graphene growth mechanism on (a) the polar (Si) face SiC with offcut toward $[11\bar{2}0]$ and (b) the nonpolar a/m face with slight offcut along $[0001]$. The EG growth on the polar face proceeds laterally while the EG growth on the nonpolar face is limited by the vertical growth rate. The zigzag structure shown on the polar face step edge is a consequence of two possible lateral growth directions [110].

3.5. Epitaxial Graphene on 3C-SiC and Comparison with other Polytypes

4H-SiC and 6H-SiC are ideal templates for the growth of graphene as they have hexagonal structure. For this reason, and because they are commercially available, an enormous number of works have been done in this field. In comparison with graphene growth on hexagonal SiC, limited attention has been given to graphene growth on 3C-SiC, which has a cubic structure. The (111) surface of this crystal is naturally compatible with the six-fold symmetry of graphene. Published works have focused on graphene formation on 3C-SiC deposited on Si, but it is known that 3C-SiC grown on Si contains

a lot of extended defects. In our study we use 3C-SiC(111) grown on 4H- and 6H-SiC(0001) which eliminates thermal and lattice mismatch, and opens a new possibility for applications. Graphene can be used for contact layers on solar cells made on 3C-SiC [146].

During annealing SiC substrates, a surface restructuring results in the formation of steps and terraces and they may have an impact on the doping uniformity (graphene conductance). The main effect of the surface restructuring is step bunching, which is different in the different SiC polytypes due to energetic reasons. The formation of graphene on 3C-SiC, and for comparison on 4H- and 6H-SiC, substrates has been analyzed with respect to step bunching, taking into account the initial roughness of the substrate surface [22]. The graphene samples grown on 4H, 6H and 3C-SiC substrates in the same conditions were characterized by LEEM in order to evaluate thickness distribution. In all LEEM images (Figure 38), the bright area represents a ML graphene and darker areas represent bilayer graphene. Figure 38a shows the LEEM image for graphene grown on a 4H-SiC substrate. Graphene on this sample consists of one and two MLs with one small area of three MLs (the black spot). Large and homogeneous ML graphene grown on 6H-SiC and 3C-SiC is shown in Figure 38b,c. The areas of one ML coverage, as extracted from the LEEM images, are about 60%, 90%, and 98% for 4H, 6H, and 3C polytypes, respectively. During heating a SiC substrate above 1200 °C, the SiC surface undergoes microscopic restructuring by forming steps. This process, called step bunching, is different from surface reconstruction and refers to surface morphology. Step bunching, which is governed by energy minimization on different terraces, is a fundamental phenomenon in SiC.

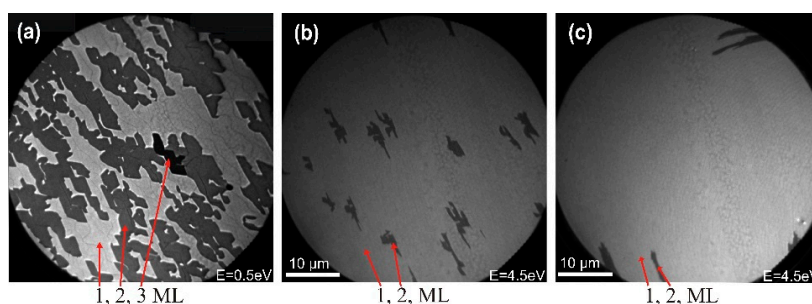


Figure 38. LEEM images of graphene on (a) 4H-SiC with 60% coverage by ML (bright area), darker areas represent bilayer while small black spot embodies three layers of graphene; (b) 6H-SiC with 92% of one ML coverage (bright area); (c) 3C-SiC with 98% one ML coverage (bright area). The black areas in (b) and (c) represent two ML graphene [22].

Several models have been proposed for the step bunching mechanism during SiC growth. Heine *et al.* considered that the energies of interaction for each SiC bilayer plane are different due to the unique stacking sequence of the polytypes [147]. Kimoto *et al.* used Heine's calculation to discuss the formation of the unit cell height steps from a viewpoint of the surface equilibrium process in which the terrace with minimal stacking energy on a stepped surface will take over during SiC epitaxial growth [148]. In the case of sublimation, specifically graphene formation, we have a reverse scenario, which is now related to decomposition/erosion of SiC bilayers from the lattice stack. In this act, since Si has the highest vapor pressure, Si leaves the surface while C nominally rests and migrates on the surface. Surface restructuring was studied by examining around 300 steps using AFM for samples annealed at 2000 °C. The results are shown in Figure 39a–c for the graphitized surfaces of 4H-, 6H-, and 3C-SiC substrates, respectively. Starting from a typical step height around 0.25 nm before heating, the steps were grouped in four major heights related to the polytype structure. Some dispersion of the step heights above 1 nm was observed in all samples but with a very low probability (not shown). Having a rather low step height distribution is one advantage of our results, since it has been reported that the resistance of epitaxial graphene on SiC increases linearly with step height on the substrate [149]. The corresponding histogram of the step height for 4H-SiC (Figure 39a) indicates that two-bilayer-height steps are the most probable and four-bilayer-height steps show a significant probability. For the 6H-SiC

sample (Figure 39b), two- and three-bilayer-height steps dominate. On the 3C-SiC graphene sample, one SiC bilayer height has the highest percentage (48%) of appearance although some larger steps are present (Figure 39c).

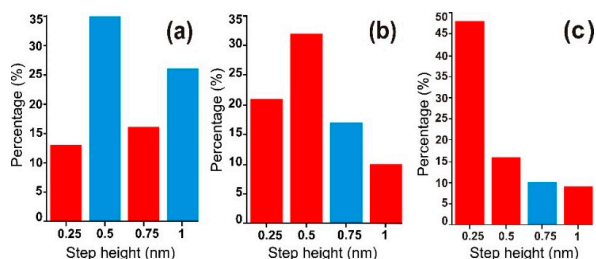


Figure 39. The respective histograms of the step height probability for the graphenized surfaces of: (a) 4H-SiC; (b) 6H-SiC; and (c) 3C-SiC substrates [22].

Based on the mentioned terrace energies (Section 3.2), on 3C-SiC all terraces have the same decomposition energy (Figure 14c) and no energetically driven step bunching is expected. In fact, the most probable step height observed (Figure 39c) is 0.25 nm, but additional step heights suggest that there are additional factors leading to surface restructuring. In 3C-SiC, a non-uniformity of sublimation can be induced by the presence of extended defects such as stacking faults which are characteristic of this material.

Figure 40 shows a hypothetical model for graphene development on 3C-SiC (4H-SiC is shown in Figure 15) without considering a buffer layer formation. The thickness uniformity of graphene on SiC depends on the uniformity of Si sublimation from the surface and C availability. The decomposition rate of all 3C-SiC terraces is the same in a defect-free crystal, thus providing a uniform source of C on the surface (Figure 40a) which results in a superior uniformity of the grown graphene layer (Figure 38c). Note the frequency of formation of one bilayer step height over the surface for the 3C sample in Figure 14c. However, the presence of defects, e.g., stacking faults, with a typical density of $5 \times 10^3 \text{ cm}^{-1}$ [150], may be a reason for step bunching on the 3C-SiC surface (Figure 40b). Actually, step decomposition becomes faster at the position of the defects (stages 1 and 2 in Figure 40b). On the 3C-SiC surface, this is resulting in nonuniformity of terrace removal, and therefore defect-induced step bunching on the 3C-SiC surface (stage 3 in Figure 40b). Our results also indicate that there exists a range of optimal terrace width which should be kept in order to maintain formation of one monolayer graphene and to avoid the increase of carrier concentration [73].

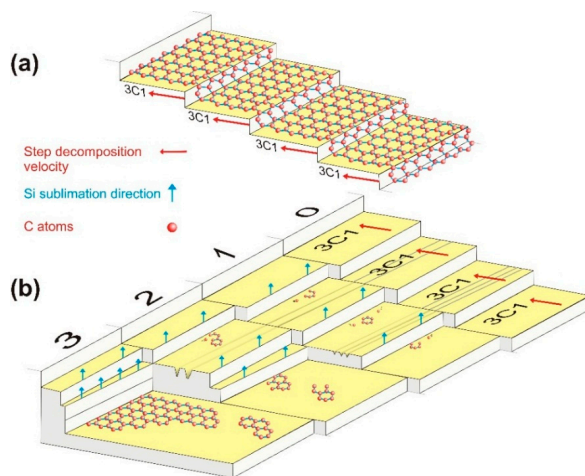


Figure 40. Graphene growth evolution (buffer layer formation not shown): (a) on a defect-free 3C-SiC substrate; (b) on a 3C-SiC with defects (lines indicate stacking faults) [22].

The relationships between surface reconstruction, graphene layer thickness, and electronic properties of epitaxial graphene grown on both polar faces of 3C-SiC were studied by using large-area μ -SE mapping (Figure 41) and LEEM/ μ -LEED investigations [95]. Large homogeneous ML graphene domains with sizes up to $\sim 2 \times 2 \text{ mm}^2$ on the Si face are observed, while on the C face, domains with homogeneous thickness are significantly smaller. The interface layer on the C face included small uncorrelated nucleation sites that have high graphene coverage within the interface layer. It seems that these nucleation sites are associated with small pit defects on the C face substrate. It is also shown that carrier mobility in the homogeneous areas of one ML graphene is higher than the mobility in the thicker graphite islands. The critical point (CP) energy position associated with an exciton-enhanced van-Hove singularity in the density of states at $\sim 4.5 \text{ eV}$ blue-shifts with decreasing the number of layers for both Si and C faces. The analysis suggests that the interaction between the graphene layer and the substrate is stronger for the Si face material. These results are consistent with the LEED observations indicating the formation of a $(6\sqrt{3} \times 6\sqrt{3})R 30^\circ$ buffer layer on the Si face and an absence of any specific reconstruction on the C face samples.

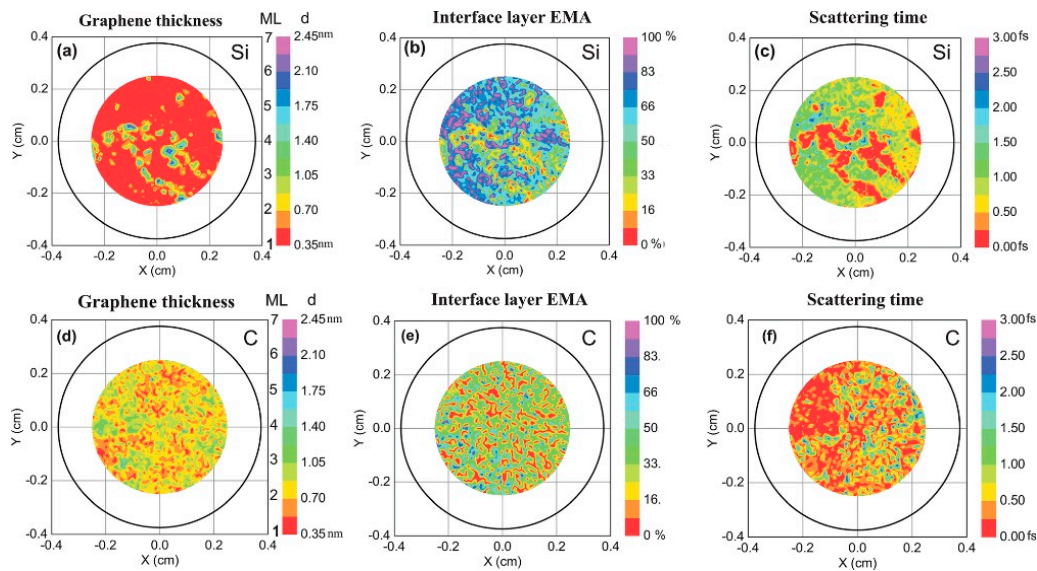


Figure 41. The μ -SE maps of best-match model parameters for graphene layer thickness (a,d), interface-layer SiC percentage (b,e), and free-charge-carrier scattering time (c,f) for EG grown on Si face (a,b,c) and C face (d,e,f) of 3C-SiC [95].

As 3C-SiC is a suitable substrate for the growth of nitride and especially epitaxial graphene layers [22], we studied defect formation in $\sim 1\text{-mm}$ -thick 3C-SiC layers grown on off-oriented 4H-SiC substrates via a lateral enlargement mechanism using different growth conditions. Based on this method, a two-step growth process was developed, which provides a balance between the growth rate and the number of defects in the 3C-SiC layers. It proved that the two-step growth process combined with a geometrically controlled lateral enlargement mechanism allows the formation of a single 3C-SiC domain which enlarges and completely covers the substrate surface. High crystalline quality of the grown 3C-SiC layers is confirmed using high resolution X-ray diffraction and low temperature photoluminescence measurements [151,152]. Figure 42 illustrates the process conditions for 3C-SiC growth.

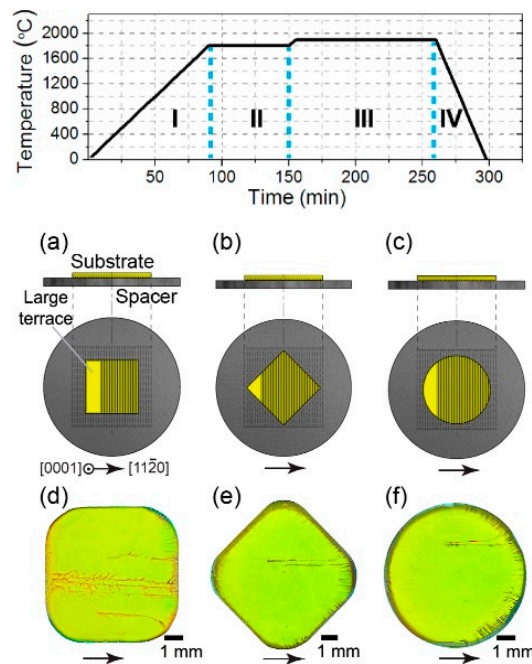


Figure 42. Sketch of two-step growth process of 3C-SiC layers (top). (a–c) Schematic illustration of spacer and substrate arrangements. Optical micrographs of the free-standing 3C-SiC grown using (d) original, (e) 45° rotated, and (f) circular spacer openings. Black arrows indicate the step-flow growth direction [151,152].

4. Graphene Growth on Etched SiC Substrates

4.1. Substrate Preparation by Etching

The substrate surface quality is crucial for semiconductor technology in general, and in specific for the growth of graphene on SiC. Using wafers with inhomogeneous surfaces containing mechanically disturbed and oxidized regions can result in low quality device performance, such as the increase of recombination. Commercial, mechanically polished SiC wafers are often damaged and show a high density of scratches in AFM (Figure 43a). Hydrogen etching [153–157], thermal etching [158–161], and tetrafluorosilane (SiF_4) etching [162] are known to improve this situation by removing several hundred nanometers of bulk material. Here we present some hydrogen etching studies.

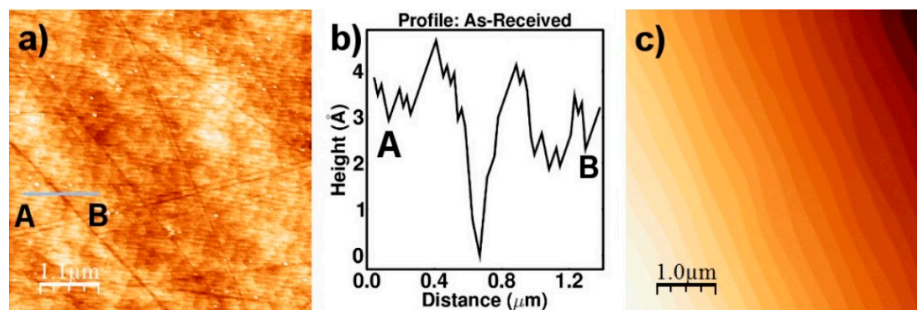


Figure 43. AFM image of an (a) as-received SiC(0001) substrate; (b) a line-profile from A to B; (c) hydrogen-etched SiC [156].

Etching in hydrogen is a common procedure in CVD reactors to remove polishing damage on SiC and provide a well-defined surface with atomically flat terraces for the growth of epitaxial graphene. A hydrogen etching study on the Si face of SiC substrates showed that there is an optimal hydrogen

flow (0.5 standard liters per minute (slpm)) and sample temperature (1500 °C) to achieve the best results [157]. Figure 44 shows AFM images of SiC samples etched in hydrogen under different process conditions. All samples were annealed for 15 min at an ambient hydrogen pressure of 1 atm. The temperature range was 1450–1550 °C and the hydrogen flow rate was varied between 0.2 and 3.0 slpm. Samples etched with a hydrogen flow ≤ 0.5 slpm and a temperature of 1450 °C still show residual scratches, and etching with the same flow at 1550 °C leads to droplet-like features at the SiC step edges. At 1550 °C and a high flow of 3.0 slpm, step bunching and large defects were observed. The best hydrogen etching conditions were used to treat the SiC samples before graphitization, and graphene growth results on these samples show that the thickness distribution is Gaussian with a mean of 1.1 ML and a standard deviation of 0.17 ML. This shows that the growth of EG is very reproducible due to the high controllability of the process parameters [157].

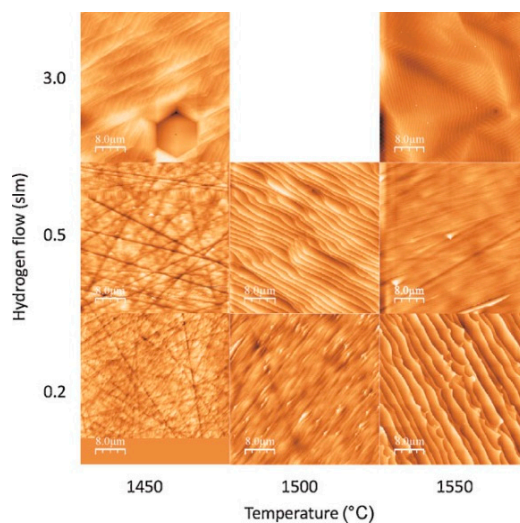


Figure 44. AFM images of hydrogen-etched Si face of SiC surfaces etched with various hydrogen flow rates and temperatures [157].

Hydrogen etching on the C face of SiC substrates was also performed at a temperature range of 1350–1550 °C, for either 0 or 30 min [156]. All samples were etched at 200 mbar of hydrogen, with a flow rate of 5 slpm. The results showed that there is an optimal temperature (1450) and time (0 min). It was found that the zero-minute etch at 1550 °C and 30-minute etch at 1450 °C were resulting in a surface with a number of pits (Figure 45a), while for zero-minute etches at 1350 °C and 1450 °C no pits were visible on the SiC surface (Figure 45b). AFM of this surface (Figure 45d) reveals a much larger terrace width (TW), about ≈ 550 nm. The formation pits are due to the preferential etching of threading screw dislocations that intersect the surface. Additionally, on a flat area, AFM results show step morphology (Figure 45c) with an average terrace width of 250 nm. Based on the results (larger terrace width lack of pits), etching at 1450 °C for 0 min was used for all the samples. The larger terrace widths are advantageous because they allow for fewer steps per electronic device, which results in improved performance.

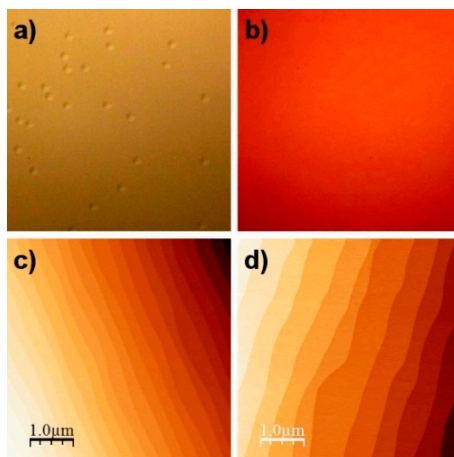


Figure 45. Nomarski and AFM images of etched SiC(000 $\bar{1}$). (a) Nomarski image of the SiC(000 $\bar{1}$) surface following a 30 min etch at 1450 °C. The small features on the surface are pits. (b) Nomarski image of etched sample for 0-min. AFM images of (c) an area in (a) (TW \approx 250 nm); (d) an area in (b) (TW \approx 250 nm) [156]. The optical images in (a) and (b) are both 150 $\mu\text{m} \times$ 150 μm .

4.2. Graphene Nanoribbons (GNRs) on SiC

Graphene is a semi-metal and does not possess a bandgap. This hinders graphene application, especially in switching devices. A bandgap can be opened by breaking the crystal symmetry of graphene. Several different approaches have been tried to find the solution of this problem. One of them is theoretical, considering the confinement of electrons into one dimension [163], which can be expected in graphene nanoribbons (GNRs). They can be produced as strips of nanometer width cut from graphene. In general, GNRs can be of two types depending upon their termination. Figure 46 shows the structures of armchair and zigzag GNRs. The width of armchair GNRs is decided by the number of hexagonal carbon rings, or generally referred to as dimer lines (N_a) across the ribbon. Similarly, the width of zigzag GNRs is dependent on the number of zigzag chains (N_z) across the ribbon [164].

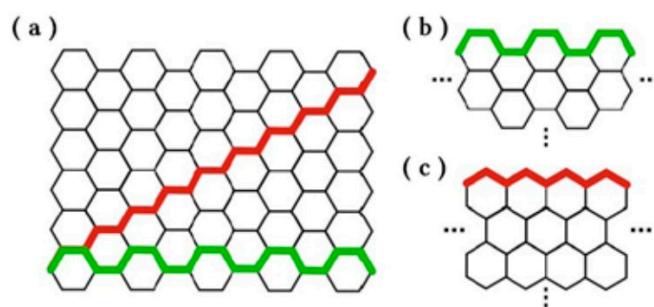


Figure 46. (a) Structure of graphene nanoribbon: (b) armchair, (c) zigzag.

Theoretical band structure calculations for GNRs, using the tight binding approach, were made in 1996 by the group of M. Dresselhaus. They show the importance of the edge type and the edge termination for the band structure.

The armchair nanoribbons are predicted to have a bandgap which is inversely proportional to the ribbon width. Mechanical cutting, etching of graphene and other published methods to produce such nanoribbons are not appropriate because often the edges are destroyed and become disordered, which compromises the aimed properties [165–167]. A different approach was proposed by de Heer and coworkers in 2010 [168]. They explore the self-organized growth of graphene nanoribbons on a templated silicon carbide substrate prepared using scalable photolithography and microelectronics

processing. A precise control over the natural step bunching mechanism during SiC heating to elevated temperatures allowed the preparation of a crystal facet for self-organized graphene growth. The natural choice for this purpose may be (1–10n) facets. Controlled facets are achieved by the reactive ion etching of trenches of defined depths since it was found that it is the etch depth that ultimately defines the width of the GNRs prepared in the subsequent treatment. Etch depths of 20 nm were readily achieved, resulting in a ribbon width (~ 40 nm) sufficiently narrow to give a sizable bandgap at room temperature. The nanoribbon growth steps are depicted in Figure 47.

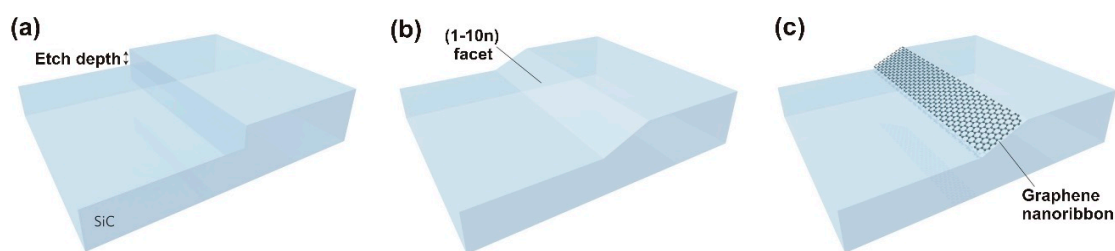


Figure 47. Process steps modifying the SiC substrate surface for graphene nanoribbon growth. (a) A nanometer-scale step is etched into SiC crystal by fluorine-based RIE. (b) The crystal is heated to 1200–1300 °C (at low vacuum), inducing step flow and relaxation to the (1–10n) facet. (c) Upon further heating to ~ 1450 °C, self-organized graphene nanoribbon forms on the facet [168].

Direct nanoribbon growth avoids the need for damaging post-processing. Raman spectroscopy, high resolution transmission electron microscopy and electrostatic force microscopy confirm that nanoribbons as narrow as 40 nm can be grown at specified positions on the substrate. Prototype graphene devices have been demonstrated to exhibit quantum confinement at 4 K, and an on-off ratio of 10. Carrier mobility up to $2700 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ at room temperature was measured. They also demonstrate the scalability of this method by fabricating 10,000 top-gated graphene transistors on a 0.24 cm^2 SiC chip.

Other methods have been suggested, e.g., in [169]. The authors describe a technique for selective graphene growth and nanoribbon production onto 4H- and 6H-SiC. They demonstrated that graphene layers can be selectively grown onto Au- and Si-implanted SiC at pressures and temperatures of 1×10^{-6} Torr and 1200 °C, respectively. Upon ion implantation, the graphitization temperature of SiC is lowered by at least 100 °C, allowing selective growth of graphene layers on ion-implanted areas. The authors believe that by optimizing process conditions and starting with better quality SiC, the growth of nanoribbons with reduced disorder can be achieved. However, they do not demonstrate any physical characteristics of such GNRs. In [170] a focused ion beam was used to pattern epitaxial graphene on SiC into an array of graphene nanoribbons as narrow as 15 nm by optimizing the Ga⁺ ion beam current, acceleration voltage, dwell time, beam center to center distance and ion dose. The ion dose required to completely etch away graphene on SiC was determined and compared with the Monte Carlo simulation result. In addition, a photodetector using an array of 300 20 nm graphene nanoribbons was fabricated and its photo-response was studied. The device's zero-bias photo-responsivity was estimated to be 7.32 mA W^{-1} . Recently, Wang *et al.* have grown nitrogen-seeded graphene from patterned stripes etched in the SiC (000-1) surface. The patterned growth produces a set of parallel nitrogen-seeded SiC stripes (400–500 nm wide). Graphene growth on these patterned surfaces leads to the formation of nitrogen-graphene ribbons with substantially improved structural and electronic properties [171].

5. Conclusions

Graphene of good crystalline quality can be fabricated on substrates by thermal decomposition of silicon carbide (SiC) at high temperature and Ar gas ambience, as related to domain boundaries, and on an area as large as the SiC wafers, those being now demonstrated up to 200 mm in diameter. Wafers

of 150 mm can be purchased from several vendors and this makes graphene production manageable on a large scale. The graphene growth mechanism on the Si face (0001) of SiC substrates is pretty well understood and the growth process can be controlled. On the Si-terminated face, the graphene lattice is commensurate with the buffer layer which offers an epitaxial lattice matching for graphene formation. However, the existing thermal expansion coefficient mismatch may result in strained graphene material and is also the reason for the appearance of extended defects such as “wrinkles”. The influence of the substrate on the electronic properties of graphene, e.g., mobility, is rather essential and this problem has been tackled by hydrogen intercalation. From a structure point of view, the step bunching which takes place upon the heating of SiC substrates is a challenge mainly due to the difficulty of obtaining one ML thickness on a large area. Here a good understanding has been reached, ultimately leading to the use of cubic SiC as a substrate.

Graphene grown on the C face was initially preferred due to the better electronic properties related to graphene decoupling from the substrate. However, the area of uniform thickness is small and is confined by grain boundaries, which is not desirable in large-scale device processing. Nevertheless, efforts to improve this type of graphene are still going on.

The main graphene limitation for applications in digital devices has been dealt with by, e.g., growing nanoribbons that have an energy bandgap. Such structures facilitate the realization of ballistic transport, as well.

Characterization methods and techniques are available to assess all properties of graphene on SiC. New methods, allowing express analysis and a feedback to growth conditions, are being developed continuously.

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