

Effect of Surface Texture on Light Extraction Efficiency for LEDs

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Abstract: The light extraction efficiency of an LED is dependent on its surface texture. However, the surface of the p-GaN layer is not easy to be etched with inverted hexagonal pyramid structures (IHPS) with small top widths and large depths using existing methods. Therefore, it is important to discuss the expected effect of the conditions of thermal annealing and inductively coupled plasma (ICP) reactive ion etching (RIE) for the generation of nano-pin-holes in the photoresist and fabrication of the top surface structure of GaN-based LEDs, in order to enhance the light output power. In this study, the following four items will be discussed: (1) the effect of thermal annealing on the composition of the photoresist; (2) the effect of thermal annealing and ICP RIE on the generation of the nano-pin-holes in the photoresist; (3) the effect of ICP RIE on the IHPS; and (4) the effect of surface texture of the IHPS on the light output power. It has been found that a nano-pin-hole structure in the photoresist etching mask is needed for the fabrication of many IHPS on the LED surface. A maskless via-hole etching technique was used for texturing the photoresist to produce nano-pore structures with diameters of less than 50 nm. The relationship between the light extraction efficiency and the surface texture is discussed in detail. The simulation results show the best light extraction efficiency (LEE) ratio of 358% to be obtained when the distance between two neighboring IHPS patterns (DBNP) is 300 nm. This in turn allowed the formation of IHPS with small top widths and large depths on the LED surface. A LEE ratio of 305% was obtained with the fabrication of IHPS with a top width of 290 nm, a depth of 170 nm and a DBNP of 180 nm on the LED surface.

Keywords: nano-pin-hole structure; inverted hexagonal pyramid structure; light extraction efficiency ratio; LED; net zero carbon emission



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1. Introduction

High-brightness LEDs are required for solid-state lighting applications, such as in automotive headlamps, full-color outdoor displays, traffic lights, etc. One of the problems with conventional GaN-based LEDs is that the large difference between the refractive indices of the LED (2.5) and the surrounding air (1.0) causes most of the light to be reflected and then absorbed before it can escape from the semiconductor. The light output power of the LED is affected by the texture of the top surface [1–6]. A variety of techniques have been used for the purpose of surface texturing, including wet etching [7,8], dry etching [9], the formation of textured n-GaN layers [10] and photonic crystalline structures [11]. Several methods for the fabrication of V-shaped textures [9,12–15] on the surface of LEDs have also been developed in order to enhance their light output powers. For example, an enhancement in the light output power value of 0.486 times that of the conventional LED (CLED) was observed after the deposition of V-shaped pits about 600 nm in diameter [13,14]. Additionally, three-dimensional GaN truncated pyramid structures, using a self-aligned twofold epitaxial lateral overgrowth technique, were fabricated with an air void and a SiO₂ layer [16]. Simulation results [17] have shown truncated cone arrays with a top radius of less than 0.4 μm to be preferable. Past studies indicate that the light extraction efficiency (LEE) can be enhanced by texturing the LED surface. However, texturing the top surface of p-GaN to obtain IHPS with top widths of less than 0.4 μm and depths deeper than 150 nm is not easy using existing methods, as shown by the lack of studies in the literature

detailing optimally designed IHPS surface textures to enhance LEE and which type of LED surface texture can be expected to result in the best LEE. LED chips must be cheap to produce and easy to fabricate, but still have high LEE. Using an optical stepper to generate nanometer patterns or holes in the photoresist for the fabrication of a semiconductor is too expensive, and the production speed is too slow. Some maskless methods were used. For example, using SiN treatment without a conventional nano lithography imprint method for patterning sapphire substrate, patterning $\text{Al}_x\text{Ga}_{1-x}\text{N}$ epilayers were naturally grown [18,19]. Therefore, in this study, it could be best to use a maskless method for the formation of a nano-pore structure in the photoresist (i.e., texturing the photoresist to generate holes of less than 100 nm), itself to be used as the etching mask for texturing the top surface of the LED. However, up to now, the correct size of pore structure required in the photoresist etching mask to fabricate IHPS with small top widths on the LED surface has been unknown. The relationship between the LEE and the surface texture needs to be examined. This is the first time that the effect of the process conditions on the top surface of the structure will be discussed.

2. Experimental Details

The structure of the LED comprised a 200 nm thick undoped GaN layer, a 2400 nm thick Si-doped n-GaN layer, 8 pairs of InGaN/GaN multiple-quantum wells, a 30 nm thick Mg-doped p-AlGaIn layer, a 165 nm thick Mg-doped GaN layer, a 5 nm thick p-InGaIn contact layer, a 300 nm thick ITO layer, and an 80 nm thick SiO_2 layer. The ITO and SiO_2 layers were coated using a sputtering system [20–25]. A 1200 nm thick photoresist (AZ6112) layer was spin-coated onto the p-GaN layer at a speed of 3000 rpm. The following processes were then carried out: samples were baked (at 120–280 °C) for 10–70 min, followed by inductively coupled plasma (ICP) reactive ion etching (RIE) for 20–60 s. Measurements were made by field emission scanning electron microscopy and film X-ray diffraction (XRD). The finite element method (FEM) used for the simulations has been described in detail in a previous report [26,27]. The current vs. light intensity relationship (I-L) of the LED was measured by a Keithley 2400, a process in which a 1 cm^2 Si photodiode placed above the LED is connected to an operation amplifier (i.e., the current generated by a Si photodiode is converted into a voltage) and then connected to a Keithley 2400.

3. Results and Discussion

3.1. Simulation of LEE

To obtain an understanding of how to enhance LED output power, it is necessary to examine the relationship between the light extraction efficiency and the surface texture, as indicated by FEM. Figure 1a shows a schematic diagram of the LED structure with the surface texture. As can be seen, the arrangement of the IHPS on the surface of LED0 is continuous and uniform. The surface textures on LED0 with the various top widths are very much like those reported in [13,17]. Figure 1b shows the enhancement in values of the LEE for LED0s, according to the FEM simulation, with various top widths at depths of 180 nm and 120 nm, when the p-GaN layer thickness is 200 nm. For all LED0s, there is a gradual change in the refractive index. Therefore, the LEE of all LED0 samples is more than that of the CLED, and the smaller the top width and larger the depth of the IHPS, the more the LEE.

In this study, the top width and depth of the IHPS were set to 300 nm and 180 nm, respectively, in the FEM simulations. The LED emitting wavelength was set to 460 nm. The CLED did not have the IHPS structure. The thickness of the p-GaN layer for all LEDs was 200 nm. For all LEDs except the CLED and LED0, a ZrO_2 thin film was coated on the surface of the IHPS to prevent short circuits and electrical burns. As a consequence, there was little or no current flow beneath the IHPS. The distances between two neighboring IHPS patterns (DBNP) on the surface of LED0, LED1, LED3, LED5, LED7, LED9, LED11 were fixed at 0 nm, 100 nm, 300 nm, 500 nm, 700 nm, 900 nm, 1100 nm, respectively. An electric field is emitted from quantum wells in the InGaIn/GaN active region. The FEM

simulated output power intensity (PI) distribution (PID) was obtained under the following condition, that is, the same initial emission power (PI_{initial}) density in the InGaN/GaN active region. The PI rate is $PI_{\text{air}}/PI_{\text{initial}}$, where PI_{air} indicates the PI in air. The light extraction efficiency ratio (LEER) is the ratio of the PI_{air} for the LED with the IHPS (IHP-LED) to that of the CLED. The power intensity distribution as simulated by FEM for LED3 is shown in Figure 1c. The power intensity value distribution at the red line in Figure 1c is also clearly indicated. The light on the surface without the IHPS is assumed to be like that of a small lamp perpendicular to the surface. In other words, the angle of the light is affected by the IHPS. A reduction in the incidence angle at the interface between the GaN and ITO layers should enhance the light extraction efficiency. Figure 1d shows the effect of the DBNP on the LEER, as obtained in the simulation at the same input current density. The light is reflected at a high emission angle by the IHPS, meaning that the LEE of the IHP-LEDs will be more than that of the CLED. The decrease in the reflected light leads to an increase in the light extraction efficiency. The simulation results showed an improvement in the LEER of more than 250%, with DBNP sizes ranging from 100 nm to 500 nm. The best LEER of 358% was obtained when the DBNP size was 300 nm.

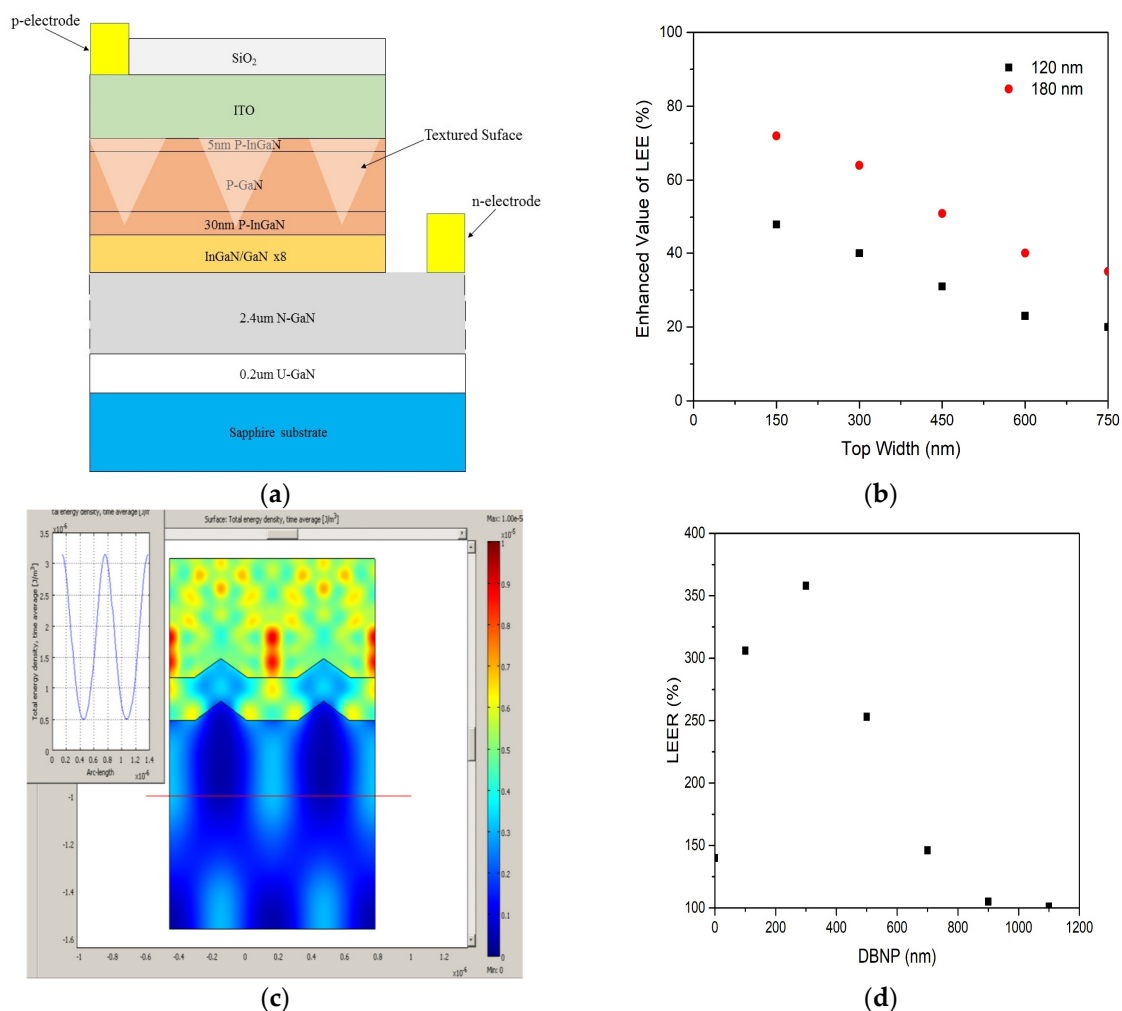
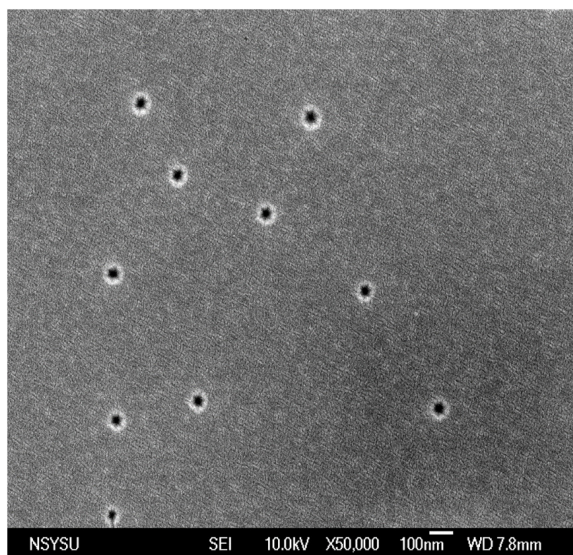


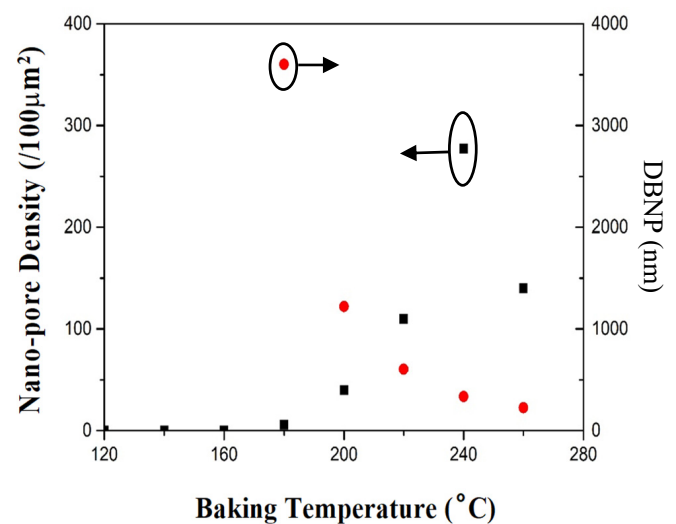
Figure 1. (a) Schematic diagram of a LED structure with textured surface. (b) Enhanced LEE values for LED0s, as simulated by FEM, with various top widths at depths of 180 nm and 120 nm when the p-GaN layer thickness is 300 nm. (c) Power intensity distribution as simulated by FEM for LED3. The power intensity value distribution at the red line is also clearly shown. (d) Effect of DBNP on LEER for LED3.

3.2. Fabrication of IHPS LED

The smaller the top width of the IHPS, the larger the LEE. However, when the pore structure in the photoresist is bigger, the top width of the IHPS will be wider after ICP etching. Therefore, a nano-pore structure in the photoresist is required for the fabrication of IHPS with a smaller top width. No pore structure on the photoresist and no IHPS on the surface of the p-GaN layer were found in LEDs produced using the standard factory processes (i.e., baking of the photoresist at 120 °C and the ICP process). It is not easy to etch the surface of the p-GaN layer to obtain IHPs with small top widths and large depths. However, since baking changes the structure of the photoresist, the effect of the baking temperature and time on the density of the nano-pore structure needs to be investigated. Figure 2a shows a top view FESEM image of the photoresist on the p-GaN layer that was baked at 220 °C and etched using ICP-RIE. Figure 2b shows the nano-pore density and DBNP in the photoresist in samples baked at various temperatures for a time of 30 min and then etched by the ICP process. Figure 2c shows the nano-pore density and DBNP in the photoresist in specimens baked at a temperature of 240 °C for various times and then etched by the ICP process. It can be clearly seen that a nano-pore structure formed in the resist without a mask after baking at a temperature of more than 160 °C and ICP etching. Clearly, except when the baking temperature exceeded 260 °C (when the photoresist was broken), the higher the baking temperature, the greater the number of nano-pore structures, although the diameter of the nano-pore structures only increased from ~40 nm to less than 50 nm. Figure 2d shows XRD patterns of the photoresist on samples baked at 160 °C and 240 °C. The peaks at C(212) and C(006) are smaller at 240 °C than at 160 °C. This indicates that the composition of the photoresist within the nano-pore structures is likely comprised of C(212) and C(006) before baking. Thus, the baking temperature affects the composition of the photoresist.



(a)



(b)

Figure 2. Cont.

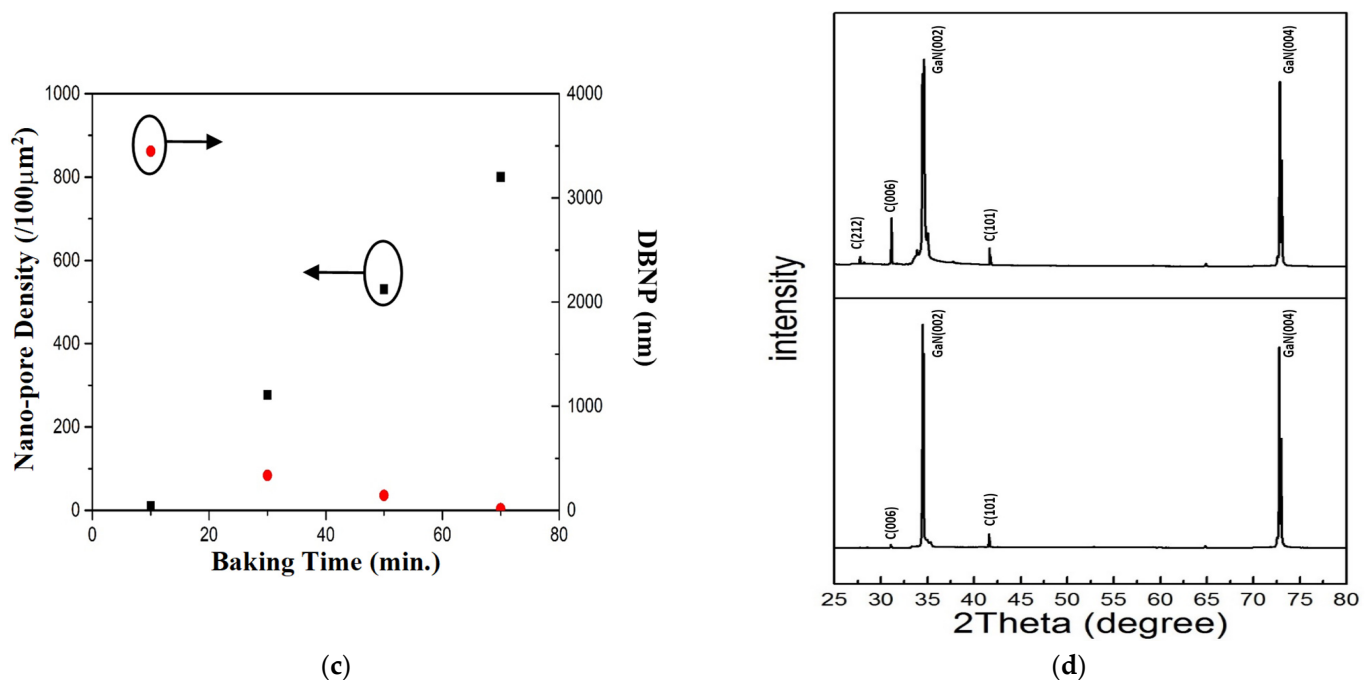


Figure 2. (a) Top view FESEM image of the photoresist on the p-GaN layer after being baked at 200 °C and etched using ICP-RIE. (b) The nano-pore density and DBNP in the photoresist baked at various temperatures for 30 min and then etched by the ICP process. (c) The nano-pore density and DBNP in the photoresist baked at a temperature of 240 °C for various times and then etched by ICP the process. (d) X-ray diffraction patterns of the photoresist on samples baked at 160 °C and 240 °C.

In order to achieve high LEE enhancement, as illustrated in Figure 1b,d, IHPS with top widths of less than 0.4 μm and depths deeper than 150 nm are required. The effect of the ICP etching time on changes in the width and depth of the IHPS was investigated next.

Figure 3a shows top-view FESEM images illustrating the procedure for the formation of the IHPS on the top surface of GaN-based LEDs: steps 1, 2 and 3. It was found that with a gradual increase in the ICP etching time, the width of the IHPS first increased, and then the depth of the IHPS in the vertical plane deepened. Furthermore, the etched patterns are hexagonal because the etching speed corresponds to the crystalline orientation in the p-GaN layer. Figure 3b shows the effect of the ICP etching time on the changes in the width and depth of the IHPS on the surface of p-GaN. The longer the etching time is, the deeper the depth. However, there is little variation in the top widths of the IHPS. This anisotropic etching occurs because the Cl^- plasma ions prefer to etch the p-GaN layer in the vertical direction [26–29], so the nano-pore structure in the baked photoresist acted as an etching mask to restrict the area etched by the Cl^- plasma ions. A cross-sectional FESEM image of the surface morphology of the p-GaN layer after being baked at 240 °C and etched is shown in Figure 4a. An IHPS with a top width of 290 nm, a depth of 170 nm and a DBNP of 180 nm on the LED surface was fabricated. The IHPS LED had an enhanced light extraction efficiency of 305%, as shown in Figure 4b. Therefore, as noted above, by controlling the baking temperature and time and the etching time, IHPS with small top widths and large depths can be easily fabricated to produce desirable high surface-density textures for an IHP-LED.

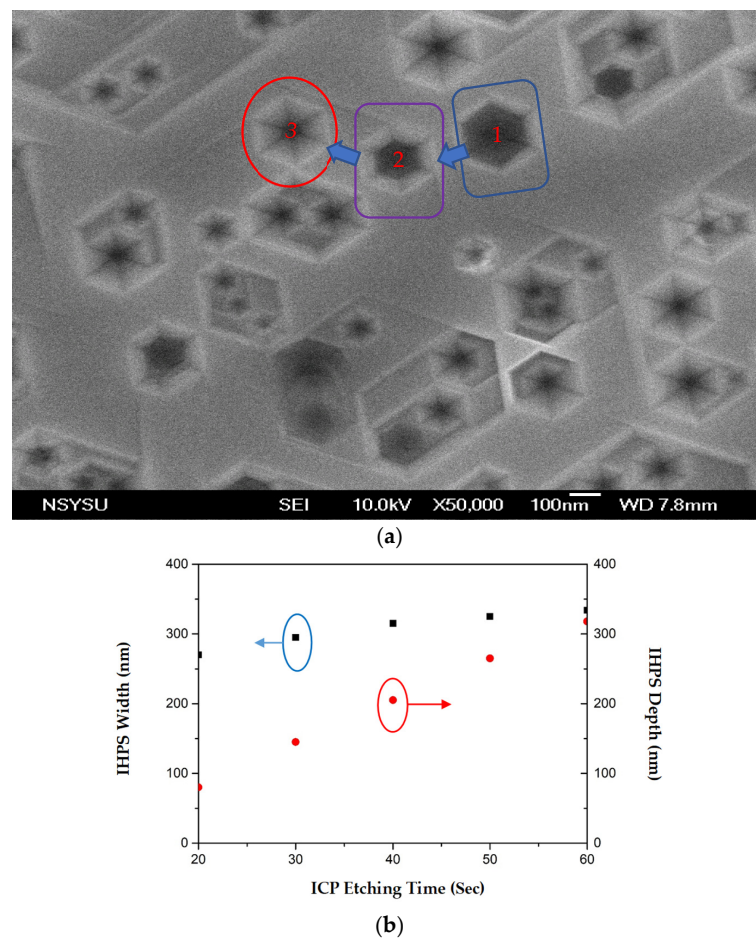


Figure 3. (a) Top-view FESEM images showing the procedure for the formation of the IHPS on the top surface of GaN-based LEDs: steps 1, 2 and 3. (b) Effect of the ICP etching time on changes in the width and depth of the IHPS on the surface of p-GaN.

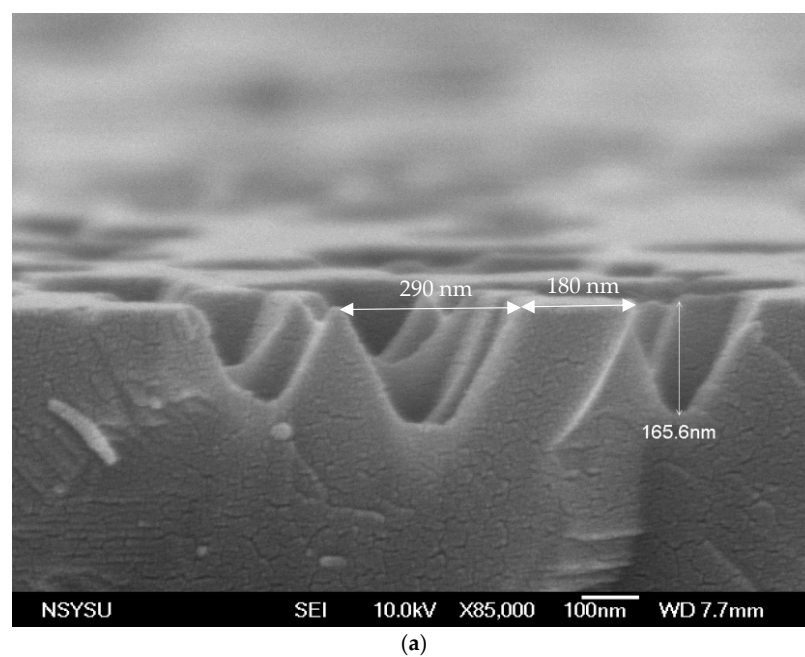


Figure 4. Cont.

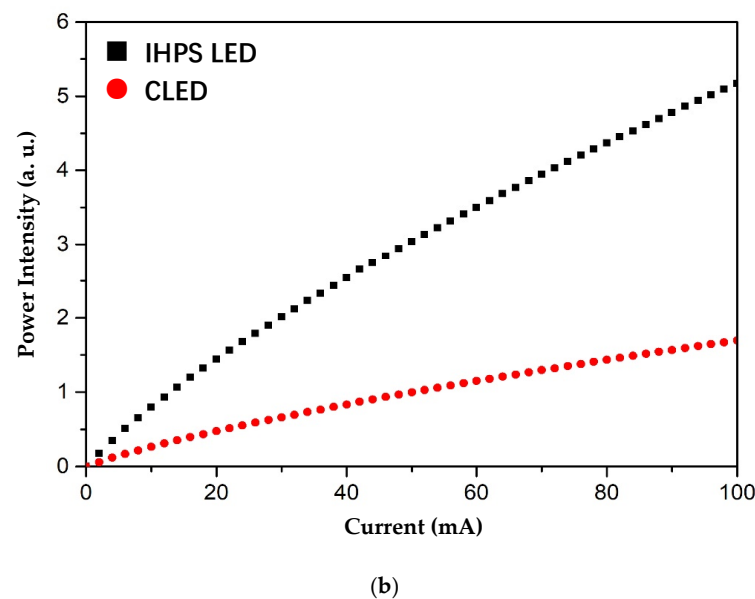


Figure 4. (a) Cross-sectional top-view FESEM image showing the surface morphology of the p-GaN layer after being baked at 240 °C and etched. (b) Power intensities of the common LED (CLED) and the IHPS LED.

4. Conclusions

The relationship between the light extraction efficiency and the surface texture (which includes the width and depth of the IHPS and the distance between two neighboring IHPS patterns) has been discussed. The LEE of the LED is completely dependent on the surface texture. IHPS with smaller top widths and larger depths will enhance the LEE. Light extraction efficiency ratios of more than 250% were obtained when the DBNP was between 100 nm and 500 nm in size. In particular, an optimal LEER of 358% was obtained when the DBNP was 300 nm. Nano-pore structures in the photoresist (used as the etching mask) could be easily fabricated by controlling the processing conditions (i.e., the baking temperature and time, and the ICP etching time) for the fabrication of surface textures with various IHPS densities for enhancement of the light extraction efficiency of the LED. When the process conditions were controlled (a baking temperature of 240 °C, a baking time of 30 min, and an ICP etching time of 60 s) it was found that the composition of the photoresist within the nano-pore structures comprised C(212) and C(006). The results showed that the baking temperature affects the composition of the photoresist. Nano-pore structures with diameters of less than 50 nm in the photoresist etching mask produced IHPS with a width of 290 nm and depth of 170 nm, and a DBNP of 190 nm on the LED surface, and an enhanced light extraction efficiency of 305% was obtained. The results show this method to be capable of forming IHP-LEDs with enhanced light extraction efficiency.

The results indicate the ICP etching can be used to produce IHPS patterns which lead to improved luminous intensity of the LED, as long as the nano-pores fabricated in the photoresist have diameters of less than 50 nm using any processing technology. Furthermore, this technology could be used to improve the yield of the future micro-LED production.

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Conflicts of Interest: The author declares no conflict of interest.

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