

Article

Effect of Gate Dielectric Material on the Electrical Properties of MoSe₂-Based Metal–Insulator–Semiconductor Field-Effect Transistor

Abdelkader Abderrahmane [†], Pan-Gum Jung [†], Changlim Woo  and Pil Ju Ko ^{*}

Department of Electrical Engineering, Chosun University, 375, Seosuk-dong, Dong-gu, Gwangju 501-759, Korea

^{*} Correspondence: pjko@chosun.ac.kr[†] These authors contributed equally to this work.

Abstract: In this study, we fabricated metal–insulator–semiconductor field-effect transistors (MIS-FETs) based on nanolayered molybdenum diselenide (MoSe₂) using two insulator materials, silicon dioxide (SiO₂) and silicon nitride (SiN). We performed morphological and electrical characterizations in which the devices showed good electronic performance, such as high mobility and high I_{on}/I_{off} ratios exceeding 10⁴. The subthreshold swing (ss) was somewhat high in all devices owing to the dimensions of our devices. In addition, the transfer curves showed good controllability as a function of gate voltage. The photogating effect was weakened in MoSe₂/SiN/Si, indicating that SiN is a good alternative to silicon oxide as a gate dielectric material.

Keywords: two-dimensional (2D) materials; transition metal dichalcogenides (TMDCs); molybdenum diselenide (MoSe₂); silicon dioxide (SiO₂); silicon nitride (SiN)



Citation: Abderrahmane, A.; Jung, P.-G.; Woo, C.; Ko, P.J. Effect of Gate Dielectric Material on the Electrical Properties of MoSe₂-Based Metal–Insulator–Semiconductor Field-Effect Transistor. *Crystals* **2022**, *12*, 1301. <https://doi.org/10.3390/cryst12091301>

Academic Editors: Jorge Souto and Jose Luis Pura

Received: 26 August 2022

Accepted: 12 September 2022

Published: 14 September 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Two-dimensional (2D) transition metal dichalcogenides (TMDCs) have attracted considerable attention because of their unique electronic [1], photonic [2], electrochemical [3], and mechanical [4] properties, which are significant advantages for the fabrication of next-generation electronic and optoelectronic devices [5]. Scaling down electronic device dimensions, in particular field-effect transistors (FETs) including metal–insulator–semiconductor field-effect transistors (MISFETs), is challenging owing to Moore's law, because the reduction in the channel size and in the thickness of the gate dielectric material cause short channel effects and increases in leakage current, respectively [6]. Moreover, devices with reduced dimensions require decreased power consumption; in other words, a low threshold voltage is necessary to achieve the best electronic performance [7]. Therefore, selecting a gate dielectric material with the best physical properties, such as a high dielectric constant and low mismatch with the channel material, is as important as selecting the 2D active layer in FET-based devices. We previously reported the investigation of van der Waals hexagonal boron nitride (h-BN) (indirect bandgap $E_g = 5.955$ eV [8] and dielectric constant $\epsilon = 3.3$ [9]) as an alternative gate dielectric material; however, the results showed low electrical performance and a kink effect due to carrier trapping at the interface between h-BN and molybdenum diselenide (MoSe₂) [10]. MoSe₂-based FETs have been reported to have excellent device characteristics, such as an on/off ratio of 10⁶ and Hall mobilities exceeding 250 cm²/V·s for both holes and electrons [11].

In this paper, we report the fabrication and characterization of MoSe₂-based MISFET transistors using silicon dioxide (SiO₂) and silicon nitride (SiN) as gate dielectric materials. The aim of our research is to investigate the incorporation of SiN, which is a high- κ dielectric material [12] (with a dielectric constant $\epsilon = 7.5$, almost two times higher than that of SiO₂, $\epsilon = 3.9$), as an insulator layer. We used the same fabrication process and device properties (i.e., device size, active-layer thickness, dielectric material thickness, etc.). The electrical

characteristics of the MISFET devices were determined, and their mobilities, subthreshold swing (ss) values, and other parameters were calculated and analyzed.

2. Materials and Methods

We used two types of substrates in this study: SiO₂/Si and SiN/Si substrates using p+-doped Si with a resistivity lower than 0.005 Ω·cm. The thicknesses of the SiO₂ and SiN were 300 nm. SiN (300 nm) was deposited using low-pressure chemical vapor deposition (LPCVD). Thereafter, Ti contacts with thicknesses of 50 nm were deposited by electron-beam evaporation. Then, nanolayered MoSe₂ flakes purchased from HQ Graphene were transferred onto the SiO₂/Si and SiN/Si substrates using polydimethylsiloxane (PDMS, Sylgard 184 Dow silicones corporation, Carrollton, KY, USA). Four devices were fabricated on the SiO₂/Si substrates using MoSe₂ flake thicknesses of 7, 21, 63, and 90 nm, and another four devices were fabricated on SiN/Si with MoSe₂ flake thicknesses of 29, 36, 47, and 87 nm. Finally, the MISFET devices were annealed at 400 °C for 2 h under Ar gas and atmospheric pressure. A semiconductor parameter analyzer (4155A, Hewlett Packard, Tokyo, Japan) and probe station were used for electrical characterization. Scanning electron microscopy (SEM, Hitachi, Jena, Germany) was used to observe the surface of the MoSe₂ flakes, and the thickness of MoSe₂ was determined using atomic force microscopy (AFM, XE-200, PSIA Corp., Seoul, Korea).

3. Results and Discussion

3.1. Electrical Characterization of All Samples

Figure 1a,b show the drain current (I_d) dependence on the drain–source voltage (V_{ds}) curves of the MISFETs fabricated on SiO₂/Si and SiN/Si substrates, respectively. All devices showed symmetric electrical characteristics, except for the device using the thinnest MoSe₂ layer (7 nm) on SiO₂/Si because of the high electrical resistivity of the layer. Figure 1c,d depict the transfer curves of the same devices. All devices showed n-type behavior with normal turn-on behavior. The devices with thinner MoSe₂ flakes exhibited poor transfer curves. The electrical properties of all eight devices were extracted from the transfer curves and are presented in Table 1. In general, the devices showed good electrical properties, with the highest carrier mobility in MoSe₂/SiN/Si with the MoSe₂ thickness of 87 nm; this device also showed a high on/off ratio exceeding 10⁴. The ss values were relatively lower in the MoSe₂/SiN/Si-based devices, indicating that using SiN as a gate dielectric material enhanced the electrical properties.

Table 1. Electrical mobilities, subthreshold swing (ss) values, and on/off ratios of MISFETs.

Property	SiO ₂	SiO ₂	SiO ₂	SiO ₂	SiN	SiN	SiN	SiN
	7 nm	21 nm	63 nm	90 nm	29 nm	36 nm	47 nm	87 nm
μ_{eff} (cm ² /V·s)	0.8	72.0	116.5	43.5	63.9	55.5	51.3	164.0
ss (mV/dec)	3.7×10^3	1.4×10^3	5.0×10^3	2.8×10^4	2.6×10^3	2.5×10^3	1.5×10^3	3.7×10^3
On/Off ratio	7.0×10^2	1.2×10^4	1.0×10^4	3.1×10^1	1.2×10^4	9×10^3	1.7×10^5	9.6×10^2

As shown in Table 1, MoSe₂/SiO₂/Si with the MoSe₂ thickness of 21 nm and MoSe₂/SiN/Si with the MoSe₂ thickness of 29 nm had similar electrical properties; these were chosen for further investigation to determine the best gate dielectric material. The field-effect mobilities (μ_{eff}) of the devices were estimated using the equation $\mu_{\text{eff}} = [dI_d/dV_g] \times [L/(WC_iV_{ds})]$, where C_i is the gate capacitance calculated using the equation $C_i = \epsilon_0\epsilon_r/d$; and ϵ_r is equal to 7.5 and 3.9, respectively, in the cases of SiN and SiO₂. The thicknesses of the SiN and SiO₂ were 300 nm, the gate capacitances were 1.15×10^{-4} and 2.21×10^{-4} F·m⁻², and L and W were the channel length and width, respectively.

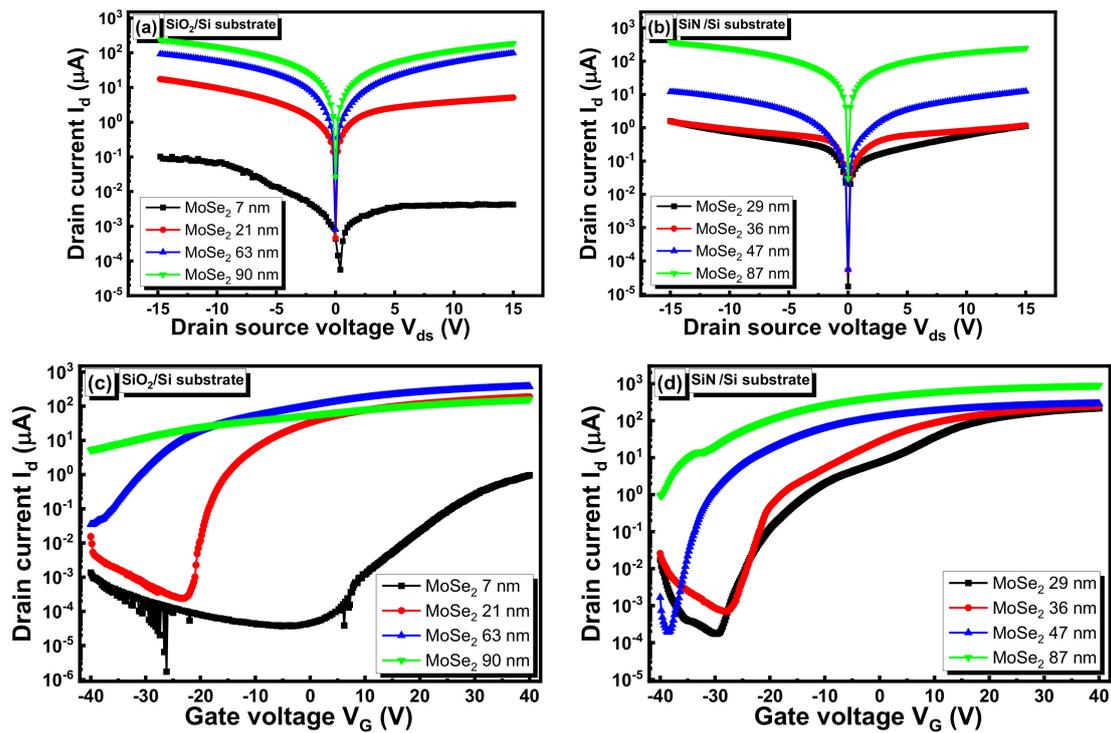


Figure 1. I_d - V_{ds} characteristics of the fabricated devices on (a) SiO_2/Si substrates and (b) SiN/Si substrates, and transfer curves of the fabricated devices on (c) SiO_2/Si substrates and (d) SiN/Si substrates.

3.2. Morphological Characterization

Figure 2a,d show the SEM images of the devices ($\text{MoSe}_2/\text{SiO}_2/\text{Si}$ with the MoSe_2 thickness of 21 nm and $\text{MoSe}_2/\text{SiN}/\text{Si}$ with the MoSe_2 thickness of 29 nm), the corresponding AFM images are shown in Figure 2b,e, and the topographic analysis for both devices are shown in Figure 2c,f. The channel length and width were 20 and 7 μm , respectively, as shown in Figure 2a.

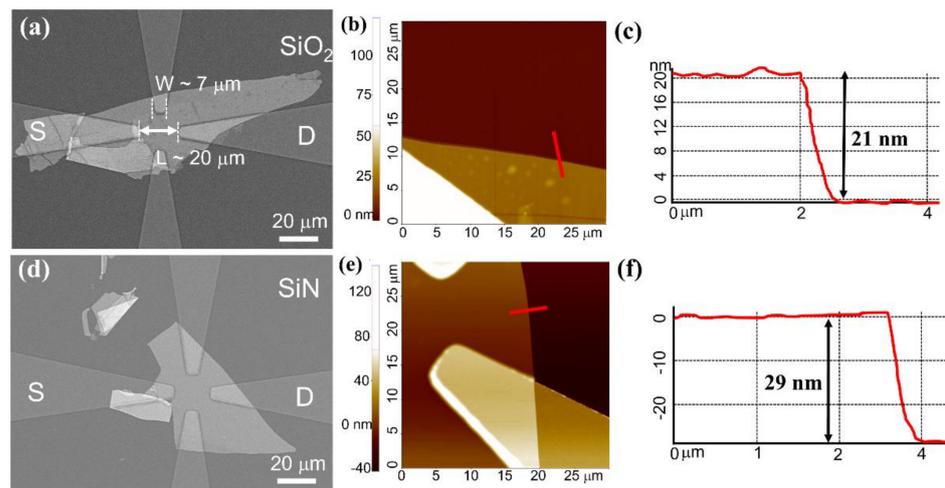


Figure 2. (a) SEM image of $\text{MoSe}_2/\text{SiO}_2/\text{Si}$ (magnification 1k); (b,c) the corresponding AFM image and topographic analysis, respectively. (d) SEM image of $\text{MoSe}_2/\text{SiN}/\text{Si}$ (magnification 1k); (e,f) the corresponding AFM image and topographic analysis, respectively.

3.3. Electrical and Optoelectronic Characterization

The I_d - V_{ds} characteristics of both devices as a function of gate voltage are shown in Figure 3a,b. The $\text{MoSe}_2/\text{SiO}_2/\text{Si}$ device exhibited Schottky-like behavior, while $\text{MoSe}_2/\text{SiN}/\text{Si}$

exhibited better and almost ohmic contact. Both devices showed good gate-voltage controllability of their current–voltage curves.

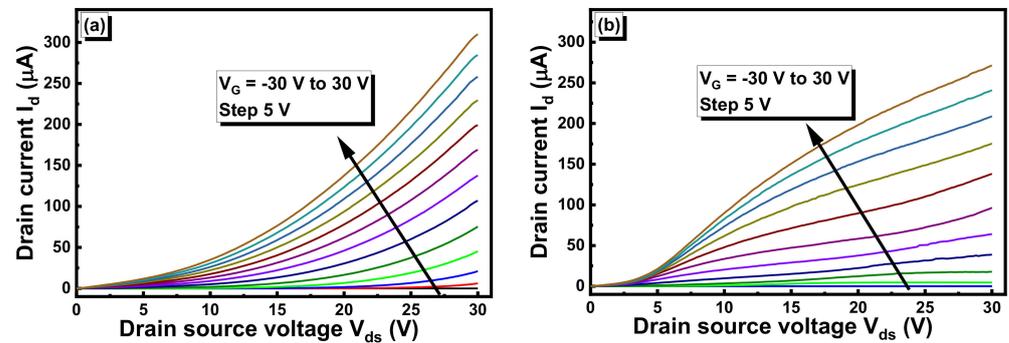


Figure 3. I_d - V_{ds} characteristics of the fabricated devices on (a) SiO_2/Si substrates and (b) SiN/Si substrates, at different gate voltages.

3.4. Electrical Characterizations of All Samples

Figure 4a,b show the variation in the transfer curves (I_d - V_G) versus the V_{ds} . The current was measured by setting V_{ds} to 1, 5, 10, or 15 V and varying the back-gate voltage from -40 V to 40 V. When V_G increased to a positive value, the carrier density increased, and the current increased. Kink effects were observed in the $\text{MoSe}_2/\text{SiN}/\text{Si}$ device (Figure 4b) at the polarization voltages of 10 and 15 V. Similar behavior was observed in a previously reported $\text{MoSe}_2/\text{h-BN}/\text{Si}$ -based FET device [10] and FET devices based on 2D materials such as black phosphorus [13] and graphene [14]. The kink effect in our device can be explained by the effect of carrier de-trapping from the interface at a high polarization voltage during carrier transport. The $I_{\text{on}}/I_{\text{off}}$ values were 6.32×10^2 , 3.49×10^3 , 8.04×10^3 , and 1.22×10^4 at V_{ds} values of 1, 5, 10, and 15 V, respectively, in the $\text{MoSe}_2/\text{SiO}_2/\text{Si}$ device. However, in the $\text{MoSe}_2/\text{SiN}/\text{Si}$ device, the values were 5.92×10^1 , 5.88×10^2 , 5.27×10^2 , and 1.27×10^4 at 1, 5, 10, and 15 V, respectively.

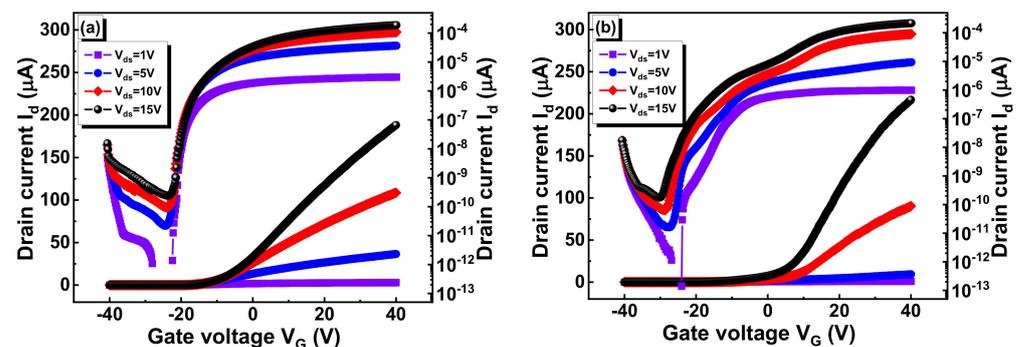


Figure 4. Transfer curves (I_d - V_G) at various V_{ds} values for MISFET devices of (a) $\text{MoSe}_2/\text{SiO}_2/\text{Si}$ and (b) $\text{MoSe}_2/\text{SiN}/\text{Si}$.

The I_d - V_{ds} curves in both devices, in the absence of an applied V_G , are shown in Figure 5. Very narrow hysteresis was observed in both devices, which originated from the trapping and de-trapping effects of charges at the interfaces and surface of MoSe_2 . It is well known that when multilayered MoSe_2 is exposed to ambient air, oxygen molecules can be converted into chemisorbed oxygen anions (O_2^-) on the surface of MoSe_2 , where they act as electron traps [15]. In addition to chemisorbed O_2^- , humidity can induce trapping center formation [16]. Annealing devices in Ar can remove surface-adsorbed water vapor and oxygen [17]. However, charged impurities at the channel/ SiO_2 interface and charge traps in SiO_2 can limit the electrical performance of FET [16,18]. Similar to SiO_2 , SiN can

exhibit extrinsic charges owing to defect density and impurities, including hosting trapped charges and surface adsorbates [19].

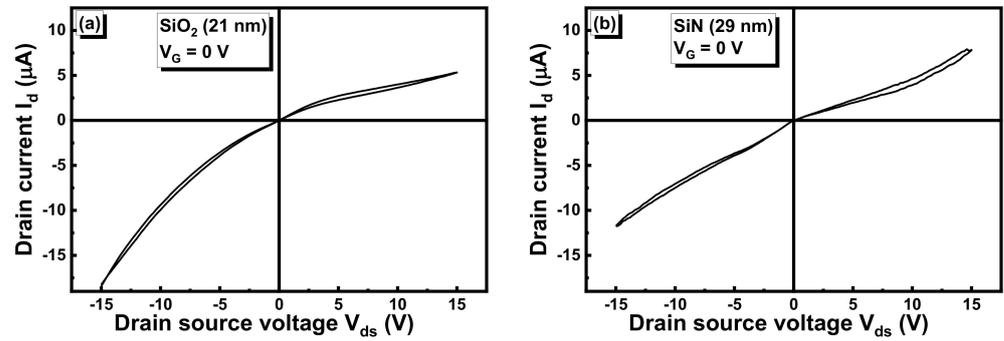


Figure 5. I_d - V_{ds} sweeps of (a) MoSe₂/SiO₂/Si and (b) MoSe₂/SiN/Si MISFET devices.

Finally, we investigated the optoelectronic properties of the same devices under different laser excitation powers of 0.00155, 0.0155, 0.155, 1.147, 4.96, and 13.95 μ W. Figure 6a,b show the I_d - V_{ds} characteristics at different laser powers of the MoSe₂/SiO₂/Si and MoSe₂/SiN/Si devices, respectively. As expected, the current increased with increasing laser power. Thereafter, we deduced the photocurrent I_{ph} according to the equation $I_{ph} = I_{ds}(illumination) - I_{ds}(dark)$, then drew I_{ph} as a function of the laser power (P) and interpolated the curve according to the equation $I_{ph} \propto P^\alpha$. Here, α can be used to determine the carrier transport origin [20,21], that is, if α is close to unity, the photoconductive effect dominates, and if α is close to zero, the photogating effect dominates. The photogating effect originates from the long-lived trap states [22,23]. As seen in Figure 6c,d, α is higher in the MoSe₂/SiN/Si MISFET device, which means that the photoconductive effect is higher in this case. Photogating is dominant in the MoSe₂/SiO₂/Si MISFET (or MOSFET) device, which means that the trap concentration is higher in this case.

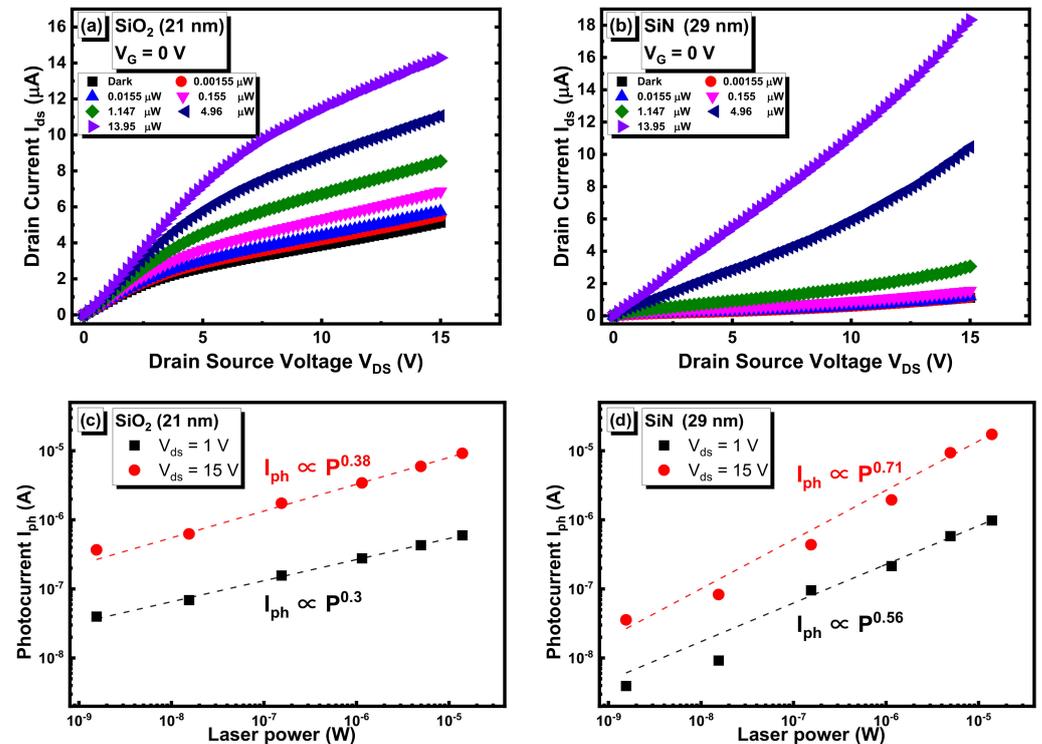


Figure 6. I_d - V_{ds} characteristics of the fabricated devices on (a) SiO₂/Si substrates and (b) SiN/Si substrates, at different laser powers. (c,d) The photocurrent I_{ph} as a function of the laser power at two polarization voltages.

4. Conclusions

We fabricated eight MISFETs based on nanolayered MoSe₂. We compared two devices with similar dimensions and different gate dielectric materials of SiO₂ and SiN. The MoSe₂/SiO₂/Si- and MoSe₂/SiN/Si-based MISFETs showed good electrical performance with high carrier mobility and high on/off ratios exceeding 10⁴. Moreover, their current–voltage characteristics showed good gate-voltage controllability. In terms of carrier transport, the photoconductive effect is more apparent in the MoSe₂/SiN/Si device, and the photogating effect is dominant in the MoSe₂/SiO₂/Si device; therefore, SiN can be a good alternative to SiO₂, especially for optoelectronic devices such as high-speed photodetectors. In future research, the temperature dependence of the electrical properties of multilayered MoSe₂-based MISFETs can be characterized with the aim of investigating the carrier trap density.

Author Contributions: Writing—review and editing, A.A. and P.-G.J.; formal analysis, C.W.; data curation, C.W.; writing—original draft preparation, P.J.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Brain Pool Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (NRF-2019H1D3A1A01102658). This study was supported by research fund from Chosun University, 2022.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Zheng, L.; Wang, X.; Jiang, H.; Xu, M.; Huang, W.; Liu, Z. Recent progress of flexible electronics by 2D transition metal dichalcogenides. *Nano Res.* **2022**, *15*, 2413–2432. [[CrossRef](#)]
2. Zhao, L.; Shang, Q.; Li, M.; Liang, Y.; Li, C.; Zhang, Q. Strong exciton-photon interaction and lasing of two-dimensional transition metal dichalcogenide semiconductors. *Nano Res.* **2021**, *14*, 1937–1954. [[CrossRef](#)]
3. Wang, L.; Xu, D.; Jiang, L.; Gao, J.; Tang, Z.; Xu, Y.; Chen, X.; Zhang, H. Transition metal dichalcogenides for sensing and oncotherapy: Status, challenges, and perspective. *Adv. Funct. Mater.* **2021**, *31*, 2004408. [[CrossRef](#)]
4. Imani Yengejeh, S.; Wen, W.; Wang, Y. Mechanical properties of lateral transition metal dichalcogenide heterostructures. *Front. Phys.* **2021**, *16*, 13502. [[CrossRef](#)]
5. Wu, M.; Xiao, Y.; Zeng, Y.; Zhou, Y.; Zeng, X.; Zhang, L.; Liao, W. Synthesis of two-dimensional transition metal dichalcogenides for electronics and optoelectronics. *InfoMat* **2021**, *3*, 362–396. [[CrossRef](#)]
6. Saha, J.K.; Chakma, N.; Hasan, M. Impact of channel length, gate insulator thickness, gate insulator material, and temperature on the performance of nanoscale FETs. *J. Comput. Electron.* **2018**, *17*, 1521–1527. [[CrossRef](#)]
7. Su, S.K.; Chuu, C.P.; Li, M.Y.; Cheng, C.C.; Wong, H.S.P.; Li, L.J. Layered semiconducting 2D materials for future transistor applications. *Small Struct.* **2021**, *2*, 2000103. [[CrossRef](#)]
8. Cassabois, G.; Valvin, P.; Gil, B. Hexagonal boron nitride is an indirect bandgap semiconductor. *Nat. Photonics* **2016**, *10*, 262–266. [[CrossRef](#)]
9. Sasama, Y.; Kageura, T.; Imura, M.; Watanabe, K.; Taniguchi, T.; Uchihashi, T.; Takahide, Y. High-mobility p-channel wide-bandgap transistors based on hydrogen-terminated diamond/hexagonal boron nitride heterostructures. *Nat. Electron.* **2022**, *5*, 37–44. [[CrossRef](#)]
10. Abderrahmane, A.; Ko, P.J.; Jung, P.G.; Kim, N.H.; Sandhu, A. Optoelectronic characterizations of two-dimensional h-BN/MoSe₂ heterostructures based photodetector. *Sci. Adv. Mater.* **2018**, *10*, 627–631. [[CrossRef](#)]
11. Memaran, S. Lateral PN Junctions Based on 2-D Materials. Ph.D. Thesis, College of Arts and Sciences Florida State University, Tallahassee, FL, USA, 2018; pp. 18–24.
12. Houssat, M.; Villeneuve-Faure, C.; Lahoud Dignat, N.; Locatelli, M.L.; Cambronne, J.P. Temperature Influence on PI/Si₃N₄ Nanocomposite Dielectric Properties: A Multiscale Approach. *Polymers* **2021**, *13*, 1936. [[CrossRef](#)]
13. Xia, Y.; Li, G.; Jiang, B.; Yang, Z.; Liu, X.; Xiao, X.; Flandre, D.; Wang, C.; Liu, Y.; Liao, L. Exploring and suppressing the kink effect of black phosphorus field-effect transistors operating in the saturation regime. *Nanoscale* **2019**, *11*, 10420–10428. [[CrossRef](#)]
14. Meric, I.; Han, M.Y.; Young, A.F.; Ozyilmaz, B.; Kim, P.; Shepard, K.L. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nat. Nanotechnol.* **2008**, *3*, 654–659. [[CrossRef](#)]
15. Zhang, D.; Yang, Z.; Li, P.; Pang, M.; Xue, Q. Flexible self-powered high-performance ammonia sensor based on Au-decorated MoSe₂ nanoflowers driven by single layer MoS₂-flake piezoelectric nanogenerator. *Nano Energy* **2019**, *65*, 103974. [[CrossRef](#)]
16. Lee, H.; Kim, J.H.; Lee, C.J. Electrical characteristics of MoSe₂ TFTs dependent on the Al₂O₃ capping layer. *Appl. Phys. Lett.* **2016**, *109*, 222105. [[CrossRef](#)]
17. Guo, S.; Yang, D.; Zhang, S.; Dong, Q.; Li, B.; Tran, N.; Li, Z.; Xiong, Y.; Zaghloul, M.E. Development of a cloud-based epidermal MoSe₂ device for hazardous gas sensing. *Adv. Funct. Mater.* **2019**, *29*, 1900138. [[CrossRef](#)]

18. Chamlagain, B.; Li, Q.; Ghimire, N.J.; Chuang, H.J.; Perera, M.M.; Tu, H.; Xu, Y.; Pan, M.; Xaio, D.; Yan, J.; et al. Mobility improvement and temperature dependence in MoSe₂ field-effect transistors on parylene-C substrate. *ACS Nano* **2014**, *8*, 5079–5088. [[CrossRef](#)]
19. Shao, F.; Woo, S.Y.; Wu, N.; Schneider, R.; Mayne, A.J.; de Vasconcellos, S.M.; Arora, A.; Carey, B.J.; Preuß, J.A.; Bonnet, N.; et al. Substrate influence on transition metal dichalcogenide monolayer exciton absorption linewidth broadening. *Phys. Rev. Mater.* **2022**, *6*, 074005. [[CrossRef](#)]
20. Fang, H.; Hu, W. Photogating in low dimensional photodetectors. *Adv. Sci.* **2017**, *4*, 1700323. [[CrossRef](#)]
21. Huang, H.; Wang, J.; Hu, W.; Liao, L.; Wang, P.; Wang, X.; Gong, F.; Chen, Y.; Wu, G.; Luo, W.; et al. Highly sensitive visible to infrared MoTe₂ photodetectors enhanced by the photogating effect. *Nanotechnology* **2016**, *27*, 445201. [[CrossRef](#)]
22. Fu, S.; du Fossé, I.; Jia, X.; Xu, J.; Yu, X.; Zhang, H.; Zheng, W.; Krasel, S.; Chen, Z.; Wang, Z.M.; et al. Long-lived charge separation following pump-wavelength-dependent ultrafast charge transfer in graphene/WS₂ heterostructures. *Sci. Adv.* **2021**, *7*, eabd9061. [[CrossRef](#)]
23. Island, J.O.; Blanter, S.I.; Buscema, M.; van der Zant, H.S.; Castellanos-Gomez, A. Gate controlled photocurrent generation mechanisms in high-gain In₂Se₃ phototransistors. *Nano Lett.* **2015**, *15*, 7853–7858. [[CrossRef](#)]