

Article

The Atomic Layer Etching Technique with Surface Treatment Function for InAlN/GaN Heterostructure

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Abstract: This paper studied an atomic layer etching (ALE) technique with a surface treatment function for InAlN/GaN heterostructures with AlN spacer layers. Various parameters were attempted, and 30 s O₂ + 15 W BCl₃ was chosen as the optimal recipe. The optimal ALE approach exhibited satisfactory etching results, with regard to the etch-stop effect, compared with other techniques. The atomic force microscopy (AFM) results showed an etching per cycle (EPC) value of 0.15 nm/cycle, with a 0.996 fit coefficient and root mean square (RMS) surface roughness of around 0.61 nm (0.71 nm for as-grown sample), which was the lowest in comparison with digital etching (0.69 nm), Cl₂/BCl₃ continuous etching (0.91 nm) and BCl₃ continuous etching (0.89 nm). X-ray photoelectron spectroscopy (XPS) and scanning transmission electron microscopy with energy dispersive X-ray spectroscopy measurements (STEM/EDS) verified the indium clustered phenomena at the bottom apex of V-pit defects in the epi structure of InAlN/GaN high electron mobility transistors (HEMTs) for the first time, in addition to the surface morphology optimization for the ALE under-etching technique used in this work. The resistor hall effect (Hall) and AFM measurements demonstrated that after 4 or 5 ALE cycles, the two-dimensional electron gas (2-DEG) density and RMS roughness were improved by 15% and 11.4%, respectively, while the sheet resistance (R_{sh}) was reduced by 6.7%, suggesting a good surface treatment function. These findings were important for realizing high-performance InAlN/GaN HEMTs.

Keywords: InAlN/GaN heterostructure; atomic layer etching; under-etching; indium clustered; surface treatment; two-dimensional electron gas density; sheet resistance



Citation: Du, F.; Jiang, Y.; Wu, Z.; Lu, H.; He, J.; Tang, C.; Hu, Q.; Wen, K.; Tang, X.; Hong, H.; et al. The Atomic Layer Etching Technique with Surface Treatment Function for InAlN/GaN Heterostructure. *Crystals* **2022**, *12*, 722. <https://doi.org/10.3390/cryst12050722>

Academic Editors: Wei Xu, Honglong Ning, Hua Zheng and Dmitri Donetski

Received: 17 April 2022

Accepted: 14 May 2022

Published: 19 May 2022

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1. Introduction

InAlN/GaN-based high electron mobility transistors (HEMTs) have recently attracted much attention. Compared to the commonly used AlGaIn/GaN heterostructure, the stronger spontaneous polarization effect of the InAlN/GaN heterostructure provides higher two-dimensional electron gas (2-DEG) density, leading to lower on-resistance (R_{on}) and a higher output current. Moreover, the lattice-matched In_{0.17}Al_{0.83}N/GaN heterostructure could also enhance device reliability. At the same time, enough 2-DEG density of InAlN/GaN contributes to a thinner barrier layer thickness, improving the radio frequency (RF) characteristics by reducing the short-channel effects of a deeply scaled device [1–5].

Owing to the advantages mentioned above, the InAlN/GaN heterostructure is considered as the most competitive candidate for GaN-based power and RF devices [6].

The etching technique is critical in GaN-based device fabrication, including the gate recess process, source/drain ohmic contact with a low annealing temperature, and regrown ohmic contact preparation. To relieve the serious etching damage and the resulting device reliability issues, an etching technique with a precisely controlled etching depth and low surface damage is urgently needed. In recent years, atomic layer etching (ALE) with two sequential quasi-self-limiting steps (O_2 plasma modification step and BCl_3 plasma removal step) has been used in the fabrication of AlGaIn/GaN HEMTs, to obtain a well-controlled recess process and leakage current suppression, becoming a potential alternative to continuous dry etching and digital etching techniques [7–16]. However, little work has been reported on the study of ALE for the InAlN/GaN heterostructure. In our previous report, the O_2/BCl_3 -based ALE technique for InAlN/GaN was proposed with good etching results [17]. However, systematic comparative studies among ALE, continuous dry etching, and digital etching techniques are still absent.

O_2 -based plasma treatment applied to InAlN/GaN HEMTs is an efficient surface treatment method for optimizing the output performance and leakage current of a device [2,18–21]. In 2011, Wang et al. reported, after 2 min of O_2 /Ar plasma treatment for the access region of the InAlN/GaN HEMTs, a high output current (2.1 A/mm) and low gate leakage (1 mA/mm), due to improvements in the electrical properties and trap state passivation. The electrical property optimizations of 2-DEG density and sheet resistance (R_{sh}) were similar to the AlGaIn/GaN heterostructure passivated by SiN [18]. Moreover, in 2011, Lee et al. reduced the gate leakage of InAlN/GaN HEMTs by more than two orders of magnitude by using O_2 plasma inductively coupled plasma (ICP) Asher treatment on the InAlN surface after ohmic preparation, which was similar to the results in the AlGaIn device [19]. In 2016, using 5 min of O_2 reactive ion etching (RIE) plasma treatment before gate metallization, Ma et al. fabricated InAlN/GaN HEMT with an output current of 2.18 A/mm and gate leakage of 10^{-2} mA/mm, which resulted in defect suppression and barrier height increase [2]. In 2021, with 1 min of O_2 RIE plasma treatment prior to gate deposition by Asher, Cui et al. realized an InAlN/GaN HEMT with a high I_{on}/I_{off} ratio of $\sim 10^7$ and low surface leakage [21]. A thin In_2O_3 and Al_2O_3 mixed oxide layer on the InAlN surface could increase the effective barrier height of InAlN and decrease the trap density of the surface, optimizing the electrical properties (2-DEG density and R_{sh}) of the epitaxy, while also leading to enhancement of the device performances, such as the output current and R_{on} , and suppressing the gate leakage [18,22–24]. Therefore, the ALE technique with an O_2 modification step has potential for surface treatment functions.

In this paper, an O_2/BCl_3 -based ALE technique for the InAlN/GaN heterostructure with a surface treatment function was studied. An etching per cycle (EPC) value of 0.15 nm/cycle, with a fit (R^2) coefficient of 0.996, was obtained. The InAlN surface root mean square (RMS) roughness after the ALE (0.61 nm) process was lower than the samples obtained using digital etching (0.69 nm), Cl_2/BCl_3 (0.91 nm) etching, and BCl_3 (0.89 nm) etching techniques. Four or five cycles of ALE surface treatment on an as-grown InAlN wafer resulted in the 2-DEG density improving by 15%, R_{sh} reducing by 6.7%, and surface RMS roughness optimizing by 11.4%. The mechanism was systematically investigated by the following measurements: atomic force microscopy (AFM), resistor Hall effect (Hall) measurement, X-ray photoelectron spectroscopy (XPS), and scanning transmission electron microscopy (STEM) with energy dispersive X-ray spectroscopy (EDS).

2. Experimental

Sample preparation: The 6" $In_{0.17}Al_{0.83}N$ /GaN wafer was grown on high-resistivity Si substrate for device fabrication, which was purchased from NTT AT Corporation. As shown in Figure 1a, a 10.6 nm $In_{0.17}Al_{0.83}N$ barrier layer and a 1 nm AlN spacer layer were grown on a 1000 nm i-GaN channel layer to form the 2-DEG characterization. Figure 1b and c show the STEM image of the InAlN wafer. The 6" wafer was diced into $2 \times 2 \text{ cm}^2$

and $1 \times 1 \text{ cm}^2$ samples. The former were used for etching experiments with AFM measurement, and the latter were used for XPS, STEM/EDS measurements and surface treatment experiments with AFM and Hall measurements.

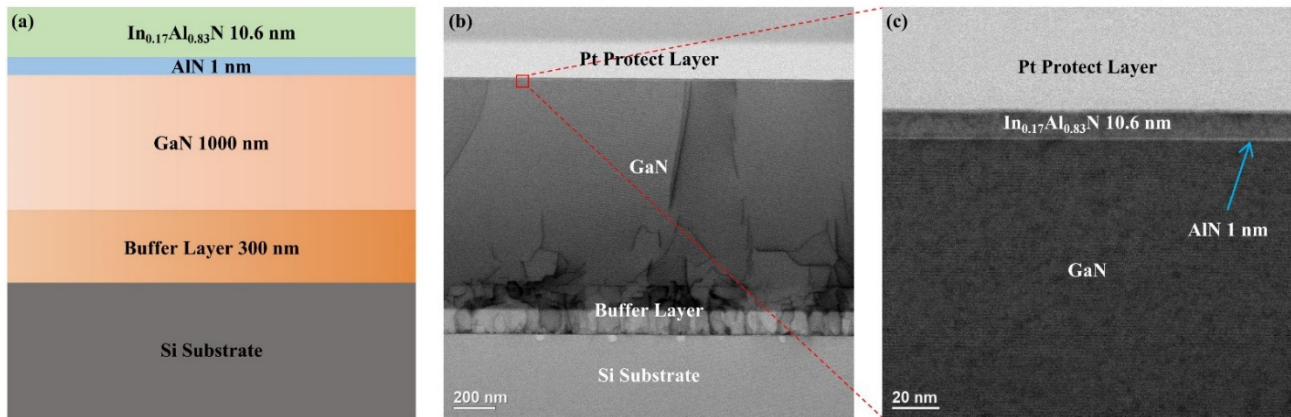


Figure 1. (a) Cross section schematic, (b) scanning transmission electron microscopy (STEM) image and (c) partially enlarged STEM image of $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ wafer.

As shown in Figure 2(a₁), a 300 nm SiO_2 hard mask for the ALE process was deposited on $2 \times 2 \text{ cm}^2$ samples by plasma-enhanced chemical vapor deposition (PECVD) at 350°C . Photolithography was utilized for determining the desired pattern. In order to remove the SiO_2 mask selectively, SF_6 plasma ICP-RIE was performed.

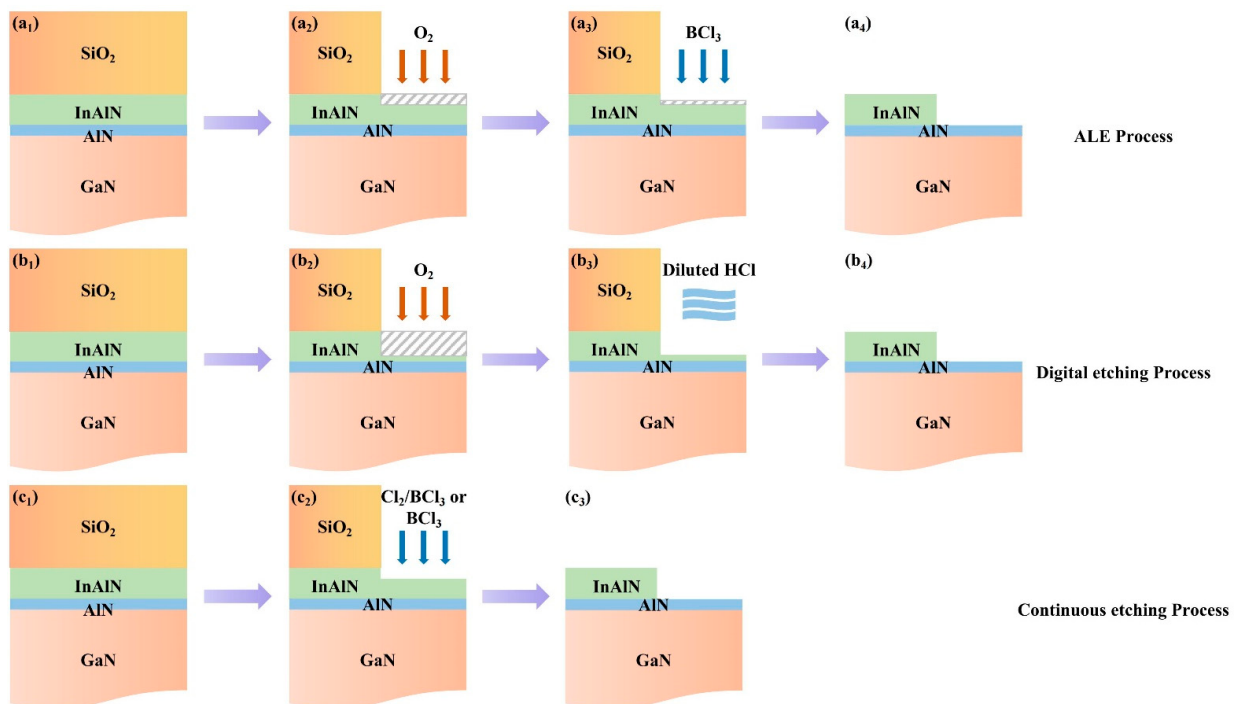


Figure 2. Cross section schematic of InAlN/GaN samples during atomic layer etching (ALE) process: (a₁) SiO_2 hard mask deposition, (a₂) O_2 modification step, (a₃) BCl_3 removal step, and (a₄) removal of SiO_2 hard mask by buffered oxide etch (BOE). Digital etching process: (b₁) SiO_2 hard mask deposition, (b₂) O_2 plasma oxidation step, (b₃) removal of the oxidation layer by diluted HCl solution, and (b₄) removal of SiO_2 hard mask by BOE. Continuous etching process: (c₁) SiO_2 hard mask deposition, (c₂) Cl_2/BCl_3 or BCl_3 plasma continuous etching, and (c₃) removal of SiO_2 hard mask by BOE.

Parameter settings: The O₂ plasma modification step and BCl₃ plasma removal step of the O₂/BCl₃ ALE approach are shown in Figure 2(a₂,a₃), respectively. For the modification step, the parameters were set at the following: ICP power = 100 W and RF power = 50 W, while the modification time was variable. For the removal step, the parameters were set at the following: ICP power = 0 W and RF power = 15 W, with the removal time at 30 s. These two steps were performed in sequence, alternatively, in the Corial 210IL 200 mm ICP system at a chamber pressure of 10 mTorr and gas flow rate of 50 sccm, with 30 s switching time. After the whole etching process, the SiO₂ hard mask was removed by buffered oxide etch (BOE), as shown in Figure 2(a₄).

The EPC and surface roughness were measured for samples with various O₂ modification times to determine the optimal parameters for the ALE technique. In Figure 3a, as the modification time increased, EPC firstly increased and then tended to saturate, while the RMS roughness firstly reduced and then stabilized gradually. Given the production efficiency, an O₂ modification time of 30 s was determined for the ALE recipe. Figure 3b demonstrates the initial calibration of this ALE technique with optimal parameters (30 s O₂ modification time), and good repeatability of single atomic-level EPC (0.15 nm/cycle) was confirmed by $R^2 = 0.996$ and low dispersion.

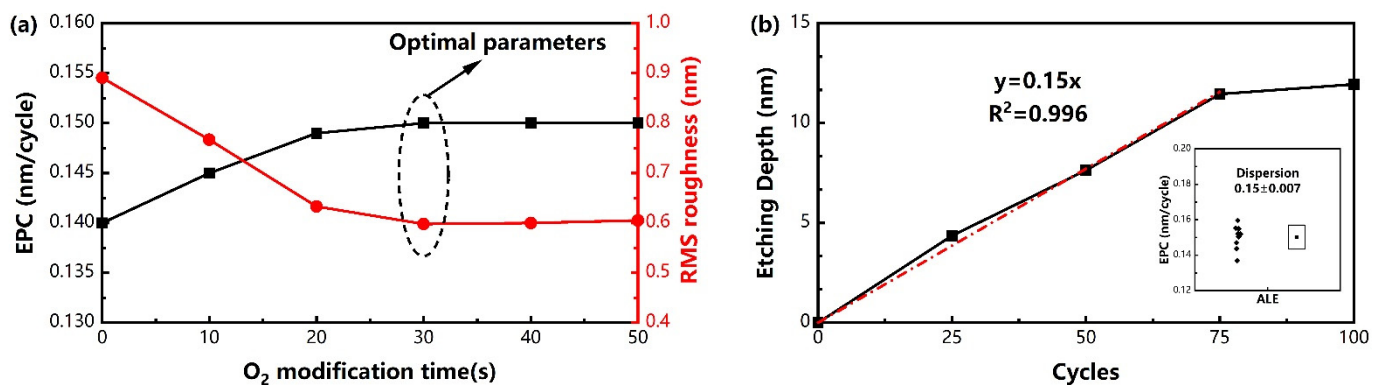


Figure 3. (a) Etching per cycle (EPC) and InAlN root mean square (RMS) roughness with various O₂ modification times for ALE technique, (b) etching depth of InAlN (11.6 nm)/GaN wafer for ALE technique (O₂ modification time = 30 s) during 0–100 etching cycles, and InAlN EPC dispersion of ALE technique.

Three representative etching techniques were used as the control groups for the ALE technique. For the digital etching technique, the process combined O₂ plasma oxidation followed by the oxidation layer being removed using diluted HCl solution, as shown in Figure 2(b₁–b₄). For the Cl₂/BCl₃ and BCl₃ continuous etching techniques shown in Figure 2(c₁–c₃), the RF/ICP power was set at 15/100 W and 15/0 W, respectively. Thus, five samples were prepared accordingly: as-grown (sample 0, S₀), ALE (sample 1, S₁), digital etching (sample 2, S₂), Cl₂/BCl₃ continuous etching (sample 3, S₃), and BCl₃ continuous etching (sample 4, S₄).

Characterization: The surface roughness was measured immediately after etching, and then after removing the SiO₂ mask, the etching depth was measured by AFM. XPS measurements were performed to investigate the ALE mechanism. Moreover, the as-grown epi wafer was measured by STEM/EDS to verify the epitaxy characteristics of the InAlN/GaN heterostructure. To explore the effect of ALE surface treatment, Ti/Al/Ti/Au (20/110/40/50 nm) metal electrodes were deposited at four corners of the samples after variable cycles of ALE surface treatment, and 45 s of 860 °C N₂ rapid thermal annealing (RTA) was used to reduce the contact resistance for Hall measurements.

3. Results and Discussion

The etching depth vs. etching cycles for samples S_{1–2} and the etching depth vs. etching time for samples S_{3–4} are shown in Figure 4, while the corresponding EPCs (nm/cycle)

or etching rates (nm/min) for the InAlN, AlN and GaN layers are listed in Table 1. The EPCs of the InAlN, AlN and GaN layers for sample S_1 were 0.15, 0.03 and 0.46 nm/cycle, respectively. An obvious etch-stop phenomenon was observed during the ALE process, as shown in Figure 4a, which could be explained by the efficient blocking function of the AlN layer with poor oxidation properties [17,25]. For sample S_2 in Figure 4b, the EPC of the InAlN layer was up to 7.46 nm/cycle, and the InAlN layer could be over etched by only two cycles of digital etching. Although the EPC of sample S_2 decreased around the AlN layer, no etch-stop effect was observed, as opposed to AlGaIn/GaN. This suggests that only the ALE technique can provide an etch-stop effect on the InAlN/GaN heterostructure, further explained below by the STEM image of the InAlN/GaN heterojunction. As shown in Figure 4c,d, due to the existence of Cl_2 plasma, the etching rate of sample S_3 (17.88 nm/min) was much bigger than that of sample S_4 (0.28 nm/min). Nevertheless, both these continuous etching techniques consisted of linear etching processes during the whole InAlN/GaN etching process. With the stable InAlN EPC shown in Figure 3b and etch-stop effect at the AlN layer, the ALE technique of sample S_1 was confirmed as the most effective way for controlling the InAlN/GaN etching depth precisely, compared to the other three etching techniques.

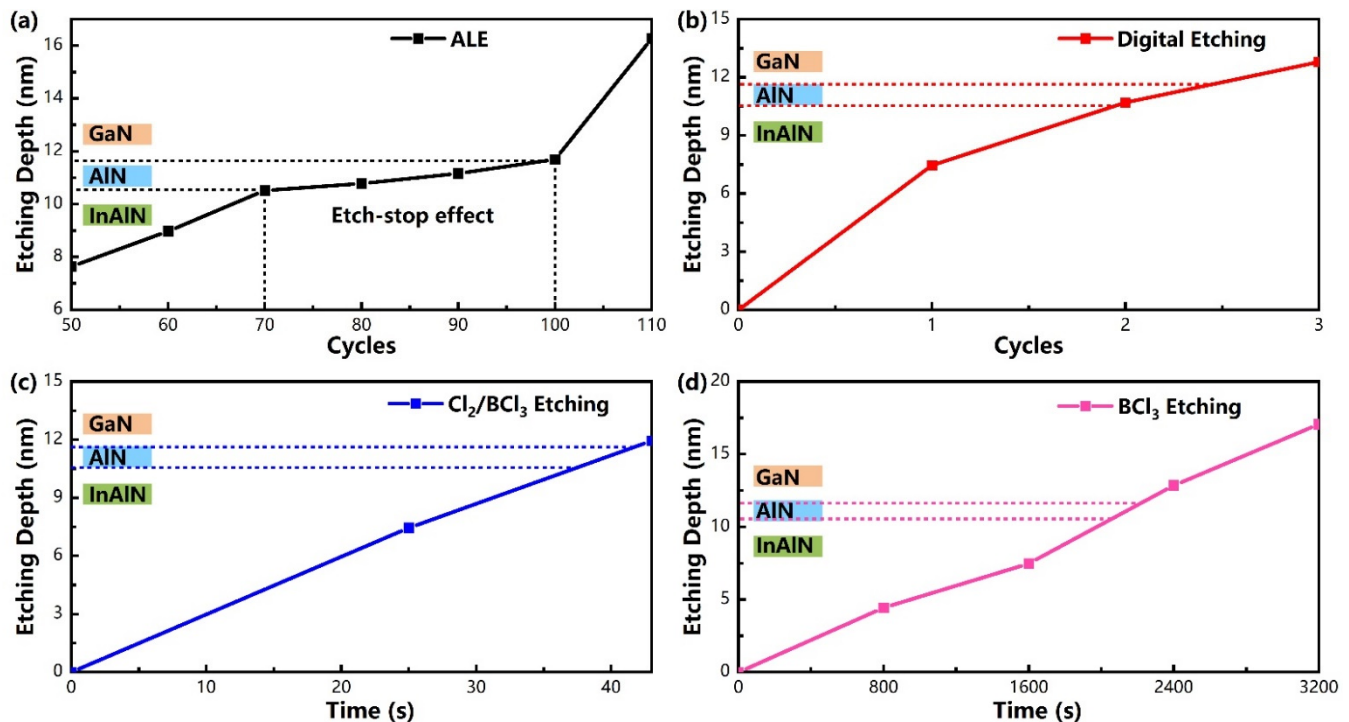


Figure 4. Etching depth vs. etching cycles for (a) ALE (sample S_1), (b) digital etching (sample S_2), and etching depth vs. etching times for (c) Cl_2/BCl_3 continuous etching (sample S_3) and (d) BCl_3 continuous etching (sample S_4).

Table 1. The EPC and etching rate of the InAlN, AlN and GaN layers for samples S_{1-4} .

Etching Method	InAlN Etching Rate	AlN Etching Rate	GaN Etching Rate
Sample S_1	0.15 nm/cycle (EPC)	0.03 nm/cycle (EPC)	0.46 nm/cycle (EPC)
Sample S_2	7.46 nm/cycle (EPC)	¹	¹
Sample S_3	17.88 nm/min	¹	¹
Sample S_4	0.28 nm/min	¹	0.32 nm/min

¹ Due to the fact that these samples will be directly etched through the InAlN/GaN layer, the partial etching rate could not be calculated for samples S_{2-4} .

Figure 5a–f show the surface morphology for the as-grown InAlN surface of sample S_0 , InAlN etched surface of sample S_{1-4} , and AlN etched surface of sample S_1 . All the InAlN etched surface morphologies were obtained at an etching depth of approximately 9 nm, while the AlN etched surface morphology of sample S_1 was measured at an etching depth of around 11.5 nm, which is in the AlN layer. The corresponding RMS and mean roughness are listed in Table 2. For sample S_1 , the InAlN and AlN etched surfaces after the ALE process showed similar RMS roughness values (0.61 nm and 0.60 nm), which were even lower than that of sample S_0 (0.71 nm). Compared to sample S_2 (0.69 nm), obtained using the digital etching technique, sample S_1 had lower roughness and dispersion (as shown in Figure 5g,h), further demonstrating that the ALE technique with quasi-self-limiting characteristics is more stable in controlling the surface morphology. Compared to samples S_3 (0.91 nm) and S_4 (0.89 nm), the ALE technique provided a much smoother surface by effectively overcoming the continuous etching limitations, such as transport-limited phenomena, highly coupled parameters, and propagation of the damaged etch front, which could be beneficial to decrease the interface trap density and device leakage current [7,12]. The ALE technique was the most effective way to control the InAlN/GaN etching surface morphology.

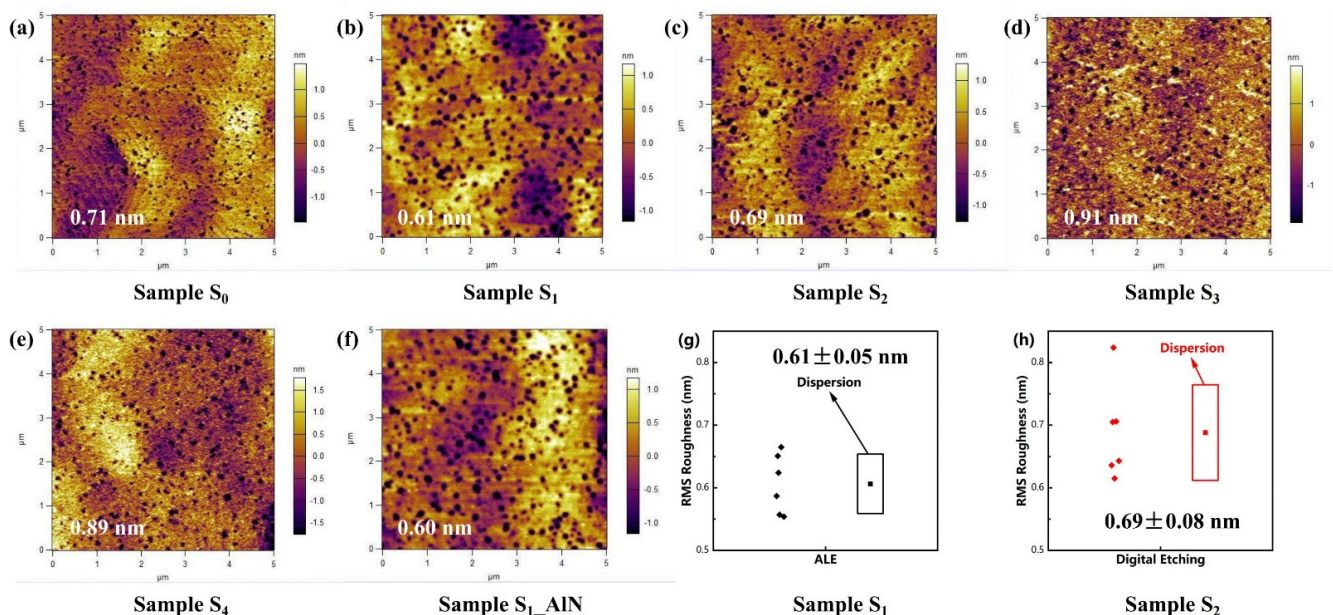


Figure 5. AFM images ($5 \times 5 \mu\text{m}^2$) for InAlN as-grown surface of (a) sample S_0 ; InAlN etched surface of (b) sample S_1 , (c) sample S_2 , (d) sample S_3 and (e) sample S_4 ; AlN etched surface of (f) sample S_1 ; and the dispersion of InAlN RMS roughness for (g) sample S_1 and (h) sample S_2 .

Table 2. The surface roughness for InAlN surface of samples S_{0-4} and AlN etched surface of sample S_1 .

Etching Method	RMS Roughness (nm)	Mean Roughness (nm)
Sample S_0	0.71	0.47
Sample S_1	0.61	0.44
Sample S_2	0.69	0.47
Sample S_3	0.91	0.75
Sample S_4	0.89	0.66
Sample S_1 _AlN	0.60	0.45

To systematically explore the mechanism of the ALE technique, XPS measurements of Al and In oxides were performed on an InAlN/GaN wafer for one cycle of ALE, as shown in Figure 6. For the Al element in Figure 6a, after one O_2 modification step of sample S_1 , the Al_2O_3 content increased significantly compared to sample S_0 , whereas a substantially reduced Al_2O_3 content was observed after the following BCl_3 etching of sample S_1 . The

In_2O_3 content shown in Figure 6b had the same change as Al_2O_3 . These results indicate the oxidation function of the ALE modification step and the effective etching of the ALE removal step. Moreover, the Al_2O_3 and In_2O_3 contents after one ALE cycle of sample S_1 were more than the as-grown sample S_0 . This implies that the ALE technique used in this work was an under-etching approach, which did not completely remove the oxides formed by the O_2 modification step.

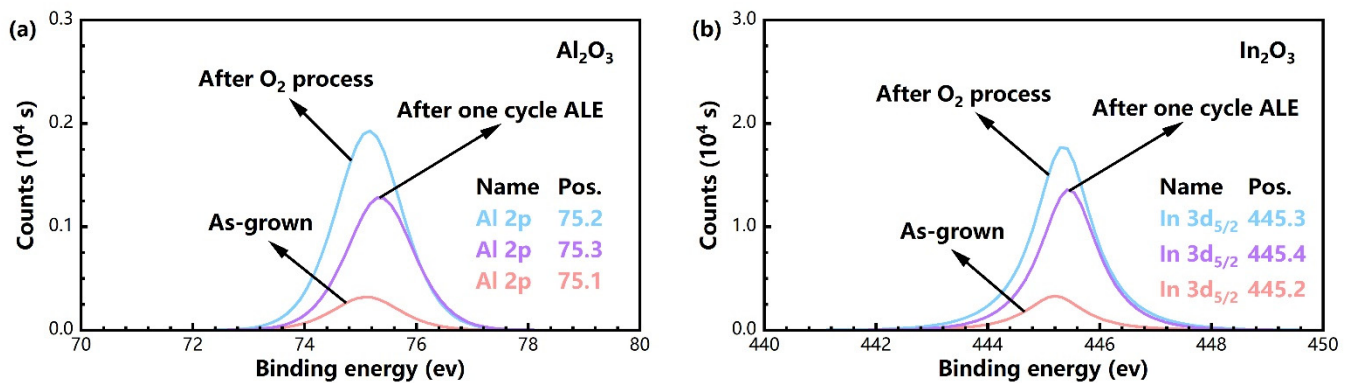


Figure 6. The X-ray photoelectron spectroscopy (XPS) measurements of the oxides on the InAlN surface during the whole process of one cycle of ALE: (a) Al_2O_3 content and (b) In_2O_3 content of as-grown sample S_0 exposed to air, sample S_1 after O_2 modification step then sealing in vacuum, and sample S_1 after one cycle of ALE then sealing in vacuum.

For the first time, Figure 7a shows the STEM image of an epi structure of InAlN/GaN HEMTs with V-pit defects penetrating through the whole InAlN barrier layer. V-pits are usually generated on the dislocations of bottom GaN, leading to poor surface morphology (as shown in Figure 5) of the InAlN epilayer, and were hardly observed in the AlGaIn/GaN heterojunction [26,27]. Figure 7c,d show the EDS results of the indium (In) atomic fraction for the InAlN/GaN heterostructure at the V-pit position (line-1) and general position (line-2) (Figure 7b). The In element was observed in the AlN/GaN region below the V-pits and was absent in the general position, verifying the In clustered phenomenon was the origin of V-pit defects [28,29]. The In elements involvement made the AlN more easily oxidized, due to the lower binding energy of In-O, and the large number of V-pits provided excessive oxidation paths of AlN in the digital etching technique, leading to loss of the etch-stop effect. The ALE technique with only 30 s of oxidation could effectively avoid this problem, which was well matched with the results shown in Figure 4a,b. Furthermore, the observed In clustered phenomenon at the V-pit apex could demonstrate why the under-etching ALE technique (oxide residue after etching) achieved better surface morphology than the over-etching ALE technique (no oxide residue after etching) in our previous work [17].

The surface treatment function of the ALE process for an InAlN/GaN heterostructure was also investigated. In Figure 8 and Table 3, the electrical properties, including the R_{sh} , 2-DEG mobility and density, of the as-grown sample S_0 and sample S_1 with 1–5 cycles of ALE surface treatment are demonstrated. The R_{sh} increased to 454 Ω/sq for one cycle of treatment, which was above the as-grown R_{sh} (386 Ω/sq), and then decreased steadily from 454 Ω/sq to around 360 Ω/sq from one cycle to five cycles of treatment, while the 2-DEG mobility exhibited an almost opposite trend to R_{sh} , and finally recovered close to the as-grown 2-DEG mobility (1210 $\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}$) for treatment of 1–5 cycles. These trends are closely related to the interface scattering changes represented by the surface morphology roughness shown in Table 3. The increasement in RMS roughness enhanced the interface scattering, thus causing R_{sh} and 2-DEG mobility to worsen, and vice versa. However, the 2-DEG density continuously increased from $1.33 \times 10^{13} \text{ cm}^{-2}$ to $1.53 \times 10^{13} \text{ cm}^{-2}$ for 1–5 cycles of ALE surface treatment with only 0.75 nm InAlN etch amount. Since the ALE technique in this work was an under-etching approach, it would gradually generate a thin oxide layer with a high O content for 1–5 cycles of treatment, similarly to O_2 -based plasma

surface treatment, which could reduce the surface barrier height of the nitrides and increase the effective barrier height, thereby subsequently increasing the 2-DEG density [18,22]. Thus, compared to sample S_0 , sample S_1 with four or five cycles of ALE surface treatment could reduce R_{sh} by 6.7% and increase the 2-DEG density by 15%, which was comparable to the optimization ability of the reported O_2 plasma surface treatment and other treatment approaches [18,30,31]. In addition, lower RMS roughness of 0.39 nm was obtained after four or five cycles of treatment, compared to sample S_0 (0.44 nm). This demonstrates that the ALE technique had an efficient surface treatment function to make InAlN/GaN HEMTs reduce R_{on} , gate leakage and increase output current density.

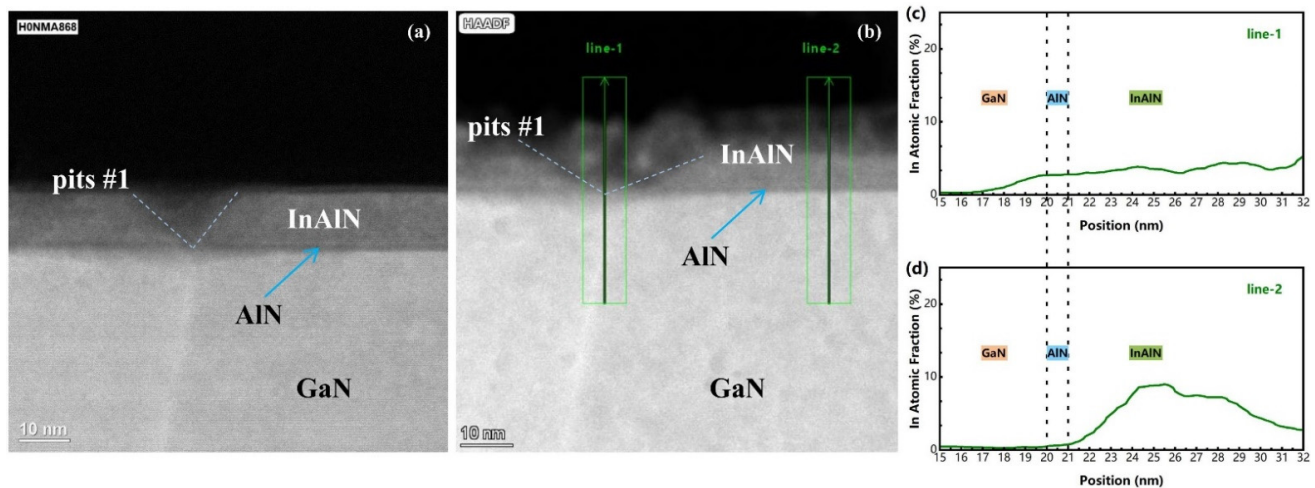


Figure 7. Epitaxy property measurements of sample S_0 with (a) STEM and (b–d) energy dispersive X-ray spectroscopy (EDS) measurements.

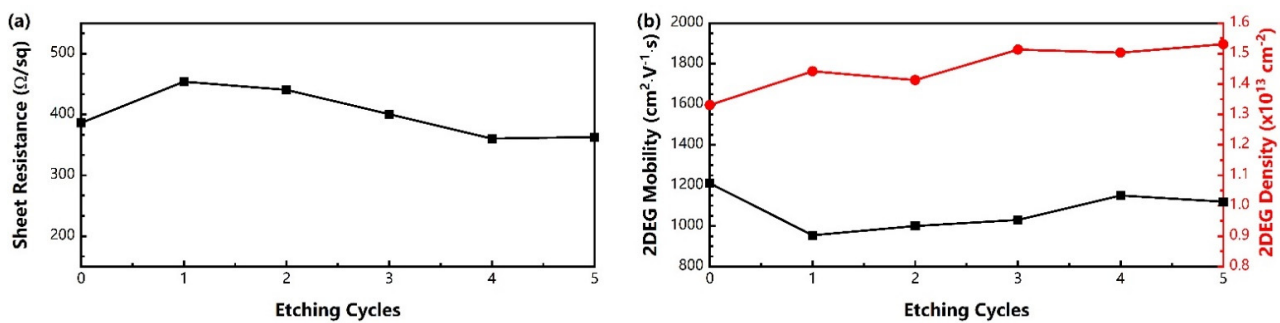


Figure 8. Resistor Hall effect (Hall) measurements of samples with 0–5 cycles of ALE surface treatment followed by rapid thermal annealing (RTA): (a) R_{sh} , (b) 2-DEG mobility and density.

Table 3. The $5 \times 5 \mu m^2$ RMS roughness and electrical properties of samples with 0–5 cycles of ALE surface treatment followed by RTA.

Surface Treatment Method	RMS Roughness (nm)	R_{sh} (Ω/sq)	2-DEG Mobility ($cm^2 \cdot V^{-1} \cdot s$)	2-DEG Density ($\times 10^{13} cm^{-2}$)
Sample S_0	0.44	386	1210	1.33
1 cycle sample S_1	0.56	454	954	1.44
2 cycles sample S_1	0.47	440	1000	1.41
3 cycles sample S_1	0.45	401	1030	1.51
4 cycles sample S_1	0.39	360	1150	1.50
5 cycles sample S_1	0.40	363	1120	1.53

4. Conclusions

In summary, this paper demonstrates an ALE technique with a surface treatment function for InAlN/GaN heterostructures. This ALE technique obtained well-controlled EPC (0.15 nm/cycle) and improved the surface RMS roughness (0.61 nm), which was much lower than that of the as-grown sample (0.71 nm), digital etching (0.69 nm), Cl_2/BCl_3 etching (0.91 nm) and BCl_3 etching techniques (0.89 nm). The XPS and STEM/EDS results confirmed the In clustered phenomenon below the V-pit defects, which was related to the surface morphology optimization of the under-etching ALE technology used in this work. Hall and AFM measurements verified the effective ALE surface treatment function on the InAlN/GaN heterostructure. A maximum reduction of 6.7% in R_{sh} and a maximum increasement of 15% in 2-DEG density, with surface roughness optimization of 11.4%, were obtained after four or five cycles of treatment. This enabled high-performance InAlN/GaN HEMTs designs to be obtained.

Author Contributions: Conceptualization, F.D. and Q.W.; data curation, H.L., Q.H., X.T. and H.H.; formal analysis, F.D.; funding acquisition, H.Y. and Q.W.; investigation, F.D., Z.W. and C.T.; methodology, Y.J.; project administration, Q.W.; resources, Z.W.; supervision, H.Y. and Q.W.; validation, Y.J., H.L., J.H. and K.W.; writing—original draft, F.D.; writing—review and editing, Q.W. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Research on R&D and industrialization of new energy vehicle drive and its special chip for charging pile (Grant No. 2019B010143001), Research and Application of Key Technologies of GaN-based Power Devices on Si Substrate (Key-Area Research and Development Program of Guangdong Province, Grant No: 2019B010128001), Research on key technologies for optimization of IoT chips and product development (Key-Area Research and Development Program of Guangdong Province, Grant No:2019B010142001), Research on the fabrication and mechanism of GaN power and RF devices (Grant No: JCYJ20200109141233476), Research on the GaN Chip for 5G Application (Grant No: JCYJ20210324120409025), Research on high-reliable GaN power device and the related industrial power system (Grant No: HZQB-KCZY-2021052) and Special Funds for the Cultivation of Guangdong College Students' Scientific and Technological Innovation. ("Climbing Program" Special Funds) pdjh2022c0073.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Acknowledgments: This work was supported by Research on R&D and industrialization of new energy vehicle drive and its special chip for charging pile (Grant No. 2019B010143001), Research and Application of Key Technologies of GaN-based Power Devices on Si Substrate (Key-Area Research and Development Program of Guangdong Province, Grant No: 2019B010128001), Research on key technologies for optimization of IoT chips and product development (Key-Area Research and Development Program of Guangdong Province, Grant No:2019B010142001), Research on the fabrication and mechanism of GaN power and RF devices (Grant No: JCYJ20200109141233476), Research on the GaN Chip for 5G Application (Grant No: JCYJ20210324120409025), Research on high-reliable GaN power device and the related industrial power system (Grant No: HZQB-KCZY-2021052) and Special Funds for the Cultivation of Guangdong College Students' Scientific and Technological Innovation. ("Climbing Program" Special Funds) pdjh2022c0073. The authors acknowledge the assistance of SUSTech Core Research Facilities.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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