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Review

Reliability, Applications and Challenges of GaN HEMT Technology for Modern Power Devices: A Review

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Abstract: A new generation of high-efficiency power devices is being developed using wide bandgap (WBG) semiconductors, like GaN and SiC, which are emerging as attractive alternatives to silicon. The recent interest in GaN has been piqued by its excellent material characteristics, including its high critical electric field, high saturation velocity, high electron mobility, and outstanding thermal stability. Therefore, the superior performance is represented by GaN-based high electron mobility transistor (HEMT) devices. They can perform at higher currents, voltages, temperatures, and frequencies, making them suitable devices for the next generation of high-efficiency power converter applications, including electric vehicles, phone chargers, renewable energy, and data centers. Thus, this review article will provide a basic overview of the various technological and scientific elements of the current GaN HEMTs technology. First, the present advancements in the GaN market and its primary application areas are briefly summarized. After that, the GaN is compared with other devices, and the GaN HEMT device's operational material properties with different heterostructures are discussed. Then, the normally-off GaN HEMT technology with their different types are considered, especially on the recessed gate metal insulator semiconductor high electron mobility transistor (MISHEMT) and p-GaN. Hereafter, this review also discusses the reliability concerns of the GaN HEMT which are caused by trap effects like a drain, gate lag, and current collapse with numerous types of degradation. Eventually, the breakdown voltage of the GaN HEMT with some challenges has been studied.

Keywords: GaN HEMT; normally off; reliability; challenges; power devices; semiconductor devices; wide bandgap

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1. Introduction

Electrical power has been a fundamental driver of humanity's progress and is indispensable in our daily life. Power electronics are critical components of electrical power usage because they control, convert, and manage electric currents, voltages, or powers. They are extensively utilized in consumer items, energy harvesting, and usage, such as switching power supplies, power converters, power inverters, motor drives, etc. Figure 1 shows the different fields of operation of power devices with the required voltage and current ratings [1,2]. As depicted in Figure 2, a typical power electronic system includes a power source, a filtering mechanism, a power conditioner, a load, and a control circuit. A power conditioner is composed of a series of semiconductor devices working in a switched mode, in which the devices are turned between the "OFF" and "ON" states under the direction of the gate driver [1]. When turned "off", an ideal switch should have no leakage

current and a full voltage drop across it. If switched "on", it should have a zero voltage drop across it (Figure 3). In actuality, the power devices exhibit a resistance during the on-state (R_{ON}) and a leakage current during the off-state. Under the common biasing conditions, the voltage across it is restricted by the off-state drain to source the breakdown voltage (BV_{DSS}). Thus, to maximize the energy efficiency and minimize conversion losses, the most crucial properties of power devices to accomplish are a low R_{ON} and a high BV_{DSS}.

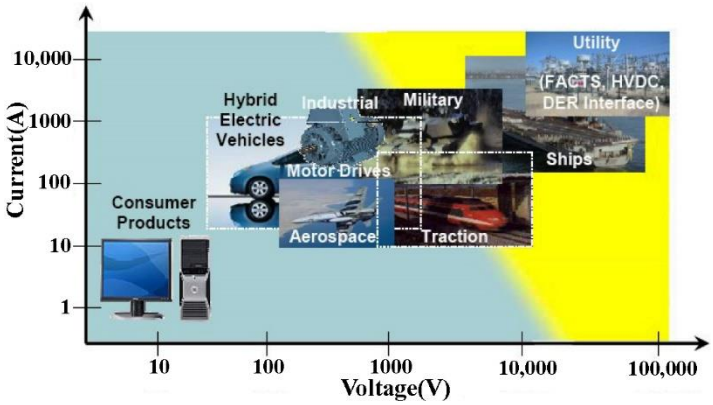


Figure 1. Applications of power electronics in power management and control. Reproduced with permission [2]. Copyright 2019, the author(s). Published by Elsevier.

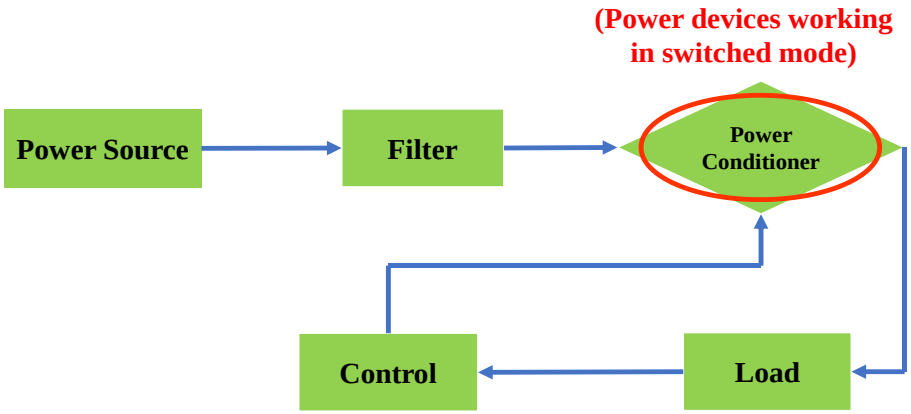


Figure 2. Components of a power electronic system and power semiconductor devices in power conditioners.

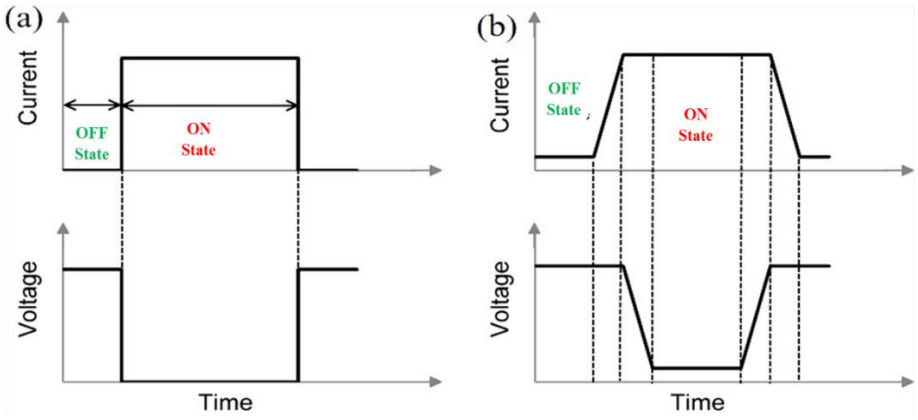


Figure 3. The current and voltage across (**a**) an ideal power switching device and (**b**) a power switching device.

Moreover, Gallium Nitride (GaN) has risen as an attractive material for fabricating semiconductor devices over the last decade. Its excellent performance characteristics, like its wide band gap, high electron mobility, high breakdown field, low noise, high saturation velocity, and low thermal impedance, are essential for modern power device technology [3].

This review article will provide a basic overview of the various technological and scientific elements of the current GaN HEMT technology, where we summarize the recent and future potential market strategy of GaN HEMT power devices. Additionally, the previous and present data of the most extensively used commercially device, the normally-off GaN HEMT, are amalgamated, focusing explicitly on the insulator's role in the recessed MISHEMT region and the metal on the p-GaN performances, which makes this review article more comprehensive compared to other review articles. Moreover, this review also discusses the reliability concerns of the GaN HEMT which are caused by trap effects like a drain, gate lag, and current collapse with numerous types of degradation.

1.1. Market Strategy of GaN HEMT Power Devices

GaN-based devices are being reported in various market-driven sectors, including RF power devices, photonics, high-frequency communications, control, and high-power conversion, which assists commerce's and corporations in meeting the constantly expanding need for more outstanding metrics. The inherent robustness of the device enables it to compete effectively in the current markets for tiny, rugged, and highly dependable electronics, such as in vehicle, military, and space applications. GaN engineering appears promising for achieving the critical performance requirements and the possibility of sustained economic benefits upon its maturity.

Figures 4 and 5 show that according to Yole Développement (Yole), the power GaN market will double by 2020, surpassing the USD one billion mark in 2026. As an additional validation of this remarkable GaN market development, Yole projects that the telecom and datacom and automotive sectors will contribute to the total growth in the mid- to long-term, owing to GaNs rise in fast chargers. In the consumer market, GaN had a good year in 2020, owing to the technology adoption by various businesses, including Xiaomi, Lenovo, Samsung, Realme, Dell, LG, and other Chinese aftermarket firms. Yole anticipates that the GaN consumer power supply industry will be the primary driver, growing from USD 29 million in 2020 to about USD 672 million in 2026 at a compound annual growth rate (CAGR) of 69%. In the telecom and datacom sectors, where more efficient, smaller power supplies must comply with the stricter energy consumption standards, data centers and telecom operators are already interested in GaN devices.

Following Eltek, Delta, and BelPower's recent small volume adoption of the GaN-based power supply, it was predicted that there would be a more significant market for GaN in 2020, with a market value of USD 9.1 million and a CAGR of 71% from 2020 to 2026, reaching more than USD 223 million in 2026. The automotive and mobility markets are also paying close attention to GaN because of significant incentives for vehicle electrification and a need to increase the driving range via A system efficiency improvement. AEC-qualified manufacturers include EPC, Transphorm, GaN Systems, and Texas Instruments. STMicroelectronics, a major IDM, also pursues GaN for EVs via partnerships and acquisitions. In 2022, GaN will likely infiltrate at limited levels, primarily via OEM and Tier-1 samples. Yole anticipates that the automobile and mobility industry will exceed a value of USD 155 million in 2026 [4].

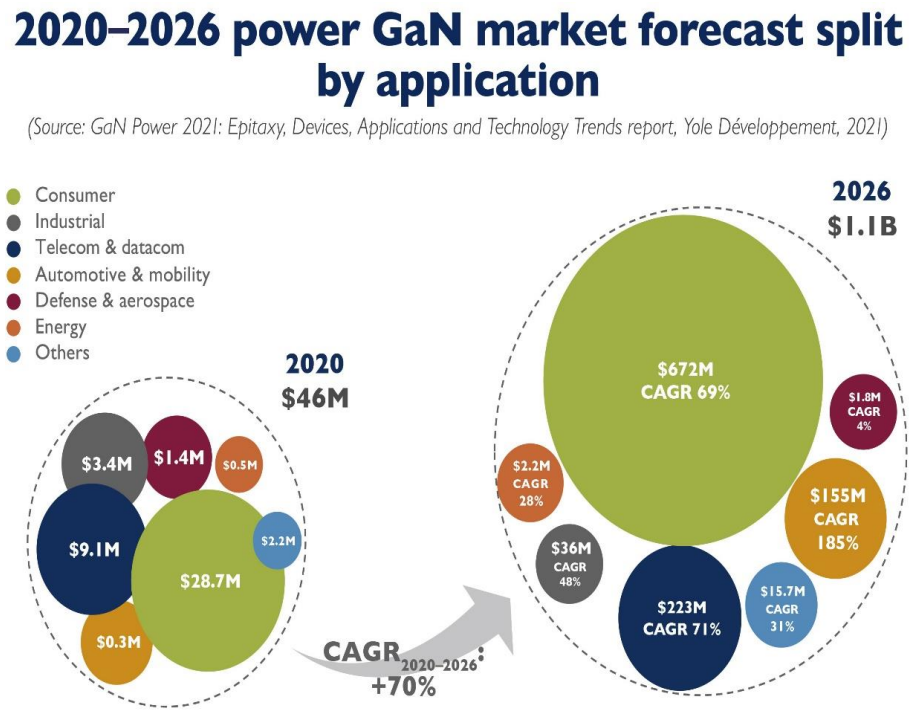


Figure 4. GaN power market forecast split by application prediction by Yole. Reproduced with permission [4]. Copyright 2021, published by Yole Développement.

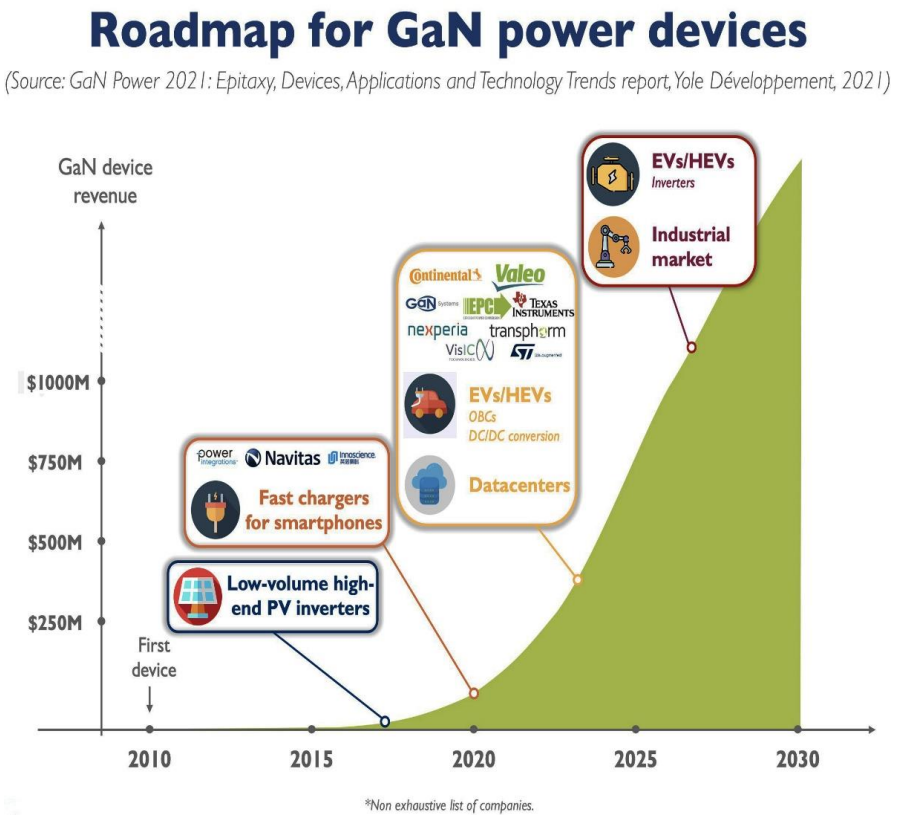


Figure 5. Roadmap for GaN power devices prediction by Yole. Reproduced with permission [4]. Copyright 2021, published by Yole Développement.

While GaN continues to gain traction in the general consumer market, telecom, datacom, automotive, and mobility businesses will benefit from the "economy of scale impact" and price erosion. Indeed, Yole anticipates that a GaN adoption will increase in these areas, where reliability and affordability are critical, beginning in 2023–2024. In the long run, after GaN has shown its durability and high current capability at a lower price, it may be able to reach the more difficult EV/HEV inverter market and the conservative industrial industry, creating an extraordinary high-volume potential for GaN. Indeed, Nexperia and VisIC are developing GaN-based xEV inverter systems to compete with SiC and Si. Furthermore, as various industry experts previously said, GaN is more suitable for low-to-medium voltage applications (200–600 V), including a sizable share of the consumer electronic market (e.g., phone chargers, audio amplifiers, and computer power supplies). GaN is the most excellent contender to replace conventional Si devices in this voltage range. The 600–900 V voltage range is strategically important since it includes converters for electric cars (EVs), hybrid EVs, and inverters for sustainable energy (e.g., photovoltaic). GaN devices are projected to compete or coexist alongside SiC devices in this voltage range. Recent industry analyst studies [5] show that the GaN power device market is expected to grow dramatically, surpassing a value of USD 700 million in 2025, as illustrated in Figure 6.

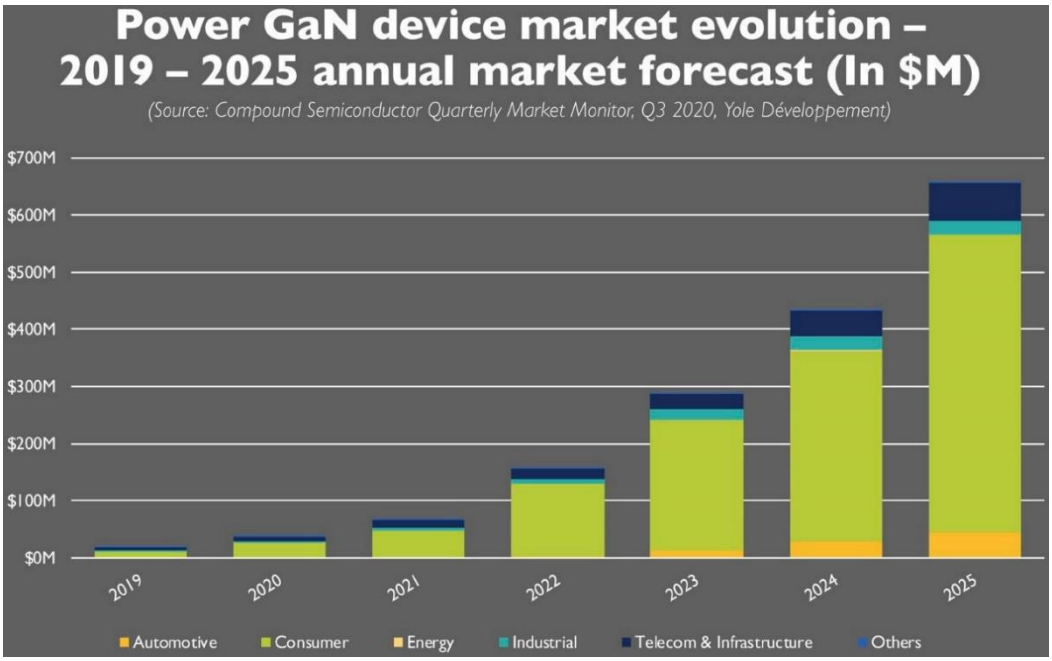


Figure 6. GaN Power device market size prediction by Yole. Reproduced with permission [5]. Copyright 2020, published by Yole Développement.

1.2. Market Strategy of GaN HEMT RF Devices

The gallium nitride (GaN) radio-frequency (RF) device market is rising at a compound annual growth rate (CAGR) of 18% from a USD 891 million value in 2020 to a more than USD 2.4 billion value by 2026, forecasts the market analyst firm Yole Développement [6]. It has been forecasted that the market will be dominated by defense and 5G telecom infrastructure applications, representing 49% and 41% of the entire market by 2026, respectively. In particular, the GaN-based macro/micro-cell sector will represent more than 95% of the GaN telecom infrastructure market in 2026, as reflected in Figure 7.

In the RF GaN industry, everything started with GaN-on-SiC (gallium nitride on silicon carbide) technology. Launched more than 20 years ago, GaN-on-SiC is now a serious rival to silicon LDMOS and gallium arsenide (GaAs) in RF power applications. Dominated by GaN-on-SiC technology, a vertical supply chain integration has been preferred in defense and 5G telecom applications. Therefore, GaN-on-SiC technology is still preferred in terms

of its high-power density and thermal conductivity. In addition to its deep penetration in the military radar, GaN-on-SiC has also been the choice of telecom OEMs such as Huawei, Nokia, and Samsung for 5G massive MIMO infrastructures. Due to their high bandwidth and efficiency, GaN-on-SiC devices continuously take a share from LDMOS of the 5G market and are starting to benefit from the 6" wafer platform transition. In this context, the GaN-on-SiC device market is growing at a 17% CAGR from USD 342 million in 2020 to USD 2.222 billion in 2026. However, as a key challenger, GaN-on-Si is still in the game, promising cost-efficient and scalable solutions. The recent entry of foundries and synergy with the emerging power electronics GaN-on-Si industry can also help GaN-on-Si RF to gain momentum in the longer term, says Yole. Driven by handsets but also defense and 5G telecom infrastructure applications, the GaN-on-Si device market is growing at a CAGR of 86% from less than USD 5 million in 2020 to USD 173 million in 2026 [6], as illustrated in Figure 8.

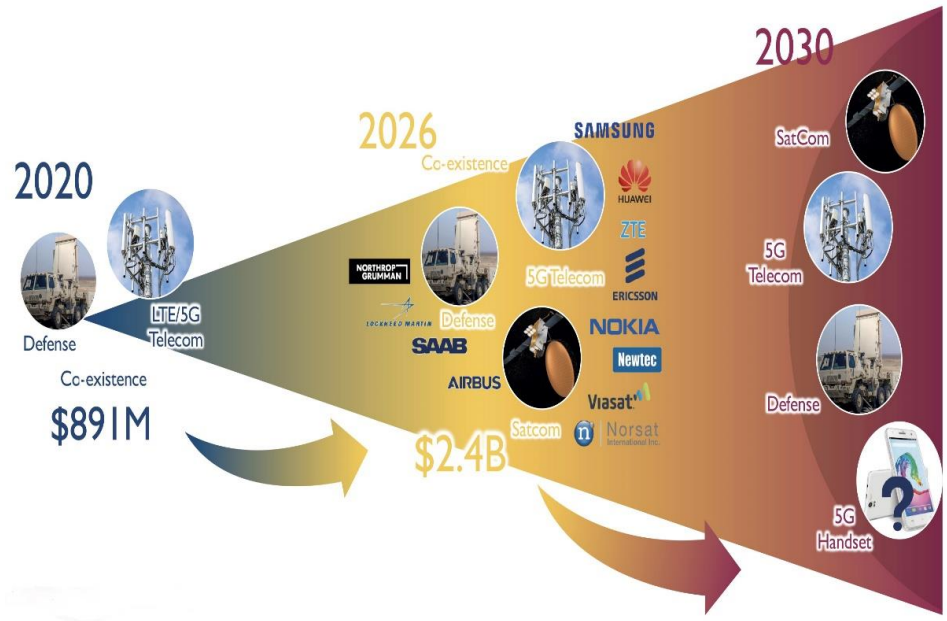


Figure 7. GaN Power RF market evaluation by Yole. Reproduced with permission [6]. Copyright 2021, published by Yole Développement.

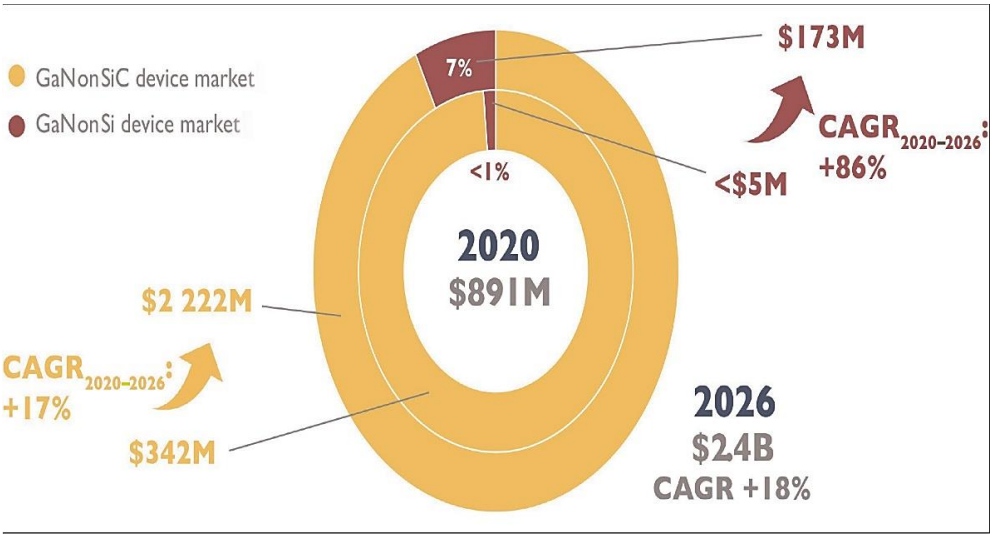


Figure 8. GaN RF application breakdown by substrate markets as compiled in 2021 by Yole. Reproduced with permission [6]. Copyright 2021, published by Yole Développement.

2. Wide Bandgap Semiconductors for Power Devices

Due to the many constraints of silicon-based power devices and the rising interest in increasing performances, new semiconductor materials for next-generation power electronic devices are being developed. Because of their better electrical properties, wide bandgap (WBG) semiconductors like GaN, β-Ga_2O_3, and SiC have emerged as market leaders in power electronic applications. Since the material's small bandgap is responsible for many of the constraints for Si-based devices, wide bandgap power devices have a better performance with a larger blocking voltage, dependability, and efficiency with less thermal constraint [7–9]. Thus, GaN, β-Ga_2O_3, and SiC have a bandgap which is two to four times that of Silicon. A bigger energy bandgap makes it more challenging to break the bonding and generate free charge carriers for a current conduction, which results in a less conductive material and transistors with lower leakage currents and a more excellent stability at high temperatures. On the contrary, β-Ga_2O_3 devices have a substantially greater breakdown voltage compared to Si devices when their on-resistances are comparable. Moreover, GaN devices have a larger saturation on-current than Si devices due to the higher saturated electron velocity of GaN. Additionally, the carrier drift velocity directly connects with the switching speed of semiconductor devices, and this device has a quicker recovery time and a lower reverse recovery current. On the other hand, SiC presents a thermal conductivity three times higher than Si and GaN and 16 times higher than β-Ga_2O_3. The characteristics of Si are compared to those of WBG semiconductors such as SiC, β-Ga_2O_3, and GaN in Figure 9 [10–12].

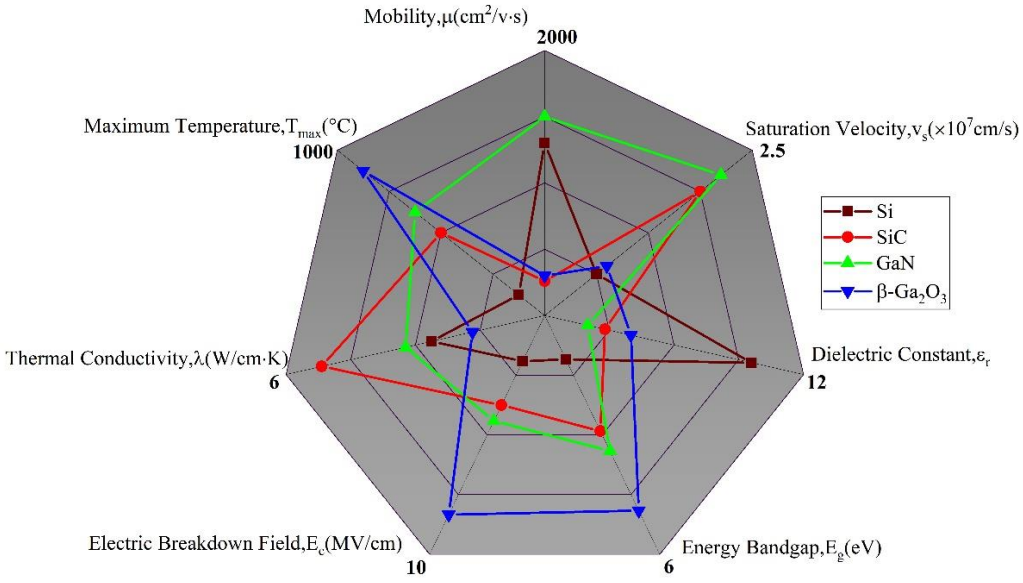


Figure 9. Comparison of wide bandgap materials with Si.

However, numerous figures of merit (FOM) have been proposed to compare the merit of several semiconductor materials for a provided application. A higher figure of merit number indicates a better performance. Hence, Johnson's figure of merit (JFOM) provides an indication of the material suitability for high-power applications at high frequencies, which can be estimated by using Equation (1) [13]:

$$\mathrm{JFOM} = \left(\frac{E_c V_{sat}}{2\pi}\right)^2 \quad (1)$$

Here, V_{sat} denotes the saturation electron velocity, and E_c denotes the critical electric field. On the contrary, to analyze the optimum results of field effect transistors in low-

frequency power switching applications, Baliga's figure of merit (BFOM) was devised where conductive loss predominates, as shown in Equation (2) [14]:

$$\mathrm{BFOM} = \varepsilon_r \mu {E_g}^3 \tag{2}$$

Here, ε_r denotes the semiconductor's dielectric constant, and μ denotes the electron mobility. For a high frequency, the Baliga high-frequency FOM (BHFOM) in Equation (3) evaluates the devices where the switching losses are the most significant [14]:

$$\mathrm{BHFFOM} = \frac{\mu {E_c}^2 {V_g}^{\frac{1}{2}}}{2{V_{BR}}^{\frac{3}{2}}} \tag{3}$$

Here, the gate drive voltage is V_g, while the breakdown voltage is V_{BR}. By using the device's on-state specific resistance, R_{on}, and the critical electric field, E_c, the latter is coupled to an experimental figure of merit on Equation (4). Eventually, to account for the high power, high temperature, and high-frequency performance simultaneously, the combined FOM (CFOM) was devised, as shown in Equation (5) [15]:

$$\mathrm{FOM} = \frac{{V_{BR}}^2}{R_{on}} = \varepsilon_r \mu \frac{{E_c}^3}{4} \tag{4}$$

$$\mathrm{CFOM} = \chi \varepsilon_r \mu V_{sat} {E_c}^2 \tag{5}$$

Table 1 shows the multiple figures of merit for the β-Ga_2O_3 potential high-frequency and high-power performance compared to other competing semiconductor materials. According to this table, β-Ga_2O_3 is a great contender for high-frequency power applications. In JFOM, the β-Ga_2O_3 is more remarkable than approximately 1.5 times that of GaN, 10 times that of SiC, and about a thousand times that of Si. Consequently, β-Ga_2O_3 outperforms Si, GaN, and SiC in terms of its high-frequency/high-power performance. Similarly, in BFOM, β-Ga_2O_3 is more remarkable than around four times that of GaN, ten times that of SiC, and a thousand times that of Si [16]. Moreover, wide-bandgap semiconductors, regardless of their FOM, provide better performance features for high-power, high-frequency applications. Thus, due to the high values of the Baliga FOM and the breakdown field, β-Ga_2O_3 is a promising candidate for the next generation of high-power devices, including HEMT, Schottky barrier diodes (SBDs), and field-effect transistors (FETs).

Table 1. Figures of merit of GaN and competing semiconductor materials in power electronics [12].

Material	Johnson's Figure of Merit, (JFOM)	Keyes Figure of Merit, (KFOM)	Baliga's Figure of Merit, (BFOM)	Baliga's High Frequency Figure of Merit, (BHFFOM)	Combined Figure of Merit, (CFOM)
Si	1.0	1.0	1.0	1.0	1.0
SiC	277.8	3.6	317.1	46.3	248.6
GaN	1089.0	1.8	846.0	100.8	353.8
β-Ga_2O_3	2844.4	0.2	3214.1	142.2	37.0

2.1. Lattice Structure and Polarization of GaN-Based Semiconductors

Wurtzite hexagonal close-packed (HCP) (α-phase), rock-salt, and cubic zincblende (β-phase) are examples of III-N-based semiconductors, mainly GaN-based semiconductors [17,18]. Figure 10 depicts the wurtzite crystal structure, which is particularly important for electronics and optoelectronics applications today. The hexagonal unit cell of wurtzite comprises two intersecting hexagonal close packed (HCP) sub-lattices. As illustrated in Figure 10, it is defined by two lattice parameters, the height of the cell c_0, and the length of a side of the hexagonal base a_0, in an ideal ratio $\frac{c_0}{a_0} = \sqrt{\frac{8}{3}} \approx 1.633$. Each sub-lattice is made

up of one kind of atom. In relation to one another, the internal cell parameter $u_0 = 3/8$ moves them along the c-axis. Table 2 presents the structural and polarization properties of III-Ns.

Table 2. Structural and polarization parameters of III-N wurtzite semiconductors [17].

Parameter	GaN	AlN	InN
$a_0(A^\circ)$	3.197	3.108	3.580
c_0/a_0	1.6297	1.6033	1.6180
$\epsilon_1 = (u_0 - u_{ideal}) \times 10^{-3}$	1.9	6.4	3.7

These ideal values are absent in the typical nitride compounds GaN, InN, and AlN and their associated alloys. The c_0/a_0 ratio deviates from the ideal lattice's 1.633 as the non-ideality of the lattice grows [19].

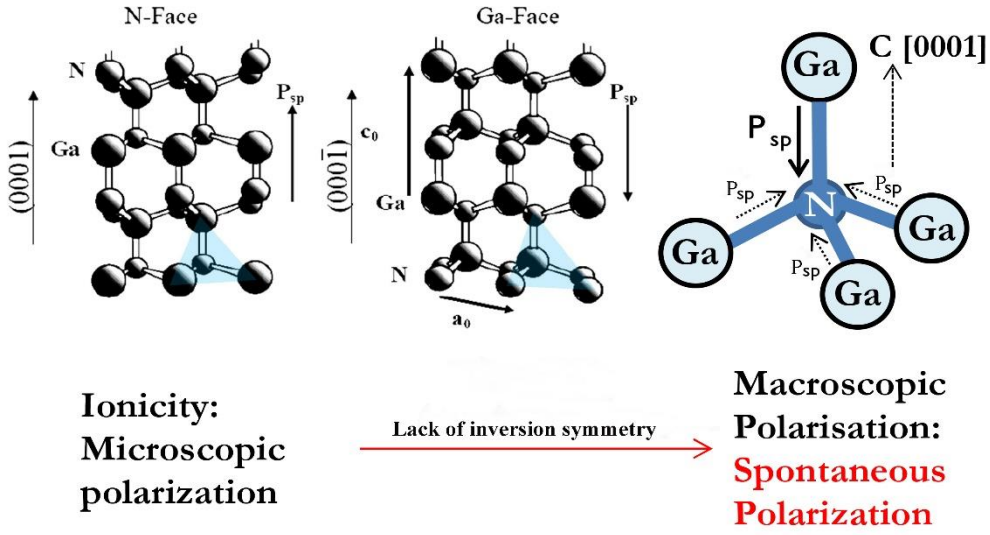


Figure 10. The alignment of P_{SP} and the tetrahedral bond structure of Ga-face and N-face heterostructures. Reproduced with permission [20]. Copyright 2019, Elsevier.

Because of the very high electronegativity of the N atom, which is 3.04 on Pauling's scale, and for Aluminum (1.61), Gallium (1.81), and Indium (1.78) atoms [19], consequently, the data for u_0 and c_0/a_0 deviate from the optimum values given earlier [21]. Group III-N semiconductors have a particularly high polarization due to the crystal structure's intrinsic electronic charge redistribution, which means a spontaneous polarization, P_{sp}, [19]. The directions <0001> and <000$\bar{1}$> are not comparable due to a lack of inversion symmetry shown along its c-axis in the wurtzite structure. Hence, cation-face, i.e., Ga-face and anion-face, i.e., N-face, are the alternative polarities of GaN. The polarization field points change their position in the cation-face, i.e., Ga-face, surface towards the substrate. On the contrary, the polarization field points move in the opposite direction in the anion-face, i.e., N-face.

Because of the lack of this inversion symmetry, when the group III-N semiconductors' lattice is imposed by stress in the <0001> direction, the ideal lattice values of the crystal structure's c_0 and a_0 will shift to adapt to the stress. As a result, the strength of the polarization would shift. In the strained group III-N crystals, this extra polarization is known as piezoelectric polarization, P_{pz} [22]. For instance, the in-plane constant of the lattice a_0 would drop, and the vertical constant of the lattice c_0 would rise if the crystal of the nitride is subjected towards a biaxial compressive stress. Due to the piezoelectric and spontaneous polarizations working in opposing directions, the ratio of c_0/a_0 will climb to 1.633 of the perfect lattices, and the overall polarization strength will be reduced in the crystal. Moreover, when the tensile stress is imposed on the crystal, the spontaneous and

piezoelectric polarization work simultaneously. As a result, the total polarization will rise. The piezoelectric coefficients e_{33} and e_{13} are evaluated for the piezoelectric polarization, P_{pz} [23,24], as shown in Equation (6),

$$P_{pz} = e_{33}\varepsilon_3 + e_{13}(\varepsilon_1 + \varepsilon_2) \quad (6)$$

Here, a_0 and c_0 are the lattice parameter equilibrium values, $\varepsilon_3 = (c - c_0)/c_0$ is the strain along the c axis, and $\varepsilon_1 = \varepsilon_2 = (a - a_0)/a_0$ is the isotropic in-plane strain. The various strains in the lattice are connected in Equation (7). The elastic constants denoted by c_{13} and c_{33}. Combining Equations (1) and (2) provides the corresponding formula in Equation (8):

$$\varepsilon_3 = -2\frac{c_{13}}{c_{33}}\varepsilon_1 \quad (7)$$

$$P_{pz} = 2\frac{a - a_0}{a_0}\left[e_{13} - e_{33}\frac{c_{13}}{c_{33}}\right] \quad (8)$$

The equation $\left(e_{13} - e_{33}\frac{c_{13}}{c_{33}}\right)$ will be negative if e_{33}, c_{13}, and c_{33} are positive, and the piezoelectric coefficient e_{13} is negative in wurtzite III-nitrides [25]. Thus, it is claimed that piezoelectric and spontaneous polarization are parallel under tensile stress layers, but they are anti-parallel under compressive stress layers. Polarization and gradients induce fixed sheet charges at the surfaces and interfaces of the AlGaN/GaN heterostructures. As a result, there are high electric fields within the heterostructure. The electric field in nitrides may approach 3×10^6 V/cm, which enhances the hole or electron formation at the AlGaN/GaN contacts. This is called polarization-induced doping, which is the root of the two-dimensional electrons gas (2DEG) (discussed more in the below segment).

Figure 11a shows that growing a tiny epi AlGaN layer on top of a thicker GaN layer generates an AlGaN/GaN heterostructure. A 2DEG is generated at the interface between the AlGaN barrier and the GaN channel because of the P_{sp} and P_{pz}, which may be a conduction channel consisting of exceptionally high mobility electrons even without any n-type doping, which is ideal for transistors. Both GaN and AlGaN have a significant P_{sp}. When the material is strained, a P_{pz} component develops in GaN, AlN, or AlGaN. The piezoelectric polarization arises in the thin layer of AlGaN because it is beneath the tensile strain. In contrast, the layer of GaN is considerably thicker and nearly relaxed in an AlGaN/GaN heterostructure. P_{sp} and P_{pz} are parallel when the AlGaN layer is under a tensile strain (Figure 11a) [23]. So, to acquire the AlGaN characteristics and determine the actual polarization-induced charge densities, we apply Equations (9) through to (14) [26].

Similarly, 2DEG is generated at the interface between the AlN barrier and the GaN channel for the reason of the P_{sp} and P_{pz}, as illustrated in Figure 11b. However, due to the large difference in the spontaneous and piezoelectric polarizations between the GaN and AlN layers, the 2DEG, which forms near the AlN/GaN interface, can reach over 3×10^{13} cm^{-2} for an extremely thin AlN barrier layer thickness (d < 5 nm), along with a high mobility (>1000 $cm^2/V{\cdot}s$) and a very low sheet resistance (R_{sh} < 150 Ω/□) [27]. On the contrary, due to the high aluminum content and the associated degree of bond polarity, a spontaneous polarization in in the $In_{0.18}Al_{0.82}N$/GaN heterostructures generates two-dimensional electrons gas (2DEG) densities which are competitive with AlGaN/GaN structures without the need for a strain-induced piezoelectric component. For InAlN alloys, the strain state can go from tensile when the In % is lower than ~18%, to compressive when the In % is higher than ~18%, as shown in Figure 11c ((1), (2)), respectively; when the InAlN is the lattice matched to the GaN buffer, the In % is around 18%. Moreover, the implementation of the InAlN barriers with the In % around 18% allows for the strain to be controlled in the InAlN/GaN heterostructure, and a lattice-matched $In_{0.18}Al_{0.82}N$ layer to the GaN sheet charge density is almost three times higher than for the conventionally grown $Al_{0.25}Ga_{0.75}N$ barriers on the GaN channels [28].

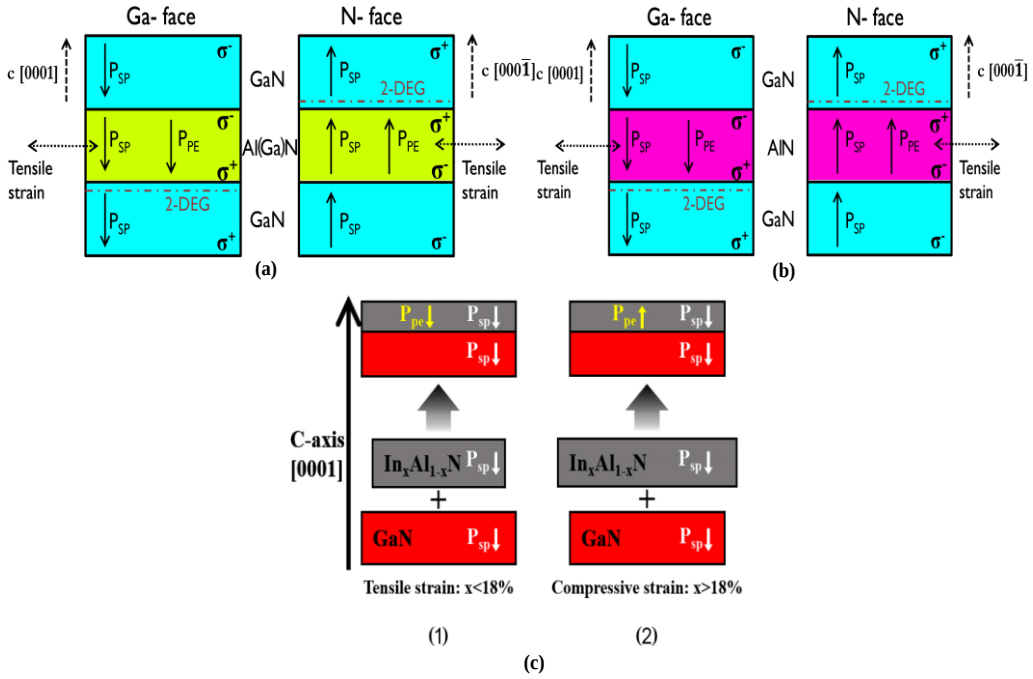


Figure 11. Polarization charges in an (**a**) AlGaN/GaN, (**b**) AlN/GaN, and (**c**) InAlN/GaN heterostructure. Reproduced with permission [20]. Copyright 2019, Elsevier.

Spontaneous polarization can be observed in Equation (9). As an alternative, for a precise interpolation, a bowing parameter b might be utilized in Equation (10) [29]. The constants of the lattice for $Al_xGa_{1-x}N$ are in Equations (11) and (12) where x = Al mole fraction. The elastic constants are presented in Equations (13) and (14).

$$P_{sp}(x) = (-0.052x - 0.029)\ \frac{c}{m^2} \tag{9}$$

$$P_{sp}(x) = \left(\left(xP_{sp}(AIN) + (1-x)P_{sp}(GaN) + bx(1-x)\right)\right. \tag{10}$$

$$a_0\ (x) = (-0.077x + 3.189) \times 10^{-10}\ m \tag{11}$$

$$c_0\ (x) = (-0.203x + 5.189) \times 10^{-10}\ m \tag{12}$$

$$c_{13}\ (x) = (5x + 103)\ GPa \tag{13}$$

$$c_{33}\ (x) = (-32x + 405)\ GPa \tag{14}$$

The above equations indicate that if the Al content in the AlGaN layer rises, the overall polarization will soar. A polarization charge density (ρp) corresponds to a polarization gradient (P) in space ($\rho p = \nabla P$). Therefore, at the AlGaN/GaN abrupt contact, a fixed polarization charge would be induced. In the case of AlGaN/GaN, fixed positive induced polarization charges form at the interface. Even without n-type doping, the positive polarization-induced charges at the interface of AlGaN/GaN attract the free electrons. Because of this, in the AlGaN/GaN interface, 2DEG is generated. The carrier density of 2DEG may also be estimated analytically by using polarization [30].

The 2DEG creation is explained in a few Figures. Thus, in the undoped AlGaN/GaN heterojunction, the 2DEG creation may be described on the AlGaN surface by introducing donor states. An the isolated AlGaN material energy band gap is depicted in Figure 12 with the presence of surface donor states. The isolated AlGaN material is believed to be free of compressive/tensile forces. The Fermi level is attained if the density of the AlGaN material is enough. So, the electrons are advanced to the conduction band and drawn to the other side by polarization-induced electric fields after the Fermi level exceeds the donor state-level E_S. The Fermi level causes the dropping of the electrons into the GaN side

when the AlGaN and GaN materials come into contact. The 2DEG results from a buildup of electrons at the interface, as displayed in Figure 13. Thus, combined with the ionized surface donor, it produces an electric field that points between the interface and the surface in the AlGaN layer to minimize the polarization field [31].

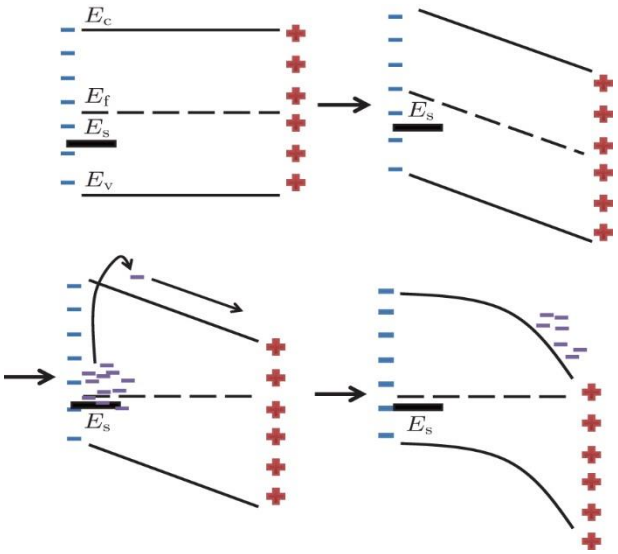


Figure 12. An undoped AlGaN material with E_S surface donor states has an energy band. Electrons are advanced into the conduction band and gravitate toward the electric field created by positive polarization. Reproduced with permission from Chin. Phys. B. [31].

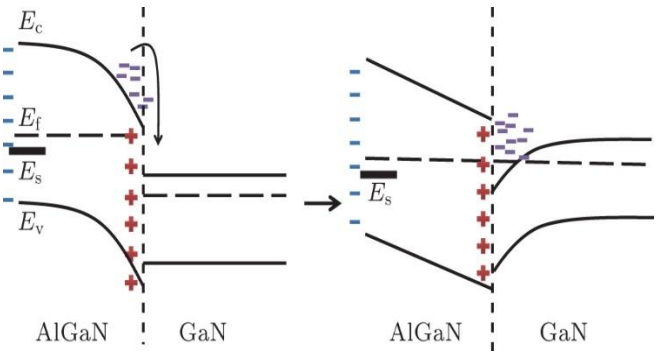


Figure 13. In the 2DEG quantum well, the buildup of electrons is shown in the energy band of an undoped AlGaN/GaN heterojunction. Reproduced with permission from Chin. Phys. B. [31].

As noted previously, the creation of 2DEG occurs naturally at the interface when a tiny strained AlGaN layer is developed on top of a thicker relaxed GaN layer. Due to the confinement of high mobility electrons, this 2DEG exhibits very conductively in the quantum well. Because of the reduced surface scattering, the electron mobility rises between the unstrained GaN and 2DEG areas at roughly 1000 $cm^2/V{\cdot}s$ and 1500–2000 $cm^2/V{\cdot}s$, respectively. For HEMTs, a transistor channel with a higher mobility and electron concentration seems appropriate. Figure 14 depicts a basic AlGaN/GaN HEMT design. The substrates are mostly SiC, silicon, sapphire, or GaN, and a buffer layer is formed to relieve the strain induced by a foreign substrate's lattice mismatch. The 2DEG creates a native channel between the source and drain of the device.. In most early AlGaN/GaN transistors, a Schottky gate electrode is formed by the deposition of Ni/Au or Pt metal on top of the AlGaN layer [32]. The GaN HEMT, with the 2DEG present at the interface of the AlGaN/GaN, was first shown in early 1993 [33]. The channel is regulated by supplying a gate voltage (V_{GS}) and, therefore, a vertical electrical field to deplete or augment the

channel, making it less conductive in the off-state or more conductive in the on-state. Later, researchers from all over the globe have progressively reported high-performance GaN HEMTs for high-power and RF applications [34,35].

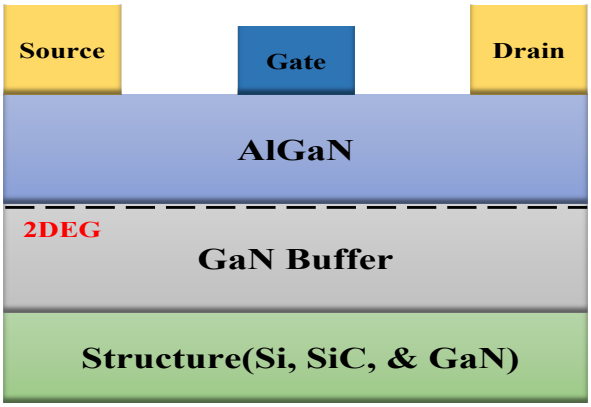


Figure 14. AlGaN/GaN HEMT layout and 2DEG generated in AlGaN/GaN contact are shown by the dashed line.

As said previously, when no bias voltage is applied from the gate to the source at the AlGaN/GaN interface, i.e., V_{GS} = 0 V, the 2DEG channel exists. This kind of HEMT is known as a normally-on HEMT or a depletion-mode (D-mode) HEMT. It signifies that a current may freely flow between the source and the drain. It also indicates that the AlGaN/GaN HEMT's threshold voltage (V_{TH}) is less than 0 V, requiring a V_{GS} to deplete the 2DEG and switch off the HEMT, as shown in Figure 15. Meanwhile, this feature is also one of the primary problems for the state-of-the-art AlGaN/GaN HEMTs utilized in higher current and power applications [36]. It has several practical limitations, including a high consumption, possible electrical safety risk, intrinsic fail-safe functioning, and complex circuit layout [32,36]. As a result, a normally-off operation, or an enhance-mode (E-mode) HEMT, is needed due to a high and positive threshold voltage (V_{TH}).

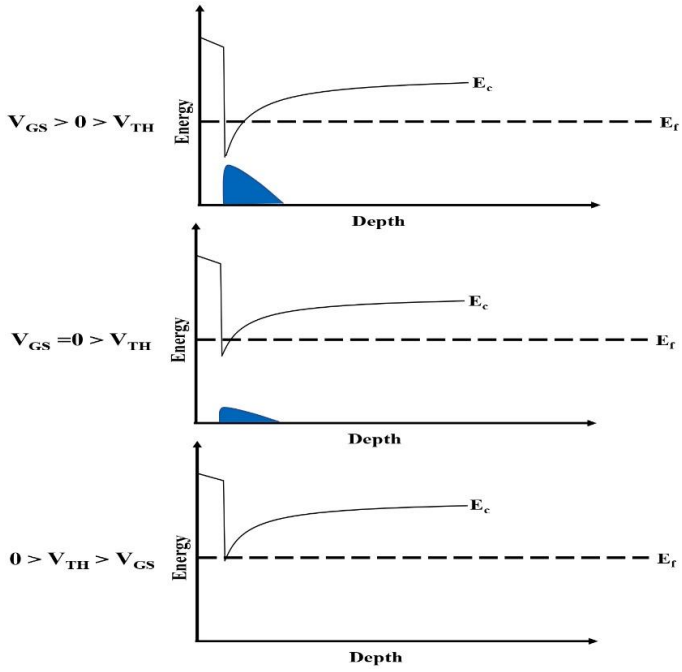


Figure 15. The band diagrams for the three locations of the 2DEGs $V_{GS} > 0 > V_{TH}$, $V_{GS} = 0 > V_{TH}$ and $0 > V_{TH} > V_{GS}$.

2.2. Lateral and Vertical GaN Power Transistors

Power transistors based on GaN are considered for two types of design: lateral and vertical structures. The lateral structure of the GaN HEMT is illustrated in Figure 16, where 2DEG formed at the AlGaN/GaN heterostructure interface. A high electron mobility (2000 cm^2/Vs) and electron velocity (1.3×10^7 cm/s saturation velocity and 2.5×10^7 cm/s peak velocity) characterize the AlGaN/GaN structure. Furthermore, due to a significant spontaneous and piezoelectric polarization, the GaN HEMT structure exhibits a density of sheet carriers over 1×10^{13} cm^{-2} in III-nitride materials. GaN HEMTs have a low on-resistance because of the device's carrier density and high electron mobility. This structure is discussed deeply in the normally-off GaN HEMT section.

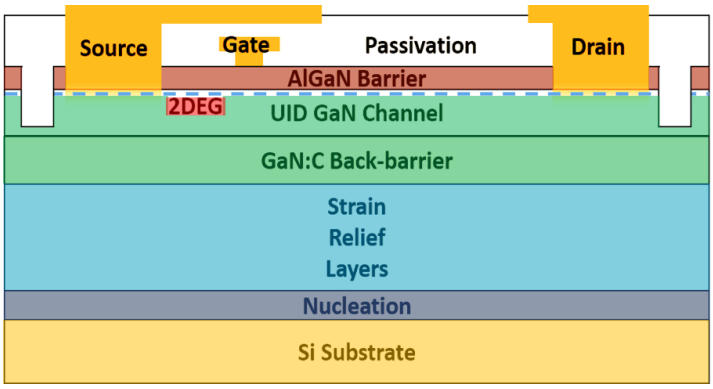


Figure 16. Typical lateral AlGaN/GaN HEMT structure. Reproduce from IOP science under the terms of the Creative Commons Attribution 3.0 license [36].

Similarly, the vertical layout is beneficial for obtaining a high breakdown voltage and low on-resistance characteristics, as displayed in the current aperture vertical electron transistor (CAVET) in Figure 17 [36]. Here, the drain at the bottom, the gate, and the source are on the top of the structure. The gate controls the current via an aperture among the current blocking layers (CBLs) into the drain, where vast amounts of material flow, which is commonly produced by an isolation implantation or P-type doping of the GaN layer. The AlGaN/GaN layer's horizontal high mobility electron channel is combined with a thick GaN drift region to obtain a low R_{ON} and a high breakdown voltage. Compared to the lateral designs, vertical devices into the bulk material of the device maintain the blocking voltage in the vertical direction, resulting in a lower chip area for a particular operation current.

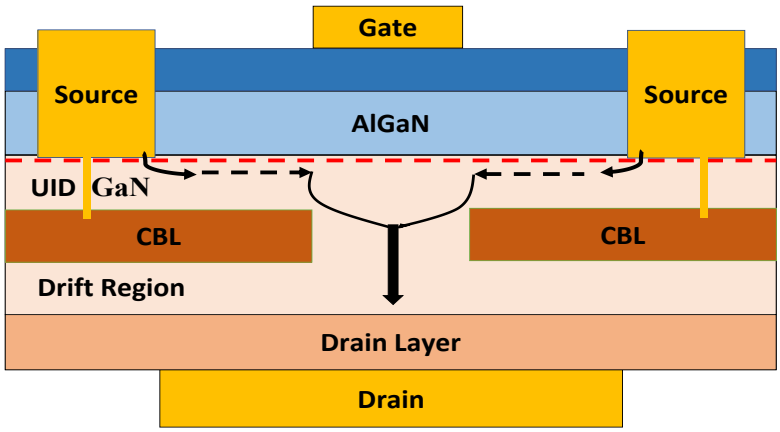


Figure 17. Vertical CAVET AlGaN/GaN HEMT structure. Reproduce from IOP science under the terms of the Creative Commons Attribution 3.0 license [36].

3. Normally on and off GaN HEMT Power Device Structure

3.1. GaN HEMT Technology (Normally on)

When the AlGaN/GaN HEMT structure is normally on, it is known as the depletion-mode (D-mode) structure. Figure 18 illustrates one of the examples of it. Where the buffer layer (1–5 µm) is deposited on the substrate for compensating the lattice mismatch stress, after that, to form a heterojunction, the GaN (UID) layer, AlN layer (0.7–1.2 nm), and $Al_xGaN_{1-x}N$ barrier (15–30 nm) layer is deposited. The thickness and Al molar fraction x of the $Al_xGaN_{1-x}N$ (usually 0.15 to 0.4) varies to maintain the number of acceptable electric charges under the relaxation's critical thickness [37]. The heterojunction's energy bands are bent downward to produce a quantum well with a sharp, where electrons of a high intensity are confined at the interface of AlGaN/GaN due to a bandgap offset and the polarization impact of AlGaN/GaN [38]. Then, the 2DEG channel generates the high-density current from the Ohmic-contact source to the drain [39]. Consequently, a Schottky gate is needed for the pinching off the 2DEG channel, which is normally on. When sufficient negative voltages are applied to the devise gate, the height of the Schottky barrier increases, allowing for the conduction band to pass through the AlGaN barrier's gate region; thereby, the HEMT is turned off. Eventually, for the device surface protection, passivating layers (often SiO_2 or SiN_x) are required [40–42].

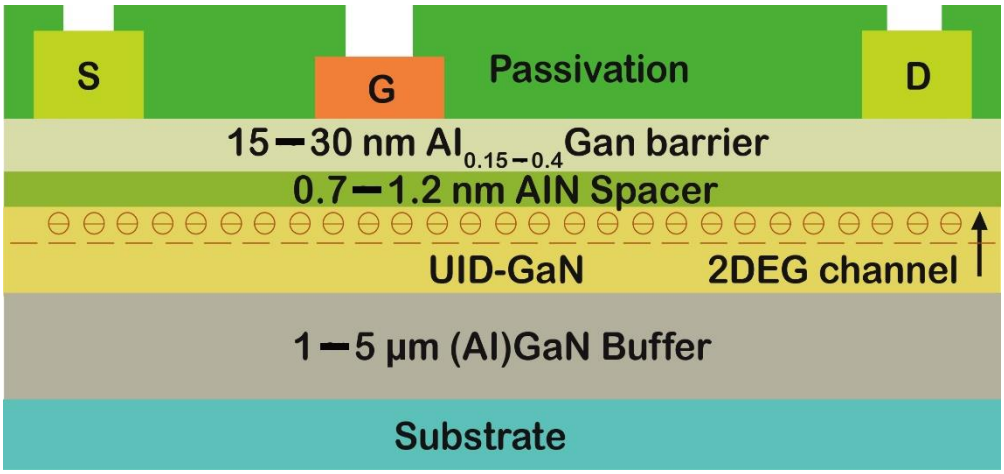


Figure 18. Device layout for a GaN HEMT structure that is normally on.

3.2. GaN HEMT Technology (Normally off)

In the field of power conversion, a negative bias is required to turn off the devices, which is the major issue for the normally-on devices. On the contrary, a normally off operation is widely wanted for safety reasons. Consequently, academia and industry (e.g., Gan Systems, Infineon, Panasonic, STMicroelectronics, and On Semiconductors) are working to create and market dependable normally-off HEMTs [43]. Thus, the threshold voltage V_{TH} in AlGaN/GaN HEMT is determined by numerous variables relating to the heterojunction and gate metal characteristics, shown in Equation (15) [44]:

$$V_{TH}(x) = \varphi_B(x) - \Delta E_C(x) - \frac{\sigma(x)}{\varepsilon_0 \varepsilon_{AlGaN}(x)} t - \frac{qN_D}{2\varepsilon_0 \varepsilon_{AlGaN}(x)} (t)^2 \quad (15)$$

where between the gate metal and the AlGaN barrier layer, φB(x) denotes the Schottky barrier height, σ(x) denotes the polarization charge at the interface of the AlGaN/GaN, $\Delta E_C(x)$ denotes the conduction band discontinuity at the interface of the AlGaN/GaN, $\varepsilon_{AlGaN}(x)$ denotes the AlGaN layer permittivity, ε_0 denotes the permittivity vacuum, t denotes the AlGaN thickness, N_D denotes the doping, q denotes the electric charge, and x denotes the Al content in the barrier layer. As ns increases at a zero bias, more significant polarization discrepancies between the AlGaN and GaN and thicker AlGaN barriers result

in a more negative V_{TH}. Hence, it is clear from the equation that the AlGaN barrier layer or modifying Schottky barrier height relies on the thickness and Al content to tune the V_{TH}. Therefore, various approaches have been suggested for obtaining the normally-off GaN HEMTs: the (a) cascode configuration, (b) fluorine implantation and thin/ultrathin-barrier, (c) p-GaN Gate, and (d) recessed gate.

3.2.1. HEMTs with Cascode Configuration (Normally off)

Figure 19 reflects a cascode setup of high-voltage normally-on GaN HEMTs and low-voltage normally-off Si MOSFETs [45,46]. When the V_{TH} of a Si MOSFET less than the positive gate-to-drain voltage is applied to the system, the GaN HEMT's gate-source voltage is 0 V; as a result, the opening of a GaN HEMT is normally on. By contrast, deactivating the Si MOSFET results in the GaN HEMT having a significant negative gate to source voltage, thus, the 2DEG channel is pinching off. Evidently, the cascode setup generates a positive V_{TH} for regulating the GaN HEMT switch that is normally on. Additionally, normally-off GaN HEMTs with the cascode design are commercially available at 600 V [43,45]. However, the parasitic effects of the packing and the high-temperature stability of the Si MOSFETs remain significant disadvantages [47,48]. If the GaN HEMT has a relatively high on-resistance compared to the Si MOSFET, the "cascode" configuration performs well at that time. In fact, since the on-resistance increases with the rated breakdown voltage, the "cascode" approach is advantageous when the normally on GaN HEMT is one of a high-voltage, and the Si MOSFET is low-voltage [49]. As an illustration, the Si MOSFET will provide just a 3% on-resistance to a 600 V GaN HEMT "cascode". On the contrary, for a lower targeted breakdown, the on-resistance of the GaN HEMT decreases; thus, the Si MOSFETs contribution becomes significant. Hence, the "cascode" approach is practically advantageous for applications above 200 V [49].

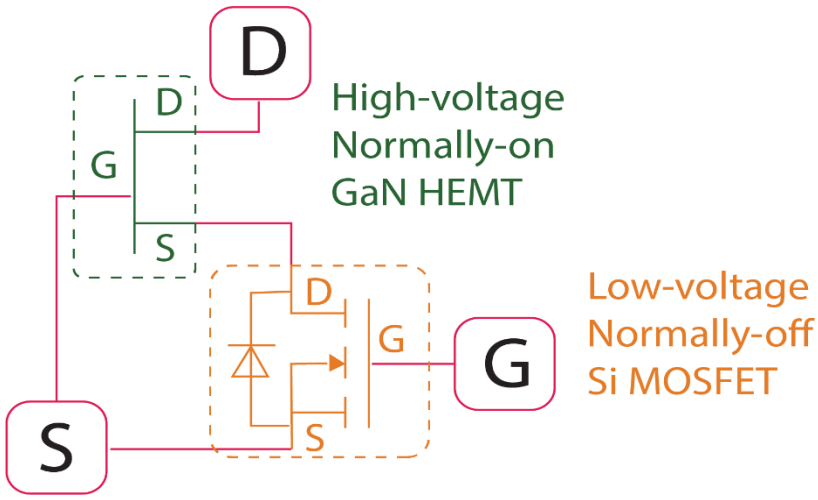
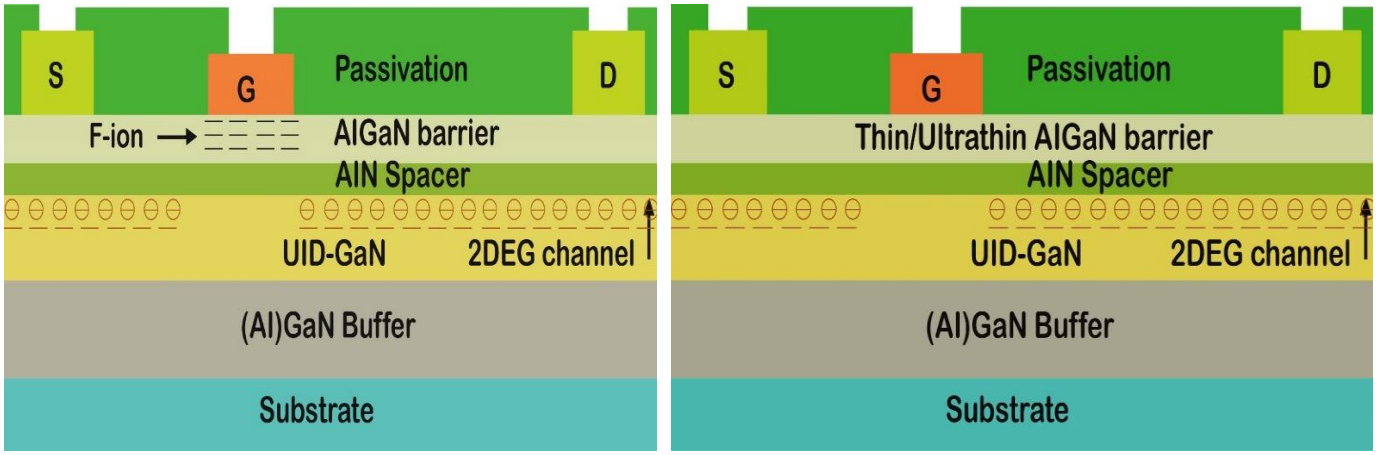


Figure 19. Normally-off HEMTs with cascode configuration structure.

3.2.2. HEMTs with Fluorine Implantation and Thin/Ultrathin Barrier (Normally off)

Figure 20a shows an alternative method of performing the normally-off operation to avoid the dry etching, which could cause damage to the device operation. Due to their considerable electron-negativity, fluorine given by the ion implantation and in the AlGaN layers may easily boost the AlGaN barrier electron potential and empty the 2DEG channel [50]. Likewise, by adjusting the height of the AlGaN conduction band, the 2DEG can be depleted by a GaN HEMT design with a thin/ultrathin barrier [51,52], as displayed in Figure 20b. When the AlGaN barrier thickness falls below a critical value, the V_{TH} shifts to a negative bias in the recessed-gate configuration. However, in various application issues, like for fluorine gates, the injection method must be repeatable, and for thin barrier HEMT designs, the output current is low, restricting these two devices [51,53].



(**a**) (**b**)

Figure 20. (**a**) Normally-off HEMTs with fluorine implantation structure.; (**b**) normally-off HEMTs with thin/ultrathin-barrier structure.

3.2.3. HEMTs with p-GaN Gate (Normally off)

A p-GaN (or p-AlGaN) layer is applied to the AlGaN/GaN heterostructure at the gate region. As illustrated in Figure 21, it is probably the most promising technique to accomplish a normally-off operation [54–56]. In fact, it is presently the only commercially available normally-off GaN HEMT technology. GaN HEMTs of this sort have received much attention from the scientific community and the industry. The p-GaN gate HEMTs working principle is generally represented in Figure 22. The AlGaN conduction band is elevated by the p-GaN cap layer on the AlGaN, resulting in 2DEG depletion. Hence, it is possible to obtain the device's normally-off mode [57]. Earlier, Uemoto et al. [55] proposed a GaN HEMT with a *p*-AlGaN gate that is normally off, with a V_{TH} of 1.0 V and a BV_{DSS} of 800 V.

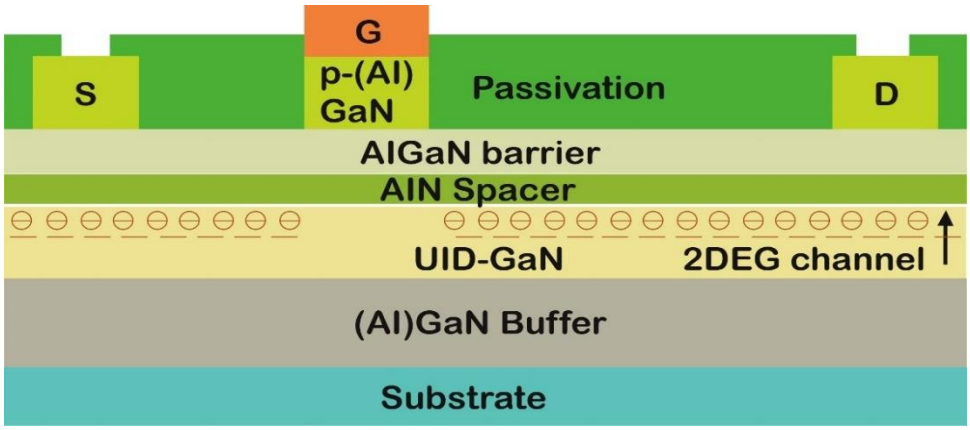


Figure 21. Normally-off HEMTs with p- GaN (or p-AlGaN) layout.

The characteristics of the AlGaN/GaN heterostructure should be specified appropriately to enable an effective depletion of the 2DEG and a high V_{TH} ($V_{TH} > 0$) [48–60]. The layer thickness of the AlGaN barrier is usually between 10 and 15 nm, whereas the content of Al is between 15 and 25%. For the effective depletion of 2DEG, a high amount of doping in the p-GaN layer (>10^{18} cm^{-3}) is frequently needed [61]. In this regard, increasing the Mg electrical activation is one of the most critical factors in improving the threshold voltage V_{TH} of the p-GaN layer for a specific Mg concentration. Adequate growth parameters for the p-GaN layer and annealing conditions may achieve the latter goal [62,63]. On the

contrary, because of the high energy of ionization (in the range from 150 to 200 m eV) of Mg as a p-type dopant, i.e., an acceptor, obtaining a high activation of Mg in p-GaN is problematic [64,65]. In most cases, an acceptor concentration of 2−−5 $\times$ 10^{19} cm^{-3} is employed, roughly two orders of magnitude more than the concentration of holes. A greater Mg concentration in p-GaN might cause the layer's crystalline quality to deteriorate, reducing the electrically active acceptors [66,67]. As a result, in the p-GaN gate HEMTs, getting a high V_{TH} is difficult. Earlier, a Pd-based Ohmic gate was implemented on the cap layer of p-AlGaN, which improved the device's hole injection and current capabilities. Therefore, the transistor was also known as a "gate injection transistor" (GIT) [55]. The GaN–GIT structure was modified to a hybrid drain-embedded GIT (HD-GIT) by Kaneko et al. [68] The Panasonic group contains a p-doped GaN area adjacent to the ohmic drain. The injected holes discharge the trapped electrons near the drain edge in the off-state from the p-GaN layer, which helps prevent the current collapse. Compared to the standard GIT structure, this new modification boosts the breakdown voltage to 850 V with a slight increase in the device's leakage current and the on-resistance of 2.6 $m\Omega \cdot cm^2$.

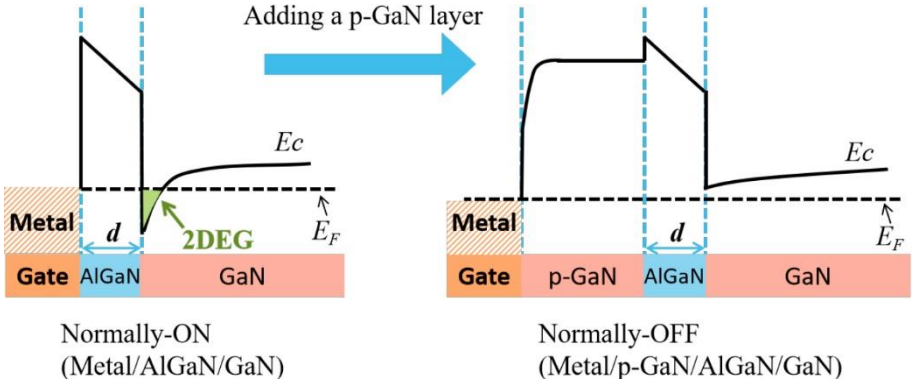


Figure 22. Metal/AlGaN/GaN energy band diagram with and without a p-GaN gate under equilibrium. Reproduced with permission [57]. Copyright 2017, Elsevier.

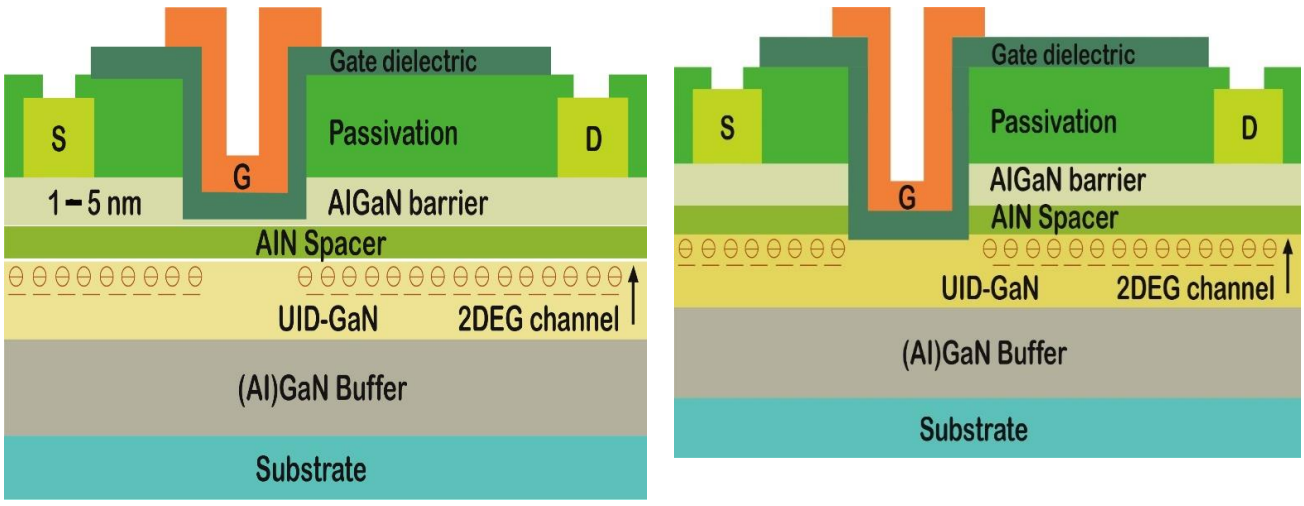
In contrast, the metal/p-GaN/AlGaN/GaN system TCAD simulations indicate that on the p-GaN, a Schottky metal gate must have a higher V_{TH} and less leakage than an Ohmic gate [55,63,64]. In the on-state, Meneghini et al. [60] demonstrated that a Schottky gate based on WSiN to the p-GaN rather than a typical Ni/Au Ohmic contact could improve the gate voltage swing of a transistor and lower the gate leakage current by roughly four orders of magnitude. Generally, the continuous power consumption of GaN HEMTs is due to the gate leakage and heat generation in the gate driver. The lack of a considerable gate side current injection due to the significant Schottky barrier is thus essential for HEMTs with a p-GaN gate for a decreased power consumption. Because of this, on the p-GaN, the Schottky gate is preferable over the Ohmic gate solution nowadays. Furthermore, several data from the literature are shown in Table 3, where some metals have been used in the Schottky gate contact to the p-GaN. Subsequently, because of its thermal and chemical durability and processing compatibility, adopting a TiN gate is now a good choice [69]. Eventually, several device and reliability difficulties still need to be investigated further, such as the low V_{TH}, high gate leakage currents, the poor gate BV, and the influence of fabrication techniques on the device's performance [57,70].

Table 3. Survey of literature data on different Schottky Contact.

Matel Gate	Doping n_{dop} and p-GaN Thickness T	V_{TH} (V)	R_{ON} (Ω·mm)	Ref
Ti $_{(40\ nm)}$/Au $_{(100\ nm)}$	$n_{dop} = 4 \times 10^{19}$ cm^{-3}, T = 100 nm	1.82	11.9	[71]
Ti $_{(25\ nm)}$/Au $_{(120\ nm)}$	$n_{dop} = 1 \times 10^{18}$ cm^{-3}, T = 70 nm	3	13.9	[72]
Ni/Au	$n_{dop} = 3.5 \times 10^{18}$ cm^{-3}, T = 50 nm	1.5	8	[73]
Ti $_{(50\ nm)}$/Au $_{(150\ nm)}$	N/A, T = 70 nm	1.2	N/A	[74]
Ni $_{(20\ nm)}$/Au $_{(200\ nm)}$	$n_{dop} = 5 \times 10^{19}$ cm^{-3}, T = 100 nm	1.5	N/A	[75]
Ni $_{(25\ nm)}$/Au $_{(200\ nm)}$	$n_{dop} = 1 \times 10^{18}$ cm^{-3}, T = 60 nm	1.7–2.1	5.65 & 5.05	[76]
Ni/Au	$n_{dop} = 3 \times 10^{19}$ cm^{-3}, T = 85 nm	1.5	29.5	[77]
Ni $_{(25\ nm)}$/Au $_{(120\ nm)}$	N/A, T = 100 nm	1.5	20	[78]
Ni/Au	$n_{dop} = 4 \times 10^{19}$ cm^{-3}, T = 70 nm	1.02	15.4	[79]
Ni $_{(15\ nm)}$/Au $_{(280\ nm)}$	$n_{dop} = 4 \times 10^{19}$ cm^{-3}, T = 70 nm	2.2	43.6	[80]
Ti/Au	$n_{dop} = 4 \times 10^{19}$ cm^{-3}, T = 85 nm	2.1	21	[81]
TiN	$n_{dop} = 3 \times 10^{19}$ cm^{-3}, T = 80 nm	1.6	17.8	[82]
W	$n_{dop} = 1 \times 10^{19}$ cm^{-3}, T = 75 nm	2.1	49	[83]
TiN	N/A, T = 60 nm	2.1	15	[62]
Pd	$n_{dop} = 3 \times 10^{19}$ cm^{-3}, T = 100 nm	1.7	8.5	[84]
Mo $_{(100\ nm)}$/Ni $_{(20\ nm)}$	$n_{dop} = 3 \times 10^{19}$ cm^{-3}, T = 80 nm	1.08	10.7	[85]
W	$n_{dop} = 1 \times 10^{19}$ cm^{-3}, T = 75 nm	1.6	26.5	[86]
Ti $_{(25\ nm)}$/Au $_{(120\ nm)}$	N/A, T = 75 nm	3.2 & 1.8	16	[87]
Ti $_{(45\ nm)}$/Au $_{(200\ nm)}$	$n_{dop} = 2 \times 10^{18}$ cm^{-3} & 2×10^{19} cm^{-3}, T = 50 nm	1.30 & 1.45	9.66 & 9.51	[88]
Ti/Au/Ni	$n_{dop} = 4 \times 10^{17}$ cm^{-3}, T = 50 nm	1.5	N/A	[89]

3.2.4. HEMTs with Recessed Gate (Normally off)

This method reduces the layer thickness of the AlGaN barrier under the gate via a plasma etching, which is the last option offered for achieving an HEMT (normally off) [90]. Because the leakage current of the gate is caused by a tunneling phenomenon that is very sensitive to the barrier layer thickness and uniformity, this approach necessitates a perfect control of the AlGaN etching process. Furthermore, etching-induced damage might increase the leakage current of the gate and non-uniformity effects in V_{TH} [91]. Additionally, there are two types of gates recessed available such as the slight MIS-HEMT of the recessed-gate design underneath the gate dielectric, a thin AlGaN barrier, and the complete MIS-FET of the recessed-gate design, known as a MOS-HFET hybrid, as shown in Figure 23a,b [92,93].



(**a**) (**b**)

Figure 23. (**a**) Normally-off HEMTs with slight MIS-HEMT of recessed-gate design; (**b**) normally-off HEMTs with complete MIS-FET of recessed-gate design.

Standard MIS-FETs may obtain an E-mode performance by entirely eliminating the AlGaN barrier layer underneath the gate, resulting in the device turning off at a zero gate voltage. Whenever the positive voltage of the gate exceeds V_{TH}, an accumulation layer of an electron forms at the interface of the gates, which operates the devices' conductive channel and is switched on. It has benefited from a high threshold voltage (V_{TH}) but suffers from a decrease in the channel mobility (μ_{FE}) due to rough surfaces in the recessed region and electrically active faults in the MIS structure. In addition, a poor channel mobility will raise the device on-resistance (R_{ON}) and system power consumption. Therefore, a slight MIS-HEMT of the recessed-gate has been offered to improve the device's channel mobility (μ_{FE}) and decline its on-resistance (R_{ON}), where the thin layer of the AlGaN barrier will hinder the 2DEG channel from the MIS interface. As a result, the channel mobility (μ_{FE}) increased and reduced the on-resistance (R_{ON}) [94]. Thus, the channel mobility (μ_{FE}) was defined as Equation (16):

$$\mu_{FE} = \frac{L_g}{WC_{ox}V_{DS}}\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) \quad (16)$$

Here, L_g and W donate the channel length and width, while C_{ox} donates the gate insulator capacitance per unit area. Moreover, Fiorenza et al. [95] have evaluated in MISHEMTs of the recessed gate the field-effect mobility by using gate insulator SiO_2 with several variables (the roughness of the surface, the temperature, the field of electric, the quality of the dielectric, and so on). This study demonstrated in the insulator/GaN system the necessity of reducing the interface state density to enhance the field effect's mobility and decrease the precise on-resistance. Eventually, these two recessed gates improved the threshold voltage, device performance, channel mobility, the reliability of the device, and overcame the gate leakage issue [96–98]. Additionally, the gate dielectric for the gate recessed depends on several characteristics, such as the permittivity, the (Al) GaN band offset, the bandgap, and the insulator chemical stability [38,94,95]. Especially for power-switching devices, a wide bandgap material is also significant. The (Al) GaN band offsets are required to reduce the gate leakage currents appropriately, even while operating the forward gate bias. On the contrary, a high permittivity value is advantageous for obtaining high transconductances [43]. In the case of MIS-HEMTs, the capacitive contribution of the gate dielectric is minimized by a high permittivity dielectric, facilitating a stronger connection between the 2DEG channel and the gate and therefore maintaining high transconductances, which is especially important for RF devices. In addition, compared to Schottky gate HEMTs, the high permittivity materials may limit the changing of the values of the threshold voltage from positive to negative of normally-on MIS-HEMTs, which helps lower the static power usage and improve the performance and the energy efficiency of the device [99].

In GaN-based insulated-gate transistors, Figure 24 demonstrates the bandgap-permittivity connection for nitride compounds and the insulators for different gate dielectrics [38,95,96]. Figure 25a illustrates that Robertson et al. [100] calculated the insulators on the GaN band offsets; they were the first to forecast the band alignment of the GaN and the insulators using charge neutrality levels (ECNL) calculations. Figure 25b shows the dielectrics on the $Al_{0.3}Ga_{0.7}N$ band offsets recently obtained by Reddy et al. [101] using the same approach. As a gate dielectric, SiO_2 on AlGaN/GaN MIS-HEMTs was first implemented by Khan et al. [102] and they noticed that it enhances the gate voltage swing capabilities and controls the leakage currents in the gates for its attractive characteristic-like large band offset to (Al)GaN, the chemical stability, and the large bandgap.

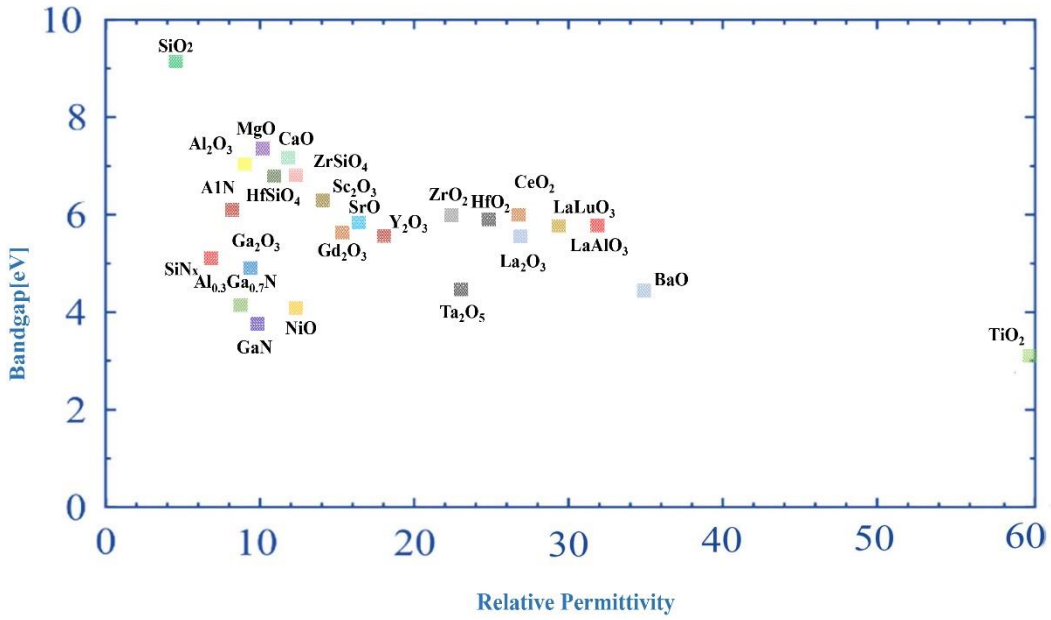


Figure 24. For primary insulators and GaN compounds, the energy bandgap (eV) vs. permittivity is shown. Reprinted with permission [42]. Copyright 2017, the author(s). Published by Elsevier.

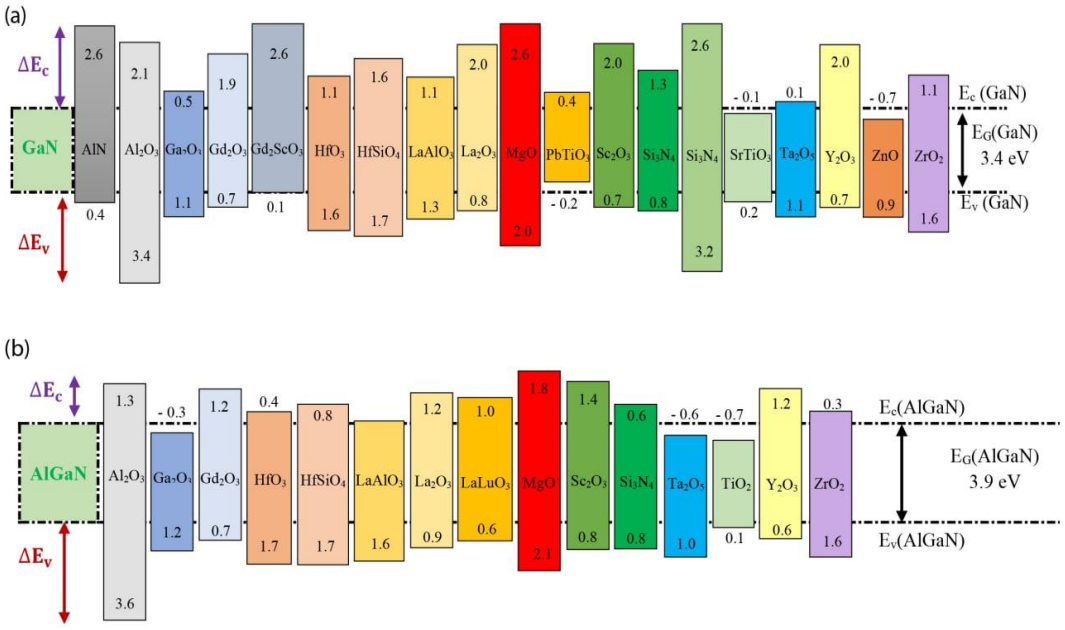


Figure 25. Various dielectric materials regarding (**a**) GaN [100] and (**b**) $Al_{0.3}Ga_{0.7}N$ [101] have different valence and conduction band offsets (ΔE_V and ΔE_C).

In contrast, for MIS gate designs utilizing dielectrics such as Ga_2O_3, SiNx, because of its small conduction band offsets, resulted in large gate leakage currents [103–105]. Likewise, the minor AlN and (Al)GaN lattice mismatch has been shown in a few investigations, whereby it is appropriate for the gate insulator and passivation layer [106,107]. Moreover, numerous high-permittivity dielectrics have been used in the MIS gate architectures of GaN HEMTs [108], including HfO_2, ZrO_2, Ta_2O_5, La_2O_3, CeO_2, and TiO_2 [109–111]. Thus, Table 4 represents the data gathered from the literature study of normally-off HEMTs with a recessed gate where several types of gate insulators (SiN, SiO_2, Al_2O_3, and processing (PECVD, LPCVD)) are shown.

Table 4. Survey literature data on difference types of gate insulators and processes.

Gate Insulator	Insulator Processing	μ_{FE} ($cm^2 \cdot V^{-1} \cdot S^{-1}$)	V_{TH}(V)	R_{ON} (Ω·mm)	On/off Ratio	G_m (mS/mm)	Ref
$SiN_{(30\ nm)}/SiO_{2\ (3\ nm)}$	SiO_2ALD + post annealing at 890 °C in N_2 + SiN LPCVD at 665 °C	116	2.4	15.9 Ω·mm at V_{GS} = 12 V	6×10^8	52	[112]
$SiN_{(100\ nm\ and\ 300\ nm)}/ZrO_{2(23\ nm)}$	SiN PECVD + ZrO_2 ALD at 200 °C	850	2.19	9.2 Ω·mm at V_{GS} = 8 V	~10^9	135	[113]
$SiO_{2\ (50\ nm)}$	PECVD + post annealing at 850 °C in N_2	110	0.7	N/A	N/A	N/A	[95]
$Al_2O_{3\ (25\ nm)}$	ALD + TMA and ozone	N/A	5	12.9 Ω·mm at V_{GS} = 19.7 V	N/A	44	[114]
$HfO_{2\ (13\ nm)}$	ALD+ ozone	1482	3.1	6.0 Ω·mm at V_{GS} = 8 V	10^5	N/A	[115]
$Al_2O_{3\ (15\ nm)}$	ALD+ ozone	1991	2.6	5.5 Ω·mm at V_{GS} = 8 V	10^5	N/A	[115]
$SiN_{\ (2\ nm)}/SiN_{\ (15\ nm)}$	LT- PECVD at 850 °C + HT-LPCVD at 780 °C	160	2.37	13.2 Ω·mm at V_{GS} = 15 V	N/A	17	[116]
$SiN_{\ (15\ nm)}$	HT-LPCVD at 780 °C	38	1.28	20 Ω·mm at V_{GS} = 15 V	N/A	2	[116]
$TiO_{2(3.4\ nm)}$	Thermal oxidation	1270	4.2	N/A	2.3×10^8	N/A	[110]
$Al_2O_{3\ (25\ nm)}$	ALD + post annealing at 830 °C in N_2	2033	2.5	6.8 Ω·mm at V_{GS} = 12 V	10^8	92	[117]
$SiN_{\ (20\ nm)}$	LPCVD on photo-electrochemical recess	49	0.8	26 Ω·mm at V_{GS} = 15 V	N/A	2	[118]
$SiN_{\ (15\ nm)}$	SiN LPCVD at 780 °C	141	1.3	12 Ω·mm at V_{GS} = 15 V	N/A	13	[118]
$SiN_{\ (30\ nm)}/AlN_{\ (5\ nm)}$	AlN PEALD + SiN LPCVD	198.80	6.28	11.62 Ω·mm at V_{GS} = 15 V	10^8	85.75	[119]
$HfO_{2\ (20\ nm)}$	ALD + post annealing at 600 °C in N_2	N/A	2.5	3.8 Ω·mm at V_{GS} = 6.5 V	2.1×10^9	81.38	[120]
$Al_2O_{3\ (30\ nm)}$	ALD + post annealing at 850 °C in N_2	1602	2.6	10.2 Ω·mm at V_{GS} = 10 V	N/A	58	[121]
$AlN_{\ (7\ nm)}/SiN_{\ (7\ nm)}$	MOCVD	180	1.2	N/A	(5−−6) × 10^8	60	[122]
$Al_2O_{3\ (4\ nm)}$	ALD + post annealing at 900 °C in O_2	1450	1.55	7.1 Ω·mm at V_{GS} = 12 V	N/A	54	[123]
$SiNx_{\ (20\ nm)}/SiON_{\ (10\ nm)}$	SiON PECVD at 350 °C in SiH_4, NH_3, N_2O, and N_2 atmospheres + SiNx LPCVD at 780 °C with an ammonia flow of 280 sccm, a SiH_2Cl_2 flow of 70 sccm.	1793	0.81	31.2 Ω·mm at V_{GS} = 12 V	N/A	N/A	[124]
$Al_2O_{3\ (18\ nm)}$	ALD + post annealing at 400 °C in N_2	65	7.6	19.5 Ω·mm at V_{GS} = 14 V	N/A	N/A	[125]
$Al_2O_{3\ (30\ nm)}$	ALD + post annealing at 850 °C in N_2	1670	0.53	24.4 Ω·mm at V_{GS} = 10 V	~10^8	42	[126]
$Al_2O_{3\ (5\ nm)}/SiN_{\ (7\ nm)}$	SiN LPCVD at 780 °C	122	1.7	12.9 Ω·mm at V_{GS} = 18 V	~10^8	53	[127]
$NiO_{x(100\ nm)}$	Sputtering	N/A	0.45	9.42 Ω·mm at V_{GS} = 4 V	10^8	~75	[128]
$SiO_{2\ (20\ nm)}$	ALD + post annealing at 780 °C	1700	1.56	7.4 Ω·mm at V_{GS} = 6 V	10^{10}	190	[129]
$Al_2O_{3\ (20\ nm)}$	ALD + post annealing at 900 °C in N_2	245	5	N/A at V_{GS} = 12 V	10^{10}	19	[130]
$Si_3N_{4\ (10\ nm)}/TiO_{2\ (20\ nm)}$	SiN PECVD + TiO_2 ALD	1200	1.81	43.81 Ω·mm at V_{GS} = 10 V	N/A	112	[131]

Subsequently, the AlGaN thickness is another important factor for the threshold voltage (V_{TH}). Medjdoub et al. [132] had shown the relation between the AlGaN thickness with a threshold voltage. From Figure 26a, notice that if the AlGaN thickness (t_{RA}) reduces, the V_{TH} increases. Similarly, other authors, Saito et al. [133], presented the relationship between the V_{TH} and the specific on-resistance ($R_{on}A$) by calculating the equation, as displayed in Figure 26b. On the contrary, the on-resistance ($R_{ON}A$) will be increased if the 2DEG mobility is decreased. Thus, from Figure 26b, the equation for calculating the specific on-resistance ($R_{on}A$) is denoted by Equation (17),

$$R_{on}A = \left(R_{gs} + R_{ch} + R_{gd} + 2R_{con}\right) \times \left(L_{gs} + L_{ch} + L_{gd} + 2L_{con}\right) \quad (17)$$

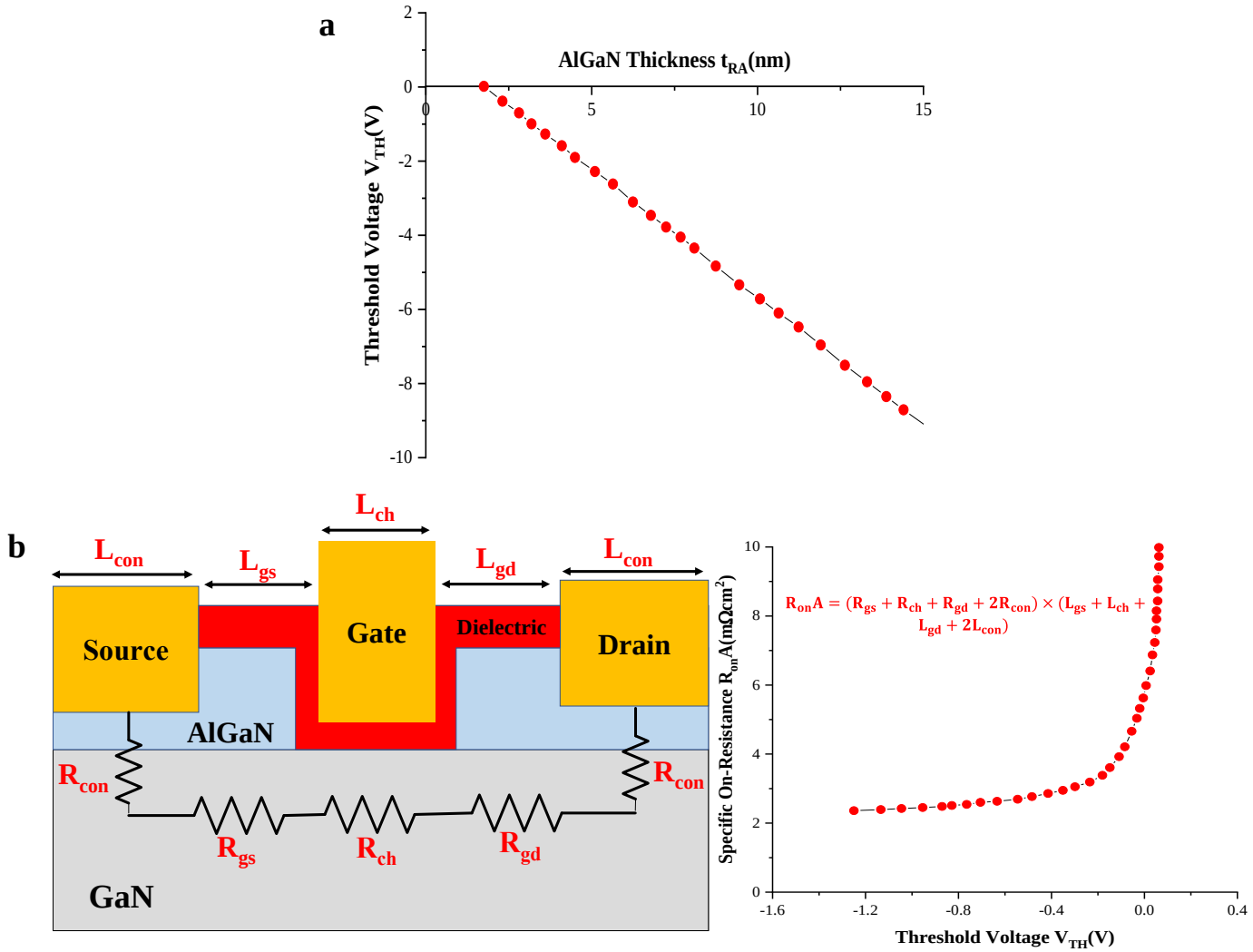


Figure 26. (**a**) The AlGaN layer thickness and gate threshold voltage relation. (**b**) In the recessed-gate GaN HEMT, the calculation of specific on-resistance and the relation between the threshold voltage and the specific on-resistance. Reprinted under the open access policy from Bentham Open [132].

Additionally, the field plate has used a device structure to reduce the current collapse. For GaN-based devices, current collapse is a well-known phenomenon that results in a trade-off between the breakdown voltage and the on-resistance by inserting the source-gate field plate; the electric field at the gate-drain edge is redistributed [134–136], as shown in Figure 16. The current collapse is discussed in the below segment.

4. Reliability of GaN HEMTs

4.1. Degradation Creation

While GaN HEMTs have improved remarkably, several material-related challenges must be resolved before they are revealed as a reliable and sustainable technology. AlGaN/GaN HEMTs' actual device performance has not yet reached the theoretically predicted levels. Even on unaged GaN HEMTs, parasitic effects could be noticed that degrade the performance metrics but do not significantly impact the reliability. Nevertheless, over time or under aging stresses, the degradation processes that accelerate with time impair not only the electrical response but also the device's resilience and dependability, resulting in shorter lifetimes and failure. The GaN industry's principal aim is to improve the dependability of its products while also reducing the parasitic effects. Further degradation

difficulties with GaN devices include thermal mismatches, heteroepitaxy, and polarization effects with the substrate, all of which are inherent to the material. Compared to other conventional technologies, AlGaN/GaN HEMTs can work at an extremely high bias, electric fields, and temperatures. Figure 27 demonstrates the various types of degradation affecting AlGaN/GaN HEMTs [137,138].

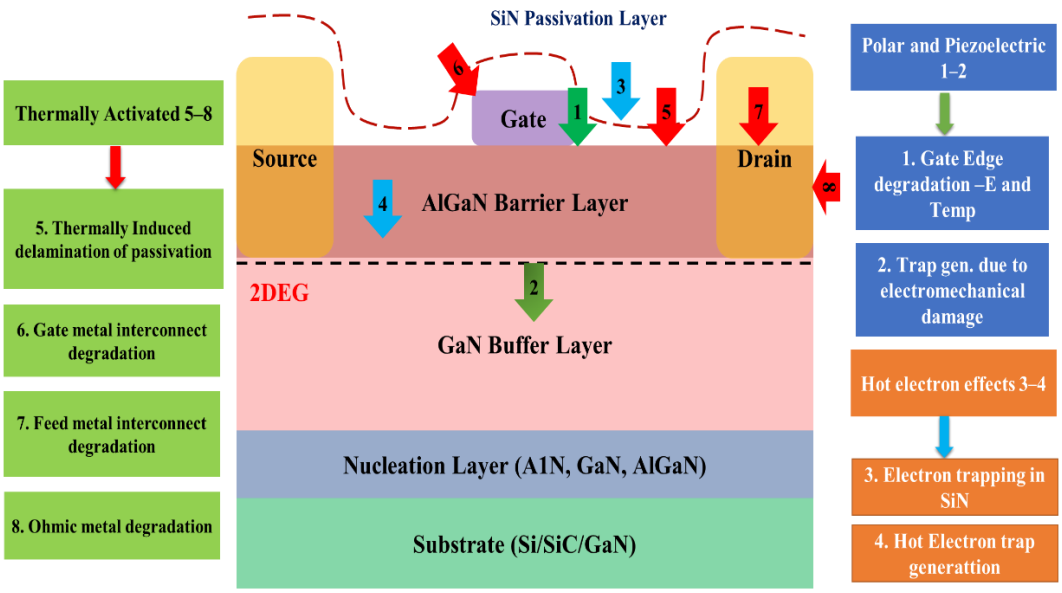


Figure 27. Several degrading problems affect AlGaN/GAN HEMTs with their origin. Reprinted with permission [138]. Copyright 2010, Cambridge University Press, and the European Microwave Association.

It is important to note that five to eight issues are associated with thermally induced degradation processes that have already been reported in other semiconductor systems (SiC, GaAs, Si, etc.). As a result, these failure mechanisms are simpler to explain and exclusive to the metallization scheme which has been adopted. Both three and four mechanisms are connected to the introduction of the hot electrons; it is a usual problem that field-effect transistors of a high voltage face. Other semiconductor devices have been proven to suffer from a deterioration, caused by hot electrons (Si, GaAs, InP, etc.). On the other hand, because of this semiconductor material's piezoelectric and polar properties, one to two issues are specific for GaN devices; consequently, those processes have not been fully defined or investigated. As a result, the GaN HEMT reliability analysis is a unique issue that needs to be devoted, as well as an in-depth physics-based study. Furthermore, high Schottky-gate leakage currents are also one of the main issues for degrading the device performance and reliability. Thus, the reduction in BV_{GD} raises the noise figure (NF) and decreases the power-added efficiency (PAE) due to the high gate leakage current [139]. In addition, there are numerous mechanisms of gate leakages, including the emission of a thermionic field [140], the emission of thermionic [141], the dislocation-assisted tunnelling [142], the trap assisted tunnelling [143], the Fowler–Nordheim tunnelling [144], the defect hoping [145], the space charged limited current [146], and the Frenkel–Poole emission [147].

4.2. Reliability Issues

These days, researchers focus on enhancing the AlGaN/GaN HEMTs reliability device because of the trapping effect during the AlGaN/GaN HEMT operation. One of the major obstacles causing performance degradation is the trapping effects in AlGaN/GaN HEMTs during operation, causing current dispersion between DC to RF or otherwise, DC to pulsed $I_D - V_D$ characteristics. Trapping effects like the frequency dispersion of transconductance,

the sensitivity of the light, the drain lag and gate lag transients, and the limited microwave power output have all been detected [148].

As shown in Figure 28, there are various trapping mechanisms usually seen in AlGaN/GaN HEMTs, such as:

- Under a high negative VGS, barrier traps and a gate electron are injected onto the surface;
- Under a high on-state VDS, the barrier/buffer traps are injected using hot electrons;
- During material growth, the electrons captured by the deep layers are induced.

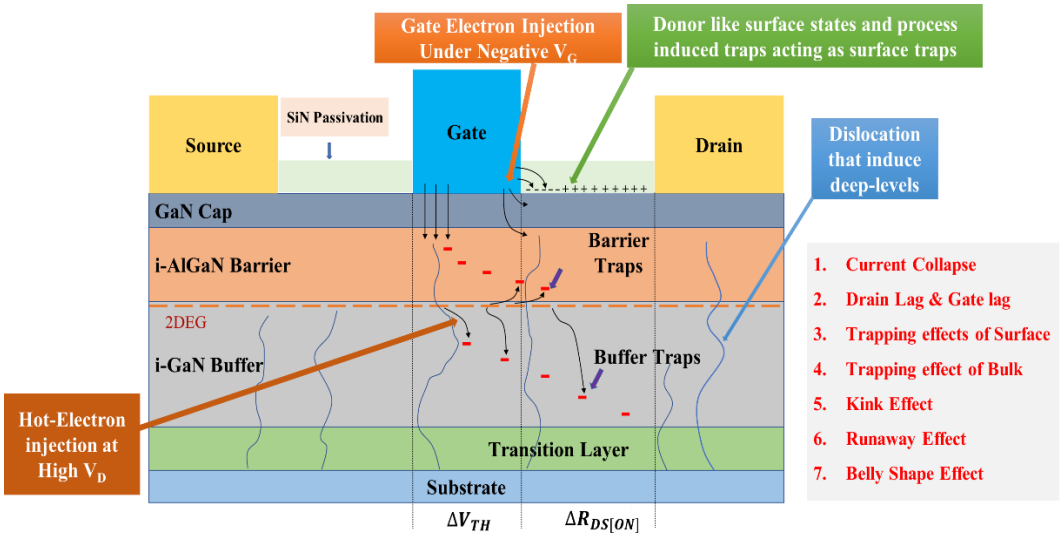


Figure 28. The AlGaN/GaN heterostructure is shown schematically, with several trapping methods and their effects on device performance. Reprinted with permission [149]. Under the terms of the Creative Commons Attribution 4.0 license.

4.2.1. Current Collapse

In order to maintain the charge neutrality, trapping electrons reduces in the 2DEG channel the density of the sheet carriers, resulting in a decreased current density in the drain. This decrease in the drain current is referred to as the "current collapse". M. A. Khan et al. [150] released the first article on AlGaN/GaN HFETs current collapse in 1994. The "drain-lag" and "gate-lag" conditions of the quiescent bias (Q-bias) are the main parameters used to characterize the current collapse phenomena [148]. In Figure 29, the characteristics curve of I_D–V_D demonstrates the current collapse's effect on the output power of HEMT. The solid and dotted lines indicate the device's I_D–V_D characteristics curve before and after the current collapse phenomena. The current collapse causes the knee voltage (V_{knee}) to grow as the maximum current decreases (I_{Dmax}). It reduces the maximum output power (P_{max}) that may be achieved, which is provided by the given equation:

$$P_{max} = \frac{(\Delta V_D \times \Delta I_D)}{8} \quad (18)$$

The dissimilarity between the V_{knee} and the breakdown voltage (BV_{GD}) equals the highest possible voltage swing (ΔV_D). I_{Dmax} specifies the maximum current swing. P_{max} is depicted in Figure 29 by the shaded region, and the current collapse phenomena have narrowed this operating window. Thus, the main reason for the current collapse is caused by the reduction in positive charges of polarization induced from the heterojunction transistor surface, followed by the loss of an equivalent number of electrons in the 2DEG [151]. $\Delta R_{DS[ON]}$ characterizes the current collapse, as illustrated in Figure 29, because the electrons are trapped in the gate-drain access area by the surface, buffer, or barrier traps. Similarly,

under the gate are the areas of electron trapping (see Figure 28), resulting in a threshold voltage shift (ΔV_{TH}), which characterizes a current collapse; therefore, the pulsing I_D–V_D characteristics are caused by a drop in the drain current in the device's saturation zone, as seen in Figure 29.

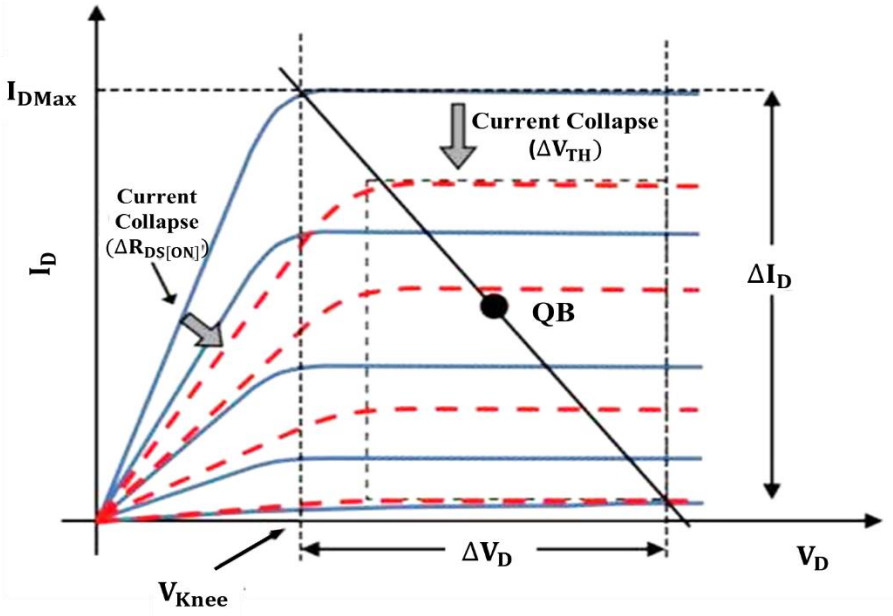


Figure 29. The I_D–V_D characteristics curve of HEMT before (solid lines) and after (graded lines) current collapse is shown in this diagram. Reprinted with permission [152]. Copyright 2003, the American Vacuum Society.

4.2.2. Drain and Gate Lag

The gate lag refers to the drain current's transient response to the gate voltage, and a drain lag is the transient response of the drain current to the drain voltage, which remains constant when the drain or gate voltage matches. According to Figure 30, Zhang et al. [153] investigated the magnitudes of collapse between the saturation and the knee voltages for the various quiescent biases. Hence, the collapse considerably reduces the performance near the knee voltage. From curve (a), when V_{DS} = 4.5 V, the collapse percentage was 4.2 and 9.8, respectively, with the Al/SiN passivation layer. On the contrary, the collapse rate increased by a 5.5 and 13.8 percentage, with the SiN passivation layer at the V_{DS} = 5 V, approximately, on the curve (b).

However, the effects of acceptor- and donor-like traps on the HEMT device were analyzed by Tirado et al. [154] The accumulating hole near the surface counteracts the acceptor-like traps, and the device is insensitive to the acceptor-like traps. Therefore, the surface donor-like traps are the primary cause of the gate lag [155]. Figure 31a presents that in addition to the dipole charge owing to polarization-induced charges, the charge due to 2DEG, the charge due to the donor-like trap ionization, and the charge due to the holes accumulating close to the AlGaN surface, the filling and emptying of the donor-like traps in the surface can impact the density of the 2DEG. When a new device is strained, the electrons that directly tunnel through the Schottky gate contact can occupy the donor-like traps and turn them neutral [156]. The 2DEG density is dropped with the reducing donor-like traps due to the charge neutrality criteria, which causes an initial fall in the current in Figure 31b [154], where the drain current instantly rises as the on-state remains stable for a while. After that, until saturation, its soars again. At the final stage, the drain current change is referred to as the delay of the current, known as a gate lag.

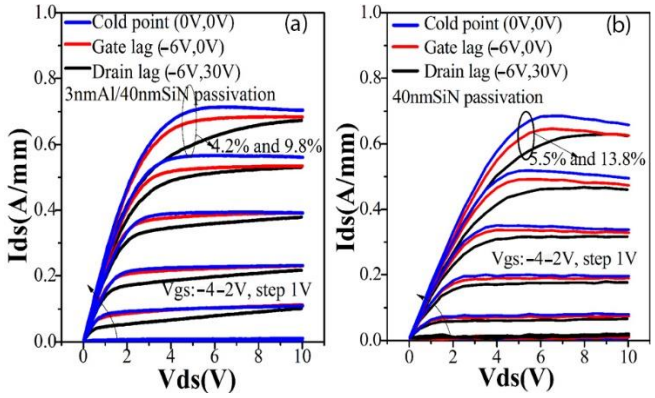
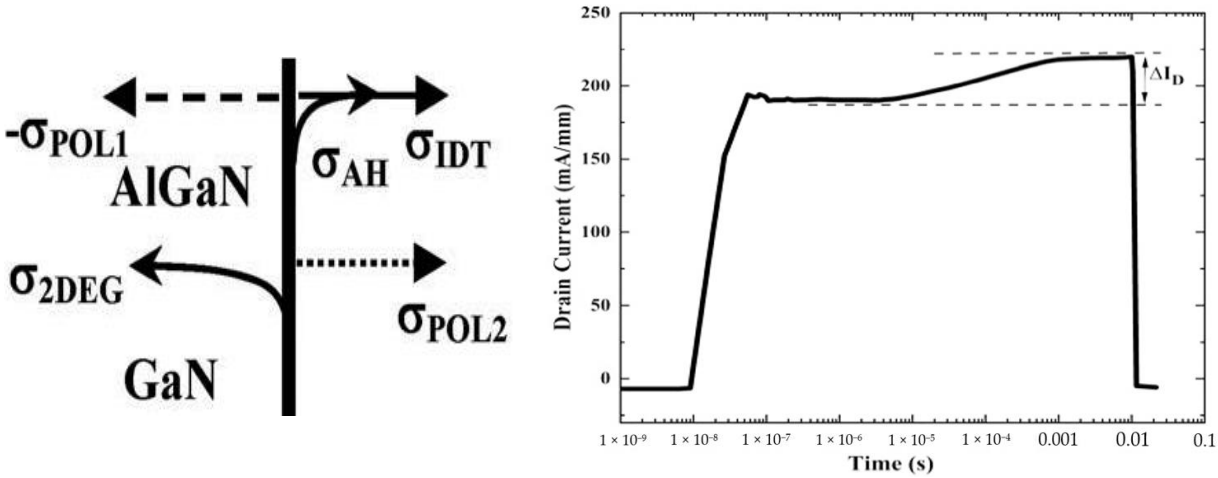


Figure 30. The gate lag and drain lag of (**a**) Al/SiN passivated and (**b**) SiN passivated AlGaN/GaN HEMT devices were measured at different passivation layers. Reproduced with permission [153]. Copyright 2019, the author (s), published by AIP Publishing.



(**a**) (**b**)

Figure 31. (**a**) Diagram of an HEMT device's space charge element. The two-dimensional electron gas is referred to as σ_{2DEG}, the dipole charge induced by polarization is denoted by $\pm$ $\sigma_{POL1,2}$, Ionized donor-like traps are referred to as σ_{IDT}, and σ_{AH} symbolizes the accumulation of holes near the AlGaN surface. (**b**) AlGaN/GaN HEMT gate lag phenomenon's transient waveform of the drain current. Reproduced with permission from IOP Publishing [154].

When measured at the turn-on pulsing mode, the observed drain current tends to reduce with time, as shown in Figure 32a. When evaluated at the turn-off pulsing mode, Figure 32b indicates a decline in the drain current when the voltage at the drain returns to 0 V. These two varieties of the drain current curves are frequently referred to as the drain lag [157]. Due to the trapping of the electron in the channel, this current reduction occurred. Some electrons might tunnel through the AlGaN barrier while the device is in the on-state and trapped by deep-level traps. Eventually, to overcome these issues, the passivation layer and field plate had to be used on the device, as presented in Figure 16.

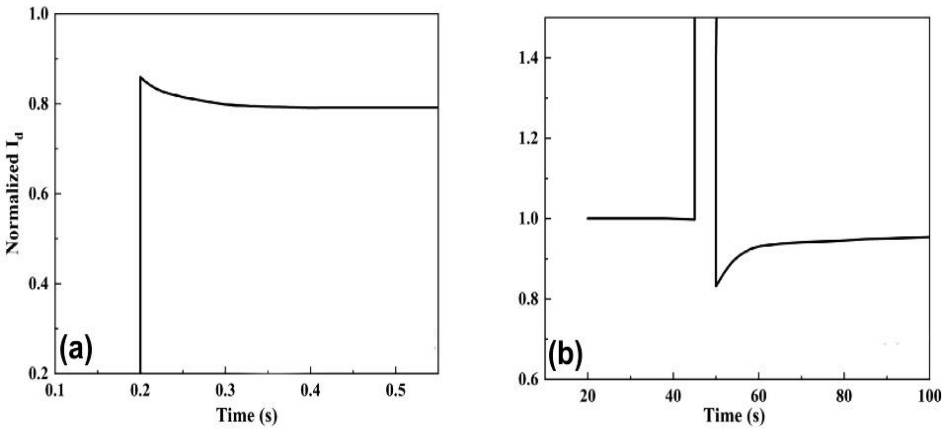


Figure 32. For AlGaN/GaN HEMTs, the transient waveform of the drain current from the drain lag phenomena. (**a**) turn-on pulsing mode (**b**) turn-off pulsing mode. Reproduced with permission [157]. Copyright 2009, the author (s), published by AIP Publishing.

The gate lag measurements compare the prompt and steady-state I_D at a constant low field drain voltage (avoid self-heating contributions) while the gate bias is modulated from a quiescent point, usually below the pinch-off voltage ~V_G = −6 V, to an open channel condition such as V_G = 0 V. At the pinch-off, a high amount of channel electrons are trapped in bulk or surface states, which do not immediately feed back into the channel instantaneously when the gate turns on. With the large-signal recovery time of constants up to the order of seconds, the responsible traps must have a significantly large activation energy and/or be fed by a "slow" conducting mechanism (like hopping) to explain the long time constants. The surface states are believed to dominate in the gate lag since the passivation significantly improves the current response.

For the drain lag measurements, the gate voltage is kept constant at around 0 V, while the drain voltage is shifted from a low equilibrium value of ~10–100 mV to a higher value of 15–30 V. The buffer traps are reported to be dominant here since the devices with higher buffer layer conductivities display lower drain lag ratios. High-drain biases inject electrons into the buffer, where they stay trapped. The passivation has a minimal effect, and the hot electrons can contribute significantly. The recovery time is often in minutes, and the reduction in the knee voltages and $I_{D,max}$ is amplified. The threshold shifts associated with the current collapse are also accounted for with the drain lag effect.

4.2.3. Trapping Effects of Surface

In GaN HEMTs, the effects of surface trapping are commonly used to describe electron trapping on the AlGaN barrier surface. R. Vetury et al. [158] utilized the "virtual gate" idea to describe the current dispersion because of surface trapping on the ungated surface between the drain and gate contacts under negative V_{GS} and a positive drain bias. Thus, Figure 33a illustrates that, at first, due to the presence of a momentous initial drain current, the 2DEG channel must remain in the slot region; from the bilateral metal gates to the AlGaN surface in the slot area, the electrons are injected and captured by the surface states when the off-state gate voltage is applied. Afterwards, from both the bilateral gate edges to the middle of the slot region, the negative trapped surface charges steadily deplete the 2DEG conduction channel, which, acting as a "virtual gate" on both sides, converges at the middle of the slot region, and the entire 2DEG channel in the slot region becomes wholly depleted. Eventually, it has gradually become a complete "virtual gate", as presented in Figure 33b [159].

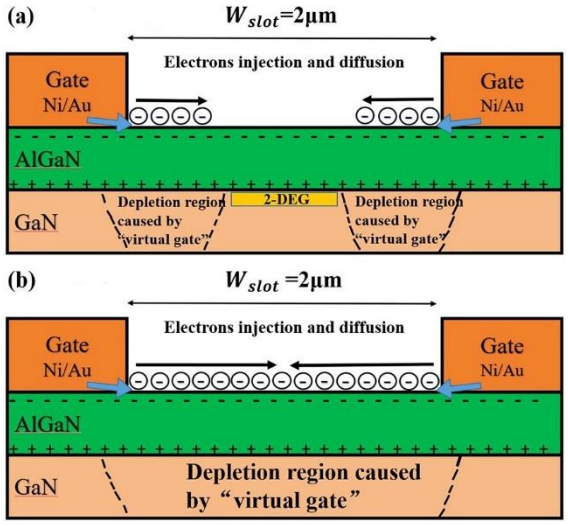


Figure 33. The device layout illustrates (**a**) electron injection in the slot region and the virtual gate in both areas. (**b**) the devices become fully virtual gates. Reproduced with permission [159]. Copyright 2019, the author (s), Published by AIP Publishing.

The impact of the virtual gate on the sheet carrier density is observed in Figure 34 [160], where the increased drain voltage at the gate edge of the drain side causes a linear reduction in the sheet carrier density. For this reason, electrons accumulate at the drain side's gate edge. Consequently, this accumulation of electrons not only influences the channel but also extends towards the lateral axis of the device, for instance, extending the depletion from 1.1 μm to 1.2 μm for the drain voltage from 0 V to 25 V.

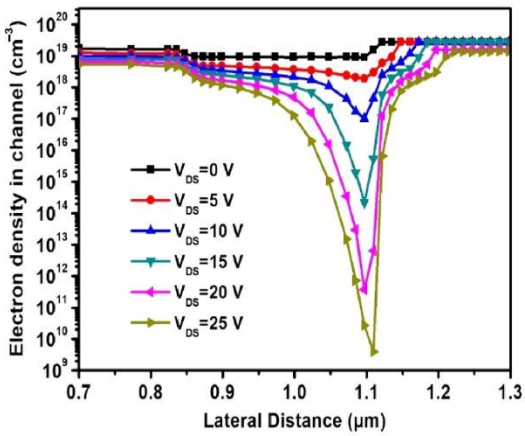


Figure 34. AlGaN/GaN HEMT sheet carrier density along the channel for different drain voltage. Reproduced with permission [160]. Copyright 2021, Elsevier.

4.2.4. Trapping Effect of Bulk

Bulk traps are traps of electrons which are found in the GaN buffer, AlGaN barrier, or other parts of the device heterostructure, as shown in Figure 27. J. Joh et al. [161] also reported that the injection of an electron into the bulk traps from the gate induced the bulk trapping effect to occur. Thus, X. Zheng et al. [162] illustrated that varying the V_{GS} has bulk trapping effects on the AlGaN barrier traps (TP2) and the GaN channel layer traps (TP1), presented in Figure 35. However, from the gate current (I_G), TP2 can capture more electrons if the V_{GS} increases the negative bias voltage. TP2s electron trapping reduces the channel carrier concentration, which lowers the drain current. Additionally, the trapping process of TP2 is speeded up by a higher negative bias voltage of V_{GS}, which decreases the

action time of TP2. Meanwhile, TP1 is insensitive to the change in $V_{GS,}$ causing little effect on TP1. Eventually, it is observed that the V_{GS} effect on TP1 is less than on TP2.

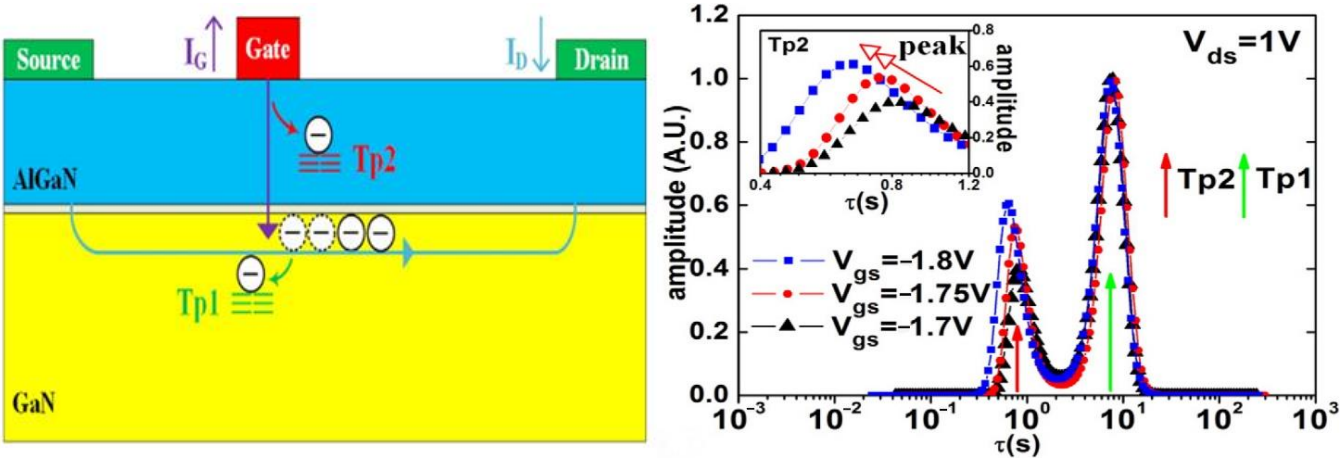


Figure 35. Trapping process of TP1 and TP2 with various values of V_{GS}. Reproduced with permission [162]. Copyright 2016, Elsevier.

P.V. Raja et al. [163] analyzed the buffer trapping effects on the AlGaN/GaN HEMT device. For the gate lag transient, the V_{GS} pulsed from −3 V to 0 V (from the off- to on-state) with a fixed V_{DS} = 10 V. The gate lag transient is simulated by changing the density of the buffer trap, N_{TB} (from 5×10^{16} to 5×10^{17} cm^{-3}), with a fixed electron trap at $E_{TB} = E_C - 0.47$ eV and an electron capture cross-section $\sigma_{nB} = 7 \times 10^{-17}$ cm^2. As a result, by increasing the N_{TB}, the signal magnitude of the gate transient is reduced, but variations of the transient are unchanged, as presented in Figure 36a. On the contrary, the V_{GS} remains at 0 V, and the V_{DS} is switched from 2 V to 10 V in the drain lag transient. The parameters of N_{TB} and σ_{nB} remain the same on the buffer trapping. Consequently, reducing the magnsitude of I_{DS} does not affect the current dispersion behavior, as displayed in Figure 36b.

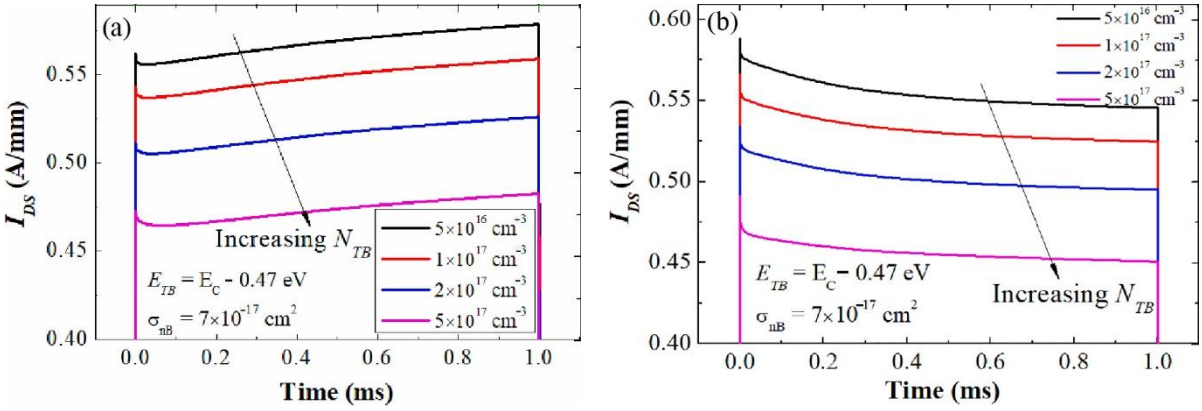


Figure 36. By varying buffer trap density, transient response of (**a**) gate lag and (**b**) drain lag are observed. Reproduced with permission [163]. Copyright 2021, Elsevier.

4.2.5. Kink Effect

The kink effect refers to the output I–V characteristics of an undesirable change phenomenon caused by changes in the conductivity of the drain [164]. This is determined by the working point of the device, as well as the temperature, voltage, and current. As is evident in Figure 37, lengthy integration durations while comparing the output characteristics were achieved with a downward and upward V_{DS} pumping. When the V_{DS}

is pushed down from a high value, the drain current drops at the V_{DS_kink} position, but it reappears when the V_{DS} is pumped up. As a result, the lower g_d is due to trapping the states and is connected among the source and drain electric field. This is also supported by the fact that the magnitude of the kink is unaffected by the running V_{GS} value, demonstrating that a large drain current is not required for a trap filling. The kink phenomenon has threshold characteristics related to the V_{DS_kink}. There is no kink in the I_{DS}. if the $V_{DS.max}$ does not exceed the V_{DS_kink}. As the gate voltage (V_{GS}) is increased from 0 V to $V_{GS.max}$, the nonmonotonic behavior of the V_{DS_kink} is noticed. In the region of a relatively high V_{GS}, the V_{DS_kink} rose with V_{GS}. Nevertheless, the V_{DS_kink} rose when V_{GS} reduced in the near pinch-off zone. The inset figure demonstrates the nonmonotonic behavior of the kink voltage (V_{DS_kink}) when the V_{GS} is stepping from 10 V to 0 with $\Delta V_{GS} = -0.2$ V. Each sweep of V_{DS}, is followed by a 5 min rest [165].

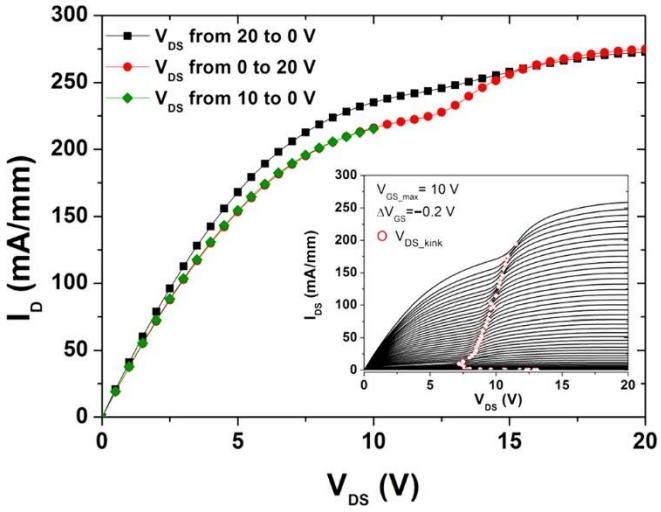


Figure 37. The kink effect in the I_D is clearly observed with a strong dependence on the V_{DS} sweep direction. Reproduced with permission [165]. Copyright 2016, the author(s), published by the American Vacuum Society.

4.2.6. Runaway Effect

When the drain voltage is raised in the saturation regime, the runaway effect occurs, defined by a simultaneous increase in the drain and gate currents [166,167]. Usually, the gate-to-drain diode component dominates the gate leakage, which rises as the V_{DS} approaches the threshold. The gate leakage is projected to decrease when the V_{GS} is minimized. As shown in Figure 38, the absolute gate current in the runaway mode is larger for the lower V_{GS} levels. After the runaway-inducing aging testing, the reliability characterizations might be severely detrimental since a continuous rise in the I_G and I_D could result in catastrophe failures, turning the runaway into an end-of-life mechanism. For the runaways, the significant drain and gate voltage will be noticed. Under open channel situations, the runaway shifts to a lower V_{DS} and greater negative V_G values. Lower activation voltages result from higher temperatures and longer aging durations. According to conduction mechanism research, the runaway seems to be linked to the Fowler–Nordheim tunnelling process.

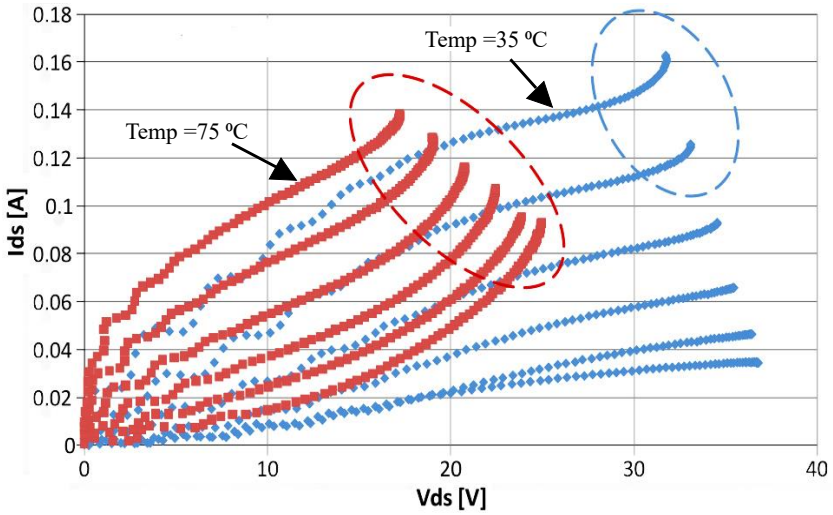


Figure 38. Output characteristics of the device reveal a runaway mechanism on the ellipse area with different temperatures. Reproduce with permission [167]. Copyright 2012, Elsevier.

4.2.7. Belly Shape Effect

According to Brunel et al. [168], after the HTOL or HTRB reliability testing, the electrical parasitic phenomena known as the belly shape effect (BS) in which on the Schottky forward characteristic, an excess of the gate leakage current resembling a "belly shape" character is noticed [168,169]. Figure 39 shows a standard belly shape. After just a few hours of aging, a belly shape forms, with varying magnitudes during the aging process, indicating degradations due to variations in the epitaxial layers, metal, or surface states. Nonetheless, the mechanics of its development are still unknown, and additional research is needed to address the dependability manifestations. Without compromising the overall dependability, it may result in high leakage currents for fascinating research on the situation and internal physics.

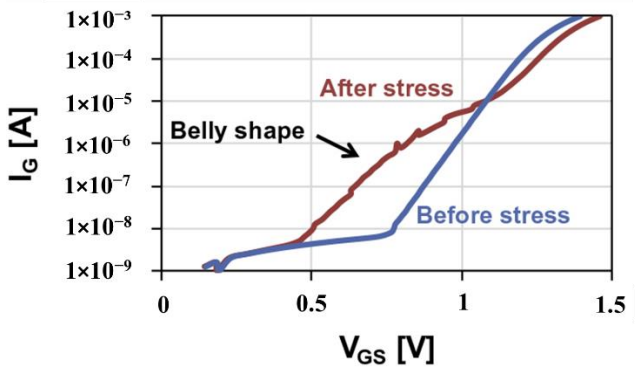


Figure 39. Before (**blue**) and after (**red**) 4000 h of HTRB stress, the forward characteristics of an HEMT with BS are shown. Reproduced with permission [168]. Copyright 2013, Elsevier.

4.3. Breakdown Voltage in GaN HEMTs Device

Gallium nitride transistors are expected to play an essential role in the next-generation power converters, thanks to the high expected breakdown voltage, which is a direct consequence of the high breakdown field of GaN (>300 V/µm). Thus, in switching the operation, the transistors alternate between the on-state, where the gate opens the channel and allows the carriers to flow through the device, and the off-state, where the gate closes the channel and blocks the carriers' current. At the off-state, the gate potential, V_{GS}, is lower than the device's threshold voltage, V_{TH}, and is considered a subthreshold condition. For

an efficient switching, the off-state operation point conditions should be at a high positive drain voltage and negligible drain current; therefore, a strong gate-blocking capability is required. At very high positive drain voltage conditions, the blocking capability of the device degrades and gives rise to the subthreshold leakage (STL) current. The subthreshold leakage current will increase and become significant, thereby reducing the efficiency of the switching. A significant leakage current is three orders of magnitude lower than the device's maximal output current. At high voltages, currents higher than this value may initiate destructive processes in the device; therefore, it is considered the starting point of the device breakdown. In most cases, the breakdown voltage is either the sub-threshold drain leakage, or the gate leakage increases above 1 mA/mm.

The main physical reasons for sub-threshold current leakages (STL) increased at a higher drain bias voltage are sketched in Figure 40. The STL has to be taken into account for a high voltage GaN device engineering and it is explained as follows:

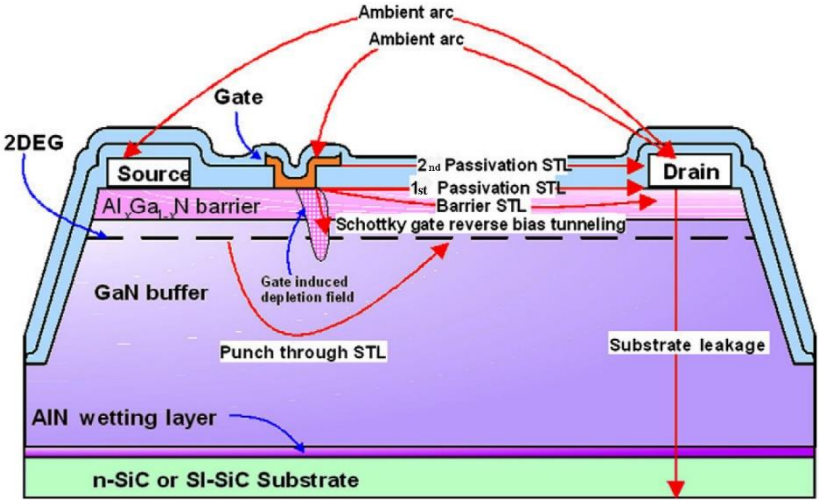


Figure 40. Illustration of most important sub-threshold current leakages (STL) and breakdown paths might appear during high voltage in GaN-based HEMTs. Reproduced with permission [170]. Copyright 2011, Elsevier.

First, the electrons punch through in the buffer underneath the gated channel region [171]: this effect depends on the magnitude of the vertical electric field in the gate region and the ability of the buffer structure to confine electrons to the channel, as shown in Figure 41a. Second, the Schottky gate reverses the bias tunnelling: this originates from the drain side edge of the gate and is triggered by the high electric fields present in this particular device region, as displayed in Figure 41b. Third, Figure 41c presents the vertical device breakdown or the substrate leakage across the epitaxial layers to the conductive substrates such as n-SiC or Si: this is mainly an issue of the buffering technology and can be prevented by suitable epitaxial concepts [171]. High-voltage GaN devices place very stringent demands on high-voltage buffer structures since, in most cases, these devices are fabricated on conductive substrates (Si, n-SiC) which are usually connected to either the drain or the source terminal of the power devices. Fourth, surface-related breakdown: this is mainly associated with the quality of device passivation, whether the interface is between the passivation layers or the semiconductor surface itself, as indicated in Figure 41d. Finally, an ambient arcing between the closely spaced device electrodes may also occur if the devices are operated in the air. Thus, this has to be taken into account by the device layout design, the technology, and design of the passivation, and also the device packaging.

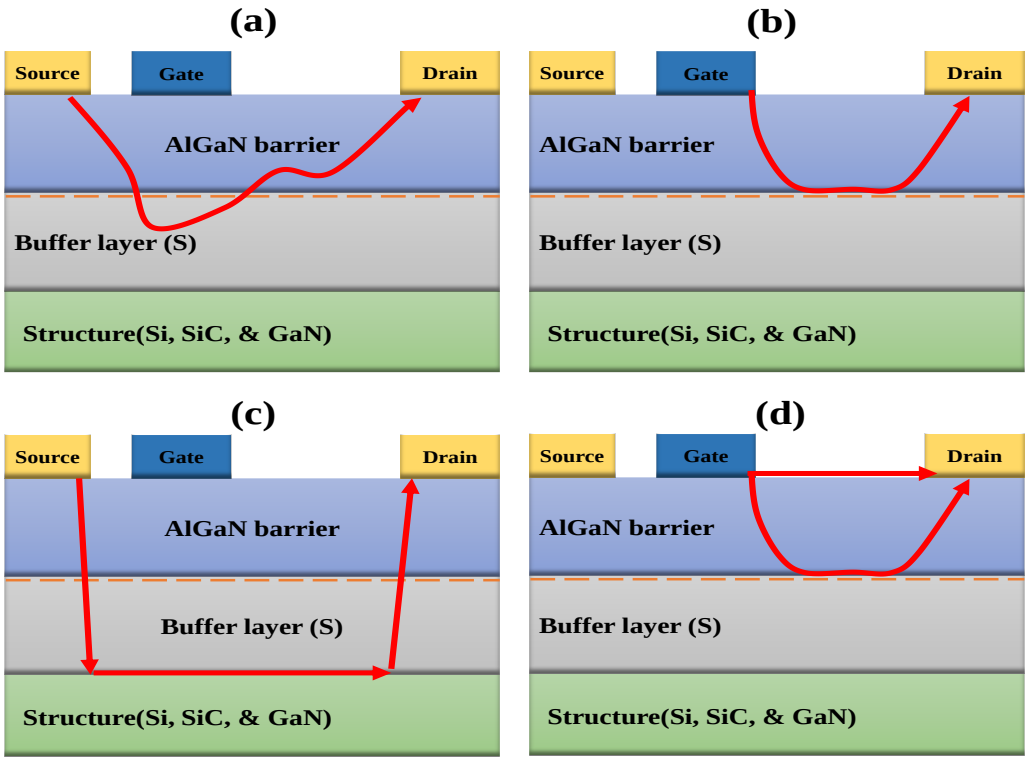


Figure 41. Schematic represents the main source of limiting the high voltage capability of AlGaN/GaN HEMT on substrates (Si, SiC, or GaN). (**a**) Punch through effect, (**b**) Breakdown along channel region, (**c**) Breakdown through buffer layer, (**d**) Leakage currents originating from the gate structure.

5. Challenges for GaN HEMTs Device

Next-generation power-efficient converters might be created using GaN-based power devices if the fundamental problems pertaining to the material's quality, device's fabrication, and its performance can be resolved. However, challenges arise, such as it is impossible to crystallize GaN from melted material because the bulk GaN crystal development process is more challenging compared to Si and SiC. Bulk GaN substrates require high temperatures, >2200 °C, and a nitrogen pressure >6GPa, plus they have tough growth methods, such as a hydride vapor-phase epitaxy (HVPE), sodium flux, and an acidic/basic ammonothermal method is required. On top of that, these GaN substrates have a defect density of between 10^4 and $10^6/cm^2$, which necessitates a careful examination before they can be used for commercial purposes [172]. Ion implantation is used to dope the conventional Si and SiC power devices selectively. However, for GaN, it is still a highly complex process requiring specialized instruments capable of high-temperature (>1200 °C) and high-pressure conditions (>1 GPa) [173]. Bulk GaNs commercialization is hampered not only by the high cost and small size of these substrates, but also by the enormous initial investment required to set up GaN-specific fabs, which could drive up the average selling price (ASP) of discrete devices and further impede the adoption of these devices. Therefore, achieving significant advancements in both the cost and substrate size of these bulk GaN substrates is crucial.

Moreover, some other challenges, such as the GaN HEMT PAs, operate at high-frequency and high-power conditions, where the drain and the gate metals meltdown because of the Eddy current triggered by the magnetic field from the nearby coil. On the contrary, the high operating current may also facilitate the issue. The meltdown occurs at the Au layer, and several hints of Au can be traced in either subsequent layer [174]. The heavy ion irradiation makes the challenge for the GaN HEMT because this ion irradiation induces a device damage by creating lattice defects and accelerating the degradations of

the GaN HEMT under tests (CGHV1J006D, manufactured by Wolfspeed, Durham, NC, USA). On the other hand, a gate injection triggers an impact ionization in the channel, thus inducing failures under the off-state. Its breakdown drain bias becomes lower than the pristine one, owing to the defect generations between the channel layer and the buffer layer during the ion irradiation [175].

Furthermore, after wet etches are done to remove the ohmic contacts of electrically stressed devices; the formation of nano-cracks underneath the ohmic metal contacts of GaN HEMTs becomes challenging for the researchers [176]. This crack might grow from the metal inclusions under the influence of a vertically oriented electric field, which introduces biaxial stress in the channel layer. The hoop stresses introduced by the biaxial compressive stresses and the residual tensile stress introduced in the epitaxial process impel the cracks to extend from the alloyed S–D contacts into the channel.

6. Conclusions

GaN HEMTs appear to be a competitive semiconductor technology for the foreseeable future. The existing and projected demand for GaN-based products in power industries is outlined. The benefits and physics of III-N materials are explained to comprehend GaN-based device transistors better. The contest between Si, GaN, SiC, and β-Ga_2O_3 is anticipated to heat up in the following years since these devices are forecast to represent a crucial function in the next generation of power converters. Research at both the academic and industry levels will lead to a significant advancement in device technology. On the other hand, reliability is still a big issue. Thus, the main GaN HEMT reliability concerns caused by the trap effects like a drain, a gate lag, a current collapse, and a breakdown voltage are explained briefly. Finally, we discussed the lateral type AlGaN/GaN HEMT devices, but in the future, we will include the vertical type AlGaN/GaN HEMT devices. Overall, the future growth of the GaN research field will be aided by the continued improvement of all these features, thanks to the more sophisticated machinery and higher-quality materials.

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