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Effects of GaN Buffer Resistance on the Device Performances of AlGaN/GaN HEMTs

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Abstract: We investigated the effects of GaN buffer resistance of AlGaN/GaN high-electron-mobility transistors (HEMTs) on direct current (DC), low-frequency noise (LFN), and pulsed *I-V* characterization performances. The devices with the highest GaN buffer resistance were grown on sapphire substrate using two-step growth temperature method without additional compensation doping. The proposed device exhibited the degraded off-state leakage current due to the improved GaN buffer quality compared to the reference devices with relative low buffer resistance, which is confirmed by high resolution X-ray diffraction (HRXRD). However, the proposed device with deep-level defects in GaN buffer layer showed the reduced hysteresis (ΔV_{th}), increased breakdown voltage (BV), and enhanced pulse *I-V* characteristics. Regardless of GaN buffer resistance, all devices clearly showed $1/f$ behavior with carrier number fluctuations (CNF) at on-state but followed $1/f^2$ characteristic at off-state. From the $1/f^2$ noise characteristics, the extracted trap time constant (τ_i) of the proposed device can be obtained to be 10 ms, which is shorter than those of the reference devices because of the full compensation of deep-level defects in the GaN buffer layer.

Keywords: AlGaN/GaN; HEMT; low-frequency noise; buffer resistance; current collapse

1. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) have many advantages for power device applications because of their excellent material properties such as high band-gap and large breakdown electric field. For adopting the AlGaN/GaN HEMT to a power device, the high-resistivity (HR) or semi-insulating (SI) GaN buffer layer is required to not only minimize the off-state leakage current, but also mitigate current collapse. Many technologies for developing the HR GaN buffer layer have been reported by utilizing (1) the generation of the deep-level defects or dislocations through controlling the growth temperature [1,2] and (2) the doping of deep-level impurities such as Fe, Mg, or C atoms [3–5]. These deep-level defects and impurities mostly compensate the background *n*-type residual donors in conventional unintentional doped GaN buffer layer due to the nitrogen vacancies (V_N) and/or oxygen (O) atoms. The additional compensation doping method severely suffers from the memory effect, redistribution of dopant atoms, and unexpected trapping effects [3–5]. On the other hand, it is easy and simple method to intentionally introduce the deep-level defects by controlling the growth temperature for achieving the HR GaN buffer layer. Lee et al. [1] reported to the device performances of normally off GaN MOSFETs with extremely high resistive buffer layer by utilizing the two-step growth temperature. However, no detailed comprehensive analyses regarding the AlGaN/GaN HEMTs with the different GaN buffer resistance have been performed in view of low frequency noise (LFN) measurements.

LFN can have great advantages to investigate the interface and/or oxide traps as well as buffer traps when operated at both on-state and off-state. The effect of the passivation of AlGaN/GaN HEMTs on LFN was reported by Veriatchikh et al. [6]. Our groups investigated LFNs of AlGaN/GaN HEMTs with C-doped GaN buffer layer [7]. In this work, we fabricate and characterize AlGaN/GaN HEMTs with different GaN buffer resistance by considering direct current (DC), LFN, and pulsed I–V measurements. These characterizations give information on the origin of traps in the fabricated devices and the effects of the traps in the GaN buffer layer on the device performances.

2. Materials and Methods

The AlGaN/GaN heterostructures with different GaN buffer resistance were grown on a 4-in *c*-plain sapphire substrate by metal organic chemical vapor deposition, which consists of 30-nm-thick low-temperature-grown initial GaN layer, 3-µm-thick highly resistive undoped GaN buffer layer, and 25-nm-thick AlGaN barrier. In order to get high GaN buffer resistance, the initial low growth temperature was set to be 950 °C and then increased to 1050 °C, which is named by two-step growth. As decreased the initial growth temperature, the grain sizes are decreased and nuclei densities are increased [1]. When the growth temperature of GaN layer was 950 °C for 2 min (~100 nm thickness), the subsequently grown GaN layer was generated too many deep-level defects, which plays a role with high resistive properties in the GaN buffer layer [1,2]. For comparison, two samples were prepared using one-step growth method grown at 1000 °C and 1020 °C, respectively. The growth temperature of AlGaN barrier layer for all samples was fixed to 1100 °C. Hall effect measurements at room temperature for GaN buffer layer without AlGaN layer showed the sheet resistances (R_{sh}) of over 10^9 Ω/sq (unmeasurable value) for two-step growth. The R_{sh} for the reference samples using one-step growth was greatly reduced from 10^6 Ω/sq to 10^4 Ω/sq with increasing growth temperature from 1000 °C to 1020 °C. The detailed structure and electrical properties for the grown AlGaN/GaN heterostructure with different buffer resistances were summarized in Table 1.

Table 1. Structural and electrical properties in $Al_xGa_{x-1}N$/GaN high-electron-mobility transistors (HEMTs) with different GaN buffer resistance measured by atomic force microscopy (AFM), Hall effect, and high-resolution X-ray diffraction (HRXRD).

Samples	AFM	Hall Effect			HRXRD		
R_{sh} for the GaN Buffer Layer [Ω/sq.]	RMS [nm]	R_{sh} [Ω/sq.]	μ_e [$cm^2/V{\cdot}s$]	n_s [cm^{-2}]	Al Composition [%]	GaN FWHM (002)	GaN FWHM (102)
10^9 (proposed device)	0.389	496	1420	0.88×10^{13}	25	292	659
10^6 (reference device)	0.603	440	515	2.75×10^{13}	25	299	748
10^4 (reference device)	0.466	501	228	5.45×10^{13}	25	311	745

For the device isolation, mesa etching was performed to a etch depth of 500 nm using inductively coupled plasma-reactive ion etching (ICP-RIE) using a Cl_2 gas. After cleaning the wafer, a Si/Ti/Al/Ni/Au stack for ohmic contacts was deposited by electron-beam evaporator and then followed by rapid thermal annealing at 850 °C for 30 s. Finally, Ni/Au gate metal was deposited to form the gate length (L_g) of 5 µm (gate-drain spacing (L_{gd}) of 4 µm). The device structure is illustrated in Figure 1.

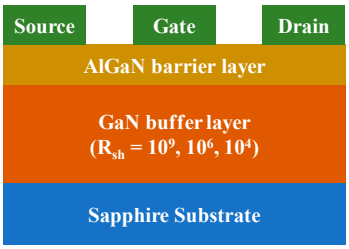

Figure 1. Schematic illustration of the AlGaN/GaN HEMTs with different GaN buffer resistance (no surface passivation).

3. Results and Discussion

The drain currents for the fabricated AlGaN/GaN HEMTs with different GaN buffer resistance were measured with applying double gate voltage sweep (negative to positive sweep and then positive to negative sweep) in Figure 2a. The proposed device using two-step growth exhibits the positive shift of threshold voltage (V_{th}) with approximately −3 V compared to the reference devices. The reason for the positive V_{th} is due to the relatively small carrier concentration (n_s) compared to large n_s of the reference devices induced by the combination of two-dimensional electron gas (2DEG) channel and the GaN channel (Hall results in Table 1). It is also interesting to note that the proposed device presents negligible hysteresis of 20 mV, while the devices with R_{sh} = 10^6 and 10^4 indicate to large hysteresis of 180 mV and 220 mV, respectively. This means that the proposed device has less trapping effect into the deep-levels in GaN buffer layer, as discussed later. On the other hand, the off-state leakage current in the proposed device is the highest value that those of the reference devices, as shown in Figure 2. It is attributed to the improved crystal quality of GaN buffer layer for the proposed sample, which is confirmed by high-resolution X-ray diffraction (HRXRD) and atomic force microscopy (AFM) (Table 1). Another possible explanation is the fully compensated GaN buffer layer of the proposed device, which hardly captures some electrons from the off-state leakage and hence do not reduce the leakage current. However, the breakdown voltages (BV) with the devices with R_{sh} = 10^9, 10^6, and 10^4 demonstrate 185 V, 64 V, and 39 V at I_d = 1 mA/mm, respectively, as shown in Figure 2b. The highest BV characteristic for the proposed device is due to the extremely high GaN buffer resistance property.

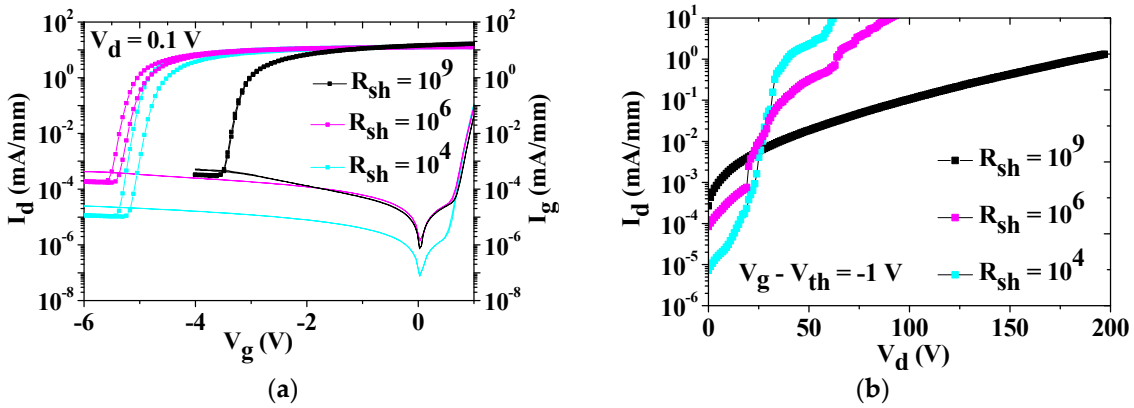

Figure 2. (**a**) Drain currents with double sweep of gate voltage at V_d = 0.1 V and (**b**) breakdown voltages at V_g = −6 V in the fabricated AlGaN/GaN HEMTs with different GaN buffer resistance.

To find the conduction mechanism, the LFN characterizations are conducted using a fully automatic noise measurement system from Synergie Concept (Meylan, France). Noise measurements were performed sweeping the gate voltage (V_g) from subthreshold to strong accumulation region in the linear region (V_d = 0.1 V) and the frequency (f) ranges from 4 Hz to 10^4 Hz. Regardless of the GaN buffer resistances, all devices exhibit almost identical $1/f^\gamma$ shape with $\gamma \approx 1$ in entire f range (Figure 3a). Figure 3 shows the normalized noise power spectral densities (S_{Id}/I_d^2) according to the drain currents at f = 10 Hz. Applying to the carrier number fluctuations (CNF) model, we can obtain the origin of trapping-related fluctuations and the trap density using Equation (1) [8,9],

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} \quad (1)$$

where S_{Vfb} is the flatband voltage fluctuations ($=q^2kT\lambda N_t/WLC_{ox}{}^2f$), including q is the electron charge, kT is the thermal energy, λ is the oxide tunneling attenuation distance, N_t is the volumetric oxide trap density, WL is the channel area, C_{ox} is the gate dielectric capacitance per unit area, and f is frequency.

When we match S_{Id}/I_d^2 and $(g_m/I_d)^2$, the S_{Vfb} are calculated to be 3.0×10^{-10} V^2·Hz^{-1} (Figure 3b), 1.0×10^{-10} V^2·Hz^{-1} (Figure 3c), and 5.0×10^{-11} V^2·Hz^{-1} (Figure 3d) for the devices with $R_{sh} = 10^9$, 10^6, and 10^4, respectively. Considering the equivalent C_{ox} is the value of $C_{AlGaN} = 3.2 \times 10^{-7}$ F/cm^2, the corresponding trap density (N_t) calculated using Equation (1) with $\lambda = 0.11$ nm [10] is 1.0×10^{20} cm^{-3}· eV^{-1}, 3.4×10^{19} cm^{-3}· eV^{-1}, and 1.7×10^{19} cm^{-3}· eV^{-1}, respectively. It is remarkable that the N_t value of the proposed device is highest compared to those of the reference devices. This is because the incremental electron trapping/detrapping process from the 2DEG into the improved crystal quality of AlGaN barrier and GaN channel layer when the channel is on-state, as discussed earlier.

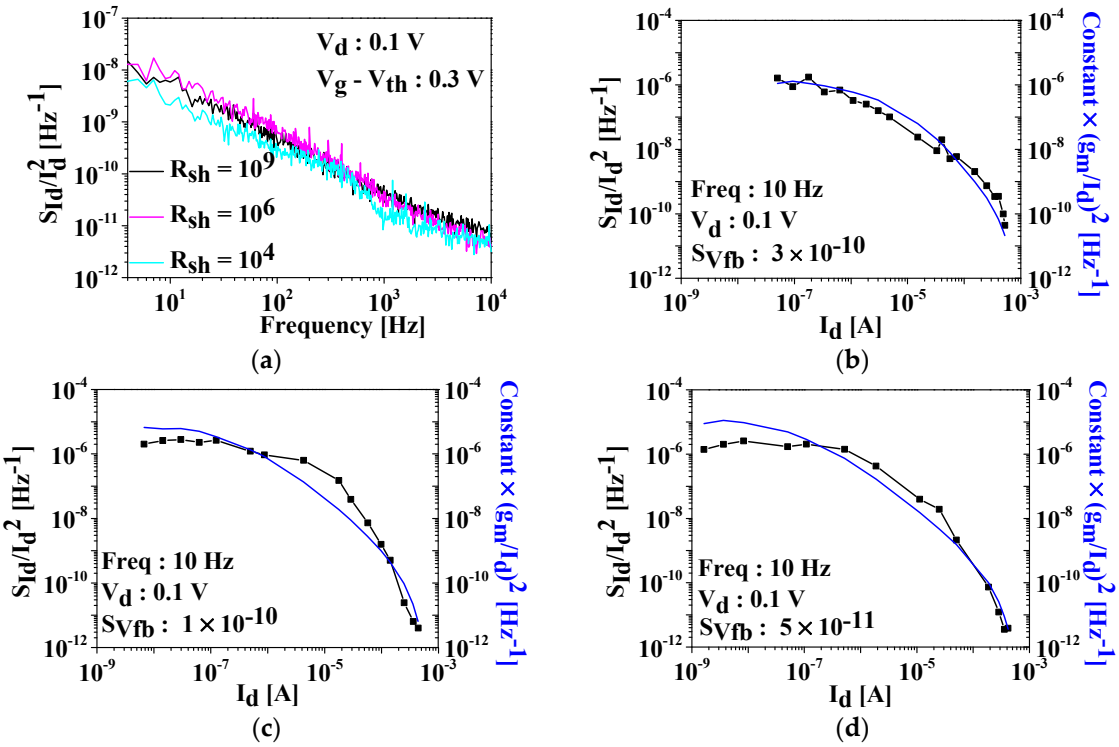

Figure 3. (**a**) Normalized noise spectral density (S_{Id}/I_d^2) according to the frequency and S_{Id}/I_d^2 (black square) matching with (constant × $(g_m/I_d)^2$) (blue line) versus I_d at $V_d = 0.1$ V and $f = 10$ Hz for the devices with R_{sh} = (**b**) 10^9, (**c**) 10^6, and (**d**) 10^4, respectively.

To investigate the noise characteristics according to the buffer resistance, the noise at off-state is measured. Figure 4 shows the product of $S_{Id} \times f$ for all devices at $(V_g - V_{th}) = -1$ V and $V_d = 0.1$ V to find the generation-recombination (g-r) noise presence on top of $1/f$ noise. The noise spectra for the proposed device are observed to plateau at low frequency but become suddenly to fall down with $1/f^2$ at higher frequency, which reflect the co-existence in the spectra of g-r noise with $1/f$ noise in Equation (2). The reason for the $1/f$ noise at off-state is because all devices suffer from significant electron trapping/de-trapping into the GaN buffer layer despite at off-state. It is also clearly observed due to the spectral deformations for all devices, which indicated that the g-r process of the deep-level traps in the GaN buffer layer is existed. From the cutoff frequency f_o in Figure 4, the trap time constant (τ_i) can be calculated using the following Equation (2) [11].

$$S_I \times f = K_f + \sum_{i=0}^{N} \frac{A_i f}{1 + \left(\frac{f}{f_{oi}}\right)^2} \; with \; \tau_i = \frac{1}{2\pi f_o} \tag{2}$$

where K_f is the coefficient of $1/f$ noise component, A_i is the plateau value of g-r component, and f_{oi} is the cutoff frequency. The τ_i is extracted to be 1.0×10^{-4} s, 1.5×10^{-4}, and 3.9×10^{-4} s for the device with

R_{sh} = 10^9, 10^6, and 10^4, respectively, using f_o = 1.5, 1.0, and 0.4 kHz. The proposed device presents the shortest trap time constant, which indicates that the device suffers from less trapping effects through the fully compensated deep-level traps in the GaN buffer layer, as described later.

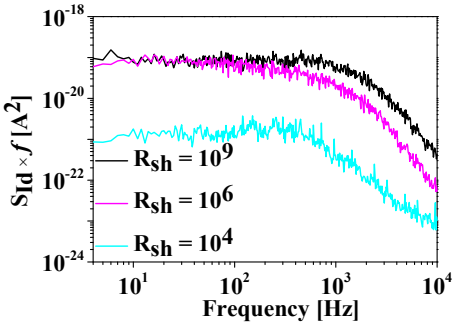

Figure 4. Product S_{Id} × frequency versus frequency in the fabricated GaN HEMTs with different GaN buffer resistance at (V_g – V_{th}) = –1 V and V_d = 0.1 V.

To further identify the trapping effect observed from the DC and noise results, the pulse I-V curves for all devices are measured using B1500 machine from Keysight (Figure 5). The pulse width and pulse length are 1 ms and 1 ms, respectively, and the drain voltage is varied from 0 V to 10 V at V_{th} < V_g < 1 V. The quasi-bias pulse conditions are set to (i) $V_{Q,g}$ < V_{th} and $V_{Q,d}$ = 0 V (red lines) to check the gat lag and (ii) $V_{Q,g}$ < V_{th} and $V_{Q,d}$ = 10 V (green lines) to find the drain lag. The static or dc I_d-V_d curves (black lines) are compared to those of the pulse I_d-V_d curves as a reference. As shown in Figure 5a,b, the proposed device exhibits the small current collapse for all pulse conditions due to the fully compensated GaN buffer layer. On the other hand, the reference devices present severe current collapses because of uncompensated or unoccupied neutral deep traps in the GaN buffer layer, which can easily capture some electrons from the 2DEG channel when applying high drain voltage (Figure 5c–f) [5]. These pulsed I–V results of the AlGaN/GaN HEMTs are consistent with hysteresis, BV, and noise performances at off-state observed from the devices with different GaN buffer resistance.

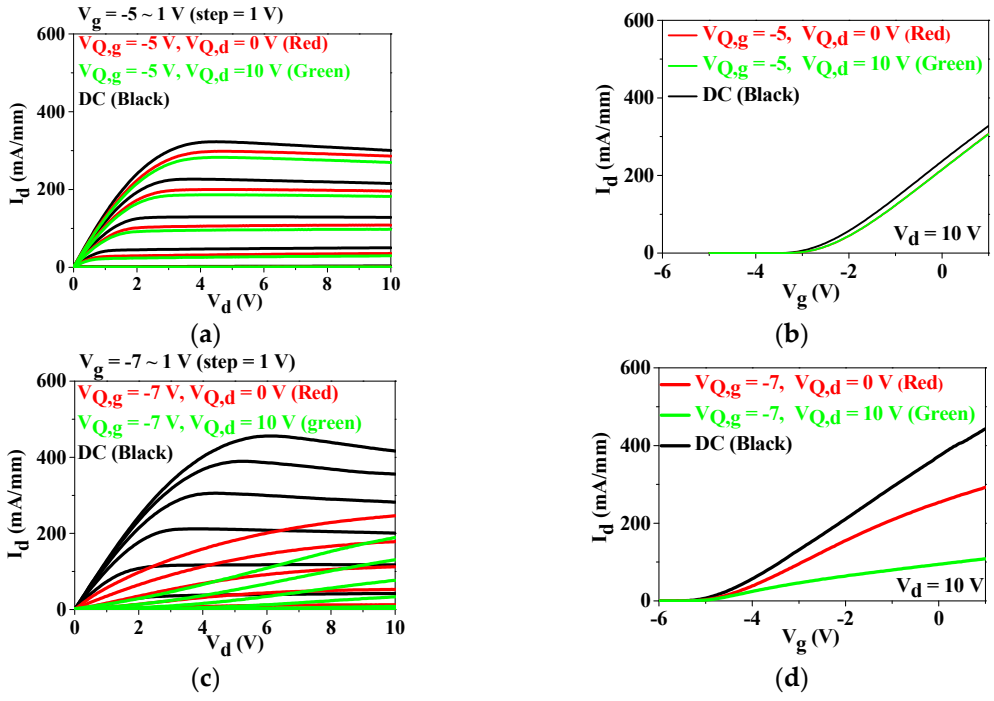

Figure 5. *Cont.*

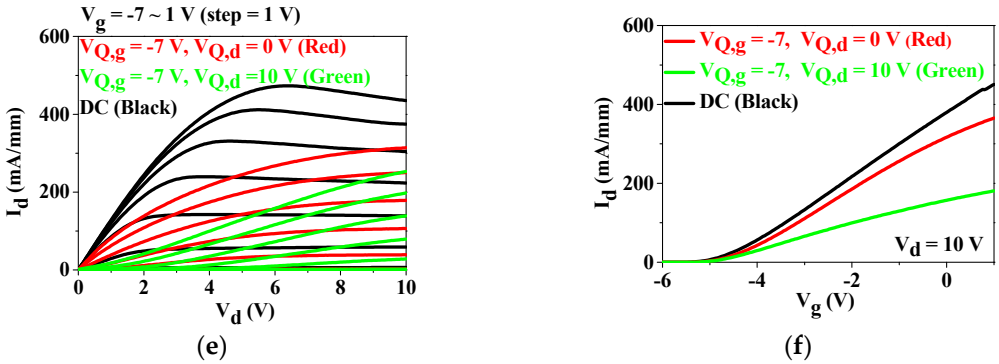

Figure 5. Pulsed I_d-V_d and I_d-V_g curves for the devices with R_{sh} = (**a**), (**b**) 10^9, (**c**), (**d**) 10^6, and (**e**), (**f**) 10^4 sweeping V_d = 0~10 V.

4. Conclusions

To investigate the effects of GaN buffer resistance on the device performances, AlGaN/GaN HEMTs are fabricated, characterized, and compared using DC, noise, and pulse measurements. The proposed device using two-step growth shows high off-state leakage current and increased N_t due to the improved crystal quality in GaN buffer layer. However, the deep-level traps of the proposed device are fully compensated, which leads to the improved hysteresis, high BV characteristic, short trap time constant, and enhanced pulse I–V performances.

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