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Experimental and Modeling Study on the High-Performance p⁺⁺-GaAs/n⁺⁺-GaAs Tunnel Junctions with Silicon and Tellurium Co-Doped InGaAs Quantum Well Inserted

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Abstract: The development of high-performance tunnel junctions is critical for achieving high efficiency in multi-junction solar cells (MJSC) that can operate at high concentrations. We investigate silicon and tellurium co-doping of InGaAs quantum well inserts in p⁺⁺-GaAs/n⁺⁺-GaAs tunnel junctions and report a peak current density as high as 5839 A cm⁻² with a series resistance of $5.86 \times 10^{-5} \Omega$ cm². In addition, we discuss how device performance is affected by the growth temperature, thickness, and V/III ratio in the InGaAs layer. A simulation model indicates that the contribution of trap-assisted tunneling enhances carrier tunneling.

Keywords: tunnel junction; MOCVD; quantum well; co-doping; solar cells

1. Introduction

Solar energy is a renewable and environmentally friendly source of energy. Efforts to generate greater electric power from solar energy have benefited from the high efficiency of solar-cell technology [1]. Tunnel junctions are an important component of multi-junction solar cells because they connect the subcells, where each subcell is designed to absorb a specific range within the solar spectrum. Therefore, as the number of subcells increases, the overall absorption of the solar spectrum is enhanced and the thermalization losses are reduced, resulting in a 6-junction solar cell with an efficiency as high as 47.1% [2]. The peak tunneling current density of tunnel junctions must be greater than the photocurrent density of the devices, and the tunnel junctions should have low electrical resistivity and high optical transparency [3].

The peak tunneling current is described below [4]:

$$J_{\rm peak} \propto \exp \frac{-E_{\rm g}^{3/2}}{\sqrt{N_{\rm eff}}} \tag{1}$$

where E_g is the energy bandgap of the depletion region, and $N_{eff} = (N_{p++}N_{n++})/(N_{p++} + N_{n++})$ is the effective doping concentration, where N_{p++} and N_{n++} are the doping concentrations of the p++and n++ regions, respectively. Equation (1) implies that increased effective doping concentration or a



narrower bandgap leads to increased peak tunneling current density. The tunnel-junction resistance is defined as the reciprocal of the initial slope of the *J*-*V* curve [4].

The usual way to fabricate tunnel junctions with high peak tunnel-current density and low electrical resistivity is to use highly doped material. Take the p⁺⁺-GaAs/n⁺⁺-GaAs tunnel junction as an example: obtaining heavy *p*-type doping is easily done by using carbon as the dopant. However, it is more complicated for *n*-type GaAs with a high doping level because, for common epitaxial growth conditions, the compensation and saturation issues of silicon-doped GaAs limits the performance of GaAs tunnel junctions with a doping level around 1×10^{19} cm⁻³ [5]. Therefore, the peak tunneling current density of silicon-doped GaAs tunnel junctions is around 25 A cm⁻² [6]. However, the tunnel junction should be able to operate at current densities up to 90 A cm⁻² in a high concentration photovoltaic (HCPV) system (HCPV > 6000 suns, CPV: 500–1000 suns) under non-uniform optical irradiation [7].

A promising way to improve the electrical performance of the tunnel junction is to insert a quantum well (QW) in the *p*-*n* interface [8,9]. The band structure of the tunnel junctions with and without quantum well were calculated by solving Poisson's equation, taking the bandgap narrow into account. As shown in Figure 1, the tunneling distance is shortened with the In0.07GaAs quantum well inserted due to the band offset, so a higher peak tunneling current density can be obtained. However, K. Louarn et al. obtained a peak tunneling current of 30 A cm⁻² by using a silicon-doped InGaAs quantum well inserted in a GaAs tunnel junction, which does not satisfy the requirements for the HCPV system [10].



Figure 1. Band structure of (1) p^{++} -GaAs// n^{++} -In_{0.07}GaAs/ n^{++} -GaAs (solid line) and (2) p^{++} -GaAs/ n^{++} -GaAs (dashed line) tunnel junctions. The differences in band bending shorten the tunneling distance for the InGaAs quantum well inserted in the GaAs tunnel junction structure.

In this work, we proposed the silicon (Si) and tellurium (Te) co-doped InGaAs quantum well inserts in a p⁺⁺-GaAs/n⁺⁺-GaAs tunnel junction. Te likely acts as a surfactant that helps the incorporation of Si [11], and Si compensates for the delay time between the injection of DeTe into the reactor and the onset of Te incorporation into the epitaxial layer [12], resulting in a higher doping level in this layer.

The present study investigates the performance of the tunnel junction device, which is affected by the growth conditions of the co-doped InGaAs layer, including the temperature, thickness, and V/III ratio. A peak tunneling current density of 5839 A cm⁻² with a resistance of $5.86 \times 10^{-5} \Omega$ cm² is

achieved in this study. In addition, a simulation model was proposed to investigate the high peak tunneling current density.

2. Materials and Methods

By using metal-organic chemical vapor deposition (MOCVD), a series of tunnel junctions were grown on (100) *n*-type GaAs substrates misoriented 6° toward the <111> A direction. We used C (CBr₄ source) and Si (Si₂H₆ source) as *p*-and *n*-type dopants, respectively, and the InGaAs quantum well layer was doped with Si and Te (DeTe source). Figure 2 shows a typical tunnel junction structure, which consists of a 30 nm thick n⁺⁺ (1 × 10¹⁹ cm⁻³) GaAs layer and a 20 nm thick p⁺⁺ (1 × 10²⁰ cm⁻³) GaAs layer, with an InGaAs quantum well layer embedded at the p⁺⁺-n⁺⁺ junction interface. The doping level was assessed by using the electrical capacitance-voltage (ECV) profile and secondary ion mass spectroscopy (SIMS). The tunnel junction was surrounded by a 150 nm *n*-type (2 × 10¹⁸ cm⁻³) GaAs buffer layer and a 100 nm *p*-type (5 × 10¹⁹ cm⁻³) GaAs cap layer on the top to ensure good ohmic contact. The growth conditions of the InGaAs quantum well layer were varied, as summarized in Table 1.



Figure 2. Schematic of tunnel-junction structure. The growth conditions of the InGaAs layer are summarized in Table 1.

Sample No.	Thickness (nm)	V/III	Temperature (°C)
a-1	16	74	600
a-2	16	74	580
a-3	16	74	550
b-1	11	74	550
c-1	16	15	550
c-2	16	5	550

Table 1. Summary of growth conditions for In_{0.07}GaAs layer.

The tunnel junction devices were patterned to different sizes, and chemical etching was used to form square mesa structures of 50×50 , 100×100 , 200×200 , 500×500 , 1000×1000 , and $1500 \times 1500 \ \mu\text{m}^2$. Figure 3 schematically illustrates the device structure. A AuGe/Ni/Au alloyed metal was sputtered onto the backside of the thinned substrates. The devices were fabricated by using conventional photolithographic and wet-etching techniques, and $100 \ \text{nm SiO}_x$ was deposited by plasma-enhanced chemical vapor deposition (PECVD) to isolate the mesa sidewalls. A Ti/Pt/Au top contact metal was deposited by thermal evaporation. To ensure accurate resistance measurements, the four-probe technique was used to measure the *J-V* curve.



Figure 3. Schematic illustration of the tunnel-junction device structure.

3. Results and Discussion

3.1. Devices Performance of the Tunnel Junctions

We investigated how device performance is affected by growth temperature, thickness, and V/III ratio of the $In_{0.07}$ GaAs layer.

3.1.1. Influence of Growth Temperature

As shown in Figure 4, the *J*-*V* curve depends on the growth temperature, with both the peak current density and resistance changes. The results are summarized in rows a-1 to a-3 of Table 2. As the growth temperature decreases from 600 to 550 °C, the peak current density increases from 16 to 2130 A cm⁻², and the resistance decreases from 1.25×10^{-2} to $1.17 \times 10^{-4} \Omega$ cm².



Figure 4. Experimental results of tunnel-junction devices under various growth temperature of the In_{0.07}GaAs layer.

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	Sample No.	Doping Level (cm ⁻³)	Peak Current Density (A cm ⁻²)	Resistance (Ω cm ²)
	a-1	1.13×10^{19}	16	1.25×10^{-2}
	a-2	2.00×10^{19}	472	3.17×10^{-4}
	a-3	4.03×10^{19}	2130	$1.17 imes10^{-4}$
	b-1	3.55×10^{19}	1222	$1.94 imes 10^{-4}$
	c-1	4.22×10^{19}	3320	9.00×10^{-5}
	c-2	5.09×10^{19}	5839	$5.86 imes 10^{-5}$

Table 2. Summary of experimental results.

The growth temperature is a critical factor for Te incorporation, which occupies the arsenic sublattice, especially when aiming for high doping levels. The decrease in carrier concentration with increasing growth temperature can be explained as follows: As the growth temperature increases, the degree of thermal cracking of arsine increases, arsenic overpressure occurs, and the concentration of arsenic vacancies decreases, which reduces the concentration of substitutional vacancies for tellurium [13].

3.1.2. Influence of Thickness

Consider the results shown in Figure 5 and in rows b-1 and a-3 of Table 2. As the $In_{0.07}$ GaAs thickness increases from 11 to 16 nm, the peak current density increases from 1222 to 2130 A cm⁻², and the resistance decreases from 1.94×10^{-4} to $1.17 \times 10^{-4} \Omega$ cm².



Figure 5. Experimental results of tunnel-junction devices under various thickness of the In_{0.07}GaAs layer.

According to K. Louarn et al. [3], with a thick InGaAs layer, the depletion region expands because the *p*-side doping concentration exceeds that of the n side. Increasing the thickness of the *n*-side InGaAs layer reduces the band bending that extends up to the n-GaAs layer and increases the density of states of the direct band-to-band tunneling (DBBT) process [14], resulting in an increased peak tunneling current density because the tunneling probability is increased. With a thin InGaAs layer, a significant band offset occurs at the n⁺⁺-GaAs/n⁺⁺-InGaAs interface due to band misalignment, resulting in a quantized energy level due to the potential drop near the tunneling area. Quantum confinement reduces the density of states during the DBBT process, resulting in the reduction of the tunneling probability. Increasing the thickness of the InGaAs quantum well layer reduces the quantum confinement and weakens the discretization of states in the tunnel junction area.

3.1.3. Influence of V/III Ratio

Consider the results shown in Figure 6 and in rows c-1, c-2, and a-3 of Table 2. As the V/III ratio decreases from 74 to 5, the peak current density increases from 2130 to 5839 A cm⁻², and the resistance decreases from 1.17×10^{-4} to $5.86 \times 10^{-5} \Omega$ cm².



Figure 6. Experimental results of tunnel-junction devices under various V/III ratio for the $In_{0.07}$ GaAs layer.

Decreasing the V/III ratio in the arsine flow at a fixed dopant flow rate increases the probability of the Te substitution into arsenic vacancies due to the fact that Te atoms are n dopants. As shown in Table 2, a higher V/III ratio leads to a lower doping concentration in this layer, we see that lowest V/III ratio used (5), corresponding to a doping concentration up to 5.09×10^{19} cm⁻³ is reached, which is already above the maximum doping level of 1×10^{19} cm⁻³ achievable with Si dopant.

3.2. Role of Trap-Assisted Tunneling

The high peak tunneling current of this study cannot be explained as the usual carrier tunneling due to the doping levels and materials [15]. The contribution of the trap-assisted tunneling mechanism must be considered, which may enhance the carrier tunneling. The heavy doping of the InGaAs layer tends to create clusters [16], and the relaxation of the lattice mismatch between the InGaAs and GaAs layers promotes the formation of defects, which can act as traps in the trap-assisted tunneling (TAT) process [17].

The high peak current density is investigated by using a simulation model implemented in Crosslight APSYS software and that includes a direct band-to-band tunneling [18], bandgap narrowing, and trap-assisted tunneling. In the APSYS simulator, the tunneling probability is solved by Wenzel–Kramers–Brillouin (WKB) approximation and described as following [19]:

$$D = P_0 \exp(-E_\perp / \underline{E}) \tag{2}$$

$$J(E_{\parallel}) = \int_{x_1}^{x_2} \left| \left(\frac{2m^*}{\hbar^2}\right) \left[\left(\frac{E_g}{2}\right)^2 - (\varepsilon_c)^2 \right] / E_g + E_{\perp} \right|^{\frac{1}{2}} dx$$
(3)

$$P_0 = \exp\left[\frac{\pi m^{*\frac{1}{2}} \left(E_g\right)^{\frac{3}{2}}}{2(2)^{\frac{1}{2}} q F \hbar}\right] = \exp\left(-\frac{E_g}{4\underline{E}}\right)$$
(4)

$$\underline{E} = \frac{(2)^{\frac{1}{2}} qF\hbar}{2\pi m^{*\frac{1}{2}} (E_g)^{\frac{1}{2}}}$$
(5)

where E_{\perp} and E_{\parallel} are the electron kinetic energies in perpendicular and parallel to the tunneling direction, respectively, \underline{E} is a measure of the significance of perpendicular momentum, P_0 is the tunneling probability with zero perpendicular momentum, m^* is the effective tunneling mass.

With a highly doped InGaAs quantum well inserted in the GaAs tunnel junction, bandgap narrowing should be considered in the model [20]. The bandgap narrowing is expressed as

$$\Delta E_{\rm g} = A \left\{ \ln \frac{N}{B} + \left[\left(\ln \frac{N}{B} \right)^2 + \frac{1}{2} \right]^{\frac{1}{2}} \right\} \tag{6}$$

where *A* and *B* are constants taken from Slotboom [21], and *N* is the dopant concentration.

The TAT model is based on the assumption that the traps are able to emit carriers and thus generate a current flux, which is expressed as [22]:

$$J = q N_{\rm trap} \frac{d}{dF} (S_{\rm TAT} f_T) \Delta V \tag{7}$$

where S_{TAT} is the emission rate, N_{trap} is the bulk trap density, F is the electrical field, f_T is a correction factor due to temperature, related to thermal activation of trapped carriers. The Poole-Frenkel model of field dependence is implemented [22], where the Poole-Frenkel shift of the trap level is expressed as:

$$\Delta E_{\rm PF} = \sqrt{\frac{qF}{\pi\epsilon_0\epsilon}} \tag{8}$$

To adapt the high peak tunneling current of the sample c-2, two free changeable parameters: the trap carrier lifetimes (t_n, t_p) and the Poole–Frenkel shift (ΔE_{PF}) are used to calibrate the simulation model. Figure 7 shows how the model be tuned to get a good agreement between the simulated and experimental results, including peak tunneling current values and the secondary peak values. With lower t_p and higher Poole-Frenkel shifts, the peak tunneling current values and secondary peak values increase. The simulation results are consistent with experimental data for trap carrier lifetimes of $t_n = 0.45 \times 10^{-4}$ s and $t_p = 4 \times 10^{-2}$ s, and with a Poole-Frenkel shift in the trap level of 1.41 eV, respectively. However, the simulation results are not consistent with the experimental data in the region of negative differential resistance (NDR) because of the instability of the secondary peak [23], which is probably caused by the "two-step" tunneling through the trap states [24]. However, Figure 8 shows that the peak tunneling current density decreases if the TAT effect is not taken into account, which indicates that the trap-assisted tunneling enhances the peak tunneling current values.



Figure 7. Influence of (**a**) trap carrier lifetime and (**b**) Poole–Frenkel shift on simulated *J*-*V* curve. The experimental data are from sample c-2.



Figure 8. Simulated *J*-*V* curve with and without using the trap-assisted tunneling (TAT) model. The experimental data is from the sample (**a**) c-2 and (**b**) a-3.

4. Conclusions

We implement Si and Te co-doped InGaAs quantum well inserts in a GaAs tunnel junction and obtain the result with a peak current density as high as 5839 A cm⁻² and a series resistance of $5.86 \times 10^{-5} \Omega$ cm². The performance of the devices is investigated at various growth conditions of the InGaAs layer, including the growth temperature, thickness, and V/III ratio. A simulation model is used to investigate the performance of the devices, and the results indicate that the trap-assisted tunneling contributes to increasing the peak tunneling current.

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References

- Kabir, E.; Kumar, P.; Kumar, S.; Adelodun, A.A.; Kim, K.H. Solar energy: Potential and future prospects. *Renew. Sustain. Energy Rev.* 2018, 82, 894. [CrossRef]
- Geisz, J.F.; France, R.M.; Schulte, K.L.; Steiner, M.A.; Norman, A.G.; Guthrey, H.L.; Young, M.R.; Song, T.; Moriarty, T. Six-junction III–V solar cells with 47.1% conversion efficiency under 143 Suns concentration. *Nat. Energy* 2020, *5*, 326. [CrossRef]
- Louarn, K.; Claveau, Y.; Fontaine, C.; Arnoult, A.; Marigo-Lombart, L.; Massiot, I.; Piquemal, F.; Bounouh, A.; Cavassilas, N.; Almuneau, G. Thickness Limitation of Band-to-Band Tunneling Process in GaAsSb/InGaAs Type-II Tunnel Junctions Designed for Multi-Junction Solar Cells. ACS Appl. Energy Mater. 2019, 2, 1149. [CrossRef]
- 4. Wheeldon, J.F.; Valdivia, C.E.; Walker, A.W.; Kolhatkar, G.; Jaouad, A.; Turala, A.; Riel, B.; Masson, D.; Puetz, N.; Fafard, S.; et al. Performance comparison of AlGaAs, GaAs and InGaP tunnel junctions for concentrated multijunction solar cells. *Prog. Photovolt.* **2011**, *19*, 442. [CrossRef]
- 5. Northrup, J.E.; Zhang, S.B. Dopant and defect energetics: Si in GaAs. *Phys. Rev. B* 1993, 47, 6791. [CrossRef] [PubMed]
- 6. Hermle, M.; Létay, G.; Philipps, S.P.; Bett, A.W. Numerical simulation of tunnel diodes for multi-junction solar cells. *Prog. Photovolt.* **2008**, *16*, 409. [CrossRef]
- Bedair, S.; Carlin, C.Z.; Harmon, J.L.; Sayed, I.E.H.; Colter, P. High Performance Tunnel Junction with Resistance to Thermal Annealing. In Proceedings of the 12th International Conference on Concentrator Photovoltaic Systems (CPV-12), Freiburg, Germany, 25–27 April 2016; p. 020003.
- 8. Lumb, M.P.; Yakes, M.K.; Gonzalez, M.; Vurgaftman, I.; Bailey, C.G.; Hoheisel, R.; Walters, R.J. Double quantum-well tunnel junctions with high peak tunnel currents and low absorption for InP multi-junction solar cells. *Appl. Phys. Lett.* **2012**, *100*, 213907. [CrossRef]
- 9. Bedair, S.; Harmon, L.J.; Carlin, C.Z.; Hashem, I.E.; Colter, P.C. High performance as-grown and annealed high band gap tunnel junctions: Te behavior at the interface. *Appl. Phys. Lett.* **2016**, *108*, 203903. [CrossRef]
- 10. Louarn, K.; Claveau, Y.; Marigo-Lombart, L.; Fontaine, C.; Arnoult, A.; Piquemal, F.; Bounouh, A.; Cavassilas, N.; Almuneau, G. Effect of low and staggered gap quantum wells inserted in GaAs tunnel junctions. *J. Phys. D Appl. Phys.* **2018**, *51*, 145107. [CrossRef]
- Law, J.J.M.; Carter, A.D.; Lee, S.; Huang, C.Y.; Lu, H.; Rodwell, M.J.W.; Gossard, A.C. Co-doping of InxGa1-xAs with silicon and tellurium for improved ultra-low contact resistance. *J. Cryst. Growth* 2013, 378, 92. [CrossRef]
- 12. Nguyen, X.S.; Yadav, S.; Lee, K.H.; Kohen, D.; Kumar, A.; Made, R.I.; Lee, K.E.K.; Chua, S.J.; Gong, X.; Fitzgerald, E.A. MOCVD growth of high quality InGaAs HEMT layers on large scale Si wafers for heterogeneous integration with Si CMOS. *IEEE Trans. Semicond. Manuf.* **2017**, *30*, 456. [CrossRef]
- 13. Hamon, G.; Paillet, N.; Alvarez, J.; Larrue, A.; Decobert, J. Te doping of GaAs and GaInP using diisopropyl telluride (DIPTe) for tunnel junction applications. *J. Cryst. Growth* **2018**, *498*, 301. [CrossRef]
- 14. Louarn, K. Development of Tunnel Junctions Based on III-V Semiconductors Heterostructures for High Efficiency Multi-Junction Solar Cells. Ph.D. Thesis, Paul Sabatier University, Toulouse, France, 2018.
- Jandieri, K.; Baranovskii, S.D.; Rubel, O.; Stolz, W.; Gebhard, F.; Guter, W.; Hermle, M.; Bett, A.W. Resonant electron tunneling through defects in GaAs tunnel diodes. *J. Appl. Phys.* 2008, 104, 094506. [CrossRef]
- 16. Park, Y.; Qian, W.; Skowronski, M. Precipitation of Tellurium-Rich Phase in Heavily Diethyltellurium-Doped GaAs during Organometallic Vapor Phase Epitaxy. *J. Electrochem. Soc.* **1995**, *142*, 4294. [CrossRef]
- 17. García, I.; Rey-Stolle, I.; Algora, C. Performance analysis of AlGaAs/GaAs tunnel junctions for ultra-high concentration photovoltaics. *J. Phys. D Appl. Phys.* **2012**, *45*, 045101.
- 18. Crosslight Software Inc., Canada. Available online: http://www.crosslight.com/ (accessed on 20 October 2019).
- 19. Li, Z.Q.; Xiao, Y.G.; Li, Z.M.S. Modeling of multi-junction solar cells by Crosslight APSYS. In *High and Low Concentration for Solar Electric Applications*; International Society for Optics and Photonics: San Diego, CA, USA, 2006; p. 633909.
- 20. Colter, P.; Hagar, B.; Bedair, S. Tunnel junctions for III-V multijunction solar cells review. *Crystals* **2018**, *8*, 445. [CrossRef]

- 21. Slotboom, J.W.; Degraaff, H.C. Measurements of bandgap narrowing in Si bipolar transistors. *Solid-State Electron.* **1976**, *19*, 857. [CrossRef]
- 22. Gehring, A. Simulation of Tunneling in Semiconductor Devices. Ph.D. Thesis, Technical University, Vienna, Austria, 2003.
- 23. Wheeldon, J.F.; Valdivia, C.E.; Walker, A.; Kolhatkar, G.; Hall, T.J.; Hinzer, K.; Masson, D.; Fafard, S.; Jaouad, A.; Turala, A. AlGaAs tunnel junction for high efficiency multi-junction solar cells: Simulation and measurement of temperature-dependent operation. In Proceedings of the 34th IEEE Photovoltaic Specialists Conference (PVSC), Philadelphia, PA, USA, 7–12 June 2009; pp. 106–111.
- Narasimhan, V.K.; Yastrebova, N.; Valdivia, C.E.; Hall, T.J.; Hinzer, K.; Masson, D.; Fafard, S.; Jaouad, A.; Arès, R.; Aimez, V. Effect of parameter variations on the current-voltage behavior of AlGaAs tunnel junction models. In Proceedings of the 1st Microsystems and Nanoelectronics Research Conference, Ottawa, ON, Canada, 15 October 2008; p. 165.

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