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An Efficient Quantum-Dot Cellular Automata Memory Architecture for Internet of Things Systems

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Abstract

Internet of Things (IoT) nodes continuously acquire, buffer, and transmit sensor data under strict constraints on area, latency, and energy consumption. However, conventional complementary metal–oxide–semiconductor (CMOS)-based memory-access circuits face increasing power loss, parasitic effects, interconnect complexity, and sensitivity to process variations at the nanoscale. To address these limitations, this paper proposes a quantum-dot cellular automata (QCA)-based decoder-driven static random-access memory (SRAM)-access architecture for compact and energy-efficient IoT perception-layer memory. The proposed framework integrates three main components: a majority-logic RAM cell with feedback-based storage and non-destructive readout, a compact 2 × 4 decoder with enable and auxiliary asynchronous set/reset control, and a 1 × 4 SRAM array in which the decoder is embedded to reduce routing and clocking overhead. The circuit layouts were implemented and functionally verified using QCADesigner 2.0.3, while the energy behavior was evaluated using QCADesigner-E. Simulation results confirm correct write/read (W/R) and address-selection behavior. The proposed 2 × 4 decoder achieves 86 QCA cells, 0.08 μm^2 occupied area, and one clocking unit, reducing cell count, area, and clocking by 48.19%, 50.00%, and 20.00%, respectively, compared with the best selected decoder baseline. The integrated 1 × 4 SRAM array achieves 684 cells and 14 clocking units, improving timing by 30.00% compared with the closest SRAM-array baseline. These results demonstrate that the proposed QCA-based memory-access structure provides a compact and low-overhead solution for energy-constrained IoT communication systems.

Keywords: quantum-dot cellular automata; SRAM array; 2 × 4 decoder; nanoscale memory; IoT perception layer; energy dissipation

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1. Introduction

The Internet of Things (IoT) is a network of distributed sensors, embedded devices, controllers, and cloud platforms that enhance real-time monitoring and data collection as well as automated decision-making. It supports the seamless transfer of information

between smart sensors, edge nodes, gateways, and servers across industrial, environmental, transportation, agricultural, and smart-home environments [1]. These systems find widespread application in condition monitoring, asset tracking, supervision of infrastructure, and automated intelligent operation. Since IoT devices are commonly limited in energy, area, and reliability, effective memory and communication units for storing and retrieving collected data enable the seamless functioning of IoT nodes [2]. In addition, Figure 1 illustrates the IoT ecosystem: smart sensors and devices are used across industrial and environmental, transportation, agricultural, and smart home applications, transmitting data via edge nodes and cloud platforms [3]. The information is analyzed to support real-time monitoring, analytics, and automated decision-making, enabling programs such as condition monitoring, asset tracking, infrastructure control, and intelligent automation, all of which are aided by efficient memory, storage, and communication.

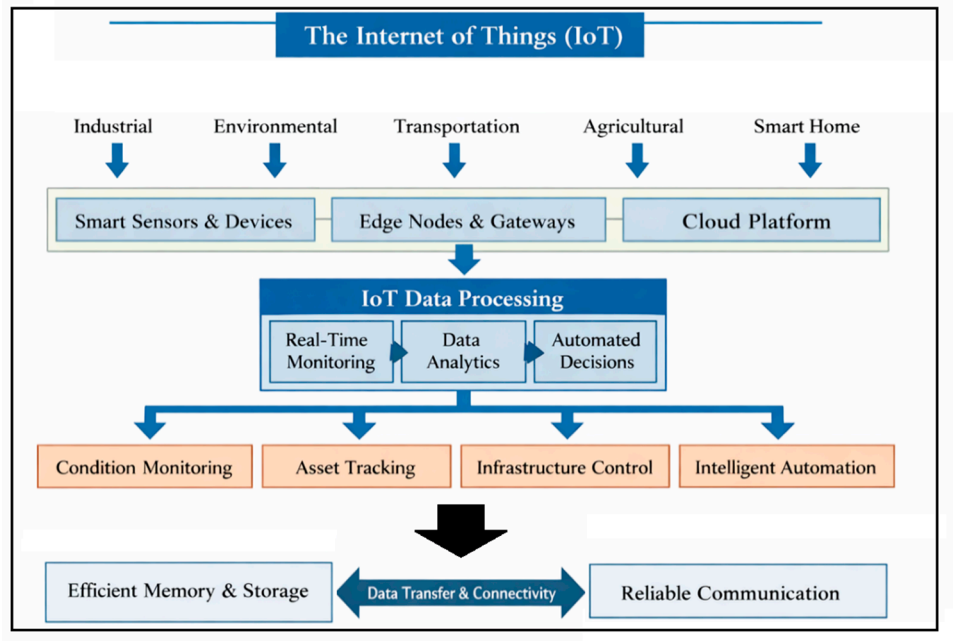


Figure 1. General overview of IoT communication systems.

The most important parts of embedded memory architecture are decoders and SRAM blocks. Decoders are digital logic circuits that pick a single output depending on the input, usually to direct memory access during operations involving reading and writing data [4]. In a 1 × 4 SRAM array, one of four memory lines is selected by the 2 × 4 decoder using a 2-bit address input. SRAM is preferred in embedded systems because it offers fast access, uses little power when standing by, and integrates easily with main processing units [5]. Nevertheless, when transistors become very small, nanometer-sized, their complementary metal–oxide–semiconductor (CMOS)-based decoders and SRAM circuits lead to more power loss, more parasitic capacitance, and more complex links between elements [6]. Consequently, memory access becomes slower, and noise and process variations exist [7]. This is particularly alarming for IoT communication systems that appreciate reliability and energy-efficient operation.

Despite the progress made in QCA-based memory and decoder circuits, several limitations remain unresolved. Many previous designs focus either on decoder optimization or on isolated RAM/SRAM cell structures, while the interaction between address decoding, memory-cell activation, write/read control, and array-level integration is not always considered together. For IoT perception-layer devices, this limitation is important because sensor data must be temporarily buffered and accessed with low latency, low area overhead,

and low energy dissipation. Therefore, an efficient memory-access architecture should not only minimize the cell count of a standalone decoder but should also support controlled line selection, stable data storage, non-destructive readout, and scalable integration within SRAM arrays. This paper addresses this gap by developing a quantum-dot cellular automata (QCA)-based [8] decoder-driven SRAM-access framework in which the decoder, RAM cell, and 1 × 4 SRAM array are designed and evaluated as connected memory-access components.

QCA replaces current-based states, such as normal logic gates, with electrons in quantum cells, thus consuming less energy and eliminating switches that require current [8]. In QCA technology, a quantum dot is a nanoscale potential well that can confine mobile electrons. A standard QCA cell is commonly modeled as four quantum dots positioned at the corners of a square, with two mobile electrons occupying opposite corners due to Coulombic repulsion. The two stable diagonal electron configurations represent binary logic states, usually denoted as polarization P = +1 and P = −1, corresponding to logic "1" and logic "0". Unlike CMOS circuits, where information is transferred by current flow through transistors, QCA circuits propagate information through electrostatic interaction between neighboring cells [8]. In this paper, quantum dots are used as the physical basis for all proposed memory-access components. The RAM cell, decoder, and SRAM array are implemented as arrangements of QCA cells, where majority gates, inverters, and inter-cell polarization interactions realize the required storage, selection, and read/write functions. The proposed architecture will reduce the number of cells and power consumption through the use of QCA-based logic gates and a four-zone clocking scheme. The memory cell (MC) makes use of a 2:1 multiplexer [9] and a D latch [10].

The purpose of this paper is to improve the decoder-driven SRAM-access structure and evaluate its area, timing, and energy characteristics. The designs are generated with the QCADesigner 2.0.3 [11] in order to aid in the ease of data routing and reduce gate delays. The auxiliary set/reset control lines provide additional initialization and clearing capability for the selected output state. Its design is efficient in terms of area and operationally accurate, and its modularity makes it easy to scale to larger memory arrays without any profound impact on area or latency, and it enhances performance consistency, making it suitable for resource-constrained and energy-sensitive IoT environments.

The primary findings of this research are as follows. This article's main contributions are summarized below:

- Designing a compact QCA-based 2 × 4 decoder with enable control and auxiliary asynchronous set/reset control lines for controlled SRAM line selection.
- Developing a decoder-driven 1 × 4 SRAM-access architecture that integrates the decoder with QCA RAM cells to reduce routing and clocking overhead.
- Providing waveform-level functional verification of the decoder and SRAM array using QCADesigner 2.0.3 under defined simulation parameters.
- Evaluating the proposed architecture in terms of QCA cell count, occupied area, clocking requirement, and energy dissipation using QCADesigner-E.
- Demonstrating the suitability of the proposed memory-access architecture for compact and energy-aware IoT perception-layer data-buffering applications.

The remainder of this paper is organized as follows. Section 2 presents the background of QCA technology and reviews related QCA-based decoder and SRAM designs. Section 3 describes the proposed QCA-based memory-access architecture, including the RAM cell, 2 × 4 decoder, and integrated 1 × 4 SRAM array. Section 4 presents the simulation setup, functional verification, comparative analysis, and energy evaluation. Section 5 discusses the significance, limitations, and IoT relevance of the proposed design. Finally, Section 6 concludes the paper and outlines future research directions.

2. Background and Literature Review

2.1. QCA Fundamentals

QCA represents a different way of using nanotechnology that shows promise as an alternative to CMOS for devices requiring low power and high density. QCA circuits encode binary information simply by directing electrons in certain patterns within cells, rather than using transistors. The structure of each QCA cell involves four quantum dots at the corners of a square that can move between the dots. Because of the repelling forces between electrons, they usually arrange themselves so that they display a stable representation of '0' or '1' [8,12].

The main logic units used in QCA are called the majority and inverter gates. The majority gate calculates three-input logic, and it forms the foundation for building AND, OR, and XOR gates. The cells in QCA circuits communicate through interactions and not physical wires, allowing the circuit to be packed more closely together. Moreover, clocking in QCA helps organize data movement and provides the power required to drive switches. The four main phases in clocking consist of switch, hold, release, and relax [8,12]. This allows the circuit to function efficiently and reliably because pipelining and organization of data are possible. Low power consumption, small design features, and scalability make QCA technology attractive for designing nano-scale digital circuits. It is useful for next-generation computing systems such as memory architectures, cryptographic modules, and components of IoT communication systems.

2.2. QCA Decoders

Heydari, Rezai [13] proposed two new designs of 2:4 QCA decoders as an alternative to CMOS. One of the designs was based on a single-layer coplanar QCA structure, and the other used a multilayer structure. The designs were simulated by QCADesigner to verify their functionality. The coplanar decoder required 34 cells, had an area of 0.02 μm^2, and a 0.5 clock-cycle delay. The multilayer design also used 34 cells but had a smaller area of 0.01 μm^2 (with the same delay), and average energy dissipation of 2.08 and 2.33 Ebath, respectively. The designs were better than previous works but had drawbacks such as fabrication challenges associated with multilayer designs, potential energy/thermal issues, and a lack of experimental results.

Sherizadeh and Navimipour [14] proposed a QCA-based 2-4 decoder using a five-input majority gate within a module, hoping to improve on ordinary CMOS decoders. Since a QCA-based memory array, or other digital system, relies heavily on the decoder, the design was created to be able to handle n-to-2^n decoder scalability. QCADesigner is used to confirm the circuit's operation, and QCAPro is used to see how power is dissipated.

Patil and Rawat [15] proposed a 2-to-4 decoder using a QCA-based design. The proposed architecture included wires crossing a single layer through clock phasing, reducing reliance on different types of QCA cells and helping the design become sturdier. Simulations in QCADesigner demonstrated that the new design performed as well as the existing ones and excelled compared to older coplanar decoders because of its strong enable-input function. The authors also explored decoder designs and Boolean techniques to address issues related to wire-crossing and multilayer layouts, leading to the development of an improved single-layer decoder.

Seyedi and Navimipour [16] proposed a three-layer 2-to-4 decoder using QCA technology. When compared to existing solutions, the circuit showed significant enhancement in several key areas. Functionality of the proposed design was confirmed by simulating it with QCADesigner 2.0.3. The circuit performed better than the previous 2-to-4 decoders in terms of complexity, speed, and the number of QCA cells. Incorporating these enhancements caused the overall area of the circuit to decrease whenever it was combined with

digital circuits. The research also showed that better designs would enhance the dependability, testability, and fault tolerance of the original work. In addition, the design could be improved to support coding for multi-bit decoder algorithms.

2.3. QCA SRAM

Rathore, Beohar [17] proposed a QCA SRAM cell to address issues in existing SRAM designs. The authors employed three three-input majority gates and an inverter to implement their design. The new layout had 25 QCA cells, an area of 0.02 μm^2, and a 0.5 clock phase delay. The simulation demonstrated enhanced area, cell count, and QCA cost. It showed 76% reduction in cell count, 84.6% in area, and 98.7% in cost compared to other designs. But possible issues include high sensitivity to manufacturing imperfections, scalability, and lack of hardware verification.

Bahar and Khan [18] proposed a multiplexer-based QCA RAM cell. The design was implemented without coplanar crossovers for improved simplicity and reliability. The design was modeled and verified using QCADesigner-2.0.3. The QCAPro tool was used to analyze energy consumption. The new design demonstrated reduced latency, area, and cell-count requirements. It demonstrated 50% lower latency, 43% smaller area, and 40% fewer cells than existing designs, but possible drawbacks include scalability concerns, vulnerability to fabrication imperfections, and the lack of physical proof.

Rathore and Singh [19] proposed QCA-based design of a D-latch and an SRAM cell as alternatives to CMOS. QCA was chosen for its high density, low power, high speed, and small area. The designed D-latch had a layout area of 0.01 μm^2, a 0.5 clock-cycle delay, and 18 QCA cells. An SRAM cell was also designed with 26 cells, an area of 0.02 μm^2, and a 0.75 clock cycle delay. The outcomes showed better performance in terms of area, delay, and cell count than other designs. But drawbacks include the absence of physical realization, fabrication problems, and scalability.

Kianpour and Sabbaghi-Nadooshan [20] proposed a new 16-bit $\times$ 32-bit SRAM structure on the basis of QCA for better functioning than CMOS at the nanoscale. The design was designed to reduce delay, area, and complexity without affecting the high performance enabled by the inherent pipelining of QCA. The architecture facilitated fast and easy read/write access, and it was later developed into an n $\times$ 16-bit $\times$ 32-bit static RAM. Furthermore, the designers created new 16-bit decoders and multiplexers that required a smaller number of majority gates and cells.

Kassa, Ahmadpour [21] proposed a QCA architecture made of a majority gate and an integrated SRAM cell, delivering proof-of-concept of QCA's suitability for nanoscale applications in place of traditional CMOS designs. A few clock zones were chosen to minimize size, energy use, and reliability issues. The simulation outcomes revealed that the new design used less energy, fewer cells, and a smaller area compared to existing designs.

Although QCA has been widely investigated for low-power nanoscale logic, decoder, and memory circuits, its use in IoT systems remains at the research and simulation stage. Table 1 illustrates the existing studies, which mainly focused on reducing cell count, occupied area, latency, and energy dissipation in isolated QCA components such as RAM cells, SRAM cells, decoders, adders, and multiplexers. Recent studies also show that QCA-based memory design remains an active research topic, including RAM-cell modeling, SRAM-cell optimization, and decoder development. However, unresolved challenges remain before QCA can be practically adopted in IoT hardware, including temperature sensitivity, fabrication defects, clocking complexity, cell misalignment, robustness under noise, and the lack of mature large-scale manufacturing processes.

Table 1. Summary of recent QCA memory and decoder-related works and their limitations.

Ref.	Circuit Type	Focus	Energy Consumption	Limitation
Heydari, Rezai [13]	2 × 4 decoder	Decoder optimization	2.29×10^{-2} eV	Decoder only
Sherizadeh and Navimipour [14]	2 × 4 decoder	Decoder energy/cost reduction	5.112×10^{-2} eV	Decoder only
Patil and Rawat [15]	2 × 4 decoder	Without wire crossing techniques	NR	Decoder only
Seyedi and Navimipour [16]	2 × 4 decoder	Decoder optimization in 3 layers	NR	Decoder only
Rathore, Beohar [17]	SRAM	3-input majority gates and an inverter	1.83×10^{-2} eV	Baseline used/inspired
Bahar and Khan [18]	RAM cell	Efficient RAM modeling	NR	Cell-level only
Rathore and Singh [19]	SRAM cell	D-latch-based SRAM	1.00×10^{-2} eV	Cell-level only
Kassa, Ahmadpour [21]	SRAM	Energy-efficient SRAM	NR	Different architecture level
Proposed work	2 × 4 decoder + 1 × 4 SRAM array	Integrated SRAM-access architecture	1.92×10^{-1} eV	No fault-tolerance validation

These studies show that recent QCA memory and decoder research mainly improves isolated components, whereas integrated decoder-driven SRAM-access design with explicit IoT-oriented memory buffering remains less explored.

2.4. Research Gap and Motivation

Overall, the reviewed studies confirm that QCA technology is a promising platform for compact and low-power decoder and memory design. Decoder-oriented works mainly improve line selection, cell count, and layout complexity, while SRAM-oriented works focus on storage density, read/write operations, and array-level organization. However, most existing studies treat the decoder and memory array as separate optimization problems. Limited attention has been given to a unified decoder-driven SRAM-access structure in which address decoding, memory-cell activation, write/read control, and array-level routing are jointly considered for IoT-oriented memory buffering. This gap motivates the proposed QCA-based architecture, which integrates a compact 2 × 4 decoder with a 1 × 4 SRAM array to improve area and timing efficiency while preserving functional correctness.

3. Proposed Framework for IoT Communication Systems

This section presents the proposed QCA-based SRAM-access framework for IoT communication systems. The framework integrates a compact 2 × 4 decoder, a QCA RAM cell, and a 1 × 4 SRAM array. The objective is to reduce cell count, occupied area, and clocking overhead while preserving correct memory-line activation and read/write functionality. The proposed decoder and integrated SRAM array were functionally verified using QCADesigner 2.0.3.

The developed decoder was properly tested and integrated with an array of 1 × 4 SRAM to achieve the ultimate test, which allowed a full functional verification in a representative memory environment. Integration also demonstrates the feasibility of the decoder and its potential application in the real world.

It should be noted that this work does not claim to introduce a completely new RAM-cell concept from scratch. The basic RAM-cell principle and the block-level 1 × 4 SRAM-array organization are inspired by the previously reported architecture in [22]. However,

as summarized in Table 2, the originality of this work lies in the improved decoder-driven SRAM-access implementation, the compact 2 × 4 decoder layout with enable and auxiliary asynchronous set/reset control, the integration of a smaller decoder into the SRAM-array structure to reduce routing and clocking overhead, and the IoT-oriented evaluation of the resulting memory-access architecture. Therefore, the proposed contribution is positioned as an improved and integrated QCA SRAM-access design rather than a fully independent SRAM-cell invention.

Table 2. Distinction between inherited components and contributions of this work.

Component	Source	Role
Basic RAM-cell concept	Inspired by [22]	Used as the storage element in the memory-access architecture
Block-level 1 × 4 SRAM-array organization	Inspired by [22]	Used as the baseline array structure
Compact 2 × 4 decoder layout	Proposed in this work	Reduces cell count, area, and clocking overhead
Decoder integration into SRAM array	Proposed modification in this work	Reduces routing and timing overhead
IoT perception-layer framing	Added in this work	Positions the design for compact local memory buffering in IoT nodes
Comparative and energy evaluation	Extended in this work	Demonstrates timing and energy-related advantages

3.1. IoT Communication Systems

The IoT is revolutionizing contemporary automation by facilitating constant monitoring, anticipating events early, and responding promptly using connected devices. They have different layers so that data is acquired, moved, stored, and accessed in the most efficient way. They commonly use distributed sensors, communication networks, and cloud or edge platforms for storing and examining information, while requiring security, energy efficiency, and high performance.

These layers make up the standard architecture of an IoT communication system, depicted in Figure 2 [23]. The decoder circuit and SRAM are part of the perception layer in the illustrated IoT architecture, facilitating effective local data processing. The decoder provides low-latency, low-energy-consumption access at a high rate and selectivity to sensor outputs that are temporarily stored in SRAM. The data accessed are subsequently sent via the network layer to the application layer, where they can be stored on the cloud, analyzed, and accessed by system operators for reliable real-time monitoring and control. The architecture incorporates a 2 × 4 decoder-based 1 × 4 SRAM to meet the needs of the strict requirements of the Internet of Things applications.

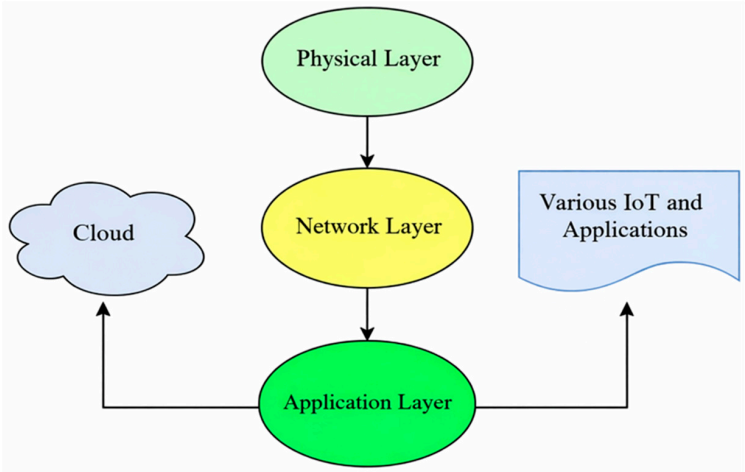


Figure 2. IoT communication system design.

The decoder controls memory-line activation at the IoT perception layer and enables efficient local buffering of sensor data. Its enable and asynchronous set/reset inputs also support controlled initialization and state clearing during memory-access operations.

3.2. Proposed RAM Cell Architecture

Random Access Memory (RAM) is a simple component building block of digital systems, with both data and instructions being instantaneously stored and having a direct influence on speed, reliability, and real-time responsiveness [4]. On-chip memory is even more vital in IoT scenarios, as distributed sensing nodes and edge devices must operate within stringent energy and size constraints while remaining reliable in data management. The proposed QCA-based RAM cell has the potential to make a substantial improvement in IoT equipment by allowing extremely low-power, small, and dependable on-chip storage, which is needed in smart sensors, portable edge nodes, and embedded platforms. Sensor data are constantly acquired and processed by such devices, and sampled data, control parameters, and interim computation results must be quickly and provisionally stored. The introduction of such a QCA RAM cell into IoT nodes will enable continuous and energy-efficient sensing, ensure safe data collection, and support timely local decision-making.

Regarding implementation, the given QCA RAM cell is constructed with the help of two three-input majority gates, one inverter, and a 2:1 multiplexer, as shown in Figure 3a, and the corresponding QCA implementation in Figure 3b [22]. The fundamental storage is provided by a multiplexer-based latch with a feedback loop that offers D-latch-like (level-sensitive latch) behavior. Specifically, the 2:1 multiplexer is used to switch between the externally fed-back stored value and the external input (in). The input data is recirculated and stored in the storage node in the control condition where one is allowed to write, and in the control condition where one uses the feedback path. The write/hold state is supported by the write/read (W/R) and select signals, which essentially offer the latch functionality in the majority-logic design [22].

The cell also offers set and reset lines to be used to initialize the stored state asynchronously when necessary, making the cell more controllable and robust. The appropriate control/selection condition (as well as a fixed polarization input) is formed by the first majority gate, so that appropriate switching between write and hold mode is achieved. The inverter produces the necessary complementary signal in front of the output stage, and the second majority gate is used to create a buffered output path that allows the internal storage loop to be isolated and a stable output to be read. As a result, the read operation is not destructive, as the result is generated by a special majority-logic buffering stage, and does not affect the storage node directly. Lastly, a clock-zone-based organizational structure of QCA is proposed to provide safe signal propagation, minimize signal interference, and enhance synchronization in the storage loop and output path. Table 3 illustrates the operating states of the proposed QCA RAM cell.

Table 3. Operating states of the proposed QCA RAM cell.

Mode	W/R	Select	Set	Reset	Expected State
Hold	0	0	0	0	Stored value recirculates through the feedback path
Write	1	1	0	0	Input data are transferred to the storage node
Read	0	1	0	0	Stored value appears at the buffered output
Asynchronous set	X	X	1	0	Storage/output forced to logic 1
Asynchronous reset	X	X	0	1	Storage/output forced to logic 0
Forbidden	X	X	1	1	Not used

The RAM cell operates through three main timing states: Write, hold, and read. During the write state, the W/R and selection signals enable the multiplexer path that transfers the external input to the storage node. During the hold state, the feedback path is selected, allowing the previously stored polarization state to recirculate and remain stable. During the read state, the stored value is propagated through the buffered majority-logic output path without directly disturbing the storage node; therefore, the read operation is non-destructive. The asynchronous set/reset inputs override the normal write/read operation and force the storage/output node to a known logic state for initialization or clearing. Moreover, the proposed QCA-based RAM is planned to include 46 QCA cells, each with an area of 0.05 μm^2, and requires four clock cycles to operate effectively.

The proposed QCA-based RAM cell can provide an important evolution in IoT equipment, offering ultra-low-power on-chip memory that is compact and reliable, essential for smart sensors, portable edge nodes, and embedded platforms. These devices continuously accept sensor data and compute it, which requires quick temporary storage of sampled data, control parameters, and intermediate computation values. Thus, with the addition of this QCA-based RAM cell to IoT nodes, it is feasible to facilitate sustained, accurate, and energy-efficient sensing, along with secure data collection and timely local decision-making.

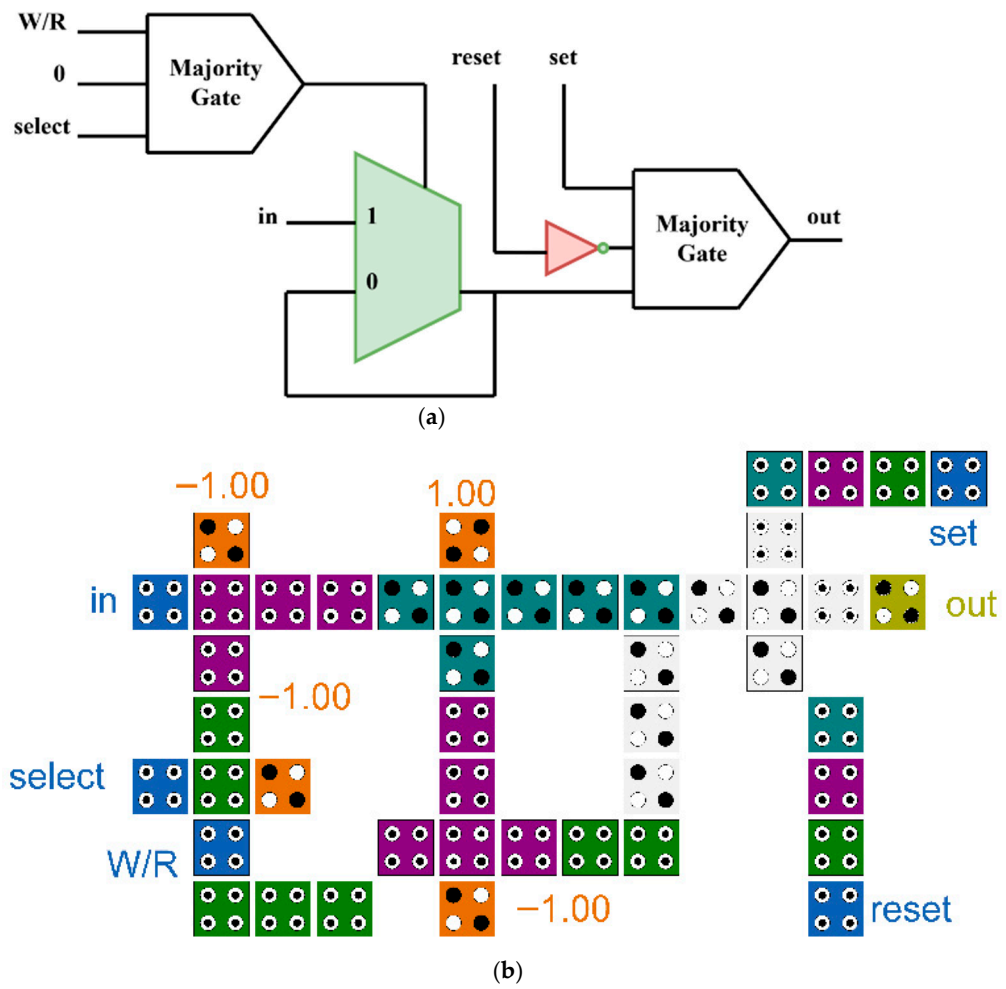


Figure 3. Proposed RAM cell. (**a**) Schematic adopted from [22] and (**b**) QCA layout. In the QCA layout, the colors are used to clarify the organization of the circuit. Green, purple, cyan, blue, and white cells represent different QCA clocking and signal-propagation regions. Orange cells denote fixed-polarization cells assigned to constant logic values of +1.00 and −1.00, while the yellow cell marks the output node. The labels "in", "select", "W/R", "set", "reset", and "out" identify the external data and control terminals of the RAM cell.

3.3. Proposed Decoder Architecture

An efficient decoder, 2 × 4, is one of the significant elements in consuming power to minimize energy consumption in IoT communication systems, especially when it is applied to SRAM row/column selection and specific routing of the signals. In order to overcome the power and scaling drawbacks of CMOS implementations, this paper uses QCA to achieve a small decoder with reduced energy switching, smaller physical layouts, and less complicated interconnect systems. As illustrated in Figure 4a, the decoder uses two select lines (S0 and S1) and an enable signal (EN) so that it can enable one of the four output lines (Y0–Y3) only. This unaddressed behavior guarantees proper addressing and reduces random activations of non-selected lines, which is critical to stable memory access in dense sensing nodes. Moreover, Table 4 illustrates the functional states of the proposed 2 × 4 decoder.

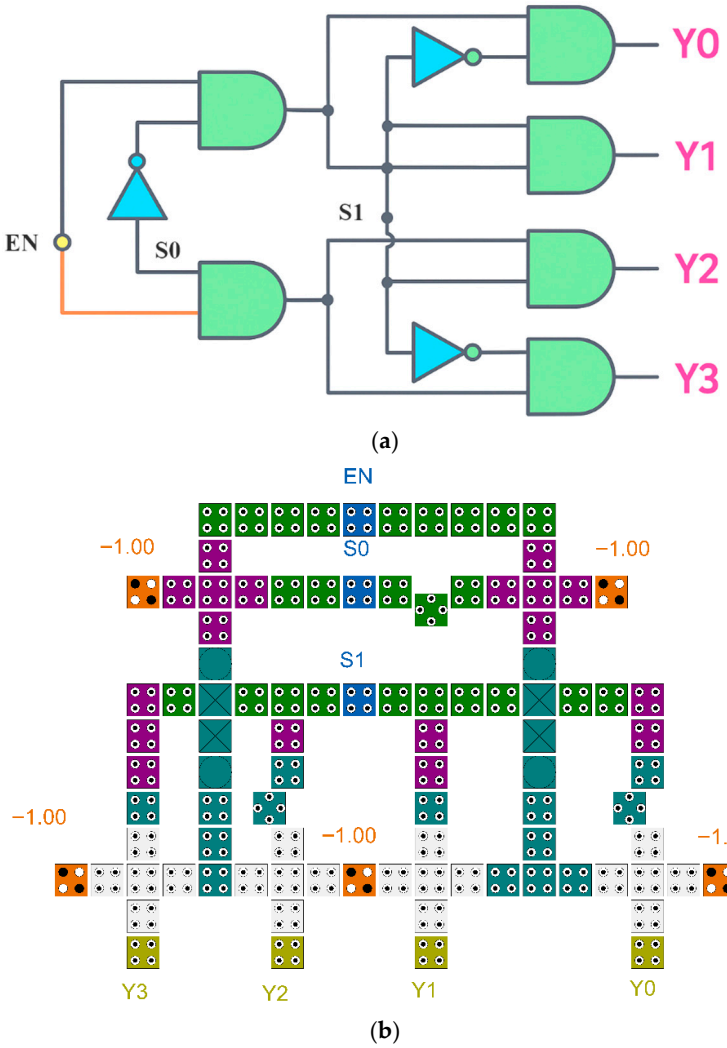


Figure 4. Proposed decoder circuit. (**a**) Gate-level schematic diagram; (**b**) QCA-based layout. In the QCA layout, the colored cells indicate different functional and clocking regions of the circuit: green, purple, cyan, and white cells represent successive QCA clocking zones used for controlled signal propagation; orange cells indicate fixed-polarization/input cells; and yellow cells indicate the output cells corresponding to Y_0, Y_1, Y_2, and Y_3. The labels S_0, S_1, and EN denote the decoder select and enable inputs.

Table 4. Functional states of the proposed 2 × 4 decoder.

EN	S1	S0	Y0	Y1	Y2	Y3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Compared with previous QCA decoder designs, the proposed decoder specifically targets three limitations: high cell count, larger occupied area, and higher clocking requirement. The proposed layout reduces the decoder to 86 QCA cells, an occupied area of 0.08 μm^2, and one clocking unit. In addition, unlike standalone decoder-only evaluations, the proposed decoder is integrated into a 1 × 4 SRAM-access architecture to examine its role in memory-line activation.

The decoder follows a one-hot activation sequence. When EN = 0, all output lines remain inactive regardless of the address inputs. When EN = 1, the address pair S1S0 activates only one output line. For S1S0 = 00, Y0 is activated; for 01, Y1 is activated; for 10, Y2 is activated; and for 11, Y3 is activated. This one-hot behavior ensures that only one SRAM cell is selected during each memory-access operation, preventing the simultaneous activation of multiple memory cells. The most important functional element of the decoder is a 2:1 multiplexer with the properties of D-latches, which provide both controlled selection and permit state retention, and is driven by feedback. This latch-based multiplexer would be the central component of the system to enable output control and to enable the effective composition of modules with the help of this latch-based multiplexer.

The implementation of the decoder in QCA in Figure 4b occupies an area of 0.08 μm^2, and a timeline of a single clock cycle, and the implementation is good in terms of area and timing performance for IoT hardware. In addition, the decoder has built-in asynchronous Set and Reset functions that allow the output state to be brought to a known state whenever necessary. This feature is useful in distributed monitoring systems because it allows rapid initialization and controlled state recovery after temporary disturbances.

3.4. Integration with 1 × 4 Architecture SRAM Array

Multiple memory cells are arranged into a grid structure by the SRAM array architecture and address decoding, and control circuitry is combined to ensure that only the desired cell is accessed at any given time. With a standard SRAM read/write, the address bits are converted to a one-hot word-line by the decoder, the selected cell is enabled, and peripheral control signals are used to either write a new value to the selected cell or read the currently stored value into a memory bus [17]. This organization is necessary to prevent concurrent activation of multiple cells and to ensure proper data transmission along shared interconnect lines. The block-level architecture of the 1 × 4 SRAM array, as reported by Song, Xie [22] is shown in Figure 5a. The general design is considered in the form of three main blocks:

- Block of memory cell: a memory structure of 1 × 4: four memory cells in a row/column.
- Decoder block: a 2 × 4 decoder (activated by S1 and S0) that switches only one output line (Y0–Y3) to choose one memory cell.
- Control and output-selection block: control hardware to control array activity and to control memory operations, such as EN and W/R, and an output-selection stage to pass only the valid cell output.

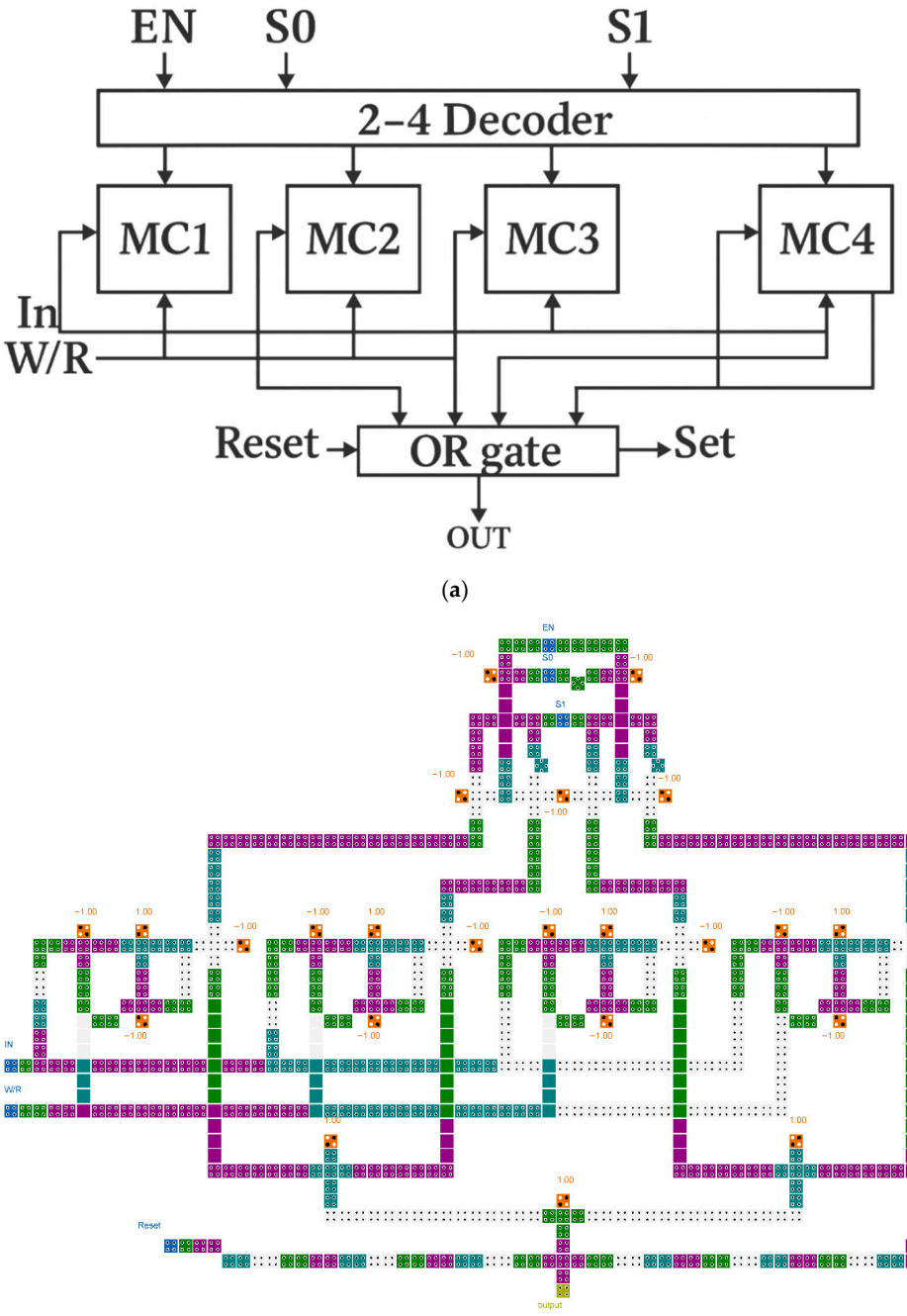


Figure 5. Proposed 1 × 4 SRAM array. (**a**) Gate-level schematic adapted from [22]; (**b**) proposed QCA-based layout. In panel (**b**), the color coding clarifies the organization of the QCA implementation. Green, purple, cyan, blue, and white cells represent distinct clocking and signal-propagation regions across the decoder, memory cells, control lines, and shared output path. Orange cells correspond to fixed-polarization cells with constant logic values of +1.00 and −1.00. The terminal labels IN, W/R, Reset, set, EN, S_0, S_1, and output denote the data input, write/read control, reset and set controls, enable input, select lines, and final output of the SRAM array.

When the array is active, the enable signal (EN) is used to decide whether the array will be active or not. To illustrate, when EN = 1 and S1S0 = 00, the decoder causes Y0, which causes the corresponding memory cell to be activated, and all other decoder outputs are low, leaving their cells inactive. The W/R signal then chooses the type of memory; logic 1 places the chosen cell in the write mode, logic 0 in the read mode. The result of the

triggered memory cell is then added by a logic OR gate that makes sure that it is only the response of the activated cell that would be sent to the common output line, as explained in Song, Xie [22].

Figure 5b demonstrates the modified QCA-based layout that is also inspired by Song, Xie [22], in which a slightly smaller decoder is inserted into the memory structure in order to minimize interconnect overhead. This re-organization was to maximize the reduction of the number of QCA cells, as well as reducing the number of wire crossovers and maximizing the clocking efficiency to reduce the complexity of hardware and to maximize the timing. The 1 × 4 SRAM implementation proposed resulted in 684 QCA cells, an occupied area of 1.14 μm^2, and 3.5 clock phases, indicating a small and time-efficient array structure. Finally, this decoder-integrated SRAM array is very congruent with IoT, in which small sensing and edge devices need to retain data in a buffer with tight power and space limits. The proposed SRAM array, when implemented on QCA, offers an efficient access memory path with a small footprint and low overhead factor to energy-sensitive on-node storage of continuous sensing and real-time processing of data on-node to enable a more dependable and scalable IoT communication infrastructure.

4. Simulation Setup and Results

The entire proposed design is tested and simulated in this section, through QCADesigner 2.0.3 [11] and QCADesigner-E [24] that are highly effective for working with QCA-based circuits. Furthermore, Table 5 depicts the default settings of the simulator engine. They simplify the process of analyzing the logic and design of a circuit, as well as its performance metrics such as delays, energy, and area consumption.

Table 5. Simulation parameters of the bistable simulator engine.

Parameters	Values
Cell size	18 nanometers
Number of samples	128 k
Convergence of tolerance	0.001
Radius effect	65.000000 nanometer
Relative permittivity	12.900000
Low clock	3.800000×10^{23} J
High clock	9.800000×10^{22} J
Shift clock	0.00000
Clocking amplitude factors	2.000000
Layers separations	11.500000
Per sample maximum iterations	00

4.1. Experimental Scheme and Simulation Setup

The simulation experiments were conducted in a step-by-step manner to verify both the functional correctness and the physical efficiency of the proposed QCA-based memory-access architecture. First, the QCA layouts of the RAM cell, 2 × 4 decoder, and integrated 1 × 4 SRAM array were constructed using QCADesigner 2.0.3 [11]. Second, clock zones were assigned to ensure proper signal propagation through the storage loop, decoder outputs, and array-level output path. Third, all relevant input combinations were applied to the decoder and SRAM array, including the address inputs S1 and S0, the enable signal EN, the write/read control W/R, and the asynchronous set/reset controls. Fourth, the output waveforms were examined to confirm correct decoder line activation, memory-cell selection, write operation, read operation, and output stability. Fifth, physical performance metrics, including QCA cell count, occupied area, and clocking requirement, were extracted from the implemented layouts. Finally, the energy behavior of the SRAM array was

evaluated using QCADesigner-E [24], and the obtained results were analyzed in terms of total and average energy dissipation. This experimental flow provides a consistent basis for comparing the proposed design with previous QCA-based decoder and SRAM architecture.

The simulation waveforms for the proposed decoder are shown in Figure 6. The performance metrics were extracted directly from the implemented QCA layouts. The cell count was obtained by counting the number of QCA cells used in each layout. The occupied area was calculated from the layout bounding box, including the maximum horizontal and vertical layout dimensions in QCADesigner. The clocking requirement was determined from the number of clock zones required for a signal to propagate from the primary inputs to the corresponding output. In QCA, one complete clock cycle consists of four clock phases: switch, hold, release, and relax. Therefore, latency was reported in terms of clock units or equivalent clock cycles, based on the number of sequential clock zones traversed by the critical signal path.

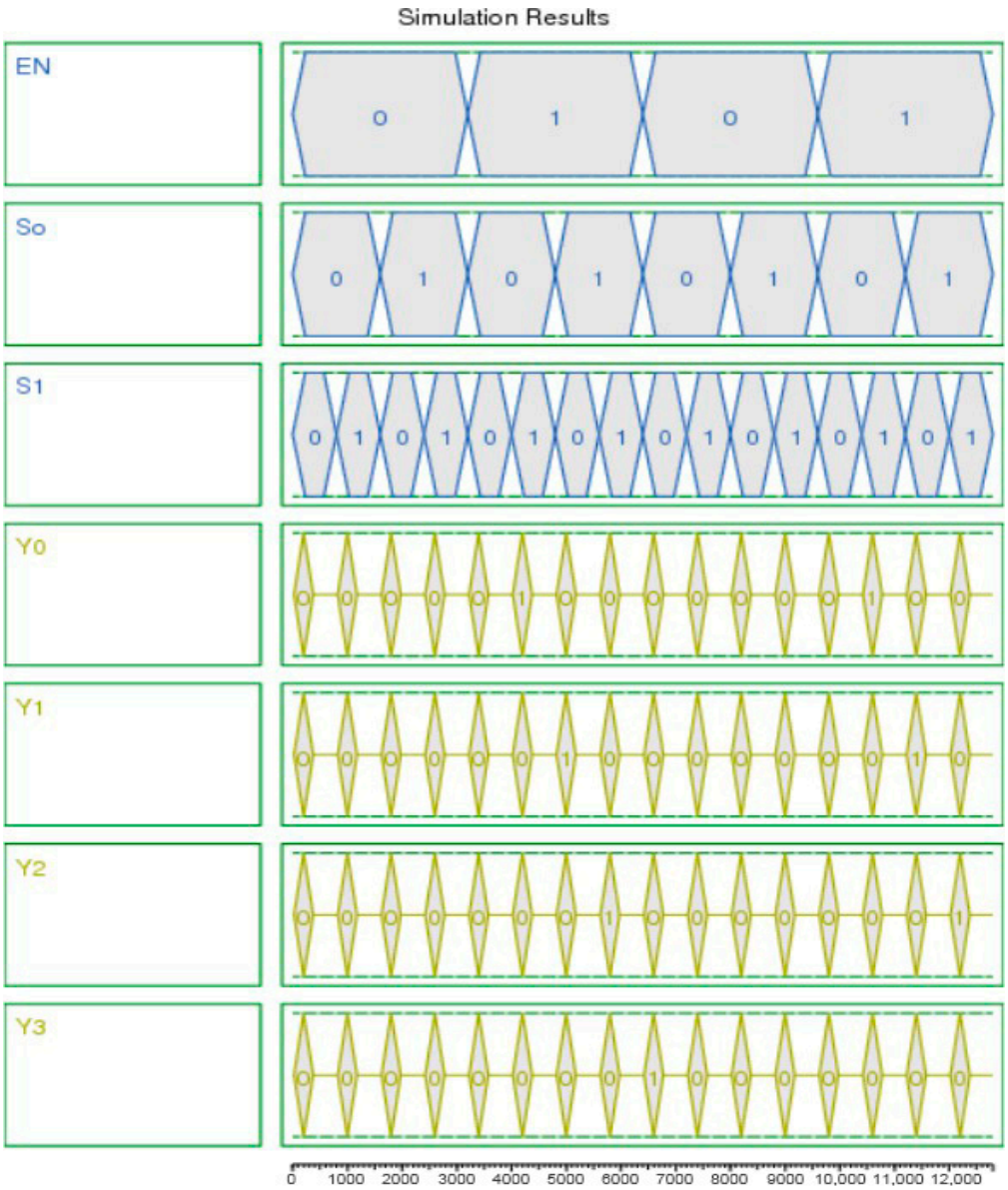


Figure 6. Simulation results of the proposed decoder.

Table 6 compares the key parameters of the decoder circuit. The waveforms confirm that the proposed structure produces outputs in accordance with the expected functionality. Compared with the decoder reported in [25], the proposed design reduces the cell count

from 166 to 86 (48.19%), decreases the occupied area from 0.16 to 0.08 μm^2 (50.00%), and lowers the clocking requirement from 1.25 to 1 (20.00%). Furthermore, Figure 7 provides a graphical comparison of the proposed decoder with previous designs.

Table 6. Performance comparison of the proposed 2 × 4 decoder with previous designs.

In	Cells	Area (μm^2)	Clocking
Misra, Pathak [26]	212	0.25	6
Sherizadeh and Navimipour [14]	200	0.22	4
Kianpour and Sabbaghi-Nadooshan [27]	270	0.38	7
Kianpour and Sabbaghi-Nadooshan [28]	268	0.3	7
Rathore and Singh [25]	166	0.16	1.25
Proposed Design	86	0.08	1

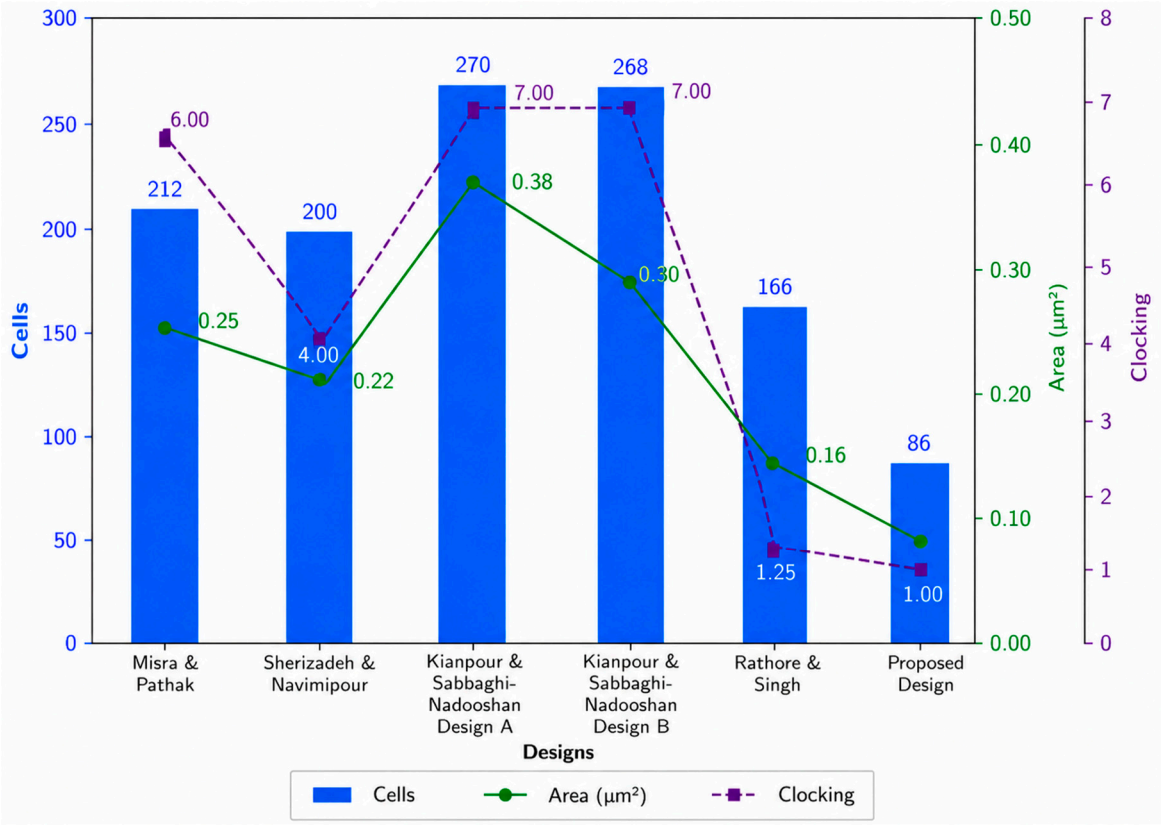


Figure 7. Graphical representation of the proposed decoder with earlier designs.

The cell count was obtained directly from the implemented QCA layouts. The occupied area was calculated using the layout bounding box in QCADesigner. The clocking requirement was determined from the number of sequential clock zones traversed by the critical input-to-output signal path. In QCA, one full clock cycle consists of four phases: switch, hold, release, and relax. Throughput is discussed qualitatively based on clocking reduction rather than as a measured hardware frequency, as the present work is a layout-level simulation study.

The simulation waveforms for the proposed 1 × 4 SRAM array are shown in Figure 8. Table 5 summarizes a comparison of the proposed 2 × 4 decoder with previous designs. The waveforms confirm that the proposed structure produces output in agreement with the expected functionality. Table 7 summarizes the performance comparison for the 1 × 4

SRAM array. Compared with the baseline SRAM architecture in [22], the proposed array reduces the cell count from 704 to 684 (2.84%) and decreases the clocking requirement from 20 to 14 (30%). Furthermore, Figure 9 provides a graphical comparison of the proposed decoder against prior designs.

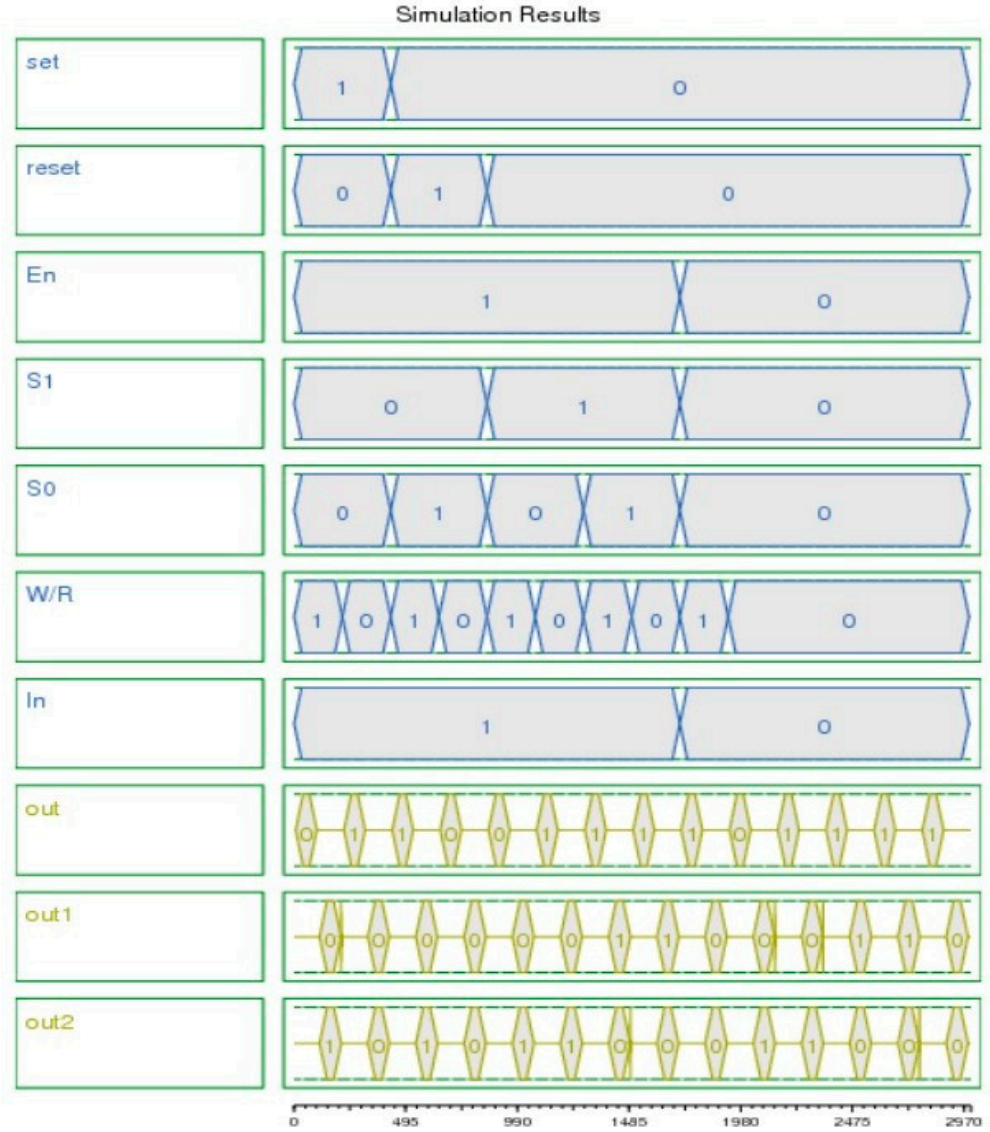


Figure 8. Simulation results of 1 × 4 SRAM array.

Table 7. Performance comparison of the proposed 1 × 4 SRAM array with previous designs.

In	Cells	Area (μm^2)	Clocking
Premananda and Dhanush [29]	3823	4.10	NR
Kianpour and Sabbaghi-Nadooshan [20]	1874	2.94	44.25
Heydari, Xiaohu [30]	860	1.16	23
Mubarakali, Ramakrishnan [31]	843	1.09	24
Song, Xie [22]	704	0.79	20
Proposed Design	684	1.14	14
NR: Not Reported			

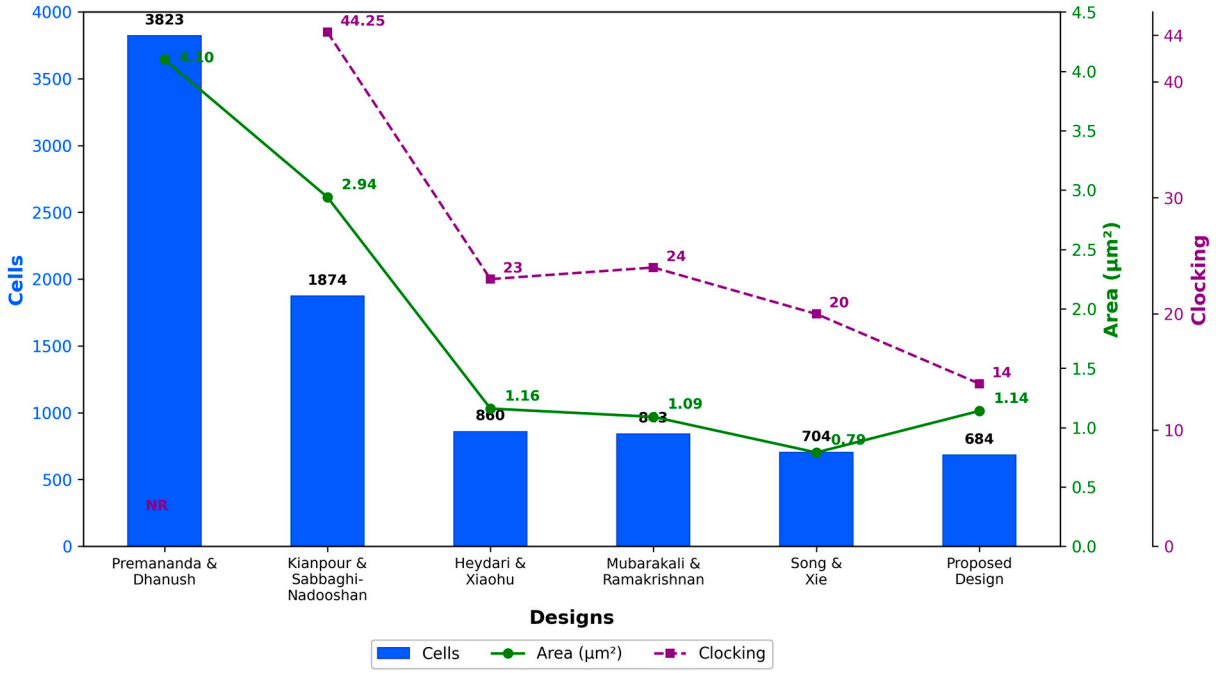


Figure 9. Graphical representation of the proposed SRAM with earlier designs.

4.2. Energy Analysis

Energy dissipation was evaluated using QCADesigner-E [24]. The total energy was interpreted using the bath-related, clock-related, and error-related energy components extracted from the simulation output [24]:

$$E_{\text{total}} = E_{\text{bath}} + E_{\text{clk}} + E_{\text{error}}$$

where E_{bath} is the energy exchanged with the thermal bath, E_{clk} is the energy contribution associated with the clocking field, and E_{error} is the error-related energy component estimated during simulation. The average energy per cycle is calculated as follows:

$$E_{\text{avg}} = \frac{E_{\text{total}}}{N_{\text{cycles}}}$$

where N_{cycles} is the number of simulated cycles.

The assumption is that each of the QCA cells attenuates the same percentage of power; so the total attenuated power is formulated in the form of Equation (1) [32,33]:

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}\cdot\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2 \quad (1)$$

where $\vec{\lambda}$ and $\vec{\Gamma}$ have the three-dimensional energy that defines the QCA cell state. Specifically, the Coherence vector $\vec{\lambda} = (\lambda_x, \lambda_y, \lambda_z)$ specifies the condition of a cell, and the state energy $\vec{\Gamma}$ shows the steady state of the cell. Now, when taking the time period of $[-\mathrm{T}, \mathrm{T}]$, the total energy is estimated as in Equation (2) [24,34]. Finally, the power dissipation design is shown as Equation (3) [32,33]:

$$E_{\text{diss}} = \frac{\hbar}{2}\int_{-T}^{T}\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}dt = \frac{\hbar}{2}\left([\vec{\Gamma}\cdot\vec{\lambda}]_{-T}^{T} - \int_{-T}^{T}\vec{\lambda}\cdot\frac{d\vec{\Gamma}}{dt}dt\right) \quad (2)$$

$$P_{\text{diss}} = \frac{E_{\text{diss}}}{T_c}\left\langle \frac{\hbar}{2T_c}\vec{\Gamma}_+ \times \left[\frac{\vec{\Gamma}_-}{\left|\vec{\Gamma}_-\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_- -\right|}{k_B T}\right) - \frac{\vec{\Gamma}_+}{\left|\vec{\Gamma}_+\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_+\right|}{k_B T}\right)\right]\right\rangle \quad (3)$$

where

P_t: instantaneous total power of cell;

P_1: energy contribution due to coherence vector variation;

P_2: energy contribution due to interaction with neighboring cells;

$\vec{\lambda} = (\lambda_x, \lambda_y, \lambda_z)$: coherence vector representing the quantum polarization state of the QCA cell;

$\vec{\Gamma}$: energy vector representing the cell's steady-state Hamiltonian/energy state;

E_{diss}: dissipated energy of the QCA cell during switching;

P_{diss}: average dissipated power;

T_c: clock period;

k_B: Boltzmann constant;

T: absolute operating temperature;

$\hbar$: reduced Planck constant.

The Coherence Vector Energy simulation reported a total bath-related dissipated energy of 1.92×10^{-1} eV and an average dissipated energy of 1.74×10^{-2} eV per cycle. The total clock-related energy component was -1.28×10^{-1} eV, while the total error-related energy component was -1.53×10^{-2} eV. The negative signs of E_{clk} and E_{Error} follow the sign convention of QCADesigner-E and indicate energy-exchange terms rather than additional dissipated energy. Since the proposed 1×4 SRAM array activates one selected 1-bit memory cell per memory operation, the energy per accessed bit is estimated as 1.74×10^{-2} eV/bit under the simulated access condition. Separate switching-energy and leakage-energy components were not independently decomposed in the present QCADesigner-E output; therefore, they are reported as tool-output limitations rather than unsupported numerical values. The energy consumption characteristics of the proposed 1×4 SRAM, developed with QCADesigner-E, are illustrated in Table 8.

Table 8. Detailed energy-consumption metrics of the proposed 1×4 SRAM array obtained using QCADesigner-E.

Metric	Value	Unit	Description
Switching energy	Not separately decomposed	eV	The present QCADesigner-E output does not provide switching energy as an independent field.
Leakage-related energy	Not separately decomposed	eV	The present QCADesigner-E output does not provide leakage energy as an independent field.
Bath-related dissipated energy, E_{bath}	1.92×10^{-1}	eV	Total dissipated energy reported as Sum_Ebath over the simulated cycles.
Clocking energy component, E_{clk}	-1.28×10^{-1}	eV	Total clock-related energy component reported by QCADesigner-E. The negative sign follows the tool's energy-exchange convention.
Error-related energy component, E_{Error}	-1.53×10^{-2}	eV	Total error-related energy component reported by QCADesigner-E. The negative sign follows the tool's sign convention.
Total energy dissipation	1.92×10^{-1}	eV	Total bath-related dissipated energy over the simulation window.
Average energy dissipation per cycle	1.74×10^{-2}	eV/cycle	Average dissipated energy per simulated cycle.
Energy per accessed bit	1.74×10^{-2}	eV/bit	Since one selected 1-bit SRAM cell is accessed per memory operation, the energy per accessed bit is equivalent to the average energy per access cycle, assuming one access per cycle.

From the Coherence Vector Energy simulation, the proposed 1×4 SRAM array reported a total bath-related dissipated energy of 1.92×10^{-1} eV and an average dissipated energy of 1.74×10^{-2} eV per cycle. The total clock-related energy component was -1.28×10^{-1} eV, while the total error-related energy component was -1.53×10^{-2} eV. The negative signs of E_{clk} and E_{Error} follow the sign convention of QCADesigner-E and represent energy-exchange terms rather than additional dissipated energy. Since the proposed 1×4 SRAM array activates one selected 1-bit memory cell per memory operation, the average energy per accessed bit is estimated as 1.74×10^{-2} eV/bit under the simulated access condition. These results support the energy-aware behavior of the proposed QCA SRAM-access architecture under nominal simulation conditions. However, the present QCADesigner-E output reports bath-related, clock-related, and error-related energy components but does not independently decompose switching-energy and leakage-energy values. Therefore, separate switching and leakage analysis is identified as a limitation and will be addressed in future work using tool-supported or analytical models capable of separating these energy components.

5. Discussion

The simulation results show that the proposed QCA-based memory-access architecture provides meaningful improvements in decoder compactness and SRAM-array timing. The proposed 2×4 decoder reduces the number of QCA cells and occupied area compared with previous decoder designs, mainly because the layout uses a compact majority-logic structure and minimizes unnecessary interconnect complexity. This is important for IoT perception-layer nodes, where memory-access circuits must support frequent sensor-data buffering while maintaining low hardware overhead. The integrated 1×4 SRAM array also improves the clocking requirement compared with the closest SRAM-array baseline. Although the occupied area is slightly higher than that of a previous SRAM design, the proposed architecture achieves a lower cell count and a lower clocking requirement, which indicates better timing-oriented trade-off. For IoT applications, this trade-off is relevant because reduced clocking overhead can improve data-access responsiveness and reduce the delay associated with local buffering.

It should be emphasized that the present work is not a fault-tolerant QCA memory design; rather, it focuses on compact decoder-driven SRAM access, functional correctness, layout efficiency, and energy-aware simulation under nominal conditions.

The energy results further support the suitability of the proposed design for energy-aware nanoscale memory systems. The low average energy dissipation per cycle indicates that the proposed SRAM structure can support repeated memory-access operations with limited energy overhead. However, the current work is limited to a 1×4 SRAM-array configuration. Larger memory organizations, such as 4×4 and 8×8 arrays, may introduce additional routing, clocking, and synchronization challenges. Therefore, future work should evaluate scalability, fabrication defects, thermal variations, and clock-skew effects in larger QCA memory systems. Overall, the proposed design is most suitable for compact IoT sensing and edge-processing scenarios where small memory buffers are required near the data-acquisition layer. The architecture does not replace full-scale conventional SRAM systems at this stage; rather, it provides nanoscale proof-of-concept for efficient local memory access using QCA technology.

Practical Limitations of QCA for IoT Hardware

It is important to note that QCA remains an emerging nanoscale computing paradigm and is not yet a mature commercial technology for IoT hardware. Although QCA offers attractive theoretical advantages, including compact layouts and low switching energy,

several physical limitations must be considered. First, QCA operation can be sensitive to temperature because the stability of cell polarization depends on the energy separation between valid logic states and excited states. Second, individual cell defects, missing cells, displacement, and misalignment can affect polarization propagation and may cause incorrect logic behavior. Third, large-scale fabrication of precisely positioned quantum-dot cells remains challenging because QCA requires nanoscale lithographic accuracy and reliable clocking-field control. Fourth, QCA circuits are sensitive to clocking organization, and clock skew or clock-zone mismatch can affect timing correctness. Therefore, the proposed design should be interpreted as a simulation-based memory-access architecture for future QCA-enabled IoT systems rather than as a commercially deployable IoT memory module.

Although auxiliary set/reset control lines are included in the proposed layout, this study does not claim a complete asynchronous-control robustness evaluation because dedicated set/reset disturbance and anti-interference waveforms are not included. This aspect will be evaluated in future work.

6. Conclusions and Future Works

This paper presented a QCA-based decoder-driven SRAM-access architecture for compact and energy-aware IoT perception-layer memory. The proposed architecture integrates a majority-logic RAM cell, a compact 2×4 decoder with enable and asynchronous set/reset control, and a 1×4 SRAM array, with the decoder embedded to reduce routing and clocking overhead. Functional verification using QCADesigner 2.0.3 confirmed correct decoder activation, memory-cell selection, and SRAM read/write behavior. The proposed 2×4 decoder used 86 QCA cells, occupied an area of 0.08 μm^2, and required one clocking unit. Compared with the best selected decoder baseline, this corresponds to reductions of 48.19% in cell count, 50.00% in area, and 20.00% in clocking requirements. The integrated 1×4 SRAM array achieved 684 cells and 14 clocking units, reducing the clocking requirement by 30.00% compared with the closest SRAM-array baseline. Energy evaluation using QCADesigner-E further confirmed low average energy dissipation per cycle, supporting the suitability of the proposed architecture for energy-constrained nanoscale memory-access applications. The main significance of this work lies in combining decoder optimization and SRAM-array integration within a unified QCA-based memory-access framework. This makes the design relevant to compact IoT nodes that require efficient local buffering of sensor and control data. Nevertheless, the current design is limited to a small 1×4 SRAM-array configuration.

Future work will focus on four specific directions. First, the architecture will be scaled from the present 1×4 SRAM array to larger 4×4 and 8×8 memory organizations while quantifying decoder, routing, and clock-zone overhead. Second, peripheral circuits, including write drivers, sense/readout circuits, and output-selection networks, will be added to evaluate a more complete QCA memory subsystem. Third, since the present work is not a fault-tolerant design, future studies will develop fault-aware QCA memory architectures using defect-tolerant majority-gate structures and systematic fault-injection analysis. Fourth, the energy evaluation will be extended by separating read-access and write-access cases and by using tool-supported or analytical models capable of independently decomposing switching and leakage-related energy components.

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