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Review

The Evolution of Lithography: From Resolution Scaling to Manufacturing Constraints

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Abstract

Lithographic patterning continues to evolve under the dual pressure of ever-finer features and manufacturable, cost-effective integration. Beyond headline resolution, industrial adoption is increasingly determined by a small set of coupled metrics: throughput, overlay (registration), defectivity, and cost, as well as by how these trade-offs shift with materials, substrate form factors, and integration flows. Here, we review lithographic techniques across three eras: traditional methods (pre-1990s), non-conventional innovations (1990s), and contemporary advancements (post-2000s), with an explicit goal that goes beyond compilation. Specifically, we provide a decision framework for interpreting each method using the same manufacturing-relevant criteria. For each class of technique, we summarize the operating principle and representative process routes, then map the dominant bottlenecks to the metric that ultimately limits scale-up. This cross-cutting lens clarifies why many emerging methods are compelling at the physics level yet remain constrained at the system level, where process windows, in-line control, and compatibility with existing fabrication ecosystems govern viability. By connecting mechanism-level innovation to manufacturing-level constraints, this review offers practical guidance for researchers and engineers seeking to position nanolithography options for applications ranging from high-volume semiconductor production to agile prototyping and materials- or substrate-limited devices.

Keywords: nanolithography; nanofabrication; nanopatterning; lithography evolution

1. Introduction

As transistors continue to scale down to the nanoscale to improve computing performance and energy efficiency, advances in lithography have played a central role in enabling major breakthroughs in semiconductor manufacturing [1–6]. To meet increasing requirements for resolution, pattern placement accuracy, scalability, and manufacturability, a wide range of patterning approaches has been developed. Importantly, however, industrial adoption is rarely dictated by resolution alone. In practice, manufacturable patterning is governed by coupled metrics such as throughput, overlay (registration), defectivity, and cost, and by how these trade-offs evolve with materials, substrate form factors, and integration flows. In parallel, the ability to fabricate nanometric structures has accelerated progress in materials science and engineering. Accordingly, lithographic tools have become key enablers for the miniaturization and integration of electronic devices [6–8], healthcare equipment [9–12], biosensors [13–15], and metamaterials [16,17], underscoring the broad

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impact of nanofabrication. Against this backdrop, it is useful to view the evolution of lithography as a progression of manufacturing trade-offs, rather than as a simple sequence of inventions. With this lens, we organize lithographic techniques into three eras and track how the dominant scale-up bottlenecks have shifted over time.

1.1. Traditional Lithography (Pre-1990s)

Traditional lithography became the mainstream of semiconductor manufacturing from the 1960s to the 1990s and drove major progress in microelectronic device fabrication [18–20]. Photolithography (PL) has enabled high-throughput patterning with reliable overlay using mature tools and standardized process flows [21]. However, further scaling has been increasingly limited by resolution and pattern fidelity because diffraction limit and process-related constraints make it difficult to create smaller feature sizes [22]. As critical dimensions approached these optical limits, tightening process windows translated directly into higher defectivity risk and yield sensitivity, elevating the importance of process control and metrology in high-volume manufacturing (HVM) [23,24]. To push beyond the diffraction limit, electron beam lithography (EBL) and X-ray lithography (XRL) were developed to achieve higher-resolution patterning [25–30]. However, these techniques remained unsuitable for large-scale fabrication. EBL inherently suffers from low throughput due to the serial exposure process, while XRL requires complex source, optics, and mask infrastructure that increases the cost and makes fab integration difficult [11,31,32]. In general, traditional patterning methods not only require tedious and iterative steps but also represent the limitations in resolution, positional accuracy, scalability, and versatility, thereby resulting in low yield and high cost in the fabrication process [2–6,11,32].

1.2. Non-Conventional Lithography (1990s)

To address these challenges, non-conventional lithography expanded the toolkit for micro and nanoscale patterning by leveraging alternative physical and chemical mechanisms, with many approaches gaining strong momentum from the 1990s onward. Compared with traditional optical projection, these methods often trade tighter design control and registration for advantages in materials compatibility, replication-based throughput, or sub-optical feature formation.

Interference lithography (IL) enables parallel pattern formation over large areas using controlled optical interference, offering attractive throughput for periodic structures but limited pattern complexity and layout-level overlay flexibility [33,34]. Soft lithography (SL) provides low-cost, materials-compatible replication routes, favoring low-cost and gentle processing on flexible or bio-related substrates while facing challenges in high-precision overlay and defect control for dense, multilayer device integration [35]. Although nanoimprint lithography (NIL) easily achieves high-resolution patterning with an excellent throughput, its scalability highly relies on template defectivity, particle control, and repeatable overlay over large areas [36–39]. Nanosphere lithography (NSL) provides a simple and scalable route to periodic nanostructures through colloidal self-assembly, typically prioritizing low cost and large-area coverage over deterministic placement and design freedom [40,41]. Although block copolymer lithography (BCL) generates nanoscale patterns through a self-assembly process in a controllable manner, scaling up is strongly limited by defect suppression, long-range order, and reliable registration to device layouts [42–44]. Dip-pen nanolithography (DPN) uses an atomic force microscope tip to deposit molecular inks with high spatial precision, enabling customized patterns for specialized applications, but remains constrained by serial-writing throughput and tool complexity that raise cost for large-area manufacturing [45,46].

Collectively, these non-conventional approaches broaden the patterning design space, but their scale-up remains constrained by recurring integration challenges, including pattern complexity, defect control, overlay (registration), materials compatibility, and compatibility with established process flows. Consequently, their impact has been strongest in application-specific niches where these trade-offs are acceptable, rather than as universal solutions for high-volume manufacturing.

1.3. Contemporary Innovations (Post-2000s)

Since the 2000s, contemporary innovations have increasingly focused on pushing the limits of resolution, overlay (registration), and manufacturability through extensions of optical systems, near-field concepts, and digitally controlled or highly parallelized pattern generation [47–51]. In this era, the central question shifts from whether nanoscale features are achievable to whether they can be delivered with acceptable throughput, defectivity, and cost within existing integration flows.

Immersion lithography (IML) enhances optical resolution and process latitude by increasing the effective numerical aperture (NA) through a high-refractive-index liquid and remains attractive due to its favorable balance of throughput, overlay control, and ecosystem maturity, despite tightening process windows at advanced nodes [52,53]. Extreme ultraviolet lithography (EUVL) uses 13.5 nm radiation and reflective optics to enable advanced semiconductor patterning, and progress toward high NA extreme ultraviolet systems highlights the continued drive toward next-generation nodes [54–57]. Plasmonic lithography (PSL) exploits near-field enhancement associated with surface plasmons at metal–dielectric interfaces to achieve sub-diffraction patterning [58,59]. Digital maskless lithography (DML), frequently implemented with spatial light modulators such as digital micromirror devices, provides reconfigurable patterning without physical masks [60]. Multi-beam maskless lithography (MBML) aims to overcome the throughput bottleneck of single-beam direct writing through massively parallel electron-beam exposure, which allows practical direct-write routes for selected high-value applications [61–63]. Electrohydrodynamic lithography (EHL) creates microscale and nanoscale patterns through a high electric field to induce the film instability and alleviates material constraints in the patterning process [64].

Although these contemporary approaches have demonstrated strong potential, scalability, defectivity, cost efficiency, and integration remain critical challenges, and ongoing efforts continue to improve their performance and practical adoption. Viewed through manufacturing-relevant metrics, they illustrate a common theme: many routes can achieve impressive resolution, but only a subset can simultaneously satisfy throughput, overlay, defectivity, and cost targets required for broad industrial deployment.

1.4. Overview of the Review

This review provides a comprehensive overview of the rapidly evolving landscape of lithographic techniques. In contrast to prior reviews, we organize lithography into three eras, namely traditional lithography (pre-1990s), non-conventional lithography (1990s), and contemporary innovations (post-2000s). Figure 1 summarizes this chronological evolution and visually connects the three eras to emphasize how dominant bottlenecks and manufacturing trade-offs have shifted over time. By connecting these three groups, this review presents a holistic and forward-looking perspective on the continuous evolution of nanoscale patterning. To clarify practical applicability, the working principles of each approach are discussed, and key advantages and limitations are summarized with respect to manufacturing-relevant criteria, including throughput, overlay (registration), defectivity, and cost, as well as resolution, pattern fidelity, scalability, and process integration.

Consistent with this decision framework, the inset plots in Figure 1 summarize the key trade-offs for serial and parallel patterning routes. Specifically, the serial-lithography map compares representative serial techniques in a resolution to throughput space with cost encoded by the color scale (low to high), whereas the parallel-lithography map compares parallel techniques in a resolution to scalability space, again with cost represented by color. In addition, we highlight major bottlenecks shared by many modern approaches, including defect control, cost efficiency, and manufacturability, and discuss the practical trade-offs required to balance scalability, cost effectiveness, and versatility.

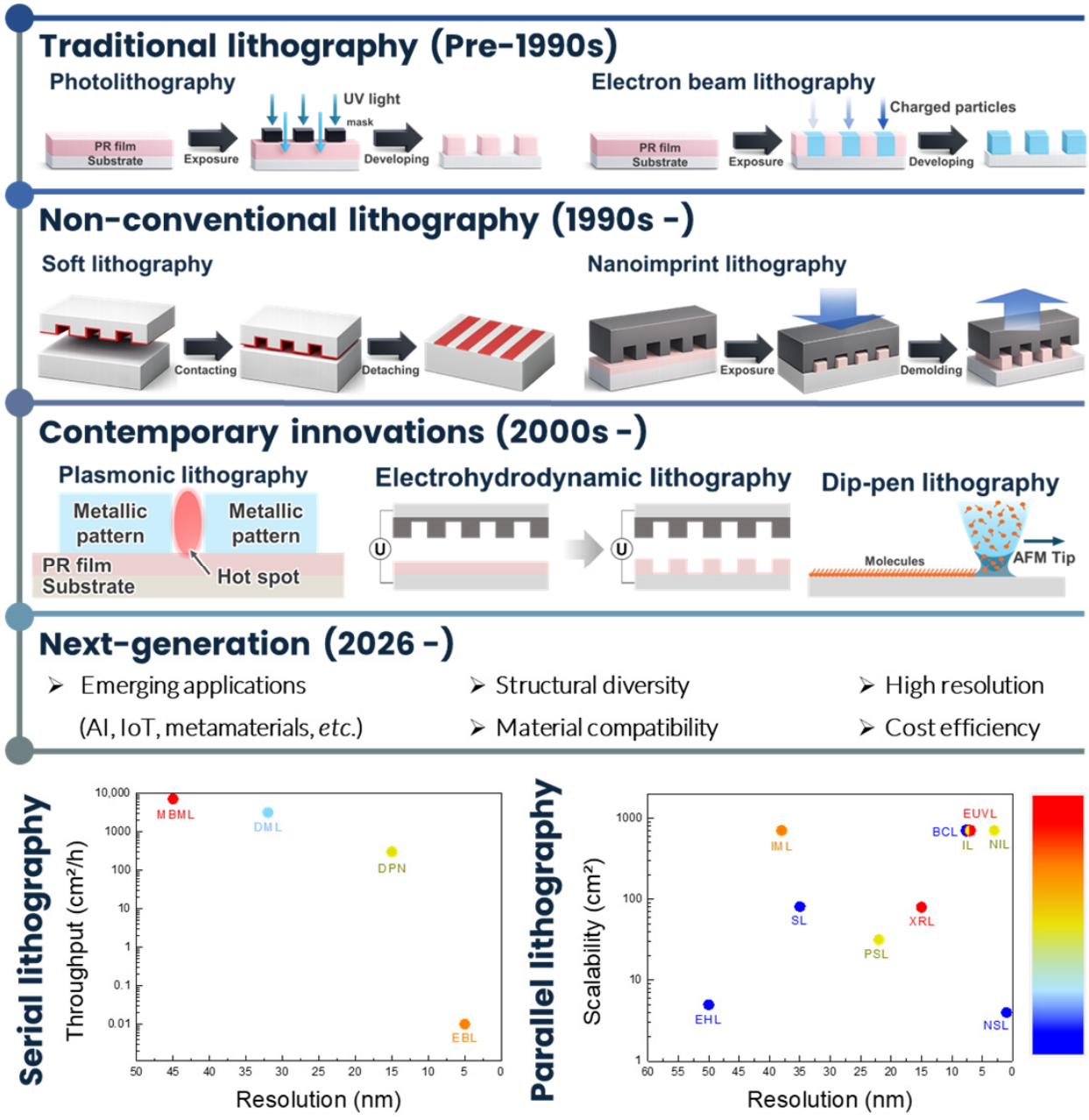

Figure 1. Chronological evolution of lithographic techniques. Patterning methods are classified into traditional, non-conventional, and contemporary innovations. Adapting recent trends for AI technology or IoT devices, next-generation lithography will be highly demanded. Inset plots summarize key trade-offs. The serial-lithography map (resolution–throughput–cost) compares serial techniques, with cost encoded by the color scale (low → high). The parallel-lithography map (resolution–scalability–cost) compares parallel techniques, again with cost represented by color [11,31,32,60,65–72].

Recent technological trends in artificial intelligence (AI), Internet of Things (IoT) devices, metamaterials, and wearable and bio-integrated systems continue to push requirements for next-generation lithography [73–82]. For example, the reliable fabrication of metamaterials and metasurfaces demands cost-effective patterning of intricate micro and nanoscale architectures, often with diverse inorganic materials and, in some cases, three-dimensional geometries [83,84]. These emerging requirements amplify the need for patterning strategies that can be compared on a common basis, because application viability is frequently determined by the coupled constraints of throughput, registration, defectivity, and total cost rather than by resolution alone. In this review, lithographic techniques are not compared solely by achievable resolution, but by whether they can simultaneously satisfy four manufacturing constraints: scalable throughput, reliable overlay and alignment, low defectivity within a practical process window, and cost predictability at scale. This perspective reframes nanolithography not as a resolution competition, but as a manufacturing discipline in which system-level integration ultimately determines viability. Unlike prior reviews that catalog lithographic techniques primarily by resolution or novelty, this work is explicitly structured to support decision-making under manufacturing constraints, addressing a gap between academic demonstrations and industrial adoption [11,31,32,60,65–72].

2. Traditional Lithography

Conventional lithographic methods have long underpinned semiconductor manufacturing and MEMS fabrication, enabling a broad range of micro and nanoscale devices. In the traditional era, photolithography established the high-volume benchmark by combining high throughput with reliable alignment and overlay control, yet continued scaling becomes increasingly constrained by diffraction-limited resolution and by the rising cost and process complexity associated with shorter exposure wavelengths, higher NA, and multipatterning. High-resolution alternatives such as electron beam lithography and X-ray lithography extend patterning capability beyond optical limits, but their industrial adoption is primarily restricted by manufacturing bottlenecks tied to throughput and cost, including serial write-time limits in EBL and the source, beamline, and mask infrastructure challenges in XRL. This section, therefore, introduces the basic principles, strengths, and limitations of PL, EBL, and XRL, and summarizes their dominant industrial bottlenecks and scalability-limiting parameters in Table 1. In Table 1, throughput is reported for serial methods, whereas scalability is reported for parallel methods.

2.1. Conventional Photolithography

Photolithography (PL) transfers a pattern from a photomask onto a photoresist (PR) film coated on a substrate through mask-based exposure and development steps (Figure 2a) [18–20]. First, a substrate, typically a flat, rigid wafer (e.g., silicon), is uniformly coated with a thin PR layer. The PR can be positive, where the exposed regions become soluble and are removed during development, or negative, where the unexposed regions are removed. The PR-coated substrate is then aligned to the photomask, and the pattern is transferred to the PR by UV-based optical exposure through projection optics. Historically, exposure sources have progressed from i-line UV (365 nm) to deep-UV systems such as KrF (248 nm) and ArF (193 nm) to support continued scaling, while further optical extensions such as immersion and EUV are discussed in later sections. Upon exposure, photochemical reactions modify PR solubility, and subsequent development selectively removes either the exposed or unexposed regions, yielding a patterned PR image. This resist pattern is then transferred to the underlying layers by etching or lift-off, completing the patterning sequence.

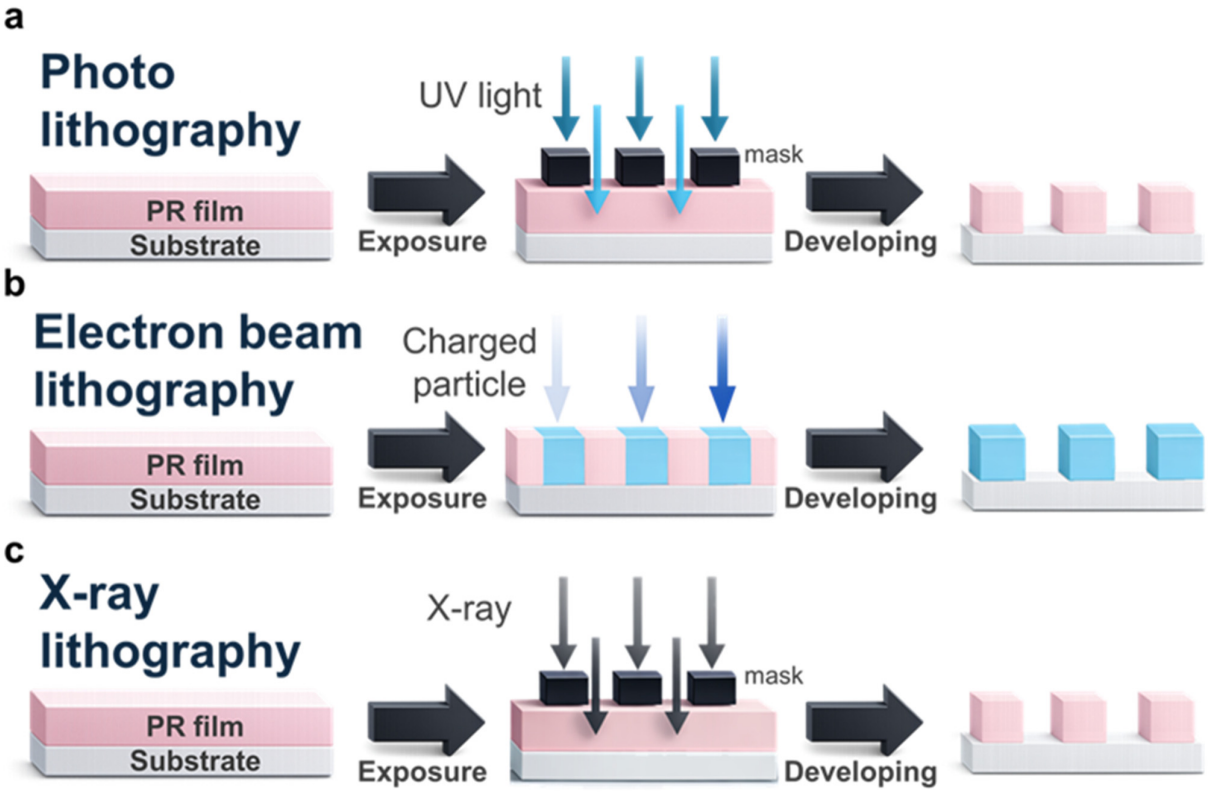

Figure 2. Schematic comparison of traditional lithographic processes. (**a**) PL uses a photomask and UV light to transfer the pattern onto a PR film on a substrate. (**b**) EBL uses a charged particle beam for direct writing on the PR surface without a mask. (**c**) XRL process utilizes an X-ray mask and X-ray exposure for patterning. These conventional methods require exposure and developing steps to generate patterned structures on the substrate.

PL remains the dominant manufacturing platform because it offers high throughput and robust overlay control enabled by mature tooling and standardized process integration. However, its resolution and pattern fidelity are fundamentally constrained by diffraction and process-window limits, which become increasingly restrictive as critical dimensions shrink [18]. In practice, continued scaling often requires shorter wavelengths, higher NA optics, and more complex process flows, which in turn increase cost and tighten defectivity and yield sensitivity.

Table 1. Summary of traditional lithographic techniques.

Technique	Strengths	Key Limitations	Industrial Bottleneck	Scalability-Limiting Parameter	Resolution (nm)	Throughput/ Scalability	TRL	Ref
Photo lithography (PL)	Mass production High throughput Alignment	Diffraction-limited resolution Multi-step flow	As finer patterns are required, the need for shorter exposure wavelengths, higher NA, and multipatterning drives a sharp rise in costs and process complexity.	Field size Stitching/overlay accumulation Focus/illumination uniformity	<1000	N/A->700 cm^2	8–9	[18–20]
Electron beam lithography (EBL)	Ultra-high resolution Maskless direct-write	Low throughput Proximity effect Beam instability	Although the resolution is excellent, the write speed (throughput) becomes a bottleneck, making it difficult to scale to large-area, high-volume manufacturing processes.	Dose per area Beam current Write time	<10	>0.01 cm^2/h N/A	7–9	[27,85–100]
X-ray lithography (XRL)	Short wavelength Deep penetration	Source/beamline X-ray mask	It is difficult to supply high-performance X-ray sources and low-defect X-ray masks economically, which limits industrial adoption.	Source irradiance uniformity Mask defect density Mask flatness/ thermal distortion	<20	N/A >50 cm^2	3–6	[28–30,101–110]

Manufacturing bottleneck summary: PL is typically resolution and defectivity limited at advanced nodes, with cost escalating as process complexity and patterning requirements increase, while throughput and overlay remain relative strengths.

2.2. Electron Beam Lithography

Electron beam lithography (EBL) uses a focused charged-particle electron beam to directly write patterns on a PR film without a photomask (Figure 2b), enabling highly customized, high-resolution patterning [25–27]. In a typical process, a substrate is coated with an electron-sensitive resist such as polymethyl methacrylate (PMMA), with thickness chosen according to the targeted resolution and pattern-transfer requirements. A finely focused electron beam is then raster-scanned across the resist surface with an accelerating voltage typically in the range of 10 to 50 keV [111–116]. During exposure, the beam induces chemical changes in the resist, including chain scission in common positive resists (e.g., PMMA) and cross-linking in negative resists, thereby modulating solubility. Because the beam position, dose, and dwell time are digitally controlled from computer-aided design data, EBL provides maskless patterning with flexible layout updates compared with photolithography. After exposure, the resist is developed so that the exposed regions of a positive resist are removed, or the unexposed regions of a negative resist are removed, yielding a patterned resist image. The pattern is subsequently transferred to the underlying layers via etching, followed by resist removal to leave the final patterned structure [85–88].

EBL can achieve exceptional resolution, often below 10 nm, owing to the short de Broglie wavelength of electrons and the ability to focus the beam to a nanoscale spot [89–95]. However, its manufacturing scalability is fundamentally constrained by serial, point-by-point writing, which imposes a throughput ceiling and drives high cost per patterned area [96]. In addition, proximity effects from electron scattering, resist charging, thermal drift, and beam instability can degrade critical-dimension control and uniformity, increasing defectivity risk and complicating process control [32,87,88,97–100].

Manufacturing bottleneck summary: EBL is primarily throughput-limited by serial exposure and consequently cost-limited for large-area production, while overlay and defectivity are often constrained by proximity effects, tool stability, and resist charging during scale-up.

2.3. X-Ray Lithography

X-ray lithography (XRL) uses short-wavelength X-ray exposure in combination with an X-ray mask to transfer patterns onto an X-ray-sensitive resist (Figure 2c), offering a potential route to high-resolution patterning beyond conventional UV optics [28–30]. In a typical configuration, the mask comprises a thin X-ray-transparent membrane (e.g., silicon carbide or related materials) patterned with a high-contrast absorber that blocks incident X-rays to define the desired layout. The substrate is coated with an X-ray-sensitive resist, and X-rays transmitted through the mask selectively expose the resist, inducing chemical changes in the exposed regions. After exposure, the resist is developed to create a patterned resist image, which is then transferred to the underlying layers by etching, followed by resist stripping to reveal the final pattern.

The short wavelength and high penetration depth of X-rays enable reduced diffraction effects, supporting fine patterning and, in some implementations, thick, high-aspect-ratio structures [101–106]. However, despite its resolution potential, XRL has faced persistent manufacturing barriers that map directly onto cost, throughput, and integration complexity. High-performance X-ray sources and beamline infrastructure are difficult to supply and operate economically, and X-ray mask fabrication and handling introduce additional challenges, including mask defect density, mask flatness, and thermal distortion, all of which

can degrade pattern fidelity and yield [107–110]. Source irradiance uniformity and the associated process window also become scalability-limiting factors as the patterning area increases. As a result, XRL has remained primarily confined to research and specialized niche applications, rather than being adopted as a mainstream high-volume manufacturing platform [30].

Manufacturing bottleneck summary: XRL is predominantly cost- and infrastructure-limited (sources, beamlines, and mask fabrication), with scalability additionally constrained by mask defectivity and stability and by source irradiance uniformity during large-area exposure.

3. Non-Conventional Lithography

Non-conventional lithography, introduced in the 1990s, encompasses diverse innovative techniques developed to overcome the practical constraints of traditional top-down lithography. In particular, to address two persistent issues, diffraction-limited resolution and escalating cost and process complexity, a broad set of alternative patterning routes was investigated during this period, and many continue to evolve today. By leveraging alternative physical, chemical, or mechanical mechanisms, non-conventional patterning methods expand the toolkit for micro and nanoscale fabrication and often enable materials-compatible and application-tailored patterning beyond conventional optical workflows. At the same time, their path to scale-up is typically determined by manufacturing-relevant bottlenecks, including throughput, overlay (registration), defectivity, and integration with established process flows. This section discusses six prominent non-conventional lithographic methods, IL, SL, NIL, BCL, NSL, and DPN, introducing their principles, strengths, and limitations, and summarizing their industrial bottlenecks, scalability-limiting parameters, and conceptual technology readiness levels in Table 2. In Table 2, throughput is reported for serial methods, whereas scalability is reported for parallel methods.

Table 2. Summary of non-conventional lithographic techniques.

Technique	Strengths	Key Limitations	Industrial Bottleneck	Scalability-Limiting Parameter	Resolution (nm)	Throughput/ Scalability	TRL	Ref
Interference lithography (IL)	Maskless Large-area periodic patterns	Periodic-only Limited arbitrary/complex patterns	Maintaining wafer-scale fringe stability (phase/coherence + vibration/thermal control) is the main hurdle for industrial use	Coherence/phase stability Vibration/thermal drift Fringe contrast uniformity	<10	N/A- >700 cm^2	4–6	[33,34,117–130]
Soft lithography (SL)	Flexible/curved substrates Low cost	Stamp/mold deformation Master dependence	Large-area, high-volume replication is limited by stamp deformation and consistent pattern fidelity	Contact uniformity Swelling/solvent compatibility	<50	N/A >50 cm^2	4–6	[31,35,131–135]
Nanoimprint lithography (NIL)	Sub-10 nm resolution Parallel replication	Particle/air trapping defects Template wear Release issues	Defect control (particles) and template lifetime/yield are the dominant barriers to HVM scaling	Pressure/gap uniformity Residual-layer uniformity	<10	N/A >700 cm^2	6–8	[37–39,136–143]
Block copolymer lithography (BCL)	~10 nm natural pitch Large-area potential	Defect density Limited pattern diversity Long anneal	Achieving wafer-scale low-defect ordering with accurate alignment/registration is the key challenge	Ordering correlation length Guide-pattern uniformity	<10	N/A >700 cm^2	4–6	[43,44,144–164]
Nanosphere lithography (NSL)	Low cost Simple process	Limited ordering control Low placement precision	Making defect-free, uniform monolayers over large areas with controlled ordering is the main bottleneck	Sphere monodispersity Monolayer uniformity	<10	N/A >4 cm^2	4–6	[40,41,165–169]
Dip-pen nanolithography (DPN)	High precision Multi material Direct-write flexibility	Very low throughput Tip wear Ink diffusion/blur	Throughput is the fundamental limit for scaling to large-area manufacturing.	Write speed Tip-array parallelization	<20	300 cm^2/h N/A	2–4	[46,70,170–193]

3.1. Interference Lithography

Interference lithography (IL), first explored for nanoscale patterning in the late 1990s, produces periodic structures in a photosensitive resist by exploiting the interference of two or more coherent laser beams [6,31,32]. As schematically shown in Figure 3a, an expanded 355 nm laser beam is split into two coherent beams and redirected by reflectors to intersect on the substrate at an angle θ, generating a spatially periodic intensity distribution [194]. The photoresist (or target surface) is selectively modified according to these interference fringes, enabling rapid formation of large-area periodic microstructures, with the pattern pitch primarily governed by the wavelength and intersection geometry. Representative SEM images (Figure 3b–e) illustrate how the resulting microstructure morphology and contrast vary with laser fluence, highlighting fluence as a practical knob for tuning feature definition and depth [194]. The achievable pitch and feature size are primarily dictated by the exposure wavelength and the interference geometry, particularly the angle between the interfering beams, and sub-50 nm periodic features can be obtained with appropriate optical configurations.

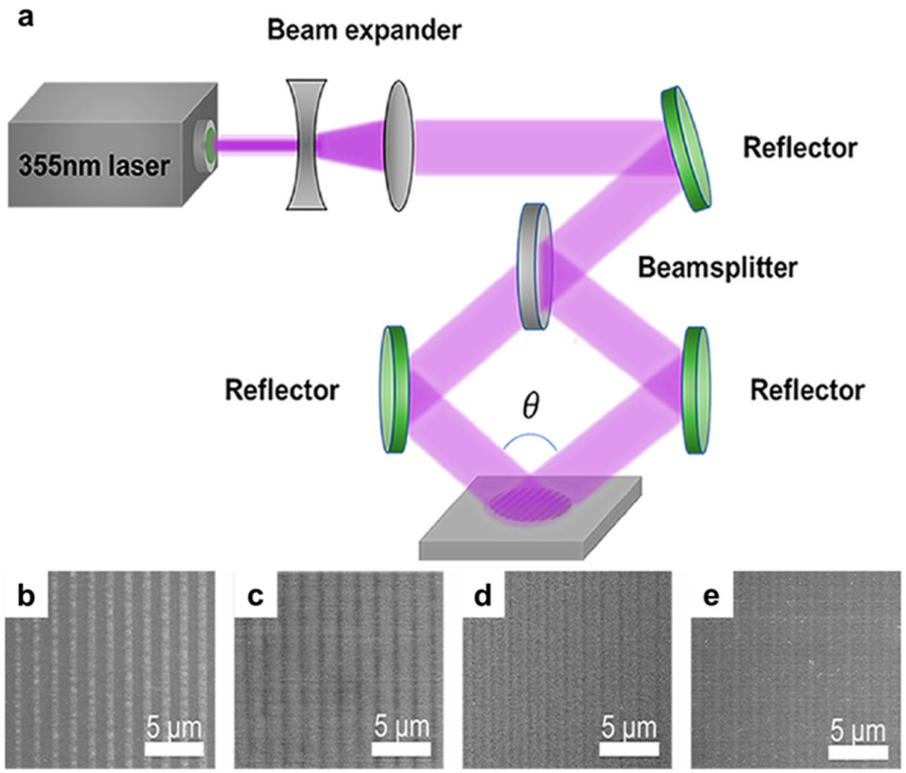

Figure 3. (**a**) The schematic image of the fabrication of periodic microstructures by laser interference. (**b**–**e**) SEM images of microstructures with laser fluences. Reprinted from Ref. [194], © 2020 MDPI (CC BY 4.0).

Because IL is a maskless, optical parallel process, it is well suited for large-area, high-throughput patterning of regular periodic structures at relatively low cost, making it attractive for diffraction gratings, photonic crystals, and other periodic nanostructures [117]. However, IL is intrinsically constrained in pattern versatility, because arbitrary and aperiodic layouts cannot be generated without additional optical complexity or hybrid process steps [125,126]. In addition, maintaining pattern fidelity over large areas requires precise alignment and stability of the optical setup, including beam coherence, vibration control, and dose uniformity, which can increase system complexity and cost [120,122,123,127–130].

Manufacturing bottleneck summary: IL is typically limited by overlay and pattern versatility for device-level integration, while throughput is a relative strength; defectivity

and cost are governed by exposure stability and uniformity requirements during large-area processing. As a result, IL is best suited for large-area periodic structures such as gratings, photonic crystals, and metasurfaces, where layout complexity and multilayer overlay are not critical. Its adoption in device-level manufacturing that requires arbitrary pattern definition and precise layer-to-layer registration remains fundamentally limited.

3.2. Soft Lithography

Soft lithography (SL), developed in the early 1990s, uses flexible elastomeric stamps, such as polydimethylsiloxane (PDMS), to transfer patterns through conformal contact with a substrate [32]. Compared with rigid imprint-based processes, SL typically requires no high pressure or elevated temperature, making it a relatively low-energy and materials-compatible route for patterning. In practice, a soft stamp is used to replicate or print patterns via several modes, including microcontact printing [131–133], replica molding [134], and microtransfer molding [135]. In microcontact printing, an elastomeric stamp is first inked with molecular or nanoparticle "inks" and then brought into conformal contact with the substrate, transferring the ink only at the contacted regions (Figure 4a). Representative AFM images of the printed nanopatterns (Figure 4b,c) confirm faithful replication of periodic line features at the micro-/nanoscale, while the corresponding height profiles indicate well-defined topographic contrast after transfer [195]. Depending on stamp fidelity, ink chemistry, and process control, SL can achieve feature sizes on the order of tens to hundreds of nanometers, and it is technically compatible with curved or irregular surfaces. Because of this versatility, SL has been applied to flexible and unconventional substrates for applications including wearable electronics, microfluidics, and biomedical and bio-integrated systems [31,196,197].

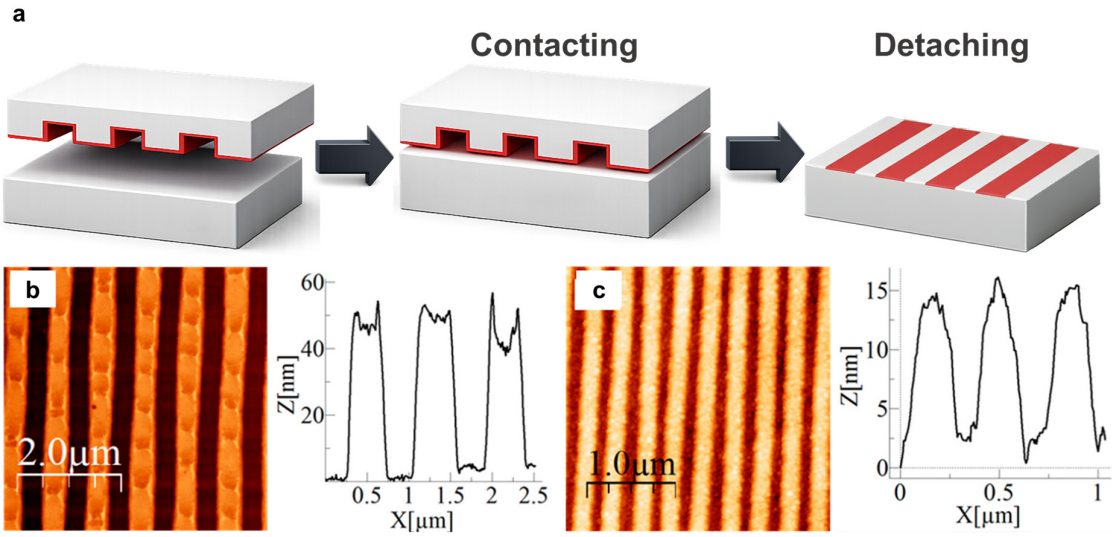

Figure 4. (**a**) Schematic representation of SL process in microcontact printing mode. (**b**,**c**) AFM images of the nanopattern fabricated by soft lithography. Reprinted from Ref. [195], © 2017 MDPI (CC BY 4.0).

Despite these advantages, SL faces intrinsic limitations in pattern fidelity and registration. Elastomeric stamps can deform during contact, leading to pattern distortion, linewidth variation, and reduced placement accuracy, particularly over large areas. Achieving finer features and better uniformity often requires high-quality master templates and tightly controlled stamp fabrication to minimize shrinkage, swelling, and mechanical creep. In addition, because SL relies on repeated contact between the stamp and substrate, practical manufacturing can be limited by contamination, ink transport nonuniformity, and stamp wear, all of which increase defectivity and degrade reproducibility over multiple cycles.

Manufacturing bottleneck summary: SL is most often limited by overlay and defectivity arising from stamp deformation and contact-induced variability, while cost and materials compatibility are relative strengths; throughput can be favorable for large-area replication when uniform contact and ink delivery are maintained.

3.3. Nanoimprint Lithography

Nanoimprint lithography (NIL) transfers nanoscale features onto a resist-coated substrate by mechanically replicating a pre-patterned mold under applied pressure [37–39]. Compared with projection-based photolithography, NIL can be cost-effective because it avoids complex imaging optics, and it can achieve high resolution without electron-beam exposure during pattern transfer. The NIL process begins with the preparation of a mold, typically fabricated from rigid materials such as silicon or quartz, in which nanoscale features are defined using high-resolution patterning methods (often including EBL) and subsequent pattern-transfer steps. The target substrate is coated with a thin polymer resist layer, which can be either a thermoplastic polymer or a UV-curable formulation [38,136]. As schematically illustrated in Figure 5a, the mold is brought into conformal contact with the resist and pressed under controlled conditions. For thermoplastic resists, the system is heated above the glass transition temperature to soften the resist and allow mold features to be embossed. For UV-curable resists, UV exposure is applied while the mold is in contact to crosslink and solidify the resist. After solidification, the mold is released, yielding a negative replica of the mold topography in the resist.

NIL can achieve sub-10 nm resolution by relying on mechanical replication rather than optical imaging, thereby avoiding diffraction-limited constraints [138,139]. Because imprinting is inherently a parallel replication process, nanoimprint lithography (NIL) is attractive for large-area nanopatterning with high pattern fidelity [139–143]. As shown in the process schematic (Figure 5a), pattern transfer is achieved through conformal contact, pressing, and demolding, enabling rapid replication once a master mold is prepared. Representative AFM data (Figure 5b) highlight both the high-fidelity transfer and the practical sensitivity to defectivity, where particle contamination or trapped defects at the mold–resist interface can propagate into catastrophic pattern defects over large areas [198,199]. Repeated mold use can also lead to wear or damage that progressively degrades yield [37,136]. In addition, overlay (registration) across multiple layers can be challenging because mechanical contact, resist flow, and demolding may introduce distortion and nonuniform residual layers, particularly at high feature density. These issues can be further amplified on compliant or flexible substrates due to pressure-induced substrate deformation, necessitating specialized tooling and process optimization. Despite these challenges, NIL has been widely employed in nanophotonic devices [200,201], biomimetic studies [202–204], biosensors [205–207], and advanced optoelectronics, where controlled nanoscale sizes and shapes are often essential [137,199,208].

Manufacturing bottleneck summary: NIL is typically defectivity-limited by particle contamination and mold-related defects during contact replication, with overlay and distortion becoming critical for multilayer integration; cost can be favorable at scale, while throughput is a relative strength once defect and alignment control are established.

3.4. Block Copolymer Lithography

Block copolymer lithography (BCL), introduced in the late 1990s, exploits the thermodynamic self-assembly of block copolymers to generate periodic nanoscale morphologies (Figure 6a) [43,144–151]. Block copolymers undergo microphase separation driven by segmental immiscibility and chain connectivity, producing ordered domains such as spheres and cylinders (Figure 6b) [152–154]. Thermal or solvent annealing promotes domain forma-

tion and ordering, and the resulting pitch and morphology are governed by molecular parameters including chain length, block volume fraction, and interaction strength [155–160]. After self-assembly, one block can be selectively removed or converted through etching, leaving a nanopatterned template that can be transferred to the underlying substrate.

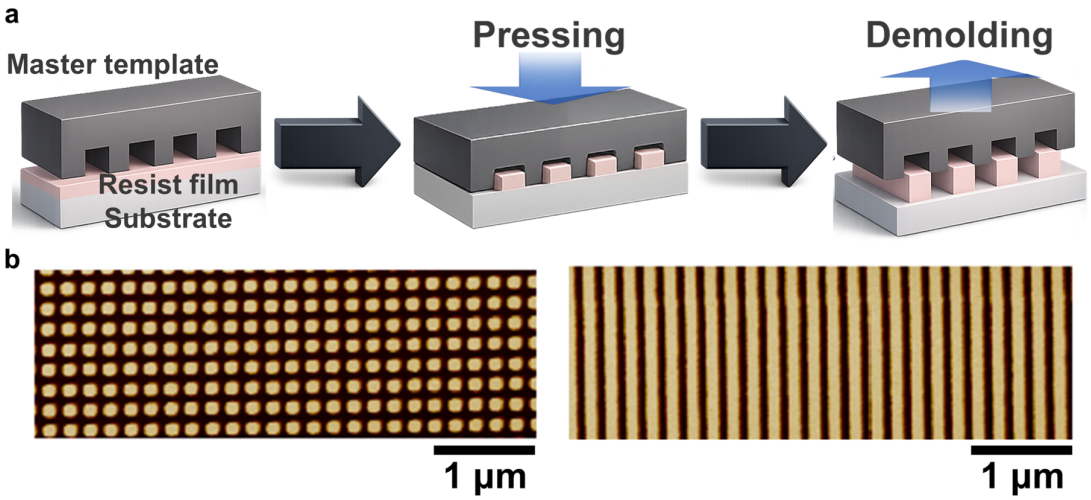

Figure 5. (**a**) Schematic representation of NIL process. (**b**) AFM data for the nanopatterns transferred by NIL process. Reprinted from Ref. [199], © 2024 MDPI (CC BY 4.0)

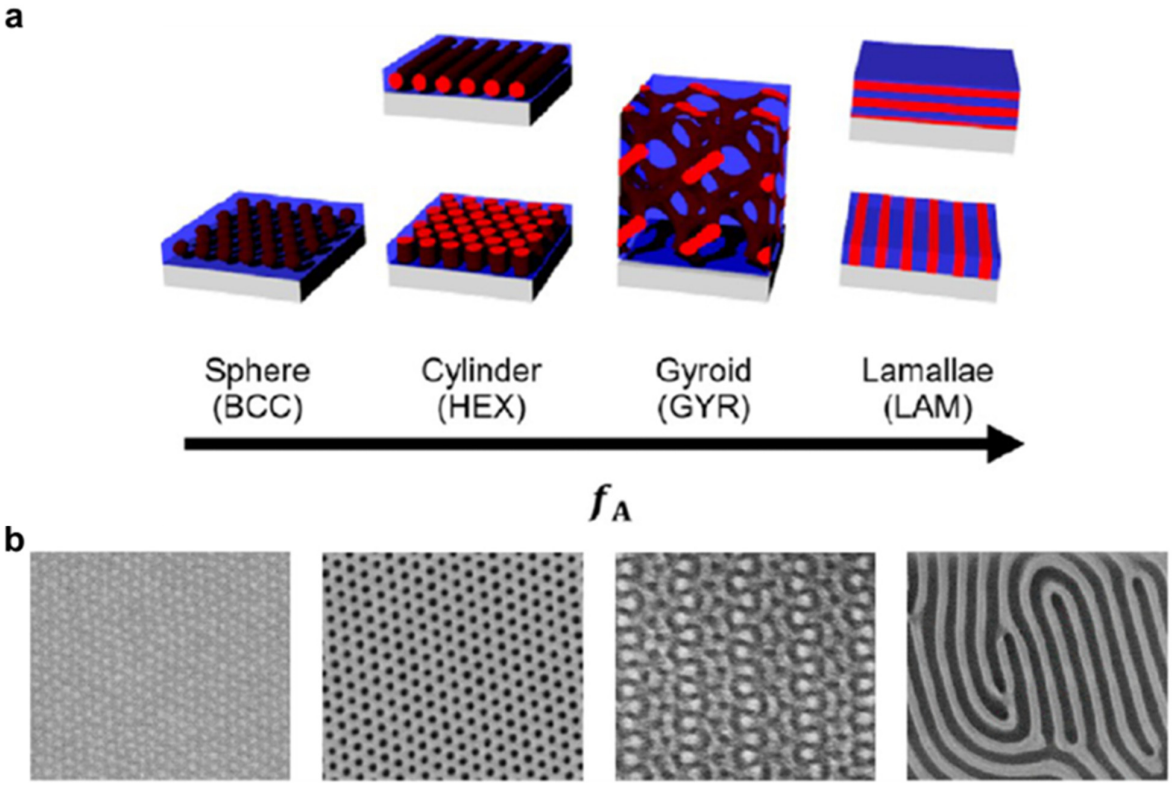

Figure 6. (**a**) Schematic illustration of block copolymer phase according to volume fraction (f_A). (**b**) SEM images show different phases of block copolymers. Reproduced with permission from Ref. [163]. © 2022 American Chemical Society.

By harnessing thermodynamically defined domain spacing, BCL can deliver feature sizes on the order of 10 nm, enabling applications in nanophotonics [152,153,161], advanced electronic pattern density extension concepts [162,163], and functional surfaces such as

liquid-repellent re-entrant arrays [164] and antibacterial nanostructures [209]. This resolution advantage originates from microphase separation, where the characteristic pitch is set by molecular length scales rather than by optical imaging, making pattern formation intrinsically parallel and attractive for large-area nanopatterning.

At the same time, the same physics that enables parallel self-assembly also defines BCL's practical scope. Self-assembly naturally generates periodic order, but it does not inherently provide deterministic, layout-defined placement of features across arbitrary device patterns. Consequently, BCL is best viewed not as a general replacement for layout-driven lithography, but as a density-multiplication or periodic-patterning strategy whose manufacturability is limited by registration and defect statistics at scale. Wafer-scale ordering is constrained by slow defect annihilation and kinetic trapping, which can leave dislocations, disclinations, orientation variability, and line-edge or line-width roughness that become yield-limiting as the patterned area increases. Directed self-assembly approaches using chemical or topographic guides can improve alignment and reduce defectivity, but they primarily shift the bottleneck to the quality and overlay of the guiding patterns and to narrow process windows, and they do not guarantee deterministic convergence to a uniformly low-defect state within manufacturing-relevant time scales [144,163]. In practice, this means that BCL is most compelling when the target pattern can tolerate periodicity and when the integration flow can supply high-quality guiding templates, rather than in applications that require arbitrary, placement-accurate layouts.

Manufacturing bottleneck summary: BCL is predominantly overlay- and defectivity-limited because deterministic placement and low-defect ordering are not intrinsic to self-assembly; throughput can be favorable due to parallel formation, but viable deployment depends on guide quality, process-window stability, and defect suppression at wafer scale. Therefore, BCL should be regarded as a density-multiplication or periodic-patterning strategy rather than a general replacement for layout-driven lithography. While sub-10 nm features are readily achievable, the lack of intrinsic deterministic placement and the difficulty of achieving wafer-scale, low-defect ordering with reliable registration fundamentally constrain its role in advanced semiconductor manufacturing.

3.5. Nanosphere Lithography

Nanosphere lithography (NSL) is a bottom-up nanopatterning approach developed in the mid-to-late 1990s that uses the self-assembly of colloidal spheres to form an ordered mask for subsequent pattern transfer [40,41]. Nanospheres, commonly composed of silica, PMMA, or polystyrene (PS), can self-assemble into closely packed hexagonal monolayers on a substrate [41]. As schematically illustrated in Figure 7a, the assembled sphere array can be modified (e.g., by controlled sphere shrinking), followed by material deposition or etching, and subsequent sphere removal to yield periodically ordered nanostructures [210]. Figure 7b,c show representative morphologies of dispersed and etched nanospheres, highlighting how sphere packing and post-processing steps govern the effective mask geometry and, consequently, the transferred pattern. Photographs in Figure 7d–f further demonstrate large-area PS-sphere monolayers formed on different surfaces, underscoring the practical scalability of NSL beyond small coupons [211]. A key practical attraction of NSL is its simplicity and scalability, including demonstrations of large-area PS-sphere monolayers on the meter scale [41,124]. Because the sphere array functions as a reusable, parallel mask, NSL can generate a range of periodic nanostructures such as nanopillars, nanodots, and nanoholes with relatively low equipment complexity. Accordingly, NSL has been widely used in applications including surface-enhanced Raman scattering (SERS) [165,166], photonics [167,168], and plasmonics [169], where periodic nanostructures and large-area coverage can be more important than arbitrary layout definition.

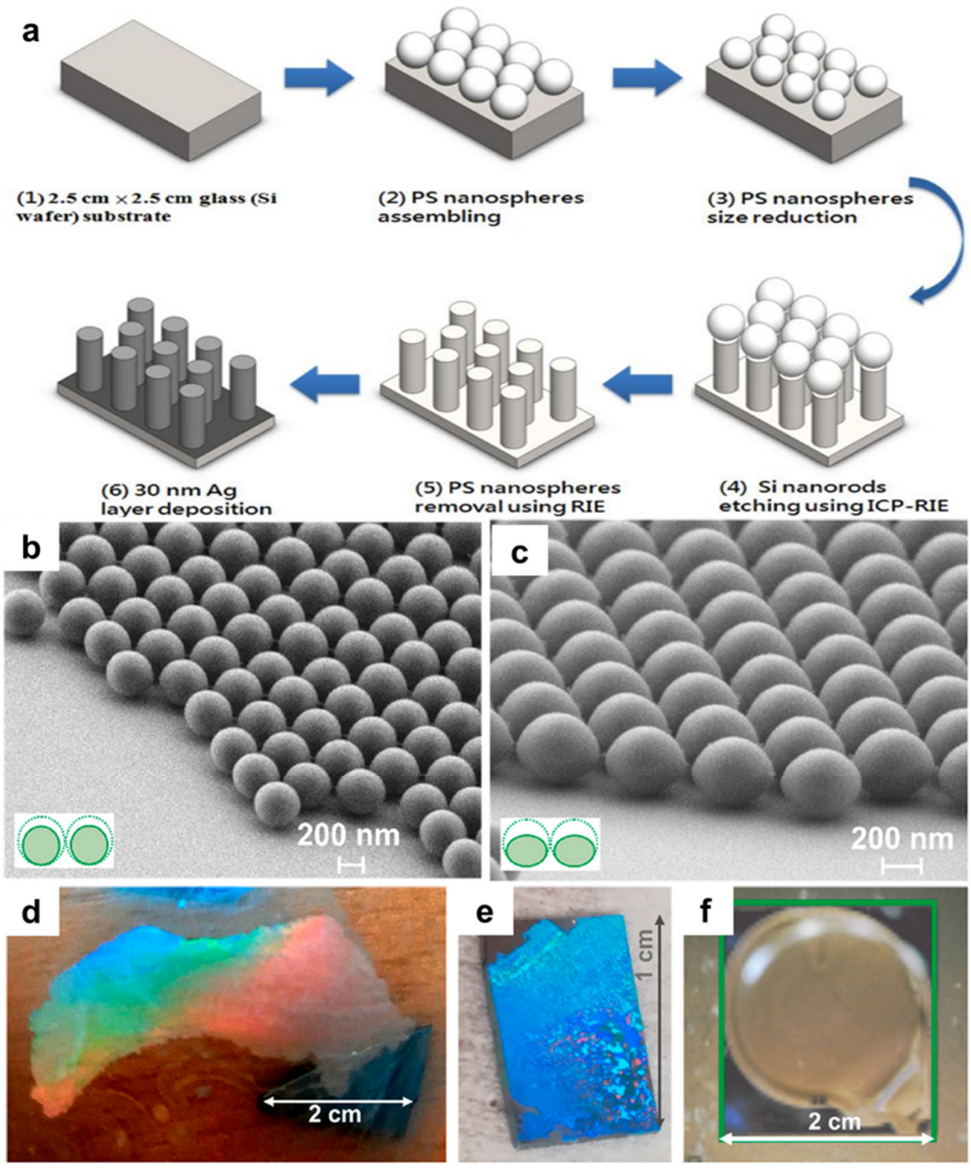

Figure 7. (**a**) Schematic diagram of the basic steps for creating ordered nanostructures through nanosphere mask. Reprinted from Ref. [210], © 2019 MDPI (CC BY 4.0) (**b**,**c**) Morphology of dispersed and etched nanospheres. The green inset schematics highlight the sphere shape change before and after etching. (**d**–**f**) Photographs of the PS-sphere monolayer on different surfaces. Reprinted from Ref. [211], © 2022 MDPI (CC BY 4.0).

Despite these strengths, NSL is best interpreted as a periodic, self-assembly defined patterning route rather than a general replacement for layout-driven lithography. Pattern quality is strongly dependent on the uniformity and long-range ordering of the nanosphere array, yet achieving reproducible monolayers requires tight control over sphere size distribution, solvent conditions, deposition parameters, and defect formation during assembly. In addition, pattern dimensions and placement are intrinsically coupled to sphere diameter and packing geometry, which limits deterministic control of feature arrangement and reduces design freedom for device-like layouts. These constraints motivate ongoing efforts to improve ordering control, defect suppression, and pattern tunability through modified assembly protocols, templated guidance, and hybrid integration schemes.

Manufacturing bottleneck summary: NSL is predominantly defectivity- and overlay-limited because long-range order and deterministic placement are not intrinsic to self-assembly; throughput and cost can be favorable due to parallel large-area masking, but

scalability depends on reproducible monolayer formation and low defect density across the target area.

3.6. Dip-Pen Nanolithography

Dip-pen nanolithography (DPN) employs the tip of an atomic force microscope (AFM) as a nanoscale "pen" to directly deposit functional inks onto a substrate (Figure 8a) [46,172–175]. As schematically illustrated in Figure 8a, an inked AFM tip delivers material to the surface through a nanoscale meniscus mediated by surface tension and interfacial interactions, while the tip trajectory is controlled by a computer-guided positioning system [175,182]. The ink can consist of molecular precursors, nanoparticles, polymers, or biomolecules, enabling direct-write patterning with high compositional selectivity and placement control [177–181]. AFM imaging is frequently used to verify the written features and surface morphology (Figure 8b) [192,193]. DPN can achieve feature sizes on the order of tens of nanometers, and arrays of nanoscale dots can be printed with controlled spacing and size [176]. Because ink chemistry is highly tunable and substrates can be diverse, DPN is particularly useful for applications that require localized functionalization and customization, including biosensors [70,190] and selected quantum or nanoelectronic devices [191].

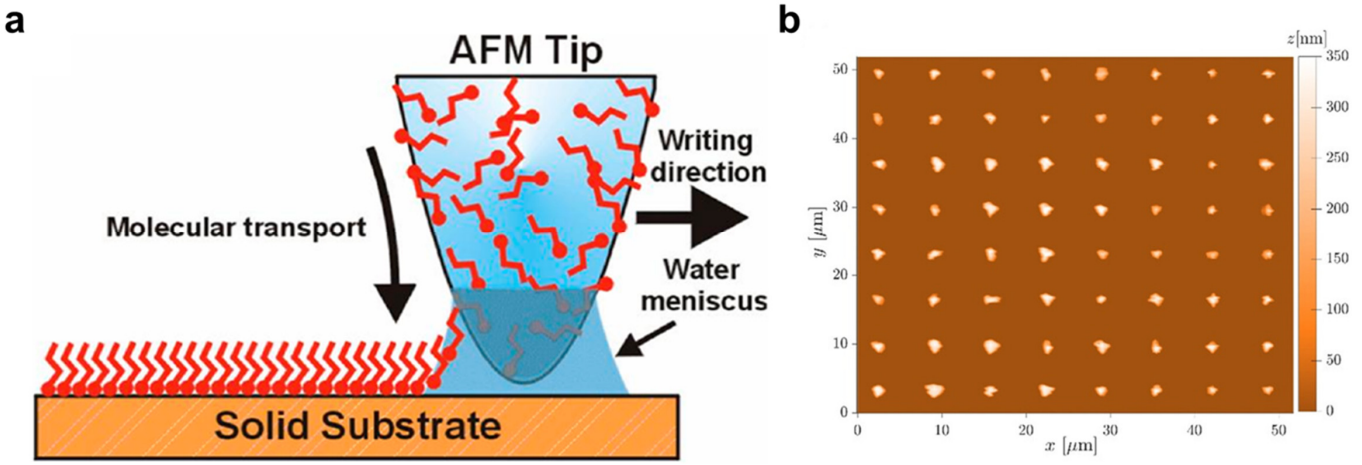

Figure 8. (**a**) Schematic representation of DPN process (**left**). Reproduced with permission from Ref. [192], © 2020 American Chemical Society. (**b**) AFM image of patterned surface (**right**). Reproduced with permission from Ref. [193]. © 2024 Wiley-VCH.

Nevertheless, DPN is fundamentally constrained by its serial writing nature, which imposes a severe throughput limitation and makes large-area manufacturing economically challenging. In addition, pattern reproducibility can be sensitive to environmental conditions such as humidity and temperature, because these factors affect ink transport, meniscus formation, and deposition kinetics, often necessitating controlled operating conditions [192,193].

Manufacturing bottleneck summary: DPN is primarily throughput-limited (serial direct writing) and therefore cost-limited for large-area patterning; defectivity and uniformity are strongly influenced by environmental sensitivity and ink transport stability, while overlay is generally strong for local placement within the tool's positioning capability. Consequently, DPN is most appropriate for research, prototyping, and application-specific functionalization where pattern customization and material selectivity outweigh throughput considerations. Its extension to large-area or high-volume manufacturing remains economically impractical due to its intrinsically serial writing nature.

4. Contemporary Innovations

Since the early 2000s, lithographic methods have made great strides to effectively overcome the drawbacks of conventional and non-conventional nanopatterning techniques. In addition to extending established optical platforms, this period also introduced new patterning concepts that leverage near-field interactions, plasmonics, and field-driven film instabilities. By drawing on novel physical phenomena such as plasmonics, evanescent waves, and film instability, innovative nanopatterning approaches have been developed to create structurally diverse nanopatterns with low costs while improving the versatility and scalability. These contemporary innovations have broadened both device targets and integration contexts, enabling applications that span advanced semiconductor patterning, functional surfaces, and emerging form factors. However, ongoing studies continuously explore how to balance exceptional resolution with manufacturing-relevant requirements, including throughput, overlay (registration), defectivity, and cost, while maintaining compatibility with practical process integration. This section introduces several innovative patterning approaches with their basic mechanisms, benefits, and challenges. Table 3 provides a comparative overview of contemporary innovations in terms of strengths, key limitations, industrial bottlenecks, scalability-limiting parameters, and conceptual technology readiness levels (TRL).

Table 3. Summary of contemporary innovations.

Technique	Strengths	Key Limitations	Industrial Bottleneck	Scalability-Limiting Parameter	Resolution (nm)	Throughput/ Scalability	TRL	Ref
Immersion lithography (IML)	High resolution Infrastructure compatibility	Bubble/particle sensitivity Overlay complexity	At high NA, stable immersion meniscus control and wafer-scale cleanliness/overlay stability become increasingly difficult during fast scanning	Scan field Scan speed Meniscus stability Bubble/particle rate	<50	N/A >700 cm^2	8–9	[52,53,212–217]
Extreme ultraviolet lithography (EUVL)	High resolution Leading-edge enablement	Tool cost Source power/uptime Resist sensitivity	Source power and uptime directly constrain dose-limited scan speed, while mask/pellicle defects and stochastic resist behavior impact wafer-scale yield	Source power Scan speed Defect yield Exposure time	<10	N/A >700 cm^2	8–9	[218–229]
Digital maskless lithography (DML)	Mask-free Design flexibility	Limited resolution Low throughput	Resolution, projected field size, and throughput trade off against each other, and stitching overhead grows quickly for large-area patterns	Field size Stitching accuracy Step/scan speed	<50	>3000 cm^2/h N/A	4–6	[230–233]
Multi-beam maskless lithography (MBML)	Massive parallelization Higher throughput	System complexity Beam uniformity	Uniform beam performance across the full array and stable long-duration calibration are required, while data streaming and charging/thermal control must remain stable at high write rates	Multi beams Per-beam write rate Long-term calibration	<50	>7000 cm^2/h N/A	4–6	[61–63,234,235]
Plasmonic lithography (PSL)	Near-field super resolution	Plasmonic loss Hotspot heating	Large-area near-field enhancement is hard to keep uniform, and localized heating/loss can degrade materials and pattern fidelity	Near-field uniformity Gap/contact uniformity Thermal dissipation	<50	N/A >30 cm^2	2–4	[58,59,66,236–250]
Electrohydrodynamic lithography (EHL)	Diffraction-free Simple setup Low cost Rapid patterning	Gap sensitivity Viscosity dependence Dielectric breakdown	Wafer-scale uniformity depends strongly on nm-level gap control and field/thickness uniformity, and breakdown/defect probability increases with patterned area	Gap/E-field/Film-thickness uniformity Breakdown probability	<50	N/A >5 cm^2	3–5	[65,251–266]

4.1. Immersion Lithography

According to the definition of NA, NA = n sin (θ), increasing the refractive index (n) of the coupling medium enables a higher NA and thus improved optical resolution,

motivating the development of immersion lithography (IML) in the 2000s. Utilizing this physical concept, IML improves resolution by inserting a high-refractive-index liquid (typically water in ArF immersion systems) between the wafer and the projection lens (Figure 9a) [52,53]. By raising the effective NA, immersion can enhance resolution while maintaining a usable depth of focus and process latitude, supporting continued device scaling. Leveraging the optical properties of the immersion fluid, IML has enabled the miniaturization of semiconductor devices, as exemplified by dense line array patterns transferred by the IML process (Figure 9b) [212,213]. Because it has enabled the fabrication of features smaller than 45 nm, IML has emerged as the industry standard for advanced semiconductor nodes. IML is highly effective in mass production because it builds on established photolithographic infrastructure and step-and-scan manufacturing flows [53]. However, this strategy faces practical limitations related to bubble and particle sensitivity, meniscus stability, and wafer-scale cleanliness, as well as the high cost of maintaining complex immersion systems, despite its widespread use [213–215]. Furthermore, as NA approaches its theoretical and materials-imposed limits, further scaling increasingly relies on system-level co-optimization, including tighter overlay control, defectivity suppression, and complex patterning strategies, rather than on NA increases alone [216,217].

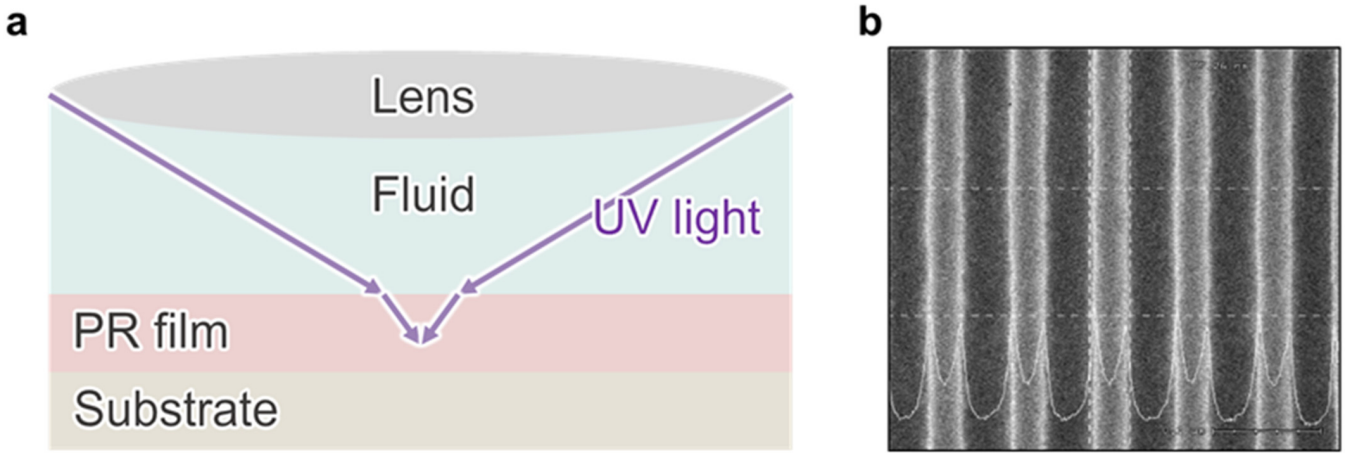

Figure 9. (**a**) Schematic representation of light traveling through lens, fluid, and PR film. (**b**) SEM image of 38 nm line array pattern transferred by IML process. Reprinted from Ref. [213], © 2022 MDPI (CC BY 4.0).

Manufacturing bottleneck summary: IML remains strong in throughput and overlay, but defectivity and cost become increasingly limiting due to contamination and bubble sensitivity and the added complexity of immersion-specific hardware and process control.

4.2. Extreme Ultraviolet Lithography

Progress in semiconductor manufacturing is intensively focused on reducing feature sizes to achieve faster and more advanced integrated circuits. This can be accomplished by lowering the exposure wavelength or increasing the NA of the projection lens in the system. Optical lithography has progressed through successive reductions in wavelength from 436 nm to 193 nm, followed by ArF immersion, to sustain continued node scaling [21,56]. Since the 2010s, extreme ultraviolet lithography (EUVL) using 13.5 nm wavelengths with the ultrahigh NAs has demonstrated the capabilities of reducing the resolution to below 10 nm, surpassing the capabilities of previously developed techniques. Instead of refractive lenses, reflected optical systems are utilized in the EUVL process due to the high EUV absorption of the equipment components (Figure 10a) [267]. The EUVL process requires a highly specialized EUV source, which is often a plasma created by powerful laser pulses

that target tin droplets. A reflective mask coated with many thin layers of silicon and molybdenum is used to define the pattern, which is then projected onto a resist-coated substrate. Because of its ultrahigh resolution (Figure 10b), EUVL has played a vital role in developing semiconductor industries until now. Future integrated circuits and transistors benefit from its high precision and ability to design denser, smaller patterns [218–222].

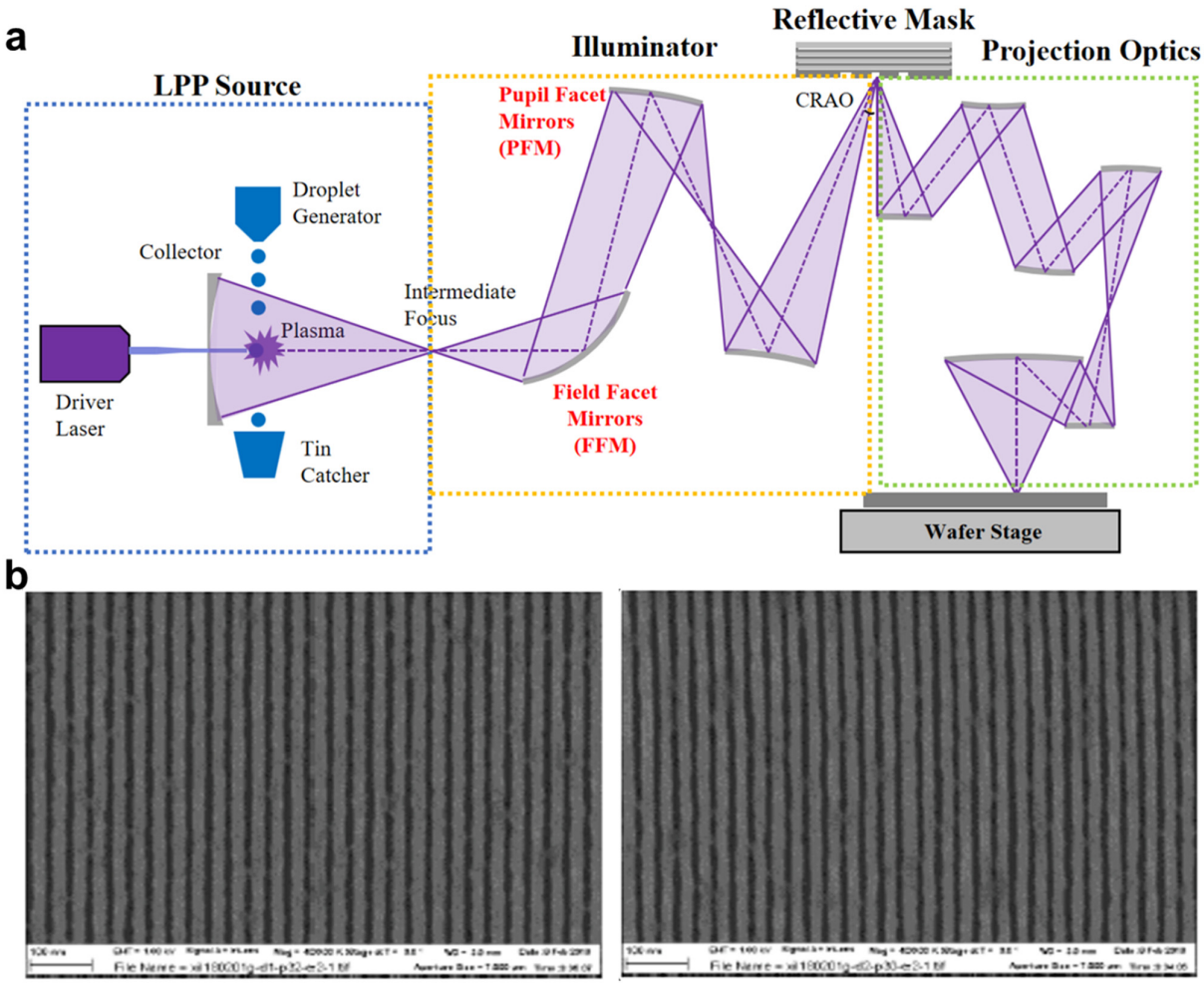

Figure 10. (**a**) Schematic image of the optical system for a EUVL process. Reprinted from Ref. [267], © 2025 MDPI (CC BY 4.0). (**b**) SEM images show the nanopatterns fabricated by EUVL (scale bar: 100 nm). Reproduced with permission from Ref. [268]. © 2018 American Chemical Society.

However, industrial scalability is governed less by nominal resolution than by coupled constraints in throughput, defectivity, and cost. Source efficiency and delivered EUV power directly limit throughput, while complex reflective optics, vacuum infrastructure, and contamination control drive high capital and operating costs. In addition, mask and pellicle defects, along with stochastic resist effects, can translate into wafer-scale yield loss, making defectivity control a central challenge for manufacturing adoption [223]. Furthermore, EUVL still requires the development of alternative PR material capable of producing dense patterns at the sub-10 nm scale [220,222,224,225]. To resolve these challenges, many researchers have extensively investigated how to improve its processing efficiency [56,57,226–229,268–271].

Manufacturing bottleneck summary: EUVL is primarily constrained by cost and defectivity. Throughput is limited by available source power and system uptime, while yield is adversely affected by mask-related defects and stochastic resist phenomena at advanced nodes.

4.3. Digital Maskless Lithography

In the traditional PL process, a physical photomask determines the patterning accuracy and quality. However, fabricating the photomask suitable for each patterning level is costly and technically challenging [230,231]. Motivated by this photomask issue, many efforts have been made to develop maskless lithography. Among these methods, maskless lithographic technique using digital light processing, known as digital maskless lithography (DML), has attracted great attention in the fields of industry and research. In the DML process, a pattern is initially prepared by design software and uploaded to the control system. The light for pattern transfer is followed by the trajectory of the uploaded pattern and accurately touches the patterning region. To achieve this, DML requires a digital micromirror device composed of many moving small mirrors, as illustrated in Figure 11a [231,272]. Depending on the tilted status and positions of mirrors, the incident light is properly guided to touch the targeted surface of the PR film [232,233]. Benefiting from this digital process, DML not only eliminates the need for expensive and time-consuming photomasks but also enables a customized patterning process and versatility. This mask-free, software-defined exposure is especially favored for application-driven manufacturing, where frequent design iterations and heterogeneous substrates can make mask-centric workflows inefficient. Especially, due to the recent advancements in AI technology, this digital patterning route will be continuously developing to further improve its lithographic capabilities.

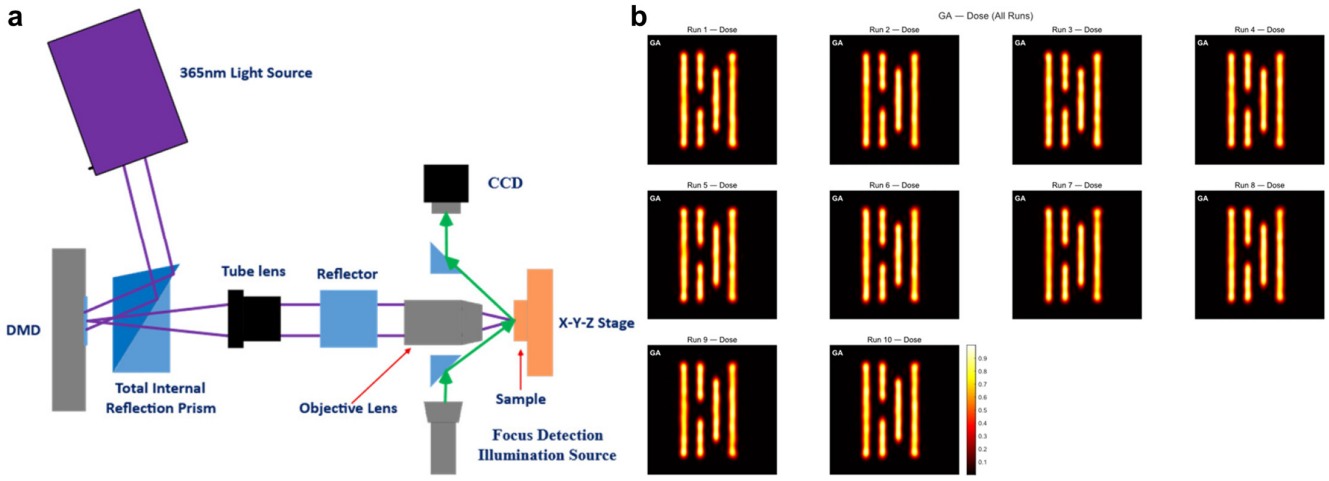

Figure 11. (**a**) Schematic representation of DML system. (**b**) Transferred line patterns. Reprinted from Ref. [272], © 2025 MDPI (CC BY 4.0).

Figure 11b shows representative transferred line patterns, demonstrating the feasibility of resist patterning through digitally controlled exposure [272]. Nevertheless, several drawbacks currently hinder broader adoption of DML. From a manufacturing perspective, DML is primarily constrained by throughput because exposure is typically performed over a limited field and must be stitched or scanned to cover large areas, which becomes considerably slower than high-volume mask-based projection. In addition, achievable resolution is strongly coupled to the DMD pixel size and projection optics, which can limit minimum feature size and pattern fidelity for advanced nodes [230]. When DML is applied to flexible or non-conventional substrates, the thermal budget of the resist and subsequent processing steps (e.g., baking/curing and post-exposure treatments) becomes an additional constraint that limits the usable process window.

Manufacturing bottleneck summary: DML is mainly throughput-limited for large-area production and can also be resolution-limited by pixel size; cost is favorable in low-to-medium volume use due to mask elimination, while overlay and defectivity increasingly

depend on stitching accuracy and calibration as patterned area grows. Accordingly, DML is best positioned for rapid prototyping, low-to-medium volume production, and heterogeneous integration scenarios where design agility is critical. In these heterogeneous platforms, manufacturability is governed not only by exposure performance but also by low-damage, low-temperature process compatibility across the full patterning and transfer flow. In contrast, for cost-sensitive HVM, its scalability is constrained by throughput and stitching overhead as pattern complexity and area increase.

4.4. Multi-Beam Maskless Lithography

Multi-beam maskless lithography (MBML) is an alternative patterning method using arrays of programmable electron beams or other focused energy sources, directly writing patterns onto a substrate without the need for conventional photomasks [61–63]. Unlike single-beam systems, this method achieves a very high resolution while greatly increasing throughput, making it ideal for fabricating intricate nanoscale structures [63,234,235,273]. A key enabler is the electron reduction optics that demagnify and project the emitter-array pattern onto the wafer through multi-element lens modules, allowing many beamlets to write in parallel within a defined focal field (Figure 12a) [273]. However, scaling to dense, stitched writing fields introduces stringent requirements on beam-to-beam uniformity, alignment, and aberration control; beamlet trajectories can exhibit distortion (e.g., field curvature and pincushion/barrel-type aberrations) without appropriate correction, directly impacting placement accuracy and pattern fidelity (Figure 12b) [273].

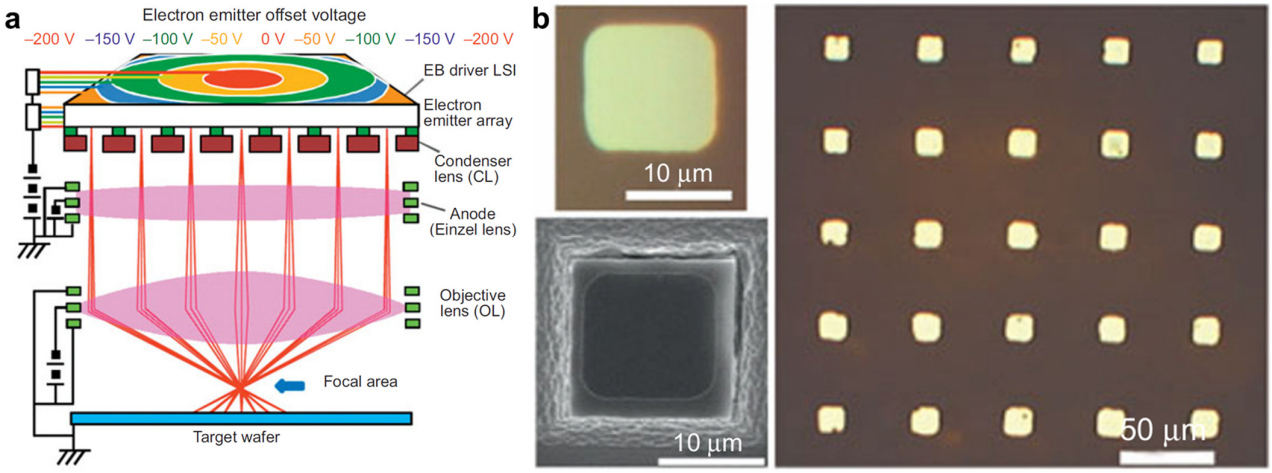

Figure 12. (**a**) Electron reduction optic system for MBML process. (**b**) Pattern image exposed by an arbitrarily selected 5 × 5 subset from the 200 × 200 electron emitter array. Reprinted from Ref. [273], © 2020 MDPI (CC BY 4.0).

MBML is attractive for applications that benefit from maskless flexibility and high patterning precision, including rapid prototyping, specialized microelectronics, and mask fabrication, where design updates and short turnaround times are important [63,234,235]. At the same time, large-scale deployment is governed by system-level constraints that scale with parallelization. High system complexity and capital cost remain major barriers, and stable operation at high write rates requires uniform beam performance across the full array, long-duration calibration, and robust control of charging and thermal effects that can otherwise degrade pattern fidelity and defectivity. In practice, the scalability-limiting parameters often shift from beam physics to architecture-level factors, including the number of beams, per-beam write rate, data-path bandwidth, and long-term calibration stability.

Manufacturing bottleneck summary: MBML is primarily constrained by system complexity and cost, while throughput and defectivity at scale depend on uniform beam-

to-beam performance, thermal and charging control, and calibration stability; overlay performance is increasingly limited by stage accuracy and multi-beam registration during high-area writing.

4.5. Plasmonic Lithography

When an electromagnetic wave is incident on the metallic surface, collective electron oscillations are excited at the metal dielectric interface and generate a highly localized electromagnetic field, as depicted in Figure 13a,b [274]. Plasmonic lithography (PSL) employs this surface plasmon resonance to confine optical energy beyond the far-field diffraction limit during pattern transfer (Figure 13c) [58,59,274]. This physical origin of advantage enables pattern formation with resolutions down to approximately 10 nm and supports applications such as plasmonic sensors, photonic circuits, and advanced memory devices [236–241]. However, the physical origin of failure is inherent to the same plasmonic mechanism. Strong field confinement in common plasmonic metals is accompanied by substantial ohmic loss that converts optical energy into heat, which directly limits energy transmission efficiency and narrows the usable exposure window [242–245]. The resulting localized heating near plasmonic hotspots can distort pattern fidelity and degrade material stability in both the resist and the plasmonic structures, especially when repeated exposures or high-intensity operation are required [246]. This heat generation also makes PSL challenging to integrate with heterogeneous stacks and flexible/conformal substrates, where the thermal budget of non-conventional materials and interfaces is often limited. In addition, the near field decays rapidly with distance, so nanoscale variations in spacing, resist thickness, or surface planarity readily translate into critical dimension nonuniformity and reduced pattern integrity, which becomes increasingly problematic when scaling to large areas.

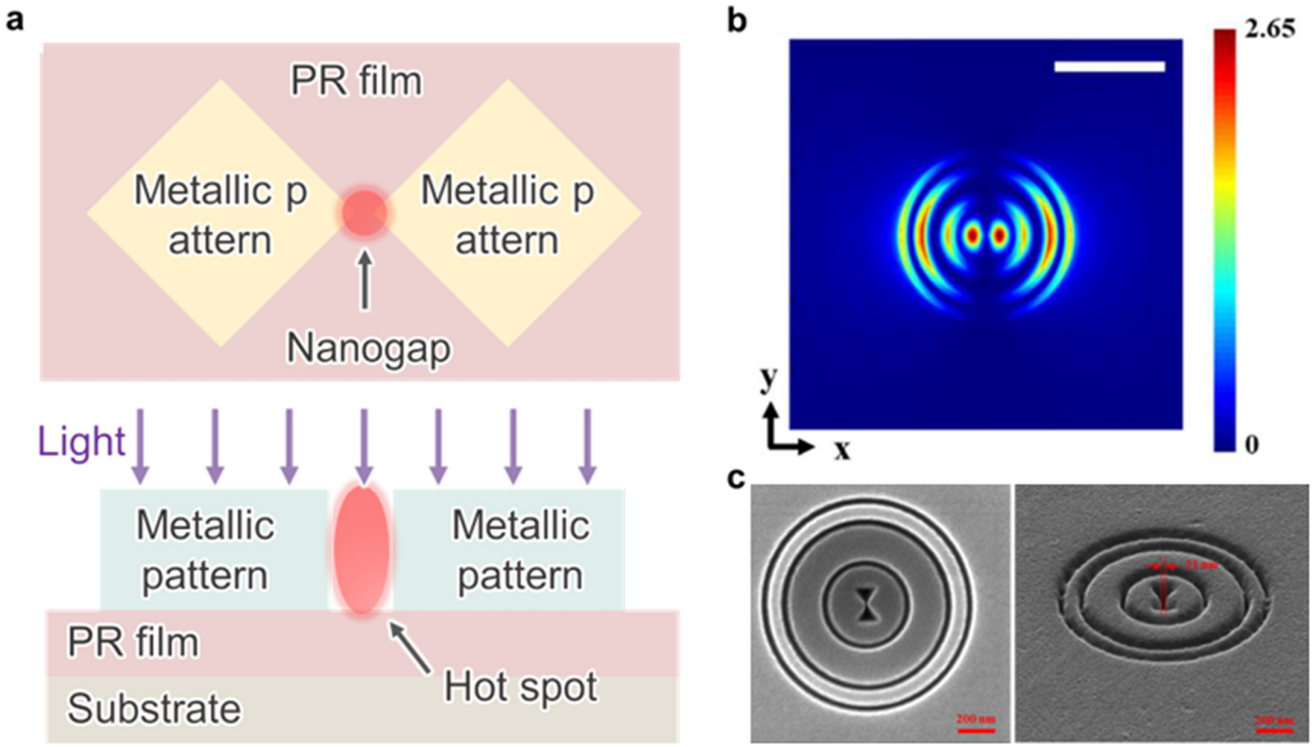

Figure 13. (**a**) Schematic design of PSL process setup. (**b**) Simulated results for locally enhanced electromagnetic field (scale bar: 500 nm). (**c**) SEM images of the nanosized structures obtained by PSL. Reprinted from Ref. [274] © 2023 MDPI (CC BY 4.0).

Engineering approaches, including hybrid patterning schemes, thermal management, and exploration of alternative low-loss plasmonic or polaritonic materials, can mitigate these effects. Nevertheless, as long as PSL relies on plasmonic confinement in practical materials, dissipation and hotspot-driven nonuniformity remain intrinsic constraints, and improvements often shift the dominant bottleneck to mask complexity, fabrication tolerance, and wafer-scale throughput. Therefore, expanding PSL beyond niche patterning scenarios would require exposure platforms and architectures that maintain nanoscale field control with uniformity while reducing dissipation-driven thermal loading in a manufacturable manner, for example, via genuinely low-loss material systems and scalable designs that avoid fragile, high-precision nanostructured masks [245,248–250]. In heterogeneous integration contexts, this requirement becomes even more stringent because thermal management needs to be achieved without exceeding the allowable thermal budget of temperature-sensitive layers.

Manufacturing bottleneck summary: PSL is primarily constrained by defectivity and scalability due to intrinsic, loss- and heat-driven limitations in process window and near-field uniformity. For temperature-sensitive materials, hotspot-induced heating can further tighten the process window and increase defectivity risk. Throughput and cost are further constrained by mask complexity and stringent fabrication tolerances required for large-area deployment.

4.6. Electrohydrodynamic Lithography

When a high electric field (>10^7 V/m) is vertically imposed on the thin polymer film, electrostatic stresses destabilize the free surface and drive the formation of surface relief structures that reduce the electrostatic energy in a system [64,251–253]. This electrohydrodynamic instability provides a physical origin of advantage for pattern transfer because it can amplify nanoscale perturbations without relying on optical imaging and can therefore produce diverse micro and nanoscale topographies on a polymer surface, as represented in Figure 14a [254]. First, a spin-coated polymer layer is placed on a bottom electrode, and a master template as a top electrode is positioned above the film to create an air gap. When applying a voltage across two electrodes, the electrohydrodynamic instability is induced on the polymer surface and results in the pattern formation that reflects the field distribution defined by the template geometry (Figure 14b) [254]. Since its first report in the 2000s [53], EHL has been extensively studied owing to its rapid processing [254–256], the absence of diffraction-limited resolution constraints [65], structural diversity [257], and relatively simple equipment requirements [253,258–261]. Recently, several studies reported its extended applications, such as biomimetic structures [262] and biosensor devices [263], to further verify its versatility [258,260,264,265].

The practical positioning of EHL depends strongly on the target manufacturing regime. In practical terms, EHL is unlikely to serve as a manufacturing workhorse for advanced CMOS semiconductor integration, where deterministic overlay control, ultra-low defectivity, and wafer-scale uniformity within wide process windows are mandatory. This limitation arises not from insufficient resolution, but from the intrinsic sensitivity of instability-driven pattern formation to nanometric variations in gap spacing, electric field strength, and film thickness. At the same time, this does not preclude the use of electrohydrodynamic lithography in semiconductor-based devices more broadly defined, including oxide, organic, or flexible electronics, sensor arrays, and functional or energy-related device layers, where overlay tolerances are relaxed and materials compatibility, large-area coverage, and structural versatility become dominant requirements. For functional surfaces, bio-integrated devices, and flexible or materials-diverse platforms, EHL is especially attractive. It enables mask-defined topographic diversity, works well with soft materials, and supports rapid

large-area patterning, which is useful when alignment does not have to be ultra-tight and heating must be kept minimal.

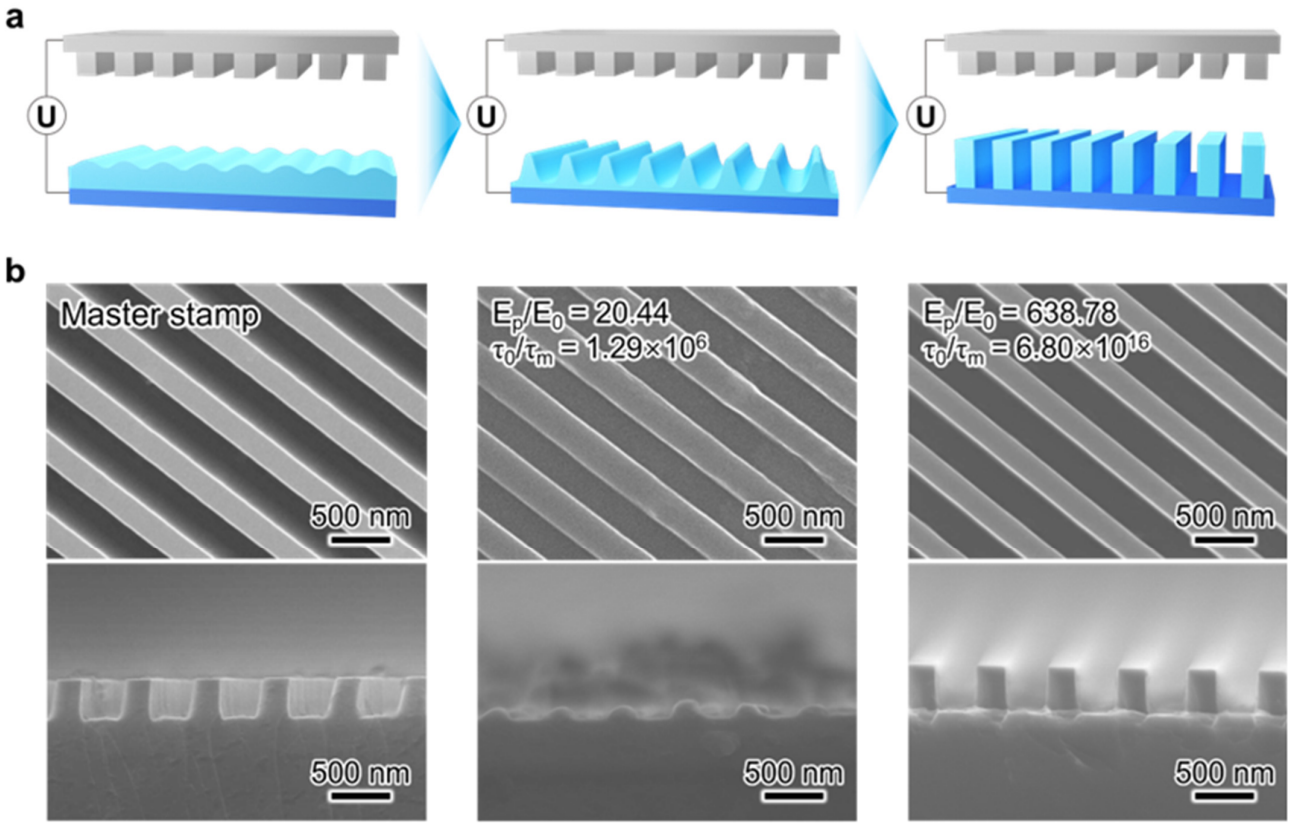

Figure 14. (**a**) Schematic representation of pattern transfer through EHL process, where *U* denotes the applied voltage and the blue and gray regions represent the polymer film and the master template, respectively. (**b**) SEM image showing the topology of the master pattern (**left**). Patterned features are controlled by electric field strength (**middle** and **right**). Reproduced with permission from Ref. [254], © 2023, American Chemical Society.

Manufacturing bottleneck summary: EHL is primarily constrained by defectivity and uniformity due to its intrinsic sensitivity to gap, field, and thickness variations, which limit its applicability to advanced CMOS manufacturing. However, for semiconductor-based functional devices and nontraditional substrates where deterministic overlay is not the dominant constraint, EHL remains a promising patterning platform owing to its materials compatibility, low-cost setup, and ability to generate structurally diverse micro- and nanoscale features within process flows that can be more compatible with low-thermal-budget materials [254].

5. Conclusions

Since the early 2000s, nanolithography has diversified rapidly, but the field's central bottleneck has barely changed: industry does not reward resolution unless it arrives with throughput, overlay control, and predictable cost. The next decade will not be decided by who prints the smallest features in the lab, but by who can manufacture nanoscale patterns with repeatability, yield, and integration compatibility.

5.1. What Worked and What Did Not

In this review, we organized the development of nanolithography into three chronological tracks: conventional semiconductor lithography, non-conventional techniques that emerged in the 1990s, and contemporary innovations since the early 2000s.

Conventional platforms such as PL, EBL, and XRL matured together with the semiconductor industry since the 1980s. Their sustained industrial relevance stems from the fact that they can be engineered for large-scale process control, including alignment, overlay, and repeatable integration across multiple layers. However, continued scaling has been constrained by fundamental and practical barriers, including optical diffraction in PL, escalating tool complexity, and rapidly rising capital and operating costs.

Non-conventional approaches such as DPN, BCL, and NIL emerged as routes to bypass optical limits by exploiting new physical or chemical mechanisms. Despite decades of effort, many of these techniques have not translated broadly to high-volume manufacturing because they fail to satisfy at least one of the key manufacturing requirements. These requirements include high throughput, reliable overlay and alignment, low defectivity with high yield, and predictable cost at scale. In particular, methods that depend on delicate interfacial physics or multi-parameter self-organization often face narrow process windows, making wafer-scale uniformity and consistently low defect density difficult to guarantee.

Since the early 2000s, a new wave of innovations pursued resolution beyond the conventional optical roadmap. PSL and IML pushed optical patterning toward smaller features by taking advantage of near-field effects and higher refractive index media. In parallel, EHL demonstrated mask-defined pattern formation driven by electric field-induced instabilities. Maskless paradigms such as DML and MBML also expanded the design space by reducing dependence on photomasks. However, a recurring lesson from these developments is that improved patternability does not automatically translate into manufacturability. Many approaches remain limited by integration challenges such as overlay and multilayer registration, by throughput limitations inherent to serial or data-intensive writing, or by yield losses caused by defects and stochastic variation.

5.2. Where the Field Should Bet Next

The field should stop treating resolution as the primary metric and instead evaluate technologies by whether they satisfy four constraints simultaneously: (i) scalable throughput, (ii) overlay/alignment control, (iii) low defectivity with process windows, and (iv) cost predictability (Figure 15). Among the emerging techniques discussed in this review, only EUVL-class optical manufacturing currently satisfies all four constraints simultaneously for leading-edge semiconductor production, albeit at an extreme cost and system complexity. That uncomfortable fact explains why "cheaper high-resolution alternatives" routinely stall: they typically fail not at feature size, but at manufacturing integration. This does not mean EUVL is the final answer. It means that the next breakthroughs will not come from resolution alone, but from integration-first engineering.

At the same time, the dominant constraint set varies widely across product classes, and many applications are defined less by minimum feature size than by the ability to pattern reliably at the required manufacturing scale and cost. For leading-edge logic and memory, overlay, defectivity, and multi-layer process control remain decisive, favoring EUVL-class optical platforms. For dense periodic or templated structures, the practical question is whether ordering, defect suppression, and registration can be made deterministic enough to justify adoption, which naturally motivates self-assembly or imprint-based routes. For heterogeneous, large-area, or customization-driven manufacturing, throughput and design agility can outweigh ultimate resolution, creating space for maskless approaches and other non-conventional methods that trade peak performance for flexibility and lower mask dependence.

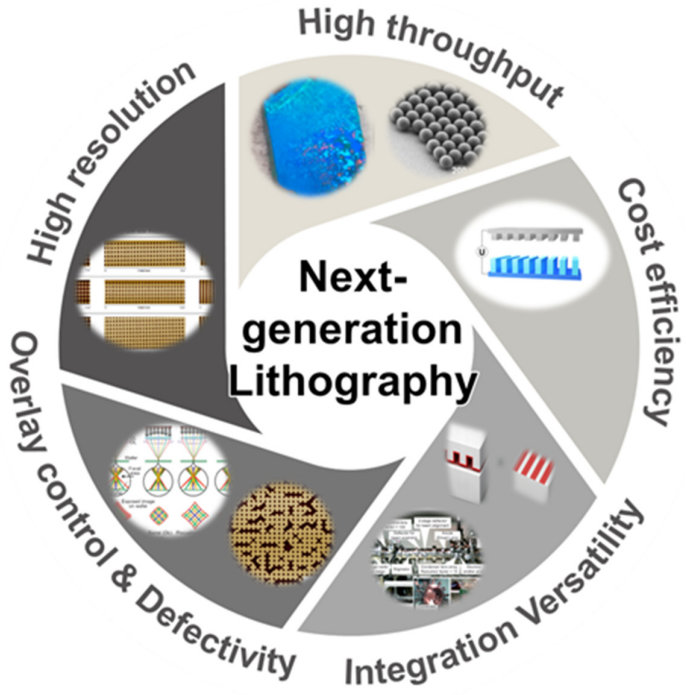

Figure 15. Conceptual summary of next-generation lithographic technologies evaluated by manufacturing-relevant criteria, including resolution, throughput, overlay control, defectivity, cost efficiency, and integration versatility. The figure emphasizes that only approaches satisfying all four manufacturing constraints simultaneously can serve as general-purpose platforms, while others are positioned as complementary or application-specific solutions. Importantly, placement along these axes reflects practical manufacturing outcomes reported across the literature, rather than idealized single-parameter demonstrations. Reprinted from Ref. [198], © 2021 MDPI (CC BY 4.0). Reprinted from Ref. [199], © 2024 MDPI (CC BY 4.0). Reprinted from Ref. [211], © 2022 MDPI (CC BY 4.0). Reproduced with permission from Ref. [254], © 2023, American Chemical Society. Reprinted from Ref. [273], © 2020 MDPI (CC BY 4.0).

Concretely:

- BCL is a prime example of a technology that may be right scientifically yet still wrong industrially unless alignment becomes deterministic. Sub-10 nm features are not the barrier. The barrier is reliable long-range orientation, defect suppression, and registration to device layouts. If directed self-assembly cannot deliver a predictable overlay and low defectivity across large areas, it will remain best suited for templated or periodic patterns rather than serving as a general manufacturing platform.
- Maskless methods such as DML and MBML will win where design agility matters more than absolute throughput, including rapid prototyping, heterogeneous integration, and application-driven manufacturing. However, for cost-sensitive high-volume environments, serial writing will remain economically constrained unless parallelization and data path architectures advance faster than the growth of pattern complexity.
- EHL deserves separate emphasis because it offers a fundamentally different path to pattern formation. Rather than pushing optics to smaller wavelengths or relying on stochastic self-assembly, EHL converts an applied electric field into controllable surface instabilities that can amplify nanoscale perturbations and generate patterns that follow a template-defined field distribution. This mechanism makes EHL attractive for low-cost, large-area patterning and for creating structurally diverse topographies on polymer films. At the same time, EHL will not become a manufacturing workhorse unless it clears its own integration barriers, particularly uniformity across large areas, defect control, and repeatable process windows that remain stable against small

variations in film thickness, air gap, and material rheology. If these sensitivities are engineered down through better process control and materials design, EHL could become one of the few routes that improve versatility without paying the full cost penalty of ultra-high-end optical systems. Importantly, the limitations of electrohydrodynamic lithography discussed here primarily apply to advanced CMOS logic and memory manufacturing. In application domains with relaxed overlay requirements and greater emphasis on materials diversity and form factor adaptability, EHL may offer a viable and complementary manufacturing route rather than a competing alternative to optical lithography.

Flexible and bio-integrated electronics represent a different constraint set in which the dominant requirement is not the minimum feature size, but materials compatibility, conformal contact, and pattern fidelity on curved or soft substrates. In addition, thermal budget constraints often become first-order considerations when non-conventional materials and hybrid stacks are involved. In these sectors, photomask-centric and rigid substrate workflows are often the wrong default. Accordingly, lithography paradigms may shift from maximizing resolution and overlay to enabling low-damage, low-temperature patterning with sufficient fidelity under curvature, roughness, and mechanical strain. Methods that tolerate curvature, roughness, and mechanical strain can dominate even at moderate resolution because they solve the system-level requirement. EHL is particularly relevant here because it operates naturally on thin polymer films and can generate patterns without direct mechanical contact, which may help preserve fragile or deformable substrates when the process is properly engineered.

Finally, machine learning and AI will matter most when used for manufacturing discipline rather than novelty. Their value is not in replacing physics-based understanding, but in tightening process windows into reproducible recipes by converting the most sensitive process degrees of freedom into measurable and controllable variables through accelerated defect inspection, parameter optimization, and tool drift compensation. In this review, the scalability-limiting parameters identified for each technique can be interpreted as high-sensitivity input features for data-driven models, including exposure dose and focus stability, overlay and stage drift, resist and film-thickness nonuniformity, gap and electric field sensitivity, and tool-to-tool variation. When coupled with in-line metrology and rapid defect inspection, such models can accelerate parameter optimization, enable early detection of excursions, and provide tool drift compensation to reduce defectivity and improve long-term process stability. Taken together, these tools reinforce the central premise of this review: practical success is determined less by peak resolution than by the ability to sustain stable, low-defect, and scalable manufacturing within realistic cost constraints.

In short, this manufacturing lens forces an uncomfortable truth. A lithography method can be scientifically elegant and still be industrially non-viable. The winners will be those who treat nanolithography not as a resolution contest, but as a manufacturing discipline in which cost, yield, overlay, and scalability determine what survives.

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Abbreviations

The following abbreviations are used in this manuscript:

AFM	Atomic force microscope
AI	Artificial intelligence
BCL	Block copolymer lithography
DML	Digital maskless lithography
DPN	Dip-pen nanolithography
DUV	Deep ultraviolet
EBL	Electron beam lithography
EHL	Electrohydrodynamic lithography
EUV	Extreme ultraviolet
EUVL	Extreme ultraviolet lithography
HVM	High-volume manufacturing
IL	Interference lithography
IML	Immersion lithography
IoT	Internet of Things
MBML	Multi-beam maskless lithography
MEMS	Micro-electromechanical systems
NA	Numerical aperture
NIL	Nanoimprint lithography
NSL	Nanosphere lithography
PDMS	Polydimethylsiloxane
PL	Photolithography
PMGI	Polymethylglutarmide
PMMA	Poly(methyl methacrylate)
PR	Photoresist
PS	Polystyrene
PSL	Plasmonic lithography
SEM	Scanning electron microscope
SERS	Surface-enhanced Raman scattering
SL	Soft lithography
UV	Ultraviolet
XRL	X-ray lithography

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