



Article

Effects of Switching on the 2-DEG Channel in Commercial E-Mode GaN-on-Si HEMT

Roberto Baca-Arroyo

Department of Electronics, National Polytechnic Institute, School of Mechanical and Electrical Engineering, Mexico City 07738, Mexico; rbaca02006@yahoo.com.mx; Tel.: +52-01-5729-6000

Abstract

In this study, the effects of switching on the two-dimensional electron gas (2-DEG) channel in an E-mode GaN-on-Si HEMT are investigated using a GS-065-004-1-L device that is commercially available for educational practice. A practical prototype with a reduced number of components is proposed, with empirical concepts used to explain its predictive performance when a coreless transformer is series-connected to the E-mode GaN-on-Si HEMT for switching-mode conduction. Conduction modes arising at the p-GaN/n-AlGaIn/i-GaN heterojunction in accordance with specifications from the manufacturer's datasheet were validated using a didactic physical-based model dependent on semiconductor parameters of gallium nitride (GaN). Test circuit-examined waveforms were analyzed, which confirmed that the switching conduction mode of the 2-DEG channel is dependent on physical parameters such as switching operating frequency, temperature, low-field electron mobility, and space charge capacitance.

Keywords: p-GaN gate HEMT; p-GaN/n-AlGaIn/i-GaN heterojunction; low-power GaN transistor; switching conduction mode; didactic physics-based model



Academic Editors: Wei Liu and Kun Wang

Received: 27 September 2025

Revised: 14 October 2025

Accepted: 14 October 2025

Published: 16 October 2025

Citation: Baca-Arroyo, R. Effects of Switching on the 2-DEG Channel in Commercial E-Mode GaN-on-Si HEMT. *Micromachines* **2025**, *16*, 1173. <https://doi.org/10.3390/mi16101173>

Copyright: © 2025 by the author. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

High-voltage GaN-on-Si transistors have been in development and the subject of intense research since 2015, when the first high-voltage solution was commercially released. These practical devices are based on a cascade configuration of a low-voltage Si-MOSFET in series connection with a high-voltage gallium nitride (GaN) MIS-HEMT, followed by enhancement-mode (E-mode) devices based on a p-doped GaN gate module for low-voltage GaN power transistors. In 2016, the first fully industrial qualified 600 V E-mode GaN power transistors were released by Panasonic and Infineon [1,2]. However, because GaN-based device technologies have been implemented with a standard silicon process to achieve economic balance, one of the biggest challenges when using GaN devices is their reliability [3].

Empirical methods have been established to understand how the formation of piezoelectric effects dependent on charge distribution can contribute to the presence of the conduction path in GaN HEMTs on a very thin (≤ 30 nm) sheet—called two-dimensional electron gas (2-DEG) in GaN-based devices—where donor states positively impact performance under high electric field conditions, inducing sheet charges at p-GaN/n-AlGaIn and n-AlGaIn/i-GaN interfaces [4,5]. Therefore, a simplified behavior model of switching effects on the 2-DEG channel is expected to encourage scholars who are researching switching-mode power circuits based on E-mode GaN-on-Si HEMTs, where mounting techniques are needed for long-term temperature cycles in real-world applications, and

gate driver techniques with low impedance and high peak current are recommended for fast switching conduction [6]. To understand the physical behavior of a commercial E-mode GaN-based device, empirical concepts used to explain the performance of a test circuit are a valuable educational resource for undergraduate and graduate students.

It is well known that, although technology computer-aided design (TCAD) software packages for power circuit analysis can be a very useful tool for initial design, they are not a substitute for young professionals' and experienced engineers' understanding of the overall performance of GaN device-based circuits, because such packages provided by device manufacturers and researchers are usually commercially private and technologically protected. Consequently, to mitigate the lack of design skills and optimize reliability issues using E-mode GaN-on-Si HEMTs, a typical design process must usually begin with specifications for the circuit application, which can proceed based on previous silicon technology-based designs—including specific components and their tolerances—to achieve the best performance by evaluating some of their key physical parameters from a phenomenological viewpoint [7].

The remainder of this study is organized as follows. In Section 2, we provide general description of the experimental setup to present the effects of switching on the 2-DEG channel. In Section 3, we utilize a physics-based model focused on standard carrier conduction equations of silicon-based semiconductor devices for reducing the workload of parameter's adjustment, and a test circuit and behavior analysis to examine how switching dependence of 2-DEG channel conduction in the commercial GS-065-004-1-L device occurs, particularly when it is driven at frequencies higher than 250 kHz using a coreless transformer in a test circuit. Conclusions about this work are presented in Section 4.

2. Experimental Procedure

To understand how the effects of switching on the 2-DEG channel behave, an empirical study with accessible measurement instruments for the user is proposed. This study focuses on a physical-based model verified in a test circuit, where a commercial low-power GaN transistor from GaN Systems (Ottawa, ON, Canada) (with part number GS-065-004-1-L) is tested using a range of electrical specifications from the manufacturer's datasheet. The dimensions for the commercial GS-065-004-1-L device (p-GaN gate structure) shown in Figure 1a comprises an i-GaN buffer, n-AlGaIn barrier, p-GaN layer, and three electrodes—namely, drain, source, and gate—where the gate electrode is asymmetrically located at $1/5 L_{DS}$ for low-power technology [8,9]. The test circuit in Figure 1b with a reduced number of components is proposed to understand how semiconductor parameters can influence switching effects in the commercial GS-065-004-1-L device.

Although GaN-based devices behave differently to silicon MOSFETs because they can exhibit an average 2-DEG channel resistance during their turn-off time, they are designed to be cooled using the printed circuit board (PCB), where the source/thermal pad is internally connected [5,10]. Thus, to prevent thermal damage, the copper path on the PCB for distributing the gate drive signal was designed to be as short as possible, while copper paths to the source and drain signals were wider, as shown in Figure 2a. The device was mounted on 0.1 mm PCB thickness phenolic resin as the material, and the copper layer under the source/thermal pad was roughly $15 \times 15 \text{ mm}^2$, as shown in Figure 2b.

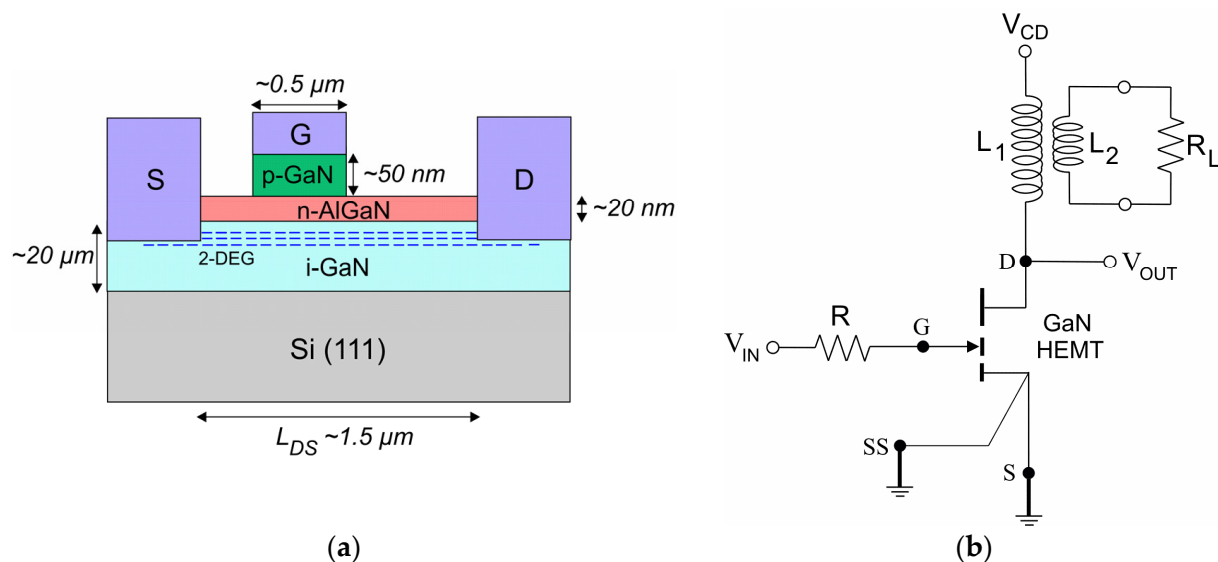


Figure 1. (a) Representation of the p-GaN gate structure of the commercial GS-065-004-1-L device; (b) schematic diagram of the test circuit for the experimental analysis.

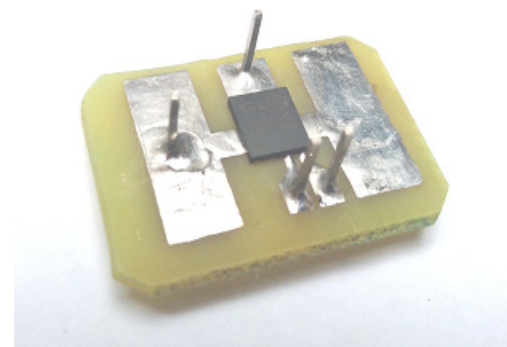
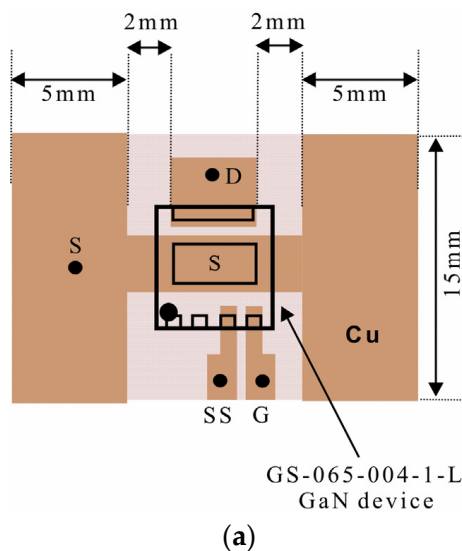


Figure 2. (a) PCB layout and related sizes of the mounted GS-065-004-1-L device; (b) PCB used to experimentally test it.

3. Results and Discussion

3.1. Conduction Modes in the E-Mode GaN-on-Si HEMT

Conduction modes for GaN-based devices must be evaluated using semiconductor parameters (e.g., doping concentration, physical dimensions, and electrical characteristics) and well-known physical principles assembled in carrier conduction equations to study its effects with available mathematics software tools. This results in an educational model that could be useful for the predictive analysis of p-GaN/n-AlGaN/i-GaN heterojunctions. To theoretically analyze the conduction modes as a function of the physical parameters, useful specifications from the manufacturer's datasheet are summarized in Table 1. Furthermore, semiconductor parameters for GaN at room temperature, as listed in Table 2 from data reported in the scientific literature, are taken into account to understand how conduction effects in the practical structure shown in Figure 1b can impact performance in switching-mode power electronics.

Table 1. Specifications for commercial GS-065-004-1-L device.

Parameter	Symbol	Value
Maximum drain-to-source voltage	V_{DS}	650 V
Gate-to-source threshold	V_T	1.1 to 2.6 V
On resistance	R_{ON}	0.45 Ω
Gate-to-source current	I_{GS}	20 μ A
Maximum switching frequency	f_{SW}	~10 MHz
Rise time	t_R	3 ns
Fall time	t_F	11.5 ns
Maximum junction temperature	T_J	150 $^{\circ}$ C

Table 2. Semiconductor parameters for GaN used to evaluate physics-based model [10,11].

Property	Symbol	Value
Bandgap	E_G	3.4 eV
Breakdown field	F_{BW}	$\sim 4 \times 10^6$ V/cm
Lateral electric field at drift conduction	F_L	$\sim 1.5 \times 10^4$ V/cm
Static dielectric constant	K_{GaN}	9
Intrinsic concentration	n_i	$\sim 3.5 \times 10^7$ cm $^{-3}$
Hole lifetime	τ_p	~7 ns
Electron lifetime	τ_n	~2 ns
Diffusion length of holes	L_p	~0.8 μ m
Diffusion length of electrons	L_n	~8.5 μ m
Saturation velocity	v_s	3×10^7 cm/s
Drift velocity	v_d	$\leq 4.5 \times 10^5$ cm/s
Surface state density	N_{SS}	2×10^{13} to 5×10^{13} cm $^{-2}$
Low concentration at i-GaN	N_i	$\sim 2 \times 10^9$ cm $^{-3}$
Donor concentration at n-AlGaN	N_D	$\sim 5 \times 10^{16}$ cm $^{-3}$
Acceptor concentration at p-GaN	N_A	$\sim 2 \times 10^{18}$ cm $^{-3}$
2-DEG channel thickness	d_{2DEG}	≤ 10 nm

Accordingly, to understand how the p-GaN/n-AlGaN heterojunction can affect 2-DEG channel conduction and transiently stimulate the n-AlGaN/i-GaN heterojunction for reliable conduction in an E-mode GaN-on-Si HEMT, standard equations for silicon devices governing static conduction modes can be established as follows.

At the p-GaN/n-AlGaN heterojunction, where both sides of the heterojunction become the same material, it is supposed that the diffusion currents are similar to a regular p $^+$ -n junction and the carrier concentrations are relatively much higher inside the depletion region [12]. Therefore, a dipole layer is supported with the built-in potential, Ψ_1 and applied bias threshold voltage, where surface effects due to ionic charges can cause the formation of depletion regions W_{Dp} and W_{Dn} , giving rise to the high injection level that may occur under a relatively small forward bias condition, as shown in the energy band diagram in Figure 3a. The current/voltage characteristics are established using the following expression:

$$\frac{I_T(\Psi_1)}{S_{J1}} = J_0 \left[e^{\left(\frac{qV_T}{kT} \right)} - 1 \right] \quad (1)$$

where $k = 8.62 \times 10^{-5}$ eV K $^{-1}$ is the Boltzmann constant; $T = T_J + 273.15$ in degrees Kelvin, where T_J is the junction temperature in degrees Celsius for the analysis proposed in accordance with the manufacturer's datasheet; S_{J1} is a cross-section area for mobile carries across the p-GaN/n-AlGaN heterojunction; V_T the gate threshold voltage; $J_0 = qn_i^2 \left[L_p(\tau_p N_D)^{-1} + L_n(\tau_n N_A)^{-1} \right]$ is the saturation current density which depends on

n_i the intrinsic carrier concentration at room temperature; the carrier lifetime for holes is τ_p and that for electrons is τ_n ; the diffusion length for holes is $L_p \gg W_{Dp}$ and that for electrons is $L_n \gg W_{Dn}$; and the impurity concentration for the donor is N_D while that for the acceptor is N_A .

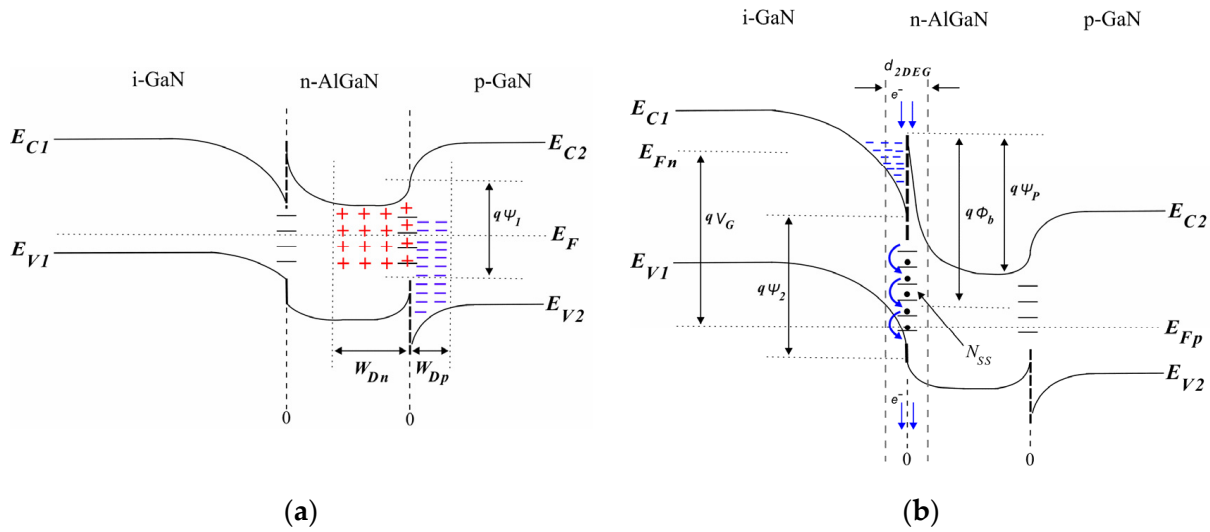


Figure 3. Energy band diagram of the p-GaN/n-AlGaN/i-GaN heterojunction: (a) forward bias regime at n-AlGaN/p-GaN heterojunction; (b) high-injection regime at i-GaN/n-AlGaN interface under reverse bias condition.

For the n-AlGaN/i-GaN heterojunction, it can be supposed that the conduction mechanism is similar to that governed by thermionic emission where the electron's conduction regime is influenced by the barrier height, ϕ_b in which high-mobility electrons can be swept in a velocity saturation regime through the 2-DEG channel length [12,13]. Accordingly, the temperature-influenced current density at the n-AlGaN/i-GaN heterojunction can behave similarly to the metal/semiconductor junction given by

$$\frac{I_G(\Psi_2)}{S_{J2}} = \frac{\Psi_2 A^* T_I}{k} \left(1 - \frac{V_J}{\Psi_2}\right) e^{\left(-\frac{q\Psi_2}{kT_I}\right)} e^{\left(-\frac{q\phi_b}{kT_I}\right)} \left[e^{\left(\frac{qV_J}{kT_I}\right)} - 1\right], \quad (2)$$

where $A^* = 26.4 \times 10^{-3} \text{ Acm}^{-2}\text{K}^{-2}$ is the pre-exponential factor (often expressed in terms of the effective Richardson constant for GaN material [11]), Ψ_2 is the built-in potential at the i-GaN/n-AlGaN interface, S_{J2} is the cross-section area for mobile electrons across the 2-DEG channel, and V_J is the junction voltage at the gate-to-source heterojunction which obeys equation $qV_J = q(\phi_b + \Psi_p)$ [7,14], where the potential $\Psi_p = qN^*d_2^2(2K_{GaN}\epsilon_0)^{-1}$ is responsible for the trapping reduction and minimizing inactive surface donors at the n-AlGaN barrier of $d_2 \sim 20 \text{ nm}$ (see Figure 1) as a function of the concentration of the ionized donor impurities N^* at the i-GaN/n-AlGaN interface, as shown in Figure 3b.

Because the i-GaN buffer is lightly doped, space charge effects independent of the electric field at the n-AlGaN/i-GaN heterojunction can be influenced by ϕ_b , which is sufficient to fully enhance the conduction dominated by the velocity saturation regime. This is due to the presence of free carrier concentrations along the 2-DEG channel length when the gate voltage $V_G > V_T$, as shown by the energy band diagram in Figure 3b [8,12]. The drain current arising from flow inside the 2-DEG channel can be accurately given by

$$\frac{I_D(\phi_b)}{S_{2DEG}} = 2 K_{GaN}\epsilon_0 v_s \frac{V_D}{(L + L_D)^2}, \quad (3)$$

where $\epsilon_0 = 8.86 \times 10^{-14} \text{ Fcm}^{-1}$, v_s is the saturation velocity, S_{2DEG} is the cross-section area across the 2-DEG channel length, $L_D = \sqrt{K_{GaN}\epsilon_0 kT(qN^*)^{-1}}$ is the Debye length which defines the start-up for conduction limited by space charge effects inside the 2-DEG channel, and $L = 1/2L_{DS}$, where $L_{DS} = V_{DS}F_{BW}^{-1}$ is initially computed using data from Tables 1 and 2.

Semiconductor parameters for commercial devices are unrevealed by manufacturers and are very hard to determine. However, for the empirical adjustment of Equations (1)–(3), it is sufficient to know initial values of the manufacturer's data summarized in Table 1 for the extraction of physical parameters J_0 , Ψ_2 , ϕ_b , and N^* to accurately reflect the characteristics of the commercial GS-065-004-1-L device. The values of the remaining physical parameters collected in Table 2 are adjusted in accordance with those reported in the scientific literature [10,11].

Based on the energy band diagram of Figure 3 for the p-GaN/n-AlGaIn/i-GaN heterojunction, it is pertinent to understand how the junction temperature disturbs the threshold current, I_T , as a function of forward threshold bias V_T (Ψ_1), as shown in Figure 3a, as well as gate current I_G , as a function of reverse bias voltage V_J (Ψ_2), together with I_D (ϕ_b) at the i-GaN/n-AlGaIn interface, as shown in Figure 3b. Thus, because the maximum junction temperature for the commercial GS-065-004-1-L device is 150 °C, current/voltage curves are examined for three temperature values: 40 °C, 80 °C, and 120 °C.

The characteristics (I_T – V_T) depicted in Figure 4a show an initial bias current flow at the n-AlGaIn/p-GaN heterojunction as a function of the built-in potential Ψ_1 , which is dependent on V_T from 1.1 to 2.6 V, as declared in Table 1. In Figure 4b, for the characteristics (I_G – V_J) under reverse bias at the i-GaN/n-AlGaIn heterojunction, the current flow begins to increase in the gate-to-source region as a function of Ψ_P in V_J ranging from -4 to -2 V when the drain current starts to flow across the drain-to-source distance, where the 2-DEG channel is created at a high injection level, as shown in the characteristics (I_D – V_D) presented in Figure 4c and governed by ϕ_b and the built-in potential, Ψ_2 , dependent on V_D from 0 to 5 V. Nevertheless, to determine how the switching conduction regime in the commercial GS-065-004-1-L device must be assisted, the evaluation of an injection level coefficient, $\alpha_I = I_G I_T^{-1}$, as presented in Figure 4d, shows how dynamic conduction regime in the p-GaN/n-AlGaIn/i-GaN heterojunction is dependent on the gate voltage, V_G , as a pulse pattern applied in the gate electrode where, to achieve an enhanced injection level at the temperature lower than 80 °C, the V_T/V_G ratio must be lower than 0.3.

Because it is assumed that electrons travel near to the saturation velocity, transit time effects can enable the switching conduction mode through the dipole charge sheet (inside the 2-DEG channel) where current flow can lag behind the voltage based on the time-variant distribution of the electron's density with respect to the ionized donor impurities' concentration, N^* , similar to the space charge-limited conduction (SCLC) formalism for the commercial D-mode GaN-on-Si HEMT [7,12]. Therefore, the trapping of electrons occurs close to the n-AlGaIn surface when they are displaced from the depleted i-GaN buffer at the i-GaN/n-AlGaIn interface, as shown in the energy band diagram of Figure 3, exhibiting capacitance/frequency characteristics at the drain-to-source heterojunction through the gate width ($L_G \sim 0.5 \mu\text{m}$), establishing a connection between Q_{SS} and Ψ_P according to $C_{2DEG} = dQ_{SS}/d\Psi_P$, assuming $dQ_{SS} = I_D(\phi_b)dt$. Substituting Equation (3) with $L \approx L_G$ and $dt \approx f_{SW}^{-1}$, taking into account that $2LL_D \gg L^2 + L_D^2$, we can define a space charge capacitance equivalent to the depletion capacitance per unit area, given by

$$C_D \approx \frac{K_{GaN}\epsilon_0}{L_D L_G} \left(\frac{v_d}{f_{SW}} \right), \quad (4)$$

where f_{SW} is the switching frequency; $v_d \propto \mu_{2DEG} F_L$ is the drift velocity (average sound velocity), being proportional to the practical 2-DEG electron mobility, μ_{2DEG} , which is

highly dependent on a lateral electric field F_L inside the gate-to-drain space, and caused by longitudinal and transverse strains at i-GaN buffer and scattering mechanisms at the n-AlGaN barrier [5,10,11].

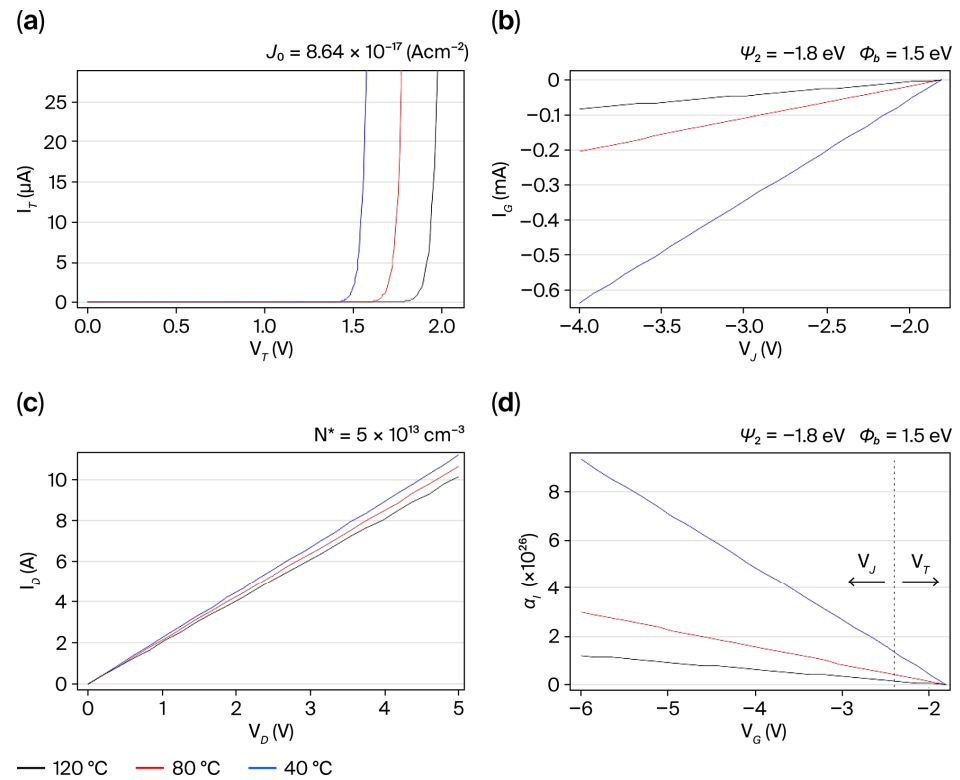


Figure 4. Current/voltage characteristics as a function of the junction temperature and specifications from Table 1: (a) I_T - V_T curves; (b) I_G - V_J curves; (c) I_D - V_D curves; (d) α_I - V_G curves.

Furthermore, the progressive reduction in N^* at the n-AlGaN/i-GaN interface and scattering mechanisms along the 2-DEG channel length can slightly impact electron mobility when the temperature rises, as shown in Figure 4c. This is because diffusion mechanisms in the drain-to-source space can occur due to the saturation of the surface state density, and the dependence of N_{SS} on Ψ_P rises during 2-DEG channel conduction.

3.2. Switching Dependence of Coreless Transformer

It is well known that the output power capability delivered by the coreless transformer to the load for square wave signal excitation [15] can be approximately defined from the stored energy density in the coreless transformer as follows:

$$P_{OUT} = 0.5A_E^2dB_{air}f_{sw}10^{-6}, \quad (5)$$

where A_E is the core effective area in cm^2 ; B_{air} is the air gap flux density; f_{sw} is the switching frequency; and $d = 1.5 \text{ Amm}^{-2}$ is the current density of wires for low-power transformer windings operating at high frequencies, where surface eddy currents are supposed to reinforce the main current flow but oppose it toward the center of the winding [16]. As a result, the induced voltage at the secondary winding of the number of turns, N_2 , could increase as f_{sw} rises, being highly dependent on the primary inductance, L_1 , empirically given by

$$L_1 = \frac{n}{2I_2f_{sw}}(DV_{CD}), \quad (6)$$

where $n = N_1 N_2^{-1} = I_2 I_1^{-1}$ is the turn's ratio and D is the duty cycle, defined as the turn-on time/full wave time ratio of a square wave signal with voltage supply V_{CD} and average current flow I_2 from the secondary winding.

Applying a pulse pattern of a short turn-on time at the gate, as deduced in Figure 4d, the power density transferred to the resistive load from the coreless transformer in Figure 1b could be improved [16,17]. Accordingly, as almost all magnetic energy is stored in air gaps and insulation between conductors, the current flowing around the windings' surface must be taken into account in terms of skin effects to determine the distribution of B_{air} as a function of its depth, $\delta = \sqrt{(\pi \mu_0 \sigma_C f_{SW})^{-1}}$, using an expression defined according to the empirical Faraday's law and $\delta(f_{SW})$ definition, given by

$$\frac{(DV_{CD})10^8}{2B_{air}N_1A_E} = \frac{1}{\pi\mu_0\sigma_C\delta^2}, \quad (7)$$

where N_1 is the number of turns for the primary winding of the coreless transformer, A_E is the core's effective area in cm^2 , $\mu_0 = 4\pi \times 10^{-7} \text{Hym}^{-1}$ is the permeability of vacuum, and $\sigma_C = 5.82 \times 10^7 \text{Sm}^{-1}$ is the conductivity of the copper wire of the windings.

To achieve good power transfer from the input to the load and to circumvent power losses, optimized analysis has been commonly supported using TCAD software packages [14,18]. Nevertheless, instead of using these powerful computer programs for behavior analysis, from empirical Equations (5)–(7), governing the coreless transformer performance can be useful in manufacturing it, because power transfer from a phenomenological viewpoint as a function of physical parameters can be realized in specifications for a practical design, including dimensions, the number of primary and secondary turns, and their operating capabilities at high switching frequencies when series-connected to the depletion capacitance deduced from Equation (4) to understand how GaN-based devices must be operated in the real world and empirically model the drain-to-source heterojunction behavior of the commercial GS-065-004-1-L device intended to be operated in low-power electronics applications. Here, in a theoretical design for the test circuit in Figure 1b, operating specifications such as $V_{CD} = 100 \text{ V}$, $D = 0.3$, $100 \mu\text{H} < L_1 < 400 \mu\text{H}$, $A_E = 1 \text{ cm}^2$, and $n = 5$ are assumed to ensure that a coreless transformer could be reliably developed [19]. The results in Figure 5a–c were computed using the MATHEMATICA 5 software to demonstrate the feasibility of the coreless transformer and space charge capacitance as a function of the switching frequency, f_{SW} , in the range from 300 to 700 kHz using Equation (4), as shown in Figure 5d at room temperature.

Figure 5a confirms that B_{air} increases when the power capability rises but, when using an L_1 higher than $200 \mu\text{H}$, as shown in Figure 5b, the I_2 at the secondary winding might decrease at switching frequencies higher than 350 kHz. However, when the skin depth is taken into account, as shown in Figure 5c, where N_1 is higher than 150 T (turns), the induced voltage at L_2 inside the coreless transformer in Figure 1b might be creased within an acceptable B_{air} level. Hence, it is theoretically confirmed that the coreless transformer manufactured using conventional winding techniques may be applied for switching-mode power circuits at high frequencies, although the winding temperature should be lower than 50°C for copper wires [18,19]. The depletion capacitance C_D decreases as switching frequency rises, as shown in Figure 5d, but its variation as a function of the electron density trapped at three different N^* concentrations, $2 \times 10^{13} \text{ cm}^{-3}$, $5 \times 10^{13} \text{ cm}^{-3}$, and $9 \times 10^{13} \text{ cm}^{-3}$, is examined.

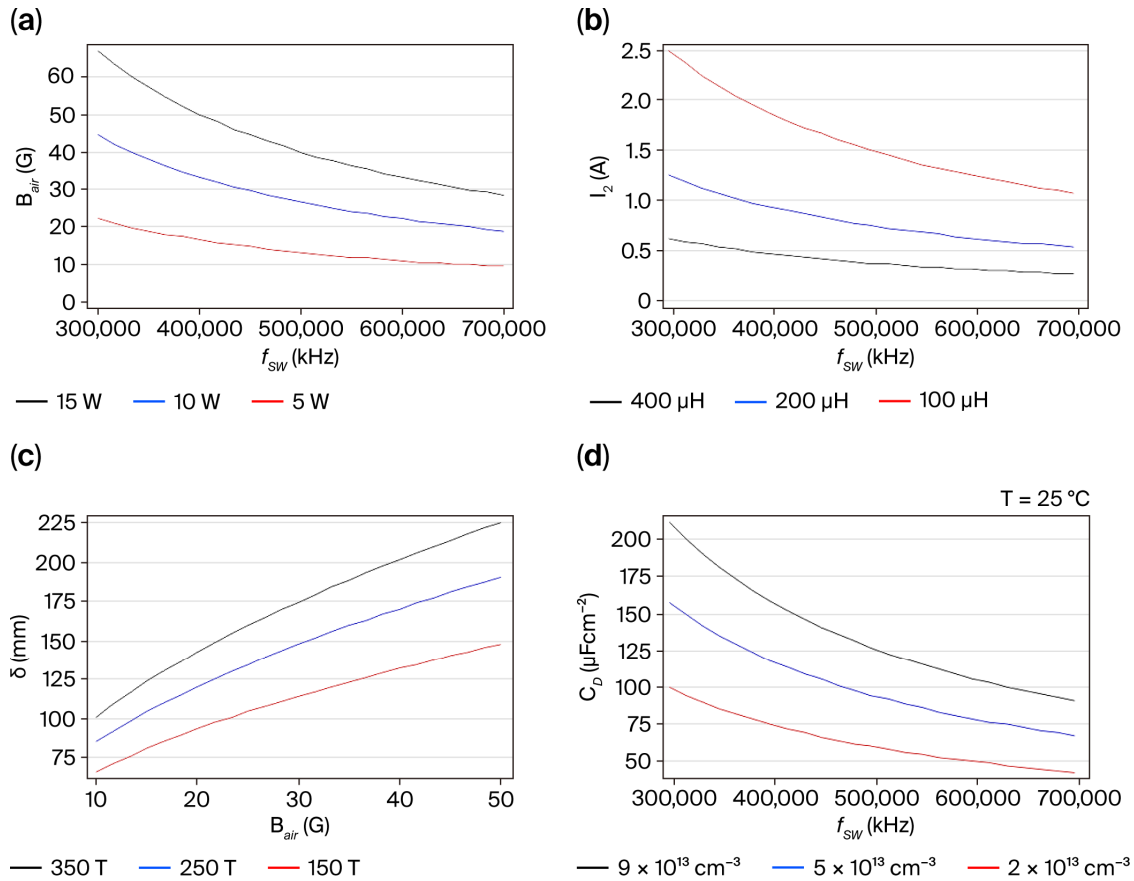


Figure 5. Predictive analysis of the coreless transformer performance at high-frequency switching conduction: (a) B_{air} - f_{SW} curves; (b) I_2 - f_{SW} curves; (c) δ - B_{air} curves; (d) capacitance/frequency characteristics for commercial GS-065-004-1-L device.

This confirmed that stable operations can be achieved only at a low injection level ($N^* = 2 \times 10^{13}$ cm $^{-3}$) to ensure an off-state condition at the V_{OUT} in Figure 1b (though lower than $\frac{1}{2} V_{DS}$; see Table 1), and quasi-resonance phenomena, observed with stored magnetic energy at L_1 and stored electric energy inside the 2-DEG channel, can result in negligible electrical breakdown effects at switching frequencies higher than 300 kHz.

3.3. Analysis of Test Circuit

In accordance with the theoretical results in Figure 5, the test circuit in Figure 1b was built and its performance was experimentally evaluated by connecting a pulse pattern of the positive square-wave signal with $D = 0.25$ to V_{IN} , where a series resistor $R = 10 \Omega$ was connected on the gate electrode. A coreless transformer series-connected to the drain electrode was built whose specifications are $N_1 = 200$ T ($L_1 \sim 250 \mu$ H) of 26 AWG wire, $N_2 = 40$ T of 22 AWG wire, $A_E \sim 1$ cm ^{2} . The load resistor $R_L = 26.6 \Omega$ (small incandescent lamp for automobile application) was used. The input voltage, V_{IN} , and output voltage, V_{OUT} , waveforms were measured using a digital storage oscilloscope (Tektronix (Beaverton, OR, USA), TDS1012C 100 MHz) to determine the physical effects of switching conduction on the 2-DEG channel in the commercial GS-065-004-1-L device.

A typical driver circuit for the switching performance of GaN devices must comprise one comparator with a programmable turn-on time [20], where the resistor R_2 can be used to adjust D in the range of 10 to 30%, and two CMOS logic inverter circuits, as shown in Figure 6a, where the capacitor C_1 and resistor R_1 are both used to adjust the chosen switching frequency. Because the driver circuit used for high-frequency operation requires a bias voltage ($V_{GS} = 6$ V) at the gate-to-source heterojunction to ensure stable

effects of i-GaN buffer. This is because the turn-off protection (freewheeling diodes and snubber networks) in the test circuit is missing [19,21], but to retain the intention of the reduced number of components, its test circuit was securely operated at $V_{CD} < 100$ V and the drain-to-source junction operated at $V_{DS} < 300$ V, as confirmed in Figure 7.

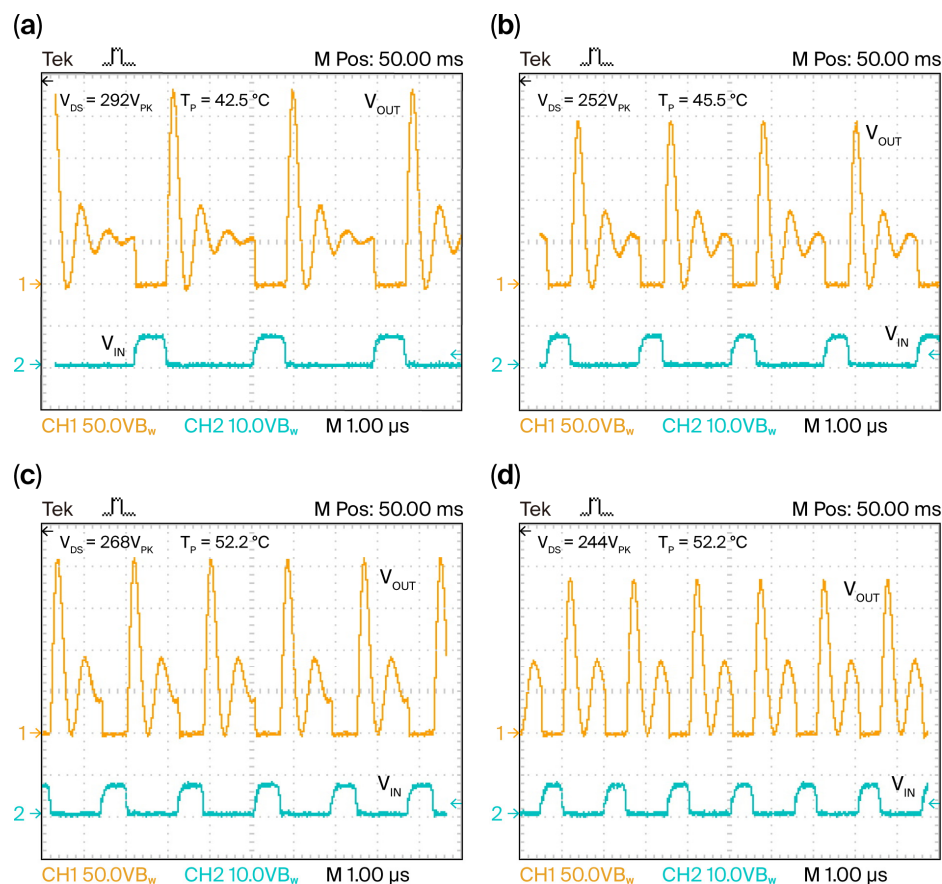


Figure 7. Input and output waveforms under four switching frequencies: (a) 350 kHz; (b) 450 kHz; (c) 550 kHz; (d) 650 kHz.

Because reactivation of flux residues from no-clean soldering paste may cause unwanted conduction paths in GaN devices, scattering mechanisms on the surface of the n-AlGaN barrier under switching conditions as a function of the T_j can impact 2-DEG channel conduction [10,22]; therefore, it is aimed to understand how heat dissipation in the source pad on the bottom side of the commercial GS-065-004-1-L device behaves when the device package temperature, T_P , remains below 100 °C during cooling cycles. The T_P was measured as indicated by the experimental results in Figure 7, showing how the temperature dependence of the 2-DEG channel changed when T_P increased from 40 to 55 °C and f_{SW} increased, while the damping effects in the wide peak of lower magnitude became negligible, as the oscillating frequency of the equivalent series R_{ON} - L_1 - C_D circuit began to be equal to the switching frequency of the pulse pattern applied to the gate. This suggests that critical strains due to the lattice and thermal expansion coefficient mismatches at the p-GaN/n-AlGaN/i-GaN heterojunction did not contribute to the presence of the surface donor states at the i-GaN/n-AlGaN interface based on anomalous piezoelectric effects [5,10,14] and the non-uniform distribution of the electric field peaks along the 2-DEG channel length [22].

To know how the temperature-dependent dynamic conduction in the 2-DEG channel behaves, a theoretical analysis was evaluated for temperatures ranging from 25 °C to 150 °C, where the commercial GS-0D65-004-1-L device must operate reliably. Figure 8a

shows curves describing how the depletion capacitance, $C_D(T_J, f_{SW})$, from Equation (4) acts as a function of T_J for the four examined switching frequencies, providing useful confirmation of the charge fluctuations in the graphs in Figure 7, where $C_D(T_J, f_{SW})$ gradually reduces as T_J increases at a medium-ionized impurity level ($N^* = 5 \times 10^{13} \text{ cm}^{-3}$). However, low-field electron mobility, $\mu_{2DEG}(V_{DS}, T_J)$, when $v_s \sim v_d$ from Equation (3), results in V_{DS} and T_J dependence of $\phi_b = 1.5 \text{ eV}$ under a low-ionized impurity level ($N^* = 2 \times 10^{13} \text{ cm}^{-3}$), whereas for the three different temperatures, namely, 50°C , 100°C , and 150°C , shown in Figure 8b, it was found that $\mu_{2DEG}(V_{DS}, T_J)$ rapidly reduces as V_{DS} increases, although it slightly decreases as T_J rises. For the empirical adjustment of Equation (3) describing $\mu_{2DEG}(V_{DS}, T_J)$ as a function of the V_{DS} and T_J , the average values of $I_D = 4 \text{ A}$ and $S_{2DEG} = 7.5 \times 10^{-4} \text{ cm}^2$ were used to accurately reflect the tendency in the curves of Figure 8b for the commercial GS-065-004-1-L device.

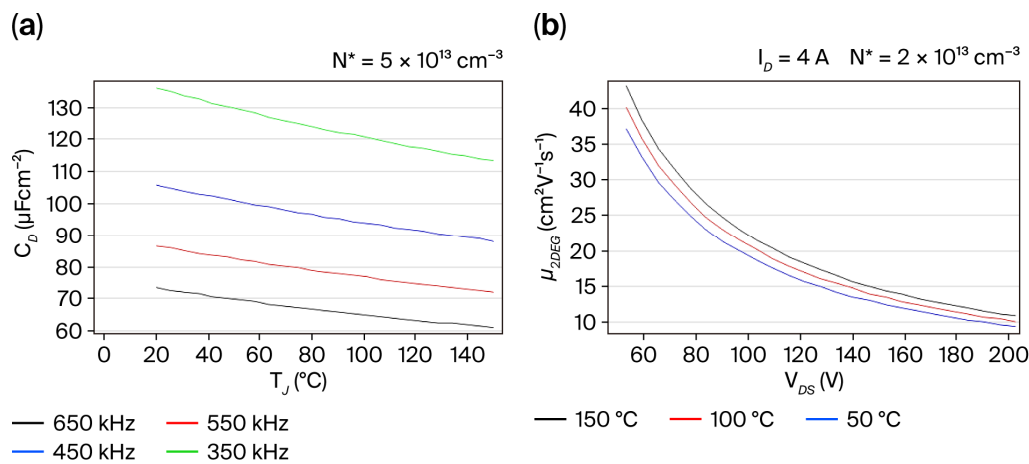


Figure 8. Temperature dependence of conduction mode in 2-DEG channel for E-mode GaN-on-Si HEMT: (a) C_D - T_J curves; (b) μ_{2DEG} - V_{DS} curves.

The above-mentioned results indicate that $C_D \leq 100 \mu\text{Fcm}^{-2}$ and $f_{SW} \geq 450 \text{ kHz}$, as well as $\mu_{2DEG} \geq 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, allowing us to provide a stable conduction mode with a surge V_{DS} peak magnitude lower than 350 V and $T_J < 100^\circ\text{C}$ in accordance with the current/voltage characteristics in Figure 4. The examined results in Figure 7 and predictive analysis in Figure 8 confirm the semiconductor parameters' dependence of $I_T(\Psi_1)$, $I_G(\Psi_2)$, $I_D(\phi_b)$, $C_D(T_J, f_{SW})$, and $\mu_{2DEG}(V_{DS}, T_J)$ in the commercial GS-065-004-1-L device.

Furthermore, the curves in Figure 8 confirm that an ionization level, N^* , between 2×10^{13} and $5 \times 10^{13} \text{ cm}^{-3}$ can be responsible for the stable conduction mode of the E-mode GaN-on-Si HEMT when switching conduction in the 2-DEG channel conforms to $N^*d_{2DEG} \gg N_{SS}$, but its package temperature can increase in a runaway manner above 150°C generating conductive paths during turn-off time which occur between the drain and Si (111) substrate, as well as between the i-GaN/n-AlGaN interface and Si (111) substrate, which would presumably be responsible for unfavorable transient changes in the occupation of interface states determined by N_{SS} , as shown in the energy band diagram in Figure 3b, leading to time-dependent breakdown effects as Si (111) is a material with 10 times lower F_{BW} compared to GaN [10,18,22].

4. Conclusions

This research is focused on the effects of switching on the 2-DEG channel of an E-mode GaN-on-Si HEMT to understand how semiconductor parameter-dependent conduction modes can be influenced. Firstly, fine tuning of the current/voltage curves was performed using geometric dimensions $S_{J1} = 1.5 \times 10^{-14} \text{ cm}^2$, $S_{J2} = 4.5 \times 10^{-14} \text{ cm}^2$, and

$S_{2DEG} = 7.5 \times 10^{-4} \text{ cm}^2$. Secondly, a physical parameter-based test circuit was proposed and built within a coreless transformer series-connected to the drain-to-source junction of a commercial GS-065-004-1-L device. Using empirical equations and a simple experiment, reliable performance was demonstrated with a voltage supply lower than 100 V and switching frequencies higher than 300 kHz, validating acceptable heat dissipation in the commercial GS-065-004-1-L device during switching-mode conduction. Based on a didactic physical-based model, this investigation offers a suitable means for behavior analysis and further research to both students and experienced specialists who may face challenges when transitioning to GaN-based devices.

Funding: This research received no external funding, and the APC was funded by the author.

Data Availability Statement: All of the data are available in the manuscript. Ultimately, the intention of the author is to encourage scholars to explore new empirical research routes by using similar methodologies to those documented here.

Acknowledgments: I would like to acknowledge to the engineers Omar David Rivera-Reyes and Ángel Ismael Velázquez-López for their valuable expertise in designing the PCB circuits and technical support.

Conflicts of Interest: The author declares no conflicts of interest.

References

1. Jones, E.A.; Wang, F.F.; Costinett, D. Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 707–719. [\[CrossRef\]](#)
2. Zhong, Y.; Zhang, J.; Wu, S.; Jia, L.; Yang, X.; Liu, Y.; Zhang, Y.; Sun, Q.Y. A review on the GaN-on-Si power electronic devices. *Fund. Res.* **2022**, *2*, 462–475. [\[CrossRef\]](#) [\[PubMed\]](#)
3. Ikeda, N.; Niiyama, Y.; Kambayashi, H.; Sato, Y.; Nomura, T.; Kato, S.; Yoshida, S. GaN power transistor on Si substrates for switching applications. *Proc. IEEE* **2010**, *98*, 1151–1161. [\[CrossRef\]](#)
4. Meneghini, M.; Hilt, O.; Wuerfl, J.; Meneghesso, G. Technology and reliability of normally-off GaN HEMTs with p-type gate. *Energies* **2017**, *10*, 153. [\[CrossRef\]](#)
5. Islam, N.; Packeer Mohamed, M.-F.; Jalaludin Khan, M.-F.-A.; Falina, S.; Kwarada, H.; Syamsul, M. Reliability, Applications and Challenges of GaN HEMT Technology for Modern Power Devices: A Review. *Crystals* **2022**, *12*, 1581. [\[CrossRef\]](#)
6. Lim, S.; Otten, D.M.; Perreault, D.-J. New AC-DC Power Factor Correction Architecture Suitable for High-Frequency Operation. *IEEE Trans. Power Electron.* **2016**, *31*, 2937–2949. [\[CrossRef\]](#)
7. Baca-Arroyo, R. Semiconductor parameters-dependent dynamic behavior in commercial depletion-mode GaN on Si HEMT. *e-Prime Adv. Electr. Eng. Electron. Energy* **2025**, *11*, 100954. [\[CrossRef\]](#)
8. Bhat, Z.; Ahsan, S.-A. A Physics-Based Analytical Model for p-GaN HMET. *IEEE Trans. Electron. Devices* **2024**, *71*, 6544–6551. [\[CrossRef\]](#)
9. Wei, J.; Tang, G.; Xie, R.; Chen, K.-J. GaN power IC technology on p-GaN gate HEMT platform. *JPN J. Appl. Phys.* **2020**, *59*, SG0801. [\[CrossRef\]](#)
10. Amano, H.; Baines, Y.; Beam, E.; Borga, M.; Bouchet, T.; Chalker, P.R.; Charles, M.; Chen, K.J.; Chowdhury, N.; Chu, R.J. The 2018 GaN power electronics roadmap. *J. Phys. D Appl. Phys.* **2018**, *51*, 163001. [\[CrossRef\]](#)
11. Pearton, S.; Ren, F.; Zhang, A.; Lee, K.; Reports, E.R. Fabrication and performance of GaN electronic devices. *Mater. Sci. Eng. R.* **2000**, *30*, 55–212. [\[CrossRef\]](#)
12. Sze, M.S.; Ng, K.K. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons, Inc.: New York, NY, USA, 2007; pp. 28–50, 124–129, 401–407.
13. Luo, H.; Hu, W.; Guo, Y. On large-signal modeling of GaN HEMTs: Past, development and future. *Chip* **2023**, *2*, 100052. [\[CrossRef\]](#)
14. Vigneshwara-Raja, P.; Nallatamby, J.-C.; DasGupta, N.; DasGupta, A. Trapping effects on AlGaIn/GaN HEMT characteristics. *Solid-State Electron.* **2021**, *176*, 107929. [\[CrossRef\]](#)
15. Chryssis, G. *High-Frequency Switching Power Supplies: Theory and Design*, 2nd ed.; McGraw-Hill Publishing Company: Columbus, OH, USA, 1989; pp. 109–133.
16. Chen, M.; Araghchini, M.; Afridi, K.-K.; Lang, J.-H.; Sullivan, C.-R.; Perreault, D.-J. A Systematic Approach to Modeling Impedances and Current Distribution in Planar Magnetics. *IEEE Trans. Power Electron.* **2016**, *31*, 560–580. [\[CrossRef\]](#)

17. Gattozzi, A.-L.; Pappas, J.-A. Circuits for Protecting and Triggering SCRs in High Power Converters. *IEEE Trans. Magn.* **2003**, *39*, 414–417. [[CrossRef](#)]
18. Sun, S.; Xie, X.; Zhang, P.; Zhao, Z.; Wei, J.; Luo, X. Improvement of single event transients' effect for a novel AlGaIn/GaN HEMT with enhanced breakdown voltage. *J. Sci. Adv. Mater. Devices* **2024**, *9*, 100692. [[CrossRef](#)]
19. Park, C.-W.; Han, S.-K. Analysis and design of an integrated magnetics planar transformer for high power density LLC resonant converter. *IEEE Access* **2021**, *9*, 499–511. [[CrossRef](#)]
20. Sedra, A.S.; Smith, K.C. *Microelectronics Circuits*, 5th ed.; Oxford University Press Inc.: New York, NY, USA, 2004; pp. 1042–1090.
21. Rashid, M.H. *Power Electronics: Devices, Circuits, and Applications*, 4th ed.; Pearson Education: Courier Westford, MA, USA, USA, 2014; pp. 931–955.
22. Hein, L.; Goller, M.; Li, G.; Losner, M.; Lutz, J.; Basler, T. Investigation on the high temperature behaviour of p-GaN HEMTs by different temperature sensitive electrical parameters. *Power Electron. Devices Compon.* **2025**, *12*, 100103. [[CrossRef](#)]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.