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Preparation and Performance Exploration of MoS_2/WSe_2 Van Der Waals Heterojunction Tunneling Field-Effect Transistor

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Abstract

Due to their high carrier mobility, thermal conductivity, and exceptional foldability, transition metal dichalcogenides (TMDs) present promising prospects in the realm of flexible semiconductor devices. Concurrently, tunneling field-effect transistors (TFETs) have garnered significant attention owing to their low energy consumption. This study investigates a TMD van der Waals heterojunction (VdWH) TFET, specifically by fabricating MoS_2 field-effect transistors (FETs), WSe_2 FETs, and MoS_2/WSe_2 VdWH TFETs. The N-type characteristics of the MoS_2 and P-type characteristics of WSe_2 are established through an analysis of the electrical characteristics of the respective FETs. Finally, we analyze the energy band and electrical characteristics of the MoS_2/WSe_2 VdWH TFET, which exhibits a drain current switching ratio of 10^5. This study provides valuable insights for the development of novel low-power devices.

Keywords: TMDs (transition metal dichalcogenides); TFET (tunneling field-effect transistor); van der Waals heterojunction

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Academic Editors: Goutam Koley, Jing Liu and Fei Zhuge

Received: 27 August 2025
Revised: 16 September 2025
Accepted: 27 September 2025
Published: 29 September 2025

Citation: Chong, C.; Liu, H.; Wang, S.; Chen, S.; Yan, C. Preparation and Performance Exploration of MoS_2/WSe_2 Van Der Waals Heterojunction Tunneling Field-Effect Transistor. *Micromachines* **2025**, *16*, 1108. https://doi.org/10.3390/mi16101108

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1. Introduction

As the manufacturing process of semiconductor devices approaches its physical limits, issues related to power consumption and heat dissipation are becoming increasingly severe. Consequently, Moore's Law is gradually becoming obsolete [1–3]. In response, researchers have begun to explore alternatives for the post-Moore era, with notable devices including TFETs [4,5], negative capacitance FETs [6,7], and two-dimensional (2D) material transistors [8–11]. Transition metal dichalcogenides (TMDs), characterized by their 2D layered structure similar to graphene, have garnered significant attention from both domestic and international scholars [12]. The layers of TMDs are held together by van der Waals forces, allowing for the detachment of single or multiple layers from the bulk material. Unlike graphene, which possesses a zero-band-gap structure, TMDs feature an adjustable band gap, resulting in unique optical and electrical properties [13–16]. Additionally, TMDs can be combined with various 2D materials to create heterojunctions, with minimal concerns regarding lattice mismatch [17]. Therefore, TMD-based FETs and TMD-based van der Waals TFETs are highly worthy of research [18].

Numerous simulation studies have been conducted on transition metal dichalcogenide (TMD) field-effect transistors (FETs) and TMD van der Waals heterostructure (vdWH) FETs [19–21]. For instance, Qianwen Wang employed the ATK simulator to theoretically investigate the effects of biaxial tensile strain on the transport characteristics of monolayer

WSe_2 double-gate tunneling FETs (DG-TFETs). The findings indicate that increased strain results in a lower subthreshold swing (SS); notably, at 2% strain, the enhancement in the on-state current and maximum transconductance is maximized [22]. Similarly, Fan Chen examined the interlayer tunneling FET of MoS_2-WTe_2, revealing that the SS of the MoS_2-WTe_2 interlayer TFET is below 60 mV/dec. Furthermore, the optimized device can achieve a drain current of 1000 μA/μm at a supply voltage (VDD) of 0.3 V [23]. To explore the transport mechanisms in vdWH FETs, A. Afzalian integrated density functional theory (DFT) with the non-equilibrium Green's function (NEGF) method within the atomic modeling solver (ATOMOS). This approach has also been applied to investigate the transport properties of HfS_2/WSe_2 TFETs and WTe_2/WS_2 vdWH FETs, both exhibiting high on-state currents [24].

Recent experimental studies on field-effect transistors (FETs) utilizing transition metal dichalcogenides (TMDs) and their van der Waals heterostructures (Vdwh FETs) have reported heterogeneous device performances and operational mechanisms [25–30]. For instance, Han et al. (2019) fabricated a MoS_2 FET with material synthesized via atmospheric pressure chemical vapor deposition (APCVD), reporting an on-state current of 2.75×10^{-1} μA/μm and an off-state current of 10^{-6} μA/μm at a drain voltage of 0.9 V [31]. Mbisike et al. (2022) integrated Ta_2O_5 as a gate dielectric in a WSe_2 FET, observing p-type transfer characteristics alongside n-type output behavior, with an on-state current of 165 nA at V_{DS} = 1 V [32]. In 2023, Arun Kumar et al. demonstrated that the on-state current in a MoS_2 FET scales linearly with optical illumination intensity, further establishing that gate bias and light collectively modulate the charge storage states in MoS_2-based optoelectronic memory [33].

In this work, we experimentally fabricated and characterized back-gated MoS_2 FETs, WSe_2 FETs, and a MoS_2/WSe_2 van der Waals heterojunction tunnel field-effect transistor (Vdwh TFET). Electrical characterization of the homogeneous devices facilitated polarity determination and informed subsequent analysis of the heterojunction device. Section 2 outlines the material synthesis and device fabrication processes. Section 3 presents a detailed theoretical and experimental analysis of the electronic transport properties in each device, culminating in a band-alignment-based interpretation of the heterojunction TFET operation. Section 4 summarizes the results.

2. Material Synthesis and Device Fabrication

The MoS_2/WSe_2 heterostructure was fabricated by employing a multi-step lithographic and dry-transfer process:

(a) Photolithographic patterning was performed on a p^+-Si substrate with 300 nm thermal oxide to define alignment markers.
(b) Few-layer MoS_2 flakes were mechanically exfoliated from bulk crystal and precisely transferred onto designated coordinates using a dry-transfer technique.
(c) Similarly, WSe_2 flakes were exfoliated onto a polydimethylsiloxane (PDMS) elastomer stamp.
(d) Using a micro-manipulator under an optical microscope, WSe_2 was aligned and transferred onto the pre-placed MoS_2 flake through thermal release to form an intimate van der Waals heterojunction.
(e) Electron-beam lithography followed by electron-beam evaporation of Cr/Au (10/30 nm) was used to define electrical contacts.

Figure 1a–c schematically illustrates the fabrication sequence. Maximization of the overlap between MoS_2 and WSe_2 flakes is critical for achieving clean heterointerfaces and minimizing interfacial contaminants, as evidenced in the optical micrograph presented in Figure 1e. In the fabricated device, MoS_2 serves as the drain, while WSe_2 functions as the

source. The dimensions of the heterostructure—length, width, and estimated area—are denoted as 10.25 μm, 9.78 μm, and 100.35 μm^2, respectively.

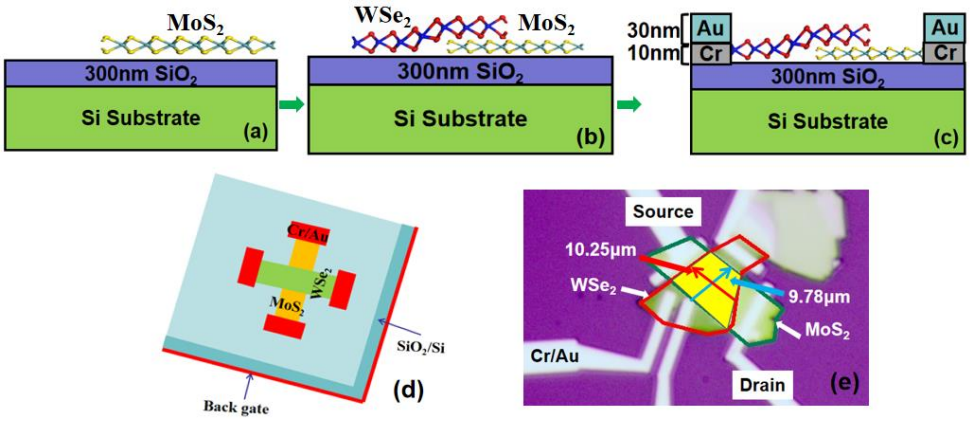


Figure 1. (**a**–**c**) Preparation process of MoS_2/WSe_2 Vdwh TFET, (**d**) schematic diagram, and (**e**) OM image of the MoS_2/WSe_2 heterojunction.

Electrical characterization was conducted using an Agilent B1500A semiconductor parameter analyzer under dark conditions at 300 K to minimize environmental noise and optoelectric effects. The system configuration emphasized high-resolution measurements. The measurement system employed two B1517A High-Resolution Source Measure Units (HRSMUs) to bias the gate and drain terminals, respectively, while the source electrode was grounded via an MPSMU. The instrument provides a current resolution of 0.1 fA and a voltage resolution of 100 nV. The range mode was set to auto-ranging to maintain optimal accuracy across the entire sweep. The number of power line cycles (NPLC) was configured between 2 and 5 to achieve a balance between measurement precision and acquisition speed; higher NPLC values were selected for low-current measurements to enhance accuracy. Additionally, a moving-average filter with a window of 8 to 16 points was applied to effectively suppress random noise.

Layer thicknesses of MoS_2 and WSe_2 were confirmed via Raman spectroscopy. The frequency difference ($\Delta k \approx 24.855\ cm^{-1}$) between the $E^1{}_2g$ and A_1g peaks (Figure 2a) confirms trilayer MoS_2. The A_1g peak position and the characteristic feature at ~310 cm^{-1} in Figure 2b indicate a multilayer WSe_2 flake.

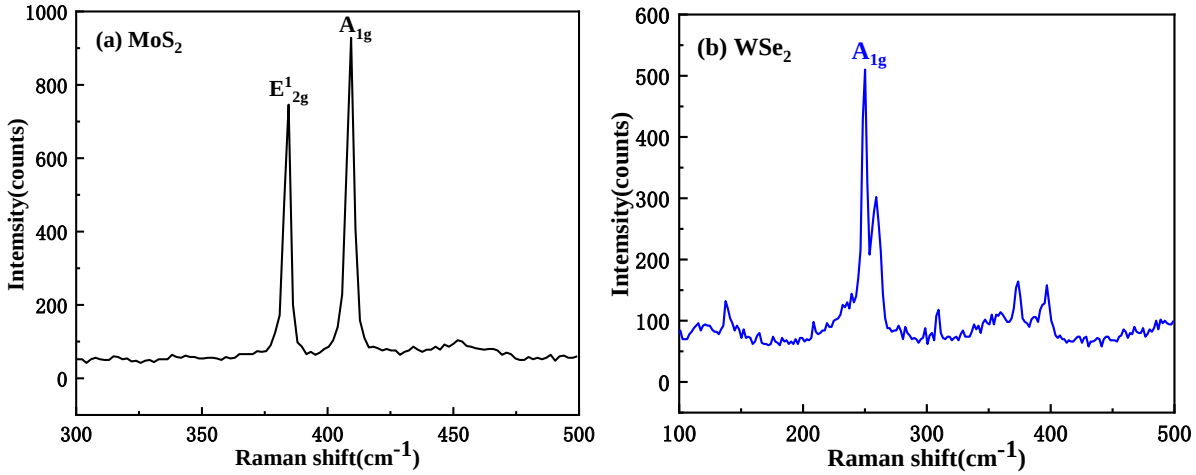


Figure 2. Raman spectrum distribution of the (**a**) MoS_2 and (**b**) WSe_2.

3. Results and Discussion

To conduct a detailed study on the performance of the MoS_2/WSe_2 Vdwh TFET, the electrical characteristics of the MoS_2 FET and WSe_2 FET were analyzed first.

3.1. MoS_2 FET

Figure 3a illustrates the schematic structure of a MoS_2 FET, in which a positive bias is applied to the drain terminal while the source is grounded. The transfer and output characteristics of the device are presented in Figure 3b and Figure 3c, respectively. As evidenced by the transfer curve in Figure 3b, the MoS_2 FET operates as an n-channel depletion-mode transistor, indicating that the channel is already conductive at zero gate voltage. The device exhibits an on-state current of 157 μA/μm and an off-state current of 6.5×10^{-6} μA/μm, yielding a current switching ratio of 2.4×10^{8}—a value indicative of high performance in switching applications.

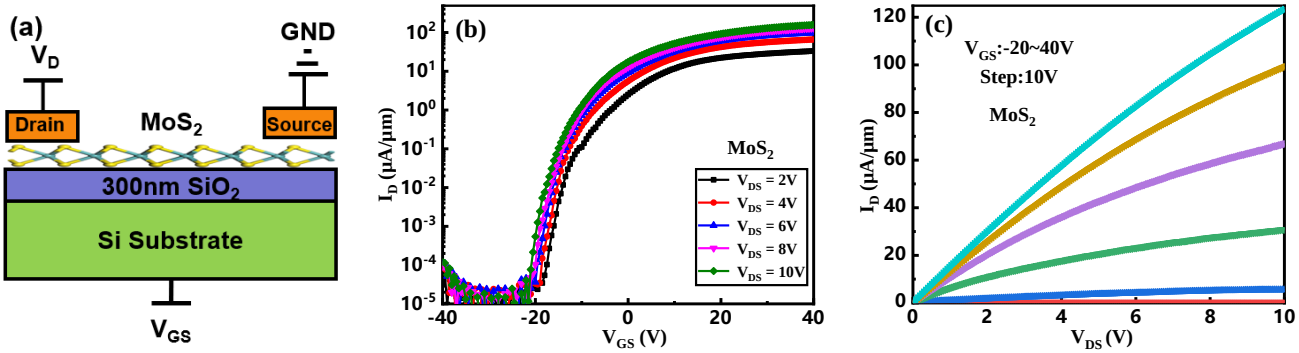


Figure 3. (**a**) Schematic diagram of MoS_2 FET, (**b**) transfer curve, and (**c**) output curve of MoS_2 FET.

From the output characteristics in Figure 3c, it can be observed that even at V_{DS} = 10 V and V_{GS} = 40 V, the current does not exhibit clear saturation. This suggests that a further increase in V_{DS} under the same gate bias could lead to additional output current enhancement. Such behavior is consistent with the electrostatic properties of two-dimensional materials, where the absence of drain-induced barrier lowering (DIBL) allows the application of high drain voltages without significant short-channel effects, thereby supporting high current drive.

3.2. WSe_2 FET

Figure 4a presents a schematic illustration of a WSe_2 FET, with a positive bias applied to the drain and the source terminal grounded. The corresponding transfer and output characteristics are displayed in Figure 4b and Figure 4c, respectively. As evidenced by the transfer curve in Figure 4b, the WSe_2 FET exhibits ambipolar conduction behavior. Specifically, the device operates as an n-channel enhancement-mode FET when the gate voltage exceeds 10 V and as a p-channel depletion-mode FET when the gate voltage is below 10 V.

Notably, the on-state current of the p-type regime reaches 2.9 μA/μm, which is two orders of magnitude higher than that of the n-type regime (3.6×10^{-2} μA/μm)—a significant disparity frequently observed in two-dimensional FETs. Given the more pronounced p-type conduction characteristics, this study focuses primarily on the p-type operation of the WSe_2 FET.

Figure 4c depicts the output characteristics of the WSe_2 FET under various negative gate voltages. Owing to the unencapsulated device structure, fluctuations observed in the output curves are attributable to unstable contact resistance during electrical measurement.

At V_{DS} = −5 V and V_{GS} = −40 V, the output current reaches saturation, with a saturation current of −2.26 μA/μm.

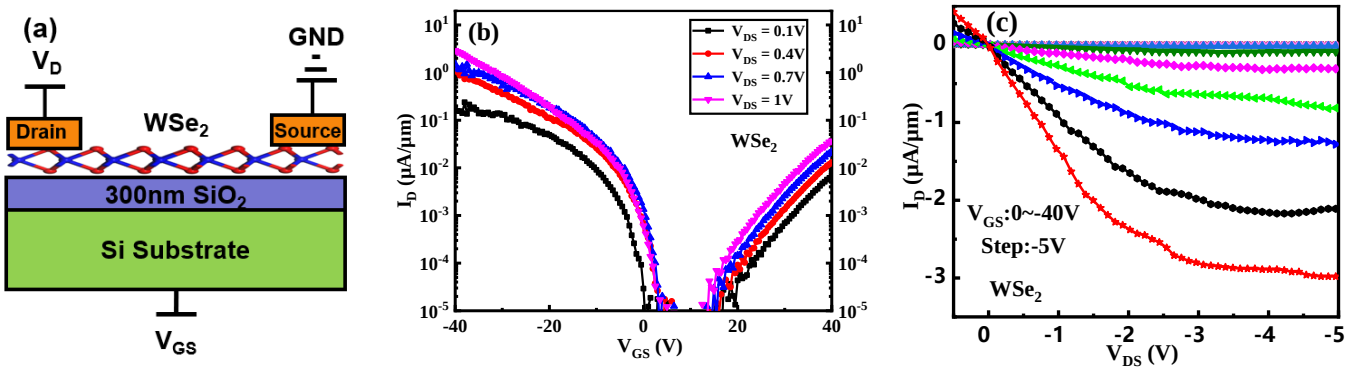


Figure 4. (**a**) Schematic diagram of WSe_2 FET, (**b**) transfer curve, and (**c**) output curve of WSe_2 FET.

3.3. MoS_2/WSe_2 Vdwh TFET

Based on the aforementioned electrical characterization, MoS_2 is identified as an n-type semiconductor, while WSe_2 exhibits predominant p-type characteristics. Accordingly, in the TFET configuration, WSe_2 was designated as the source and MoS_2 as the drain, with the MoS_2/WSe_2 van der Waals heterojunction serving as the channel region. A schematic of the resulting MoS_2/WSe_2 VdWh TFET is presented in Figure 5, illustrating the architecture in which a positive bias is applied to the MoS_2 drain and the WSe_2 source is grounded.

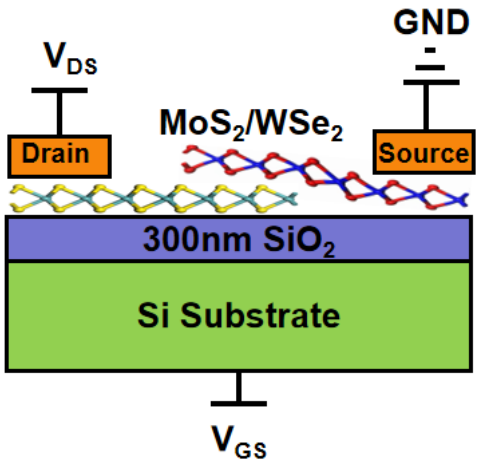


Figure 5. Schematic diagram of MoS_2/WSe_2 Vdwh TFET.

As illustrated in Figure 6a, the transfer characteristics of the MoS_2/WSe_2 van der Waals heterojunction TFET under positive drain bias can be categorized into four distinct operational regimes:

I For V_{GS} < −35 V, the device operates in a P–P state, characterized by strong hole accumulation in WSe_2 and weak hole accumulation in MoS_2.

II Within the range of −35 V < V_{GS} < −30 V, the device enters an I–P state, where WSe_2 maintains strong hole accumulation while MoS_2 remains in the off-state.

III Over the interval −30 V < V_{GS} < 15 V, an N–P state emerges, featuring strong hole accumulation in WSe_2 and pronounced electron accumulation in MoS_2. This regime further divides into two sub-regions: the heterostructure exhibits n-channel FET behavior for −30 V < V_{GS} < −14 V and p-channel FET behavior for −14 V < V_{GS} < 15 V.

IV For V_{GS} > 15 V, the device operates in an N–N state, with strong electron accumulation in MoS_2 and weak electron accumulation in WSe_2.

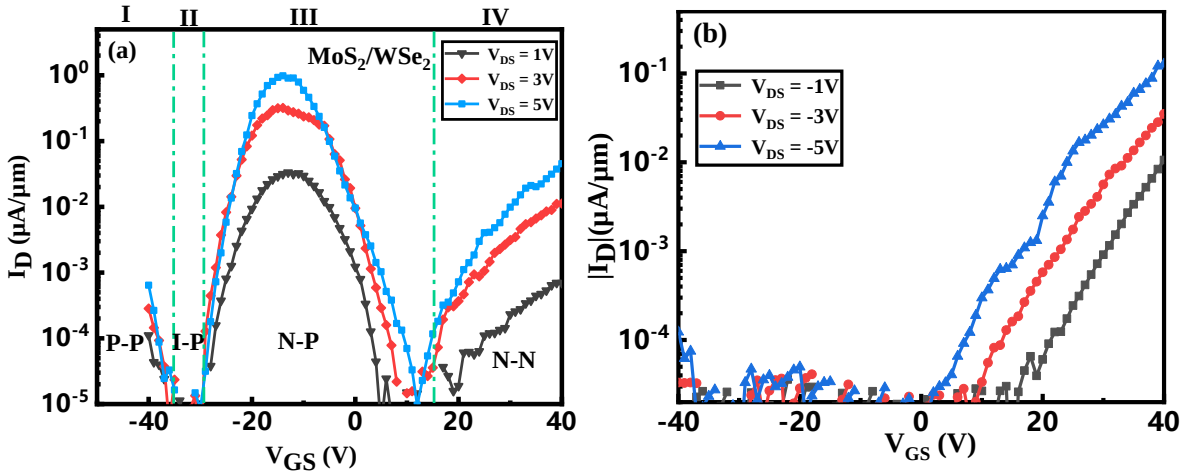


Figure 6. Transfer curve of a MoS_2/WSe_2 Vdwh TFET with (**a**) positive drain voltage and (**b**) negative drain voltage.

As shown in Figure 6b, under negative drain bias, the device exhibits negative conduction, which is that the drain current becomes negative upon application of a positive gate voltage. The transfer curve does not reach saturation even at V_{GS} = 40 V and V_{DS} = −5 V, indicating that the transistor can sustain higher gate and drain voltages without performance degradation.

In TFET devices, the calculation formula of carrier tunneling probability T_{WKB} is as follows [34]:

$$T_{WKB} = exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar\left(E_g + \Delta\Phi\right)}\right) \quad (1)$$

where m^* denotes the effective carrier mass, $\Delta\Phi$ represents the energy difference across the tunnel junction, E_g is the band gap of the semiconductor, and λ corresponds to the effective tunneling length. From Equation (1), it can be deduced that the tunneling probability can be enhanced by increasing $\Delta\Phi$ or reducing λ.

Figure 7 illustrates the energy band diagrams under various drain voltages while the gate voltage is held at 0 V. As evidenced by Figure 7a, the MoS_2/WSe_2 heterojunction forms a type-II staggered-gap heterostructure [35]. It can be inferred that as the drain voltage increases, both the enlargement of $\Delta\Phi$ and the reduction in λ contribute to an increase in carrier tunneling probability. Consequently, the tunneling current rises accordingly with drain voltage, a trend that aligns with the behavior observed in Figure 6a.

As depicted in Figure 8, the output characteristics are separately plotted under negative and positive gate voltages to facilitate a clearer comparison of the device's operational regimes under different bias conditions. Figure 8a indicates that under negative drain voltage, the saturation drain current increases with more positive gate bias, reaching a maximum value of 20 μA/μm. In contrast, under positive drain bias (Figure 8b), the saturation current ranges from 2.35×10^{-5} μA/μm at V_{GS} = −30 V to 4.33×10^{-2} μA/μm at V_{GS} = −10 V. No monotonic correlation between the saturation current and gate voltage is observed in this regime.

At V_{GS} = −30 V, the device operates in the I–P state, wherein MoS_2 is completely turned off, resulting in a significantly reduced drain current. In comparison, at VGS = −10 V, the heterojunction operates in the N–P state, with both WSe_2 and MoS_2 conducting, yielding a higher drain current of 0.99 μA/μm, as illustrated in the corresponding region of Figure 8a.

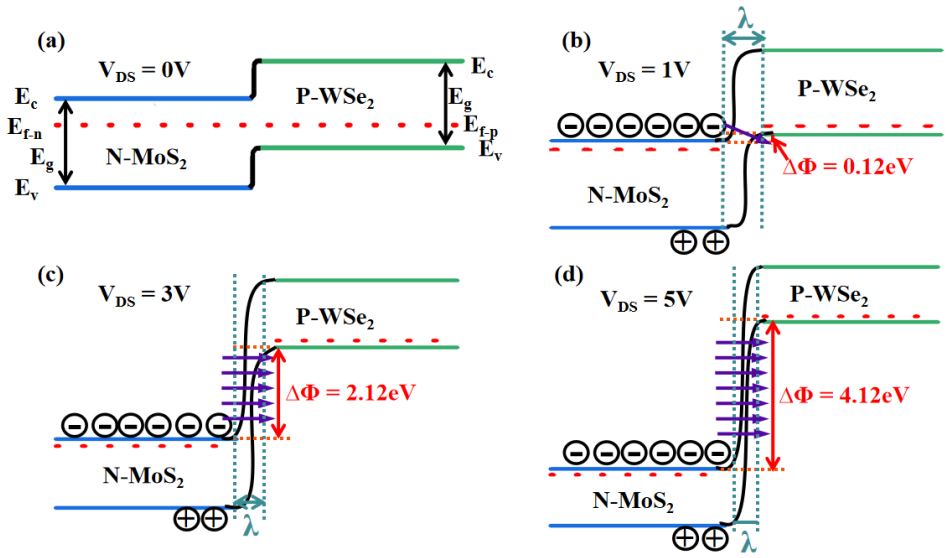


Figure 7. The band-bending diagram of the MoS_2/WSe_2 Vdwh at drain voltages of (**a**) 0 V, (**b**) 1 V, (**c**) 3 V, and (**d**) 5 V.

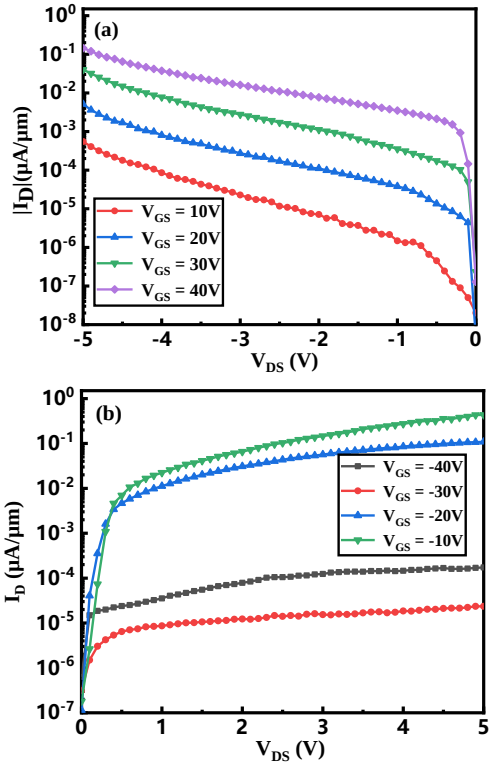


Figure 8. Output curve of a MoS_2/WSe_2 Vdwh TFET with (**a**) positive gate voltage and (**b**) negative gate voltage.

3.4. Comparison of Key Parameters of Four Different 2Dl FETs

In this study, three types of two-dimensional FETs were fabricated and characterized, namely, a MoS_2 FET, WSe_2 FET, and MoS_2/WSe_2 van der Waals heterojunction (Vdwh) TFET. Both the WSe_2 FET and the MoS_2/WSe_2 Vdwh TFET demonstrate configurable polarity through the application of different gate and drain voltages. Accordingly, this section presents a comparative analysis of the electrical properties of four distinct transistor configurations: MoS_2 nFET, WSe_2 pFET, MoS_2/WSe_2 nTFET, and MoS_2/WSe_2 pTFET.

In FETs based on two-dimensional materials, the carrier saturation mobility (μ_{sat}) is a critical parameter that governs the on-state current and switching speed, thus necessitating

accurate extraction. The saturation mobility can be derived from the saturation drain current expression in the transfer characteristics [36], as given by

$$I_D = \mu_{sat} C_g \frac{W}{2L} (V_{GS} - V_{th})^2 \quad (2)$$

where I_D denotes the drain current, μ_{sat} the saturation mobility, C_g the gate capacitance per unit area (for 300 nm SiO_2, C_g = 11.5 nF·cm^{-2}), V_{GS} the gate voltage, V_{th} the threshold voltage, and W and L the channel width and length, respectively.

The key electrical parameters of the various 2D FETs are summarized in Table 1. The MoS_2 NFET exhibits a high saturation electron mobility of 26 cm^2·V^{-1}·s^{-1} and a subthreshold swing (SS) of 3.28 V/dec, indicating superior switching performance. In contrast, the WSe_2 PFET shows a modest hole mobility of 0.34 cm^2·V^{-1}·s^{-1} and an SS of 4.65 V/dec, reflecting its relatively limited switching response. The MoS_2/WSe_2 nTFET and PTFET inherit the low off-state current from the MoS_2 NFET and the low on-state current characteristic of the WSe_2 PFET. As a result, their carrier saturation mobilities are substantially reduced—though still approximately double that of the WSe_2 PFET—while maintaining comparable SS values.

Table 1. Comparison of the electrical characteristic parameters of the different FETs.

FET	μ_{sat} (cm^2 V^{-1} s^{-1})	Vth (V)	SS (V/Dec)	I_{on}/I_{off}	I_{on} (μA/μm)	I_{off} (μA/μm)
MoS_2 NFET	26 ± 2	−21~−18	3.3	2.4×10^8	157	6.5×10^{-6}
WSe_2 PFET	0.3 ± 0.1	0~5	4.7	2.9×10^4	2.9	1×10^{-4}
MoS_2/WSe_2 NTFET	0.8 ± 0.1	−32~−30	4.0	1.15×10^5	0.99	8.6×10^{-6}
MoS_2/WSe_2 PTFET	0.5 ± 0.2	5~10	5.2	1.03×10^5	0.99	9.6×10^{-6}

4. Conclusions

In this paper, three types of two-dimensional field-effect transistors (2D FETs)—namely, a MoS_2 FET, WSe_2 FET, and MoS_2/WSe_2 van der Waals heterojunction (Vdwh) TFET—were fabricated and experimentally characterized. The electrical performance of these devices was evaluated through detailed analysis of their transfer and output characteristics. The MoS_2 NFET demonstrated a high saturation electron mobility of 26 cm^2·V^{-1}·s^{-1} and a current on/off ratio of 2.4×10^8 at a drain voltage of 10 V. Meanwhile, the MoS_2/WSe_2 NTFET, measured at a drain voltage of 5 V, exhibited a saturation electron mobility of 0.8 cm^2·V^{-1}·s^{-1} and a current on/off ratio of 1.15×10^5. The methodology employed in this work—analyzing heterojunction TFET performance through constituent single-material FETs—offers a valuable strategy for the investigation of 2D heterojunction tunnel devices. This approach not only provides insights into the design and optimization of such structures but also facilitates the development of low-power electronic devices based on two-dimensional materials.

Author Contributions: Conceptualization and writing—original draft preparation, C.C.; methodology, S.W. and S.C.; validation, C.C. and C.Y.; writing—review and editing, H.L. and S.W.; funding acquisition, C.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the China Postdoctoral Science Foundation (Grant No. 2025M770574) and National Natural Science Foundation of China (Grant No. U2241221). It was also jointly funded jointly Funded by the National Key Laboratory of Airborne Information Perception and Fusion and the Aeronautical Science Foundation: 20230001081024.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

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