micromachines

MDPI

Article

An X-Band Class-J GaN MMIC Power Amplifier with Well-Designed In-Band Output Power Flatness

Bangjie Zheng [1], Zhiqun Cheng [1,2], Zhiwei Zhang [1,3,*], Ruizhe Zhang [1], Tingwei Gong [1] and Chao Le [1]

[1] School of Electronics and Information, Hangzhou Dianzi University, Hangzhou 310018, China
[2] School of Information Engineering, Xinjiang Institute of Technology, Aksu 843100, China
[3] State Key Laboratory of Millimeter-Waves, Nanjing 210096, China
* Correspondence: zhiwei_zhang@hdu.edu.cn

Abstract: This paper presents an X-band high-power GaN MMIC power amplifier (PA). To balance efficiency, output power, and saturated power flatness, the load-line theory is employed to analyze and validate the power variation trends within an extended continuous Class B/J (CCBJ) impedance space. Theoretical constant power contours are plotted within this space. An L-C impedance matching network is used to match the amplifier's output impedance to the overlapping region of the 0.5 dB constant power contour and the CCBJ impedance space, significantly improving the in-band power flatness of the PA based on the CCBJ design approach. Additionally, an RC parallel structure is integrated into the interstage matching network to maximize gain while ensuring stability. The proposed PA, implemented using a 0.25 μm commercial GaN process, achieves a saturated output power of 47–47.6 dBm with in-band fluctuations within ± 0.3 dB, a power gain of 27.0–27.8 dB, and an efficiency of 40–45.5% across the X-band.

Keywords: power amplifier (PA); MMIC; GaN; X-band; Class-J

check for updates

Academic Editor: Piero Malcovati

Received: 12 December 2024
Revised: 7 January 2025
Accepted: 10 January 2025
Published: 13 January 2025

Citation: Zheng, B.; Cheng, Z.; Zhang, Z.; Zhang, R.; Gong, T.; Le, C. An X-Band Class-J GaN MMIC Power Amplifier with Well-Designed In-Band Output Power Flatness. *Micromachines* **2025**, *16*, 87. https://doi.org/10.3390/mi16010087

Copyright: © 2025 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

The X-band (8–12 GHz) power amplifier (PA) is crucial for applications in radar systems, phased array technologies, satellites, and communication systems [1]. With the increasing demand for higher performance in terms of saturated output power (P_{sat}), gain, efficiency, and size, power amplifiers have become a key limiting factor in the overall system performance. Among the various technologies available, gallium nitride (GaN) MMICs have emerged as the preferred choice for high-performance PAs due to their superior breakdown voltage, high thermal conductivity, and excellent power density [2]. Over the past decade, significant progress has been made in GaN MMIC PAs operating across various modes and frequency bands [3–5]. These advancements have highlighted the potential of GaN-based designs to push the boundaries of power, efficiency, and bandwidth for high-frequency applications.

The development of various operational modes for power amplifiers has significantly contributed to improving the performance of these devices. For example, Class-F amplifiers, which use a combination of harmonic termination techniques, are well known for their high efficiency due to the elimination of power losses in harmonics [6]. Similarly, Class-E amplifiers, with their resonant load network, achieve high efficiency by operating with zero voltage and current overlap, thus minimizing the losses associated with switching transitions [7]. More recently, the Class-GF mode has been introduced, which combines the advantages of Class-F and Class-E amplifiers while further extending the bandwidth and enhancing the efficiency by optimizing both fundamental and harmonic components [8].

These techniques have been successful in achieving high power output and efficiency, but they often face limitations in maintaining a broad impedance space, particularly when aiming for multi-octave bandwidths.

The Class-J mode, introduced by Cripps in 2009 [9], was a significant breakthrough as it extended Class-B into a continuous mode, offering a broader impedance space for both fundamental and second harmonic frequencies. This feature provides more flexibility for power amplifier designs, enabling better performance in terms of efficiency and output power across a wider range of frequencies. However, while Class-J offered several advantages, the need to optimize both the fundamental and harmonic impedance spaces for high-performance designs remained a challenge. In response to this, the resistive–reactive Class-J (RRCJ) mode was developed [10,11], incorporating a resistive factor (β) into the voltage waveform. This modification extended the impedance space for the fundamental frequency to the left and for the second harmonic to the right on the Smith chart, creating an overlap that significantly improved efficiency and output power across broader frequency bands.

Further advancing this approach, the extended resistive continuous class B/J (CCBJ) mode [12] introduced an additional factor (γ) that further refined the impedance space, allowing designers to achieve even higher efficiency while minimizing distortion. This mode proved especially effective in extending the bandwidth and improving the performance of GaN-based power amplifiers. However, according to load-pull results, a significant reduction in saturated power is observed within the expanded continuous Class-B/J impedance space. This behavior deviates from the ideal conditions predicted by theory. This discrepancy arises due to the fact the voltage swing limitation in actual PAs is neglected during the manipulation of the voltage waveform. As a result, despite these advancements, achieving a well-balanced design that ensures high power flatness, stable gain, and efficiency across the entire X-band remains a challenging task, especially when dealing with the complex impedance-matching requirements of modern communication and radar systems.

In this context, the work presented in this paper leverages the benefits of the CCBJ mode while addressing its limitations for achieving good power flatness. Firstly, based on load-line theory, the impedance space of equal power contours is calculated and analyzed, and for the first time, the output power variation trend within the CCBJ theory impedance space is explored. Secondly, by combining the CCBJ impedance space with the calculated constant power contours, the target impedance space for designing high-efficiency PAs with minimum in-band power fluctuation is derived. Finally, a GaN MMIC power amplifier operating in the 8–12 GHz range is designed and fabricated. The proposed amplifier achieves high saturated power and efficiency and demonstrates significant advantages in in-band power flatness when compared to similar amplifiers reported in the literature.

2. Analysis of the Proposed Design Strategy

The voltage waveform of Class-J mode [9] is defined by Equation (1):

$$V_J(\theta) = (1 - cos\theta)\cdot(1 - \alpha\ sin\theta) \tag{1}$$

where α ($-1 \leq \alpha \leq 1$) represents the continuous mode parameter and θ represents the phase angle of the output voltage related to frequency. As long as the value of α is within the range of [−1,1], the efficiency remains at the ideal Class-J efficiency of 78.7%, while the P_{sat} remains unchanged.

The voltage waveform of the RRCJ mode [12] adds a resistive factor $(1 + \beta\ cos\theta)$ to Equation (1), forming Equation (2).

$$V_{RRCJ}(\theta) = (1 - cos\theta)\cdot(1 - \alpha\ sin\theta)\cdot(1 - \beta\ cos\theta) \tag{2}$$

Here, β ($0 \leq \beta \leq 0.38$) represents the resistive modulation coefficient. The addition of the resistive factor extends the fundamental impedance of Class-J to the left from the center, while the second harmonic impedance is extended to the right from the edge of the Smith chart, thereby merging the fundamental and second harmonic impedance spaces.

The voltage waveform of the CCBJ mode is given by Equation (3):

$$V_{CCBJ}(\theta) = (1 - cos\theta)\cdot(\gamma - \alpha\ sin\theta)\cdot(1 - \beta\ cos\theta) \tag{3}$$

which adds the γ factor ($1 \leq \gamma \leq 1/(1-\beta)$) to the RRCJ mode, extending the fundamental impedance space from the center to the right. The value of γ controls the extent of the impedance space expansion. The drain-source current (i_{ds}) for the three modes mentioned above is defined as Equation (4).

$$i_{ds}(\theta) = 1 + \sum_{k=1}^{\infty} i_k cos\ k\theta = 1 + \frac{\pi}{2}cos\theta + \frac{2}{3}cos2\theta \ldots \tag{4}$$

According to formulae (3) and (4) in Ref. [12], the fundamental and second harmonic impedances of the CCBJ mode are derived as shown in Equation (5).

$$Z_1 = R_{opt}[\gamma(1-\beta) + j\alpha(1 - 0.25\ \beta)], \quad Z_2 = \frac{3\pi R_{opt}}{8}[\gamma\beta + j\alpha(1-\beta)] \tag{5}$$

The corresponding impedance space is illustrated in Figure 1, with parameter ranges defined as $-1 \leq \alpha \leq 1, 0 \leq \beta \leq 0.38, 1 \leq \gamma \leq 1.6$. The yellow area represents the fundamental impedance, defined as Z_1, and the blue area represents the second harmonic impedance, defined as Z_2.

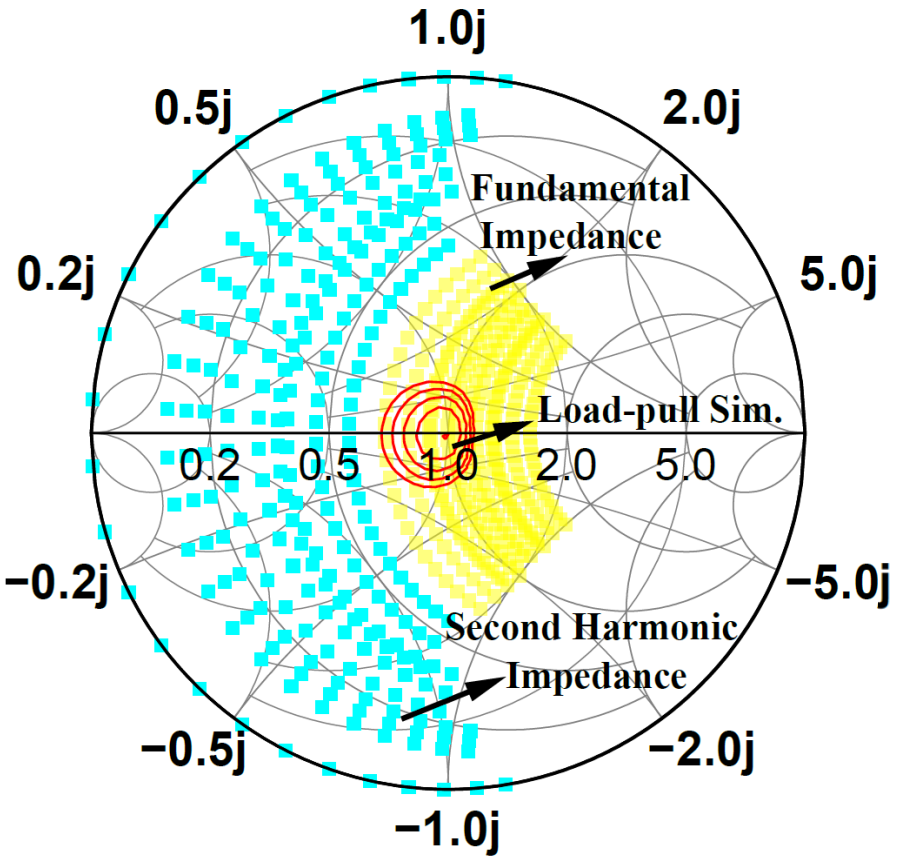


Figure 1. The impedance space of CCBJ and the load-pull simulation results.

Although efficiency within the impedance space has been extensively studied, output power analysis remains limited. As shown in Figure 1, the red circles represent power contours from load-pull simulations at 12 GHz using the GaN transistor employed in this work (normalized to R_{opt}), with power steps set to 0.3 dB and the harmonic impedance configured as open. Within the CCBJ-defined impedance space, saturated power fluctuations exceed ± 1.2 dB. This variation causes significant power fluctuations across the amplifier's bandwidth.

To address this, an analysis based on the classic load-line theory is conducted. The concept of optimal power impedance (R_{opt}) was first introduced in the load-line theory proposed in Ref. [13] and has since been widely applied in various power amplifier theories. During PA operation, the output voltage is limited by the drain supply voltage (V_{dc}), while the maximum drain-source current (I_{max}) is constrained by the product of transistor size and its power density. When either the voltage or current exceeds these physical limits, power compression occurs. Assuming that the output voltage (V_{DS}) and current (I_D) expressions are given as in Equation (6):

$$V_{DS} = V_{dc}(1 - \sin\theta), I_D = \frac{I_{max}}{2}(\sin\theta + 1), \quad I_{dc} = \frac{I_{max}}{2} \tag{6}$$

a load impedance, $R_{opt,}$ exists that allows both the voltage and current amplitudes to reach their maximum values, thereby delivering the maximum power P_{opt}, as shown in Equation (7).

$$R_{opt} = \frac{V_{dc}}{I_{max}/2} = \frac{V_{dc}}{I_{dc}}, P_{opt} = \frac{1}{2} \cdot \frac{V_{dc}}{I_{dc}} \tag{7}$$

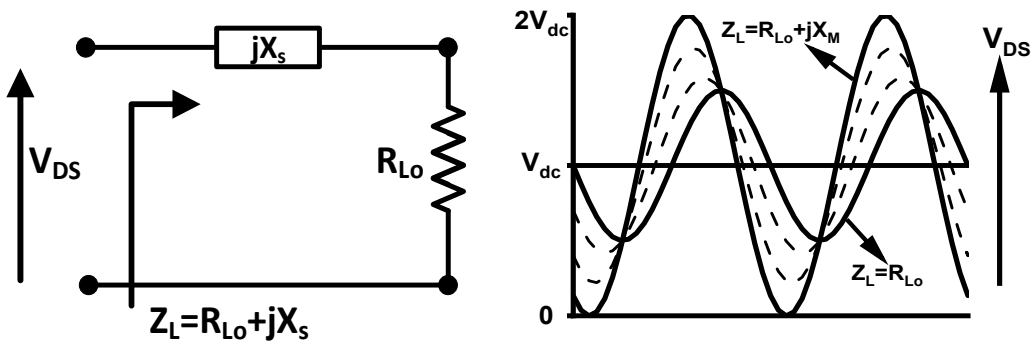
When the load impedance decreases to R_{opt}/p ($p \geq 1$), defined as R_{LO}, the voltage swing must reduce to prevent the current swing from exceeding I_{max}. Conversely, when the load impedance increases to pR_{opt}, defined as R_{HI}, the current swing must decrease to ensure that the voltage swing remains within $2V_{dc}$. The corresponding output powers, P_{LO} and P_{HI}, are given in Equation (8).

$$R_{LO} = \frac{R_{opt}}{p}, \; R_{HI} = \mathrm{p} \cdot R_{opt}, \quad P_{LO} = P_{HI} = \frac{P_{opt}}{p} \tag{8}$$

To analyze the impact of the reactance on power, the series reactance jX_s is added to the load resistance R_{LO}, as shown in Figure 2a. As X_s increases, the phase and amplitude of the voltage waveform V_{ds} change, as illustrated in Figure 2b. Notably, when X_s reaches a certain level, denoted as X_m, the voltage amplitude returns to its physical limit of $2V_{dc}$. However, if X_s continues to increase, the voltage amplitude will exceed this limit, leading to power compression. From these calculations, the conclusions presented in Equation (9) can be derived:

$$P_{RF} = \frac{P_{opt}}{p} \; (-X_m \leq X_s \leq X_m), \sqrt{{R_{LO}}^2 + {X_m}^2} = R_{opt} \tag{9}$$

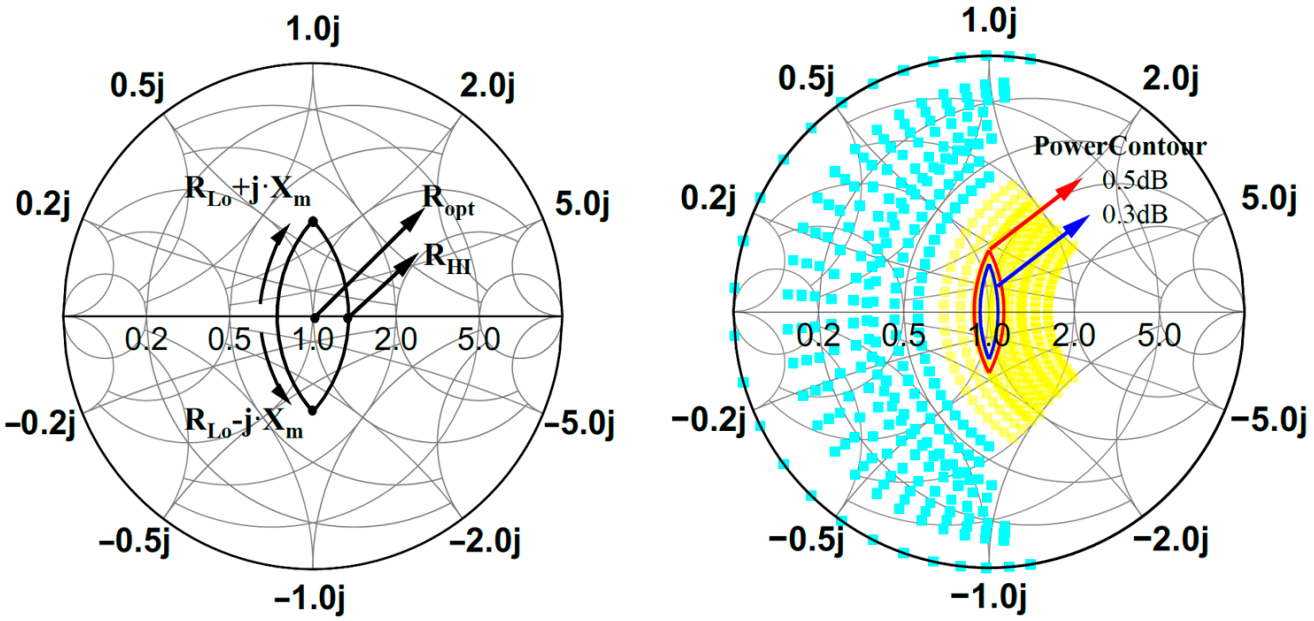
which shows that when the real part of the impedance is set to R_{LO} and the imaginary part varies between $-X_m$ and X_m, the output power (P_{RF}) remains constant. Similarly, when the load resistance equals R_{HI}, adding a parallel reactance results in an analogous conclusion; the detailed derivation process can be found in Ref. [13].



(**a**) (**b**)

Figure 2. (**a**) The impedance of the load, Z_L; (**b**) variations of V_{ds} with Z_L.

Based on the above analysis, by plotting the impedance space on the Smith chart, a closed power contour curve can be obtained, as shown in Figure 3a. By combining the load-line power contours with the theoretical impedance space of CCBJ, a more realistic representation of power variations within the CCBJ-mode impedance space can be obtained. As shown in Figure 3b, by plotting the CCBJ-mode impedance space alongside the 0.3 dB and 0.5 dB power contours on the same Smith chart, the impedance regions where the power fluctuations are less than 0.3 dB and 0.5 dB within the CCBJ-type impedance space can be identified. As a result, designing a power amplifier within the overlapping impedance space leads to a highly efficient class-J power amplifier with excellent in-band saturation power flatness.



(**a**) (**b**)

Figure 3. (**a**) Consistent power circle of the load-line theory; (**b**) 0.3 dB and 0.5 dB power contours within the impedance space of CCBJ.

3. Circuit Design and Implementation

For validation, an X-band Class-J MMIC PA is designed using a 0.25 µm commercial GaN HEMT process. The schematic of the fabricated PA is shown in Figure 4 and its corresponding photograph is presented in Figure 5. The drain DC bias voltage (V_d) of all three stages is 28 V, while the gate DC bias voltage (V_g) is set to −2.2 V. The transistor sizes

for the three stages are 2 × 6 × 80 µm, 8 × 6 × 80 µm, and 16 × 6 × 150 µm, respectively. To ensure stability, a balancing resistor is added between every two pairs of transistors in the second and third stages, and resistors are also placed on the gates of all transistors, as shown in Figure 4. The layout adopts a fully symmetrical structure, with a top-and-bottom symmetric power supply configuration. All capacitors without labeled values in Figure 4 are bypass capacitors. As shown in the blue box in Figure 4, the matching circuit is divided into four parts: the output matching network, two intermediate matching networks, and the input matching network. The details of each part are described below.

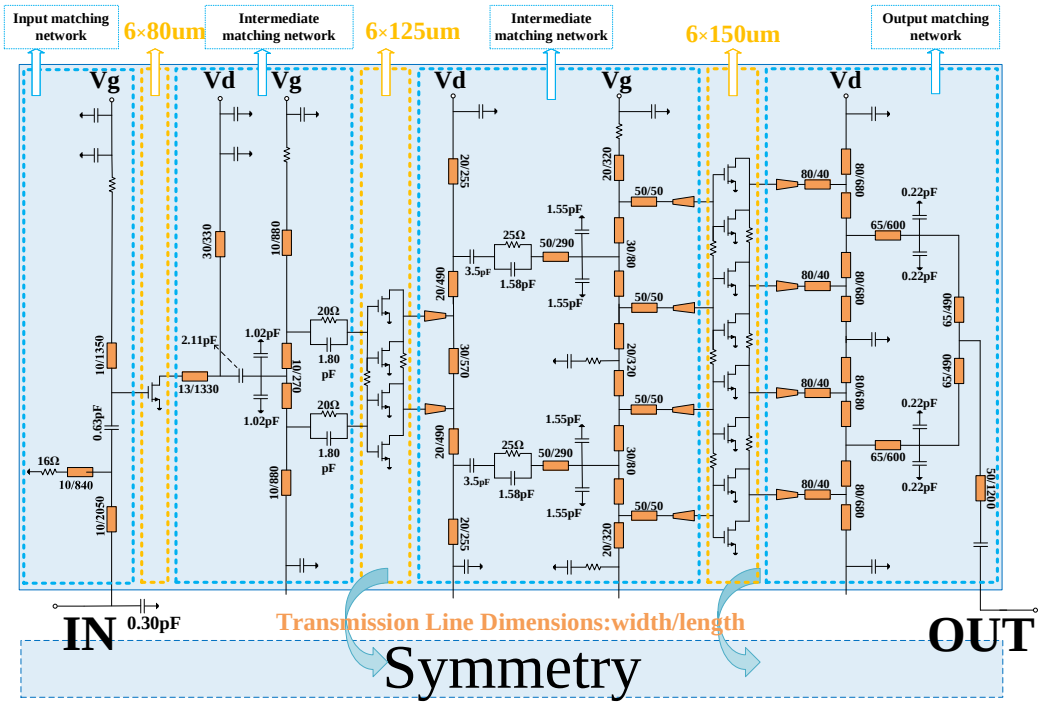


Figure 4. Schematic of the designed PA.

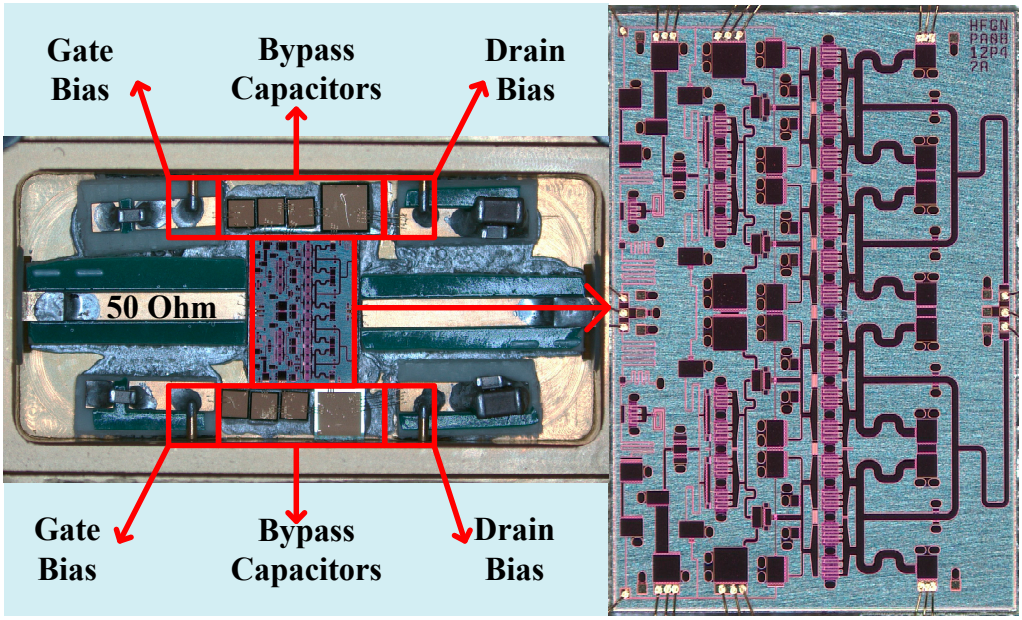


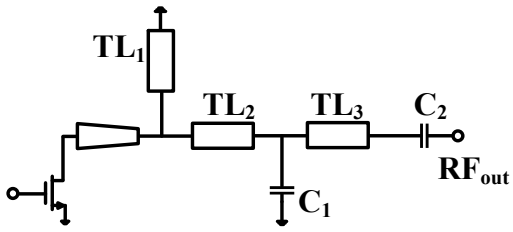
Figure 5. Photograph of the fabricated PA.

3.1. Output Matching Network

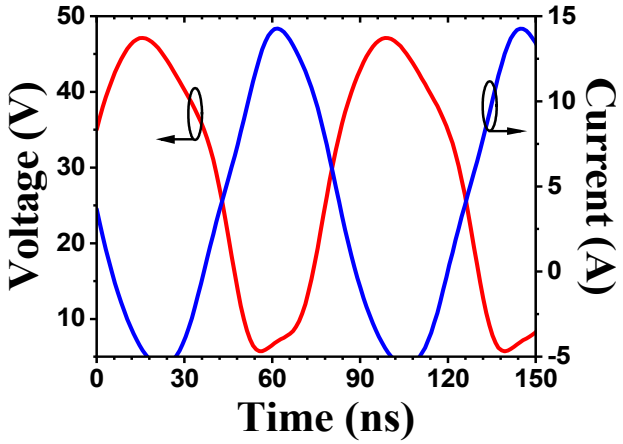
Based on the analysis in Section 2, the output fundamental impedance needs to be matched to the overlapping region of the equal power contour and the CCBJ-type impedance space. Through our calculations, the real part of the fundamental load impedance is determined to have a range of [0.89, 1.12], while the imaginary part has a range of [−0.45, 0.45]. The corresponding ranges for α, β, and γ are [−0.4, 0.4], [0, 0.13], and [1, 1.1].

To match the output impedance to the target impedance space shown in Figure 3b, an L-C-L three-section impedance matching network was employed. The equivalent lumped-element circuit is illustrated in Figure 6a, with TL_1 serving as an RF chock connected to the drain voltage supply, while C_2 serves as a DC-blocking capacitor. By combining calculations with ADS optimization, the parameters of the matching network can be determined, as shown in the table in Figure 6a. The simulated impedance trajectory of the final output matching network is represented by the black line in Figure 7. It is evident that the fundamental impedance falls perfectly within the target impedance space, while the harmonic impedance also lies within the CCBJ-defined impedance space. The simulation results show that the implemented impedance matching network achieves an insertion loss between 0.4 dB and 0.48 dB across the operating frequency band. The large-signal simulation results further demonstrate that the output stage delivers power in the range of 47.8 dBm to 48.2 dBm, exhibiting excellent in-band flatness that is consistent with the theoretical analysis. The simulated drain voltage and current waveforms of the output stage are shown in Figure 6b, aligning well with the theoretical waveforms of the CCBJ mode.

Design Parameters		
TL(impedance/electrical length)		
TL_1:6.9/25	TL_2:12.5/22	TL_3:30/60
Capacitor(pF)		
C_1:1.72	C_2:1.75	



(**a**)



(**b**)

Figure 6. (**a**) Output harmonic tuning network; (**b**) simulated drain voltage and current waveforms.

3.2. Intermediate Matching Network

The equivalent lumped-component structure of the input and interstage matching networks, along with their corresponding parameters, is shown in Figure 8. In the design of the interstage matching network, it is essential to match the output impedance of the preceding stage transistor with its optimal power impedance, ensuring sufficient power output from the preceding stage. Simultaneously, the right-side impedance must form a conjugate match with the input impedance of the subsequent stage to achieve adequate power gain.

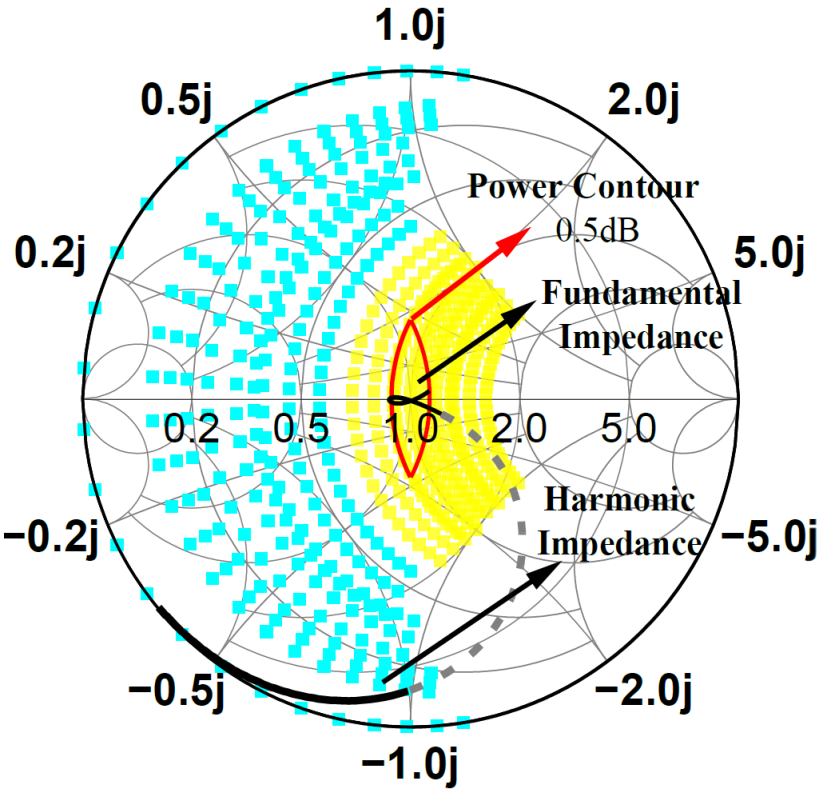


Figure 7. Simulated impedance of the output matching network.

TL (impedance/electrical length)			Capacitor (pF)			Resistor (Ω)		
Input Matching			Stage 1–2 Matching			Stage 2–3 Matching		
TL_1:90/60	TL_2:90/25	TL_3:90/40	TL_4:84/39	TL_5:62/10	TL_6:73/8	TL_8:55/15	TL_9:55/7.7	TL_{10}:30/2.6
			TL_7:73/26			TL_{11}:30/10		
C_1:0.3	C_2:1.2		C_3:4.2	C_4:4.1	C_5:3.8	C_6:14.0	C_7:6.32	C_8:12.4
R_1:8.0			R_2:9.4			R_3:6.5		

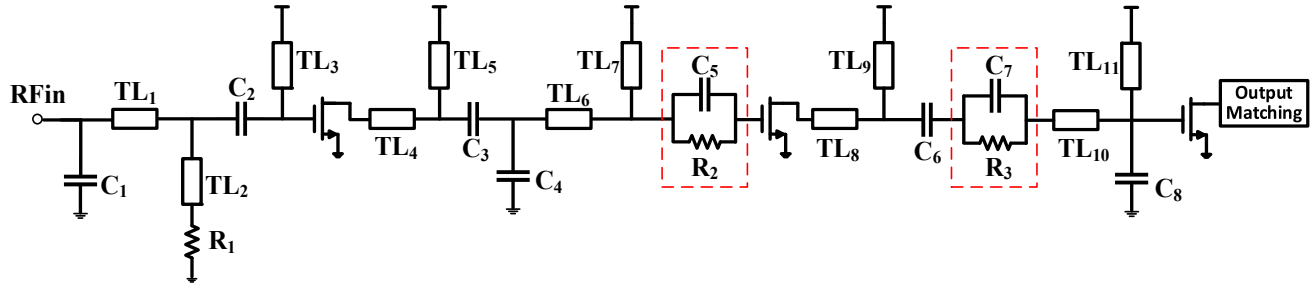


Figure 8. Equivalent lumped-component schematic of the input and intermediate matching networks.

To accomplish this, an interstage matching network composed of an RC parallel network and an LC network is employed. To enhance the flexibility of the matching network, all components contribute to impedance matching. Through a combination of calculations and tuning, the impedance is precisely conjugately matched to the input impedance of the subsequent stage transistor and aligned with the optimal power impedance of the preceding stage transistor. The RC parallel network (highlighted in the red box in Figure 8) not only broadens the bandwidth of the matching network but also allows for simultaneous adjustments to the amplifier's stability and gain by tuning the value of the resistor. Notably, the RC parallel network between the second and third stages is placed after the LC matching network rather than directly on the gate of the transistor, as seen in conventional matching networks. This placement minimizes the resistive losses that could otherwise

negatively impact the saturated output power, further enhancing the saturation performance. Additionally, TL_5 and TL_9 serve as drain supply lines for the first and second stages, while TL_7 and TL_{11} act as gate supply lines for the second and third stages. These lines participate in impedance matching while also functioning as RF chokes.

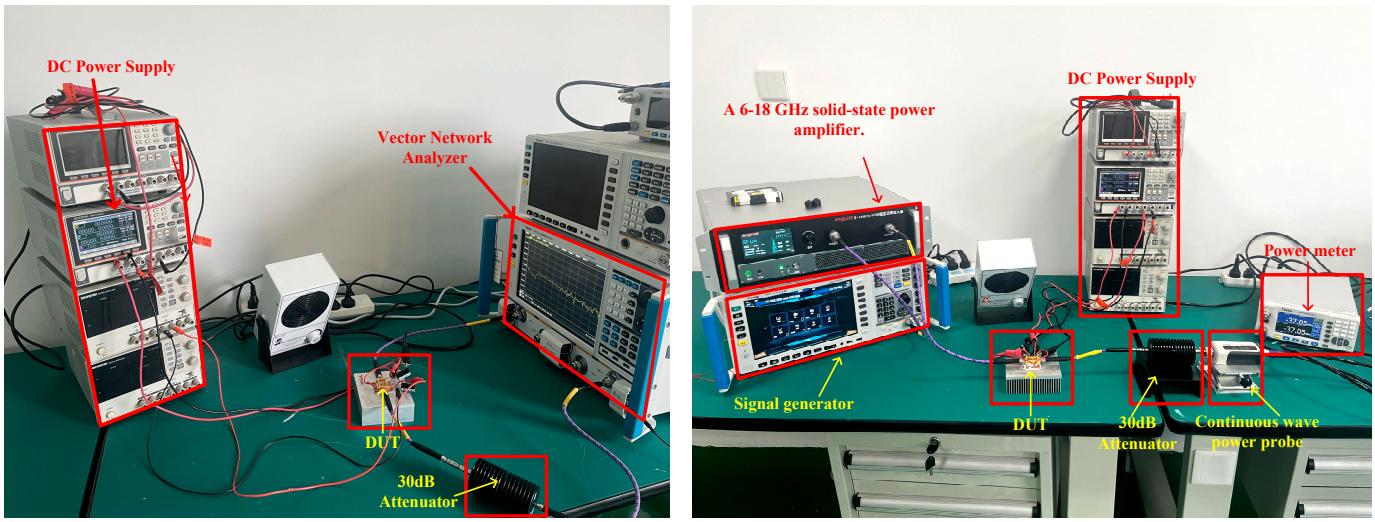
3.3. Input Matching Network

The input matching network adopts a C-L-L-C structure, with TL_3 serving as the gate supply line for the first stage and also contributing to impedance matching. To improve the bandwidth of the input impedance matching network, the resistor R_1 is placed in series below TL_2. By adjusting R_1, a trade-off between the amplifier's S_{11} and S_{21} can be achieved.

4. Measurements and Characterization

4.1. Test Environment Setup

Figure 9a shows the small-signal test setup. The test is performed using a vector network analyzer, with the drain and gate voltage supplies set to 28 V and −2.2 V, respectively. A 30 dB attenuator is added to protect the instrument but is removed during the S_{22} measurement. Figure 9b illustrates the large-signal test environment. To ensure sufficient input power for measuring the saturation power of the DUT, a 6–18 GHz solid-state power amplifier is used to amplify the signal from the signal generator. This amplifier provides up to 50 W of output power and is able to measure both the forward and reflected power, meaning that the power gain can be calculated accordingly. A power meter with a continuous wave power probe measures the output power of DUT, while a 30 dB attenuator is used to protect the instrument. The DC power supply can display the DC power consumption, meaning that the PAE can be calculated accordingly.



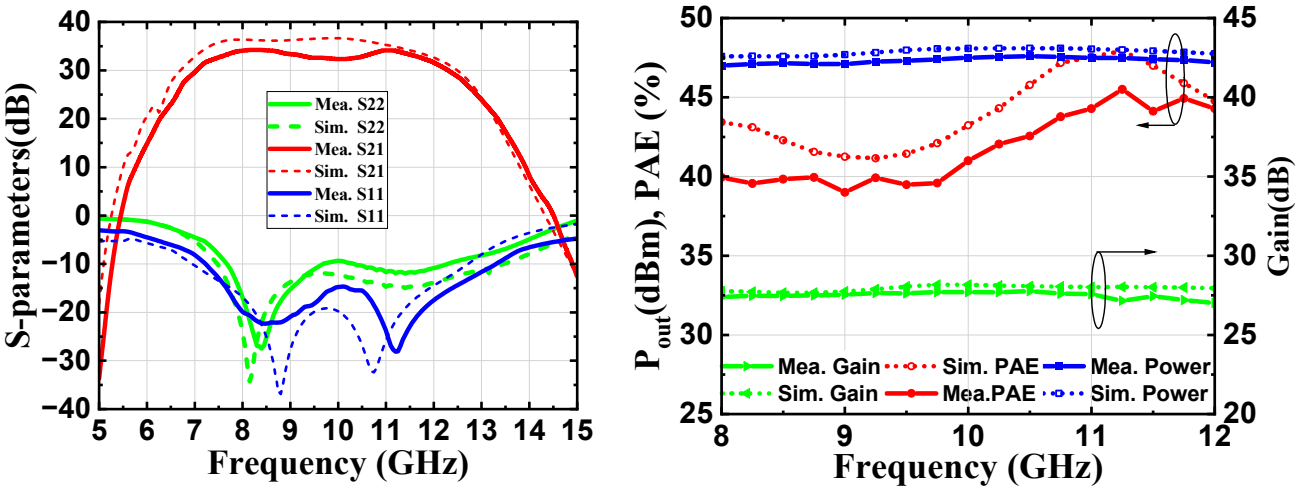
(**a**) (**b**)

Figure 9. (**a**) S-parameter measurement setup; (**b**) large-signal measurement setup.

4.2. Test Results Analysis

Figure 10a presents the measured and simulated S-parameters. As shown in Figure 10a, the input return loss (S_{11}) remains below −14.7 dB across the operating band, the small-signal gain (S_{21}) ranges from 32.4 to 34.2 dB, and the designed PA remains stable across all frequencies. The measured S-parameter results show a trend that is consistent with the simulation results, although there is a slight frequency shift toward higher frequencies. This minor discrepancy between the simulation and the measurements is likely due to

factors such as modeling, coupling, or thermal effects, which are common in MMIC design. Therefore, during the design process, the operational bandwidth was intentionally extended and a certain margin was included to ensure that the chip maintains good performance within the target frequency range, even with potential frequency offsets and performance deterioration.



(**a**) (**b**)

Figure 10. (**a**) Simulated and measured S-parameters; (**b**) simulated and measured output power, PAE, and gain versus frequency.

Figure 10b shows that the saturated output power ranges from 47.0 to 47.6 dBm across 8–12 GHz, with an in-band fluctuation of ±0.3 dBm. The power gain varies from 27.0 to 27.8 dB, while the PAE remains between 40.0% and 45.5% over the same frequency band. The large-signal test results generally align with the simulations, although some performance degradation is observed. This is likely due to the use of continuous wave testing, where the characteristics of the GaN power devices under high power and temperature conditions differ from those assumed in the modeling process. Therefore, such a degradation is to be expected. Despite this, the large-signal performance of the proposed amplifier remains competitive.

4.3. Comparison with the Existing Literature

Table 1 provides a performance comparison between the proposed X-band GaN MMIC power amplifier (PA) and other state-of-the-art designs. This comparison highlights several key parameters, such as output power, power flatness, power-added efficiency (PAE), gain, and the number of stages used in each design.

Table 1. Performance comparison with X-band GaN MMIC PAs.

Ref.	Process	Freq.	P_{out}	P_{out} Flatness	PAE	Gain	Stages	Area	Class
	(μm)	(GHz)	(dBm)	(dBm)	(%)	(dB)	(\)	(mm^2)	(\)
[1]	0.25	9.8–10.4	42	±1.1	38	18	2	18	AB
[2]	0.25	8.5–10.2	43	±1.2	43	25	3	7.7	F^{-1}
[4]	0.14	9.6–11.0	40	±1.5	61	10	1	\	F
[14]	0.25	8–12	43	±0.5	38	23	3	7.5	AB

Table 1. *Cont.*

Ref.	Process	Freq.	P_{out}	P_{out} Flatness	PAE	Gain	Stages	Area	Class
	(μm)	(GHz)	(dBm)	(dBm)	(%)	(dB)	(\)	(mm^2)	(\)
[15]	0.25	8–12	49	±0.55	45	22.7	3	13.3	AB
[16]	0.15	10–10.5	42	±0.75	50	20	2	9.2	HT_3
[17]	0.15	8–12.5	41	±0.60	52	20	2	\	AB
[18]	0.15	9.5–10.5	47	±1.0	55	10	1	12.2	AB
This work	0.25	8–12	47.6	±0.3	45.5	27.8	3	17	J

The realized PA achieves a saturated output power of 47.6 dBm across the 8–12 GHz frequency band, with an impressive in-band power flatness of ±0.3 dB. This is a notable improvement over several other designs that exhibit larger output power fluctuations, typically in the range of ±1.0 to ±1.5 dB. In terms of power-added efficiency (PAE), the proposed amplifier demonstrates an efficiency of between 40% and 45.5%, which is competitive compared to other X-band GaN MMIC amplifiers. While some designs, such as that in Ref. [17], report higher efficiencies (up to 52%), they often come at the cost of either output power or bandwidth limitations. By combining load-line theory with CCBJ, this design has precisely defined the optimal operating impedance space, which allows for a better balance between output power and efficiency. Furthermore, the well-designed RC structure enables this PA to exhibit superior gain compared to other designs.

These results validate our theoretical analysis and demonstrate the implementation of an effective design methodology for high-power, high-efficiency MMIC power amplifiers with excellent in-band P_{out} flatness.

5. Conclusions

This paper presents a novel design approach for a high-power, high-efficiency X-band GaN MMIC power amplifier, achieving significant improvements in performance and methodology. By combining load-line theory with the CCBJ impedance space, an analytical framework is developed to define the optimal impedance conditions for maximizing efficiency and minimizing power fluctuations. This approach offers a more precise and reliable path for designing high-performance power amplifiers.

The analysis of power fluctuations within the CCBJ impedance space leads to the identification of a target impedance region that ensures minimal power variation, resulting in an amplifier with excellent output power flatness. Operating across the 8–12 GHz frequency range, the amplifier delivers a saturated output power of 47.6 dBm with in-band power flatness of ±0.3 dB, outperforming similar designs in power stability.

A novel R-C interstage matching network is also introduced, enhancing the saturated output power while maintaining stability and gain. This innovation, combined with CCBJ-based impedance optimization, allows the amplifier to achieve efficiency levels of between 40% and 45.5% and a gain range of 27.0 to 27.8 dB.

In conclusion, the proposed amplifier represents a significant advancement in high-power, high-efficiency designs with superior in-band power flatness, addressing the limitations of existing amplifiers while offering a scalable approach for future X-band power amplifier development.

Author Contributions: Conceptualization, B.Z. and B.Z.; methodology, B.Z.; validation, B.Z. and C.L.; investigation, B.Z., R.Z. and T.G.; writing—original draft preparation, B.Z.; writing—review and

editing, B.Z. and Z.Z.; supervision, Z.C. and Z.Z.; project administration, Z.C. and Z.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Project of Zhejiang Provincial Science and Technology plan (Grant:2024C01076), the Open Foundation of the State Key Laboratory of Millimeter-Waves (Grant K202540), Project of Shanxi Provincial Science and Technology plan (Grant:2023-ZDLGY-49) and Project of Ministry of Science and Technology (Grant D20011).

Data Availability Statement: The data presented in this work are available within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Resca, D.; Raffo, A.; Di Falco, S.; Scappaviva, F.; Vadala, V.; Vannini, G. X-Band GaN Power Amplifier for Future Generation SAR Systems. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 266–268. [CrossRef]
2. Ghanaatian, A.; Abrishamifar, A.; Rahmati, A.; Alizadeh, A. A 15-W X-Band Inverse Class-F GaN Power Amplifier With Second-Harmonic Input Tuning. *IEEE Microw. Wirel. Technol. Lett.* **2023**, *33*, 1317–1320. [CrossRef]
3. Jiang, X.; Huang, W.; Bao, C.; Wu, X.; Wei, K.; Liu, X.; Luo, W. A High-Efficiency Continuous Class-F GaN MMIC Power Amplifier Using a Novel Harmonic Matching Network. *IEEE Microw. Wirel. Tech. Lett.* **2023**, *33*, 1321–1324. [CrossRef]
4. Kang, J.; Moon, J.-S. Highly Efficient Wideband X-band MMIC class-F Power Amplifier with Cascode FP GaN HEMT. *Electron. Lett.* **2017**, *53*, 1207–1209. [CrossRef]
5. Liu, B.; Mao, M.; Boon, C.C.; Choi, P.; Khanna, D.; Fitzgerald, E.A. A Fully Integrated Class-J GaN MMIC Power Amplifier for 5-GHz WLAN 802.11ax Application. *IEEE Microw. Wirel. Compon. Lett.* **2018**, *28*, 434–436. [CrossRef]
6. Molnar, B. Basic Limitations on Waveforms Achievable in Single-Ended Switching-Mode Tuned (Class E) Power Amplifiers. *IEEE J. Solid-State Circuits* **1984**, *19*, 144–146. [CrossRef]
7. Carrubba, V.; Clarke, A.L.; Akmal, M.; Lees, J.; Benedikt, J.; Tasker, P.J.; Cripps, S.C. The Continuous Class-F Mode Power Amplifier. In Proceedings of the 40th European Microwave Conference, Paris, France, 28–30 September 2010; pp. 1674–1677. [CrossRef]
8. Xuan, X.; Cheng, Z.; Zhang, Z.; Gong, T.; Liu, G.; Le, C. Design of an Extended Continuous-Mode Class-GF Power Amplifier With Multioctave Bandwidth. *IEEE Microw. Wirel. Tech. Lett.* **2023**, *33*, 1329–1332. [CrossRef]
9. Cripps, S.C.; Tasker, P.J.; Clarke, A.L.; Lees, J.; Benedikt, J. On the Continuity of High Efficiency Modes in Linear RF Power Amplifiers. *IEEE Microw. Wirel. Compon. Lett.* **2009**, *19*, 665–667. [CrossRef]
10. Friesicke, C.; Quay, R.; Jacob, A.F. The Resistive-Reactive Class-J Power Amplifier Mode. *IEEE Microw. Wirel. Compon. Lett.* **2015**, *25*, 666–668. [CrossRef]
11. Li, Q.; He, S.; Shi, W.; Dai, Z.; Qi, T. Extend the Class-B to Class-J Continuum Mode by Adding Arbitrary Harmonic Voltage Elements. *IEEE Microw. Wirel. Compon. Lett.* **2016**, *26*, 522–524. [CrossRef]
12. Latha, Y.M.A.; Rawat, K. Design of Ultra-Wideband Power Amplifier Based on Extended Resistive Continuous Class B/J Mode. *IEEE Trans. Circuits Syst. II* **2022**, *69*, 419–423. [CrossRef]
13. Cripps, S.C. *RF Power Amplifiers for Wireless Communications*, 2nd ed.; Artech House Microwave Library; Artech House: Boston, MA, USA, 2006.
14. Wu, H.; Wang, C.; Lin, Q.; Chen, Y.; Hu, L.; Tong, W. A High-Efficiency 15-Watt GaN HEMT X-Band MMIC Power Amplifier. In Proceedings of the 2018 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Chengdu, China, 7–11 May 2018; pp. 1–3. [CrossRef]
15. Tao, H.-Q.; Hong, W.; Zhang, B.; Yu, X.-M. A Compact 60W X-Band GaN HEMT Power Amplifier MMIC. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *27*, 73–75. [CrossRef]
16. Sardin, D.; Reveyrand, T.; Popovic, Z. X-Band 10W MMIC High-Gain Power Amplifier with up to 60% PAE. In Proceedings of the 2014 9th European Microwave Integrated Circuit Conference, Rome, Italy, 6–7 October 2014; pp. 393–396. [CrossRef]
17. Ayad, M.; Poitrenaud, N.; Serru, V.; Camiade, M.; Gruenenpuett, J.; Riepe, K.J. A High Efficiency MMIC X-Band GaN Power Amplifier. In Proceedings of the 2020 50th European Microwave Conference (EuMC), Utrecht, The Netherlands, 12–14 January 2021; pp. 788–791. [CrossRef]
18. Kamioka, J.; Tarui, Y.; Kamo, Y.; Shinjo, S. 54% PAE, 70-W X -Band GaN MMIC Power Amplifier With Individual Source via Structure. *IEEE Microw. Wirel. Compon. Lett.* **2020**, *30*, 1149–1152. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.