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A CMOS-Compatible Process for ≥3 kV GaN Power HEMTs on 6-inch Sapphire Using In Situ SiN as the Gate Dielectric

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Abstract: The application of GaN HEMTs on silicon substrates in high-voltage environments is significantly limited due to their complex buffer layer structure and the difficulty in controlling wafer warpage. In this work, we successfully fabricated GaN power HEMTs on 6-inch sapphire substrates using a CMOS-compatible process. A 1.5 μm thin GaN buffer layer with excellent uniformity and a 20 nm in situ SiN gate dielectric ensured uniformly distributed V_{TH} and R_{ON} across the entire 6-inch wafer. The fabricated devices with an L_{GD} of 30 μm and W_G of 36 mm exhibited an R_{ON} of 18.06 Ω·mm and an off-state breakdown voltage of over 3 kV. The electrical mapping visualizes the high uniformity of R_{ON} and V_{TH} distributed across the whole 6-inch wafer, which is of great significance in promoting the applications of GaN power HEMTs for medium-voltage power electronics in the future.

Keywords: GaN power HEMTs; 6-inch sapphire; CMOS-compatible process; reliability

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1. Introduction

GaN HEMTs possess excellent material and device characteristics, such as high electron mobility, high critical electric field, and low switching losses. These features have led GaN to significant success in the field of power electronics, with widespread applications in power supplies, data centers, LiDAR systems, and consumer electronics [1–5]. So far, the three semiconductor materials Si, SiC, and GaN have achieved large-scale production and commercialization. Various silicon devices are used across different voltage ranges. SiC has also been commercialized in the medium-voltage range, and devices with voltages as high as 10 kV have been reported. However, owing to GaN's superior physical properties that enable higher switching frequencies, GaN is destined to revolutionize the field of power electronics [6–9].

Currently, most commercial GaN HEMTs are based on large-diameter, low-cost Si substrates [3,10]. However, the complex buffer layer structure [11,12] and difficulty in controlling warpage in GaN HEMTs on silicon substrates limit their applications in medium–voltage power electronics. In recent years, substrates such as sapphire, SiC [13,14], SOI [15], and QST [16] have emerged. Among these, sapphire has been actively explored recently due to its low cost and high mechanical strength [17].

Recently, Transphorm reported the development of 1.2 kV GaN switches on sapphire, achieving over 99% efficiency for a 900:450 V hard-switched buck converter [18,19]. Subsequently, e-mode p-GaN gate HEMTs on sapphire substrates with a high breakdown voltage (V_{BD}) of 1.4 kV were demonstrated [20]. Further, we have fabricated 1.7 kV d-mode GaN

HEMTs on a 1.5 µm ultra-thin buffer [21] and 8 kV GaN HEMTs using CMOS-compatible processing [22], and reported e-mode p-GaN gate HEMTs on 6-inch sapphire [23], and d-mode GaN HEMTs on 8-inch sapphire [24], which are promising for ≥650 V power applications. Li et al. reported the 1.2 kV GaN half bridges monolithically integrated on sapphire substrates [25]. Lu et al. reported that GaN HEMTs fabricated on sapphire possess an ultrahigh breakdown voltage (V_{BD}) exceeding 1.9 kV [26]. It should be noted that most research is based on small transistors that cannot be applied in real applications. Therefore, ≥3 kV GaN power HEMTs are strongly needed.

In this work, we present the epitaxy and fabrication of ≥3 kV GaN power HEMTs on 6-inch sapphire substrates using a CMOS-compatible process for the first time. Then, wafer-level uniformity is preliminarily assessed. Afterwards, the blocking capability is evaluated through off-state breakdown characterization, and the capacitance–voltage characteristics are probed. Finally, the threshold voltage instability of the devices is characterized.

2. Materials and Methods

The GaN power HEMT structure was grown on 6-inch sapphire substrates using metal–organic chemical vapor deposition (MOCVD), as shown in Figure 1, which comprises a 35 nm AlGaN nucleation layer, a 1.5 µm GaN buffer layer, a 260 nm GaN channel layer, a 1 nm AlN spacer, a 20 nm $Al_{0.25}GaN$ barrier layer, a 5 nm GaN cap layer, and a 20 nm in situ SiN, as depicted in Figure 2a. The in situ SiN forms the gate dielectric of the transistor and also serves as the passivation layer. Figure 2c shows an SEM and TEM of the 20 nm in situ SiN and the AlGaN–in situ SiN interface.

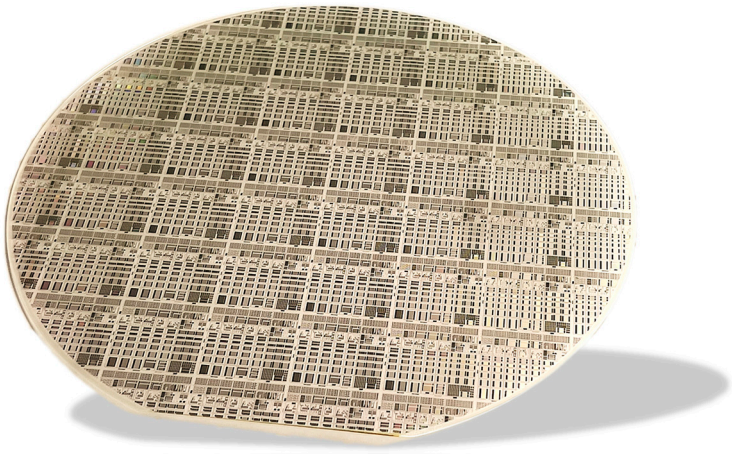

Figure 1. Photograph of the GaN power HEMTs on a 6-inch sapphire wafer manufactured by a CMOS-compatible process.

As shown in Figure 3, the device fabrication started with patterning lithography marks. Device isolation was then performed using N implantation. Next, a 150 nm SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD), and the gate window was opened via reactive ion etching (RIE). Gate metal was deposited via physical vapor deposition (PVD), followed by gate metal patterning using inductively coupled plasma (ICP) etching. The gate metal stack comprises Ti/Al/Ti (20/250/20 nm), under which is the 20 nm in situ SiN dielectric. The gate processing was finalized by the deposition of a second SiO_2 layer by PECVD. Next, Ohmic contact window opening was performed by RIE and ICP to remove the dielectric and AlGaN barrier, followed by Ti/Al (10/200 nm) Ohmic metal stack deposition and rapid thermal annealing at 565 °C for 90 s in the ambient of N_2. Finally, after the deposition of a third SiO_2 layer, Metal I of Ti/Al/Ti (20/250/20 nm) metal stack was deposited by PECVD and then patterned by ICP etching.

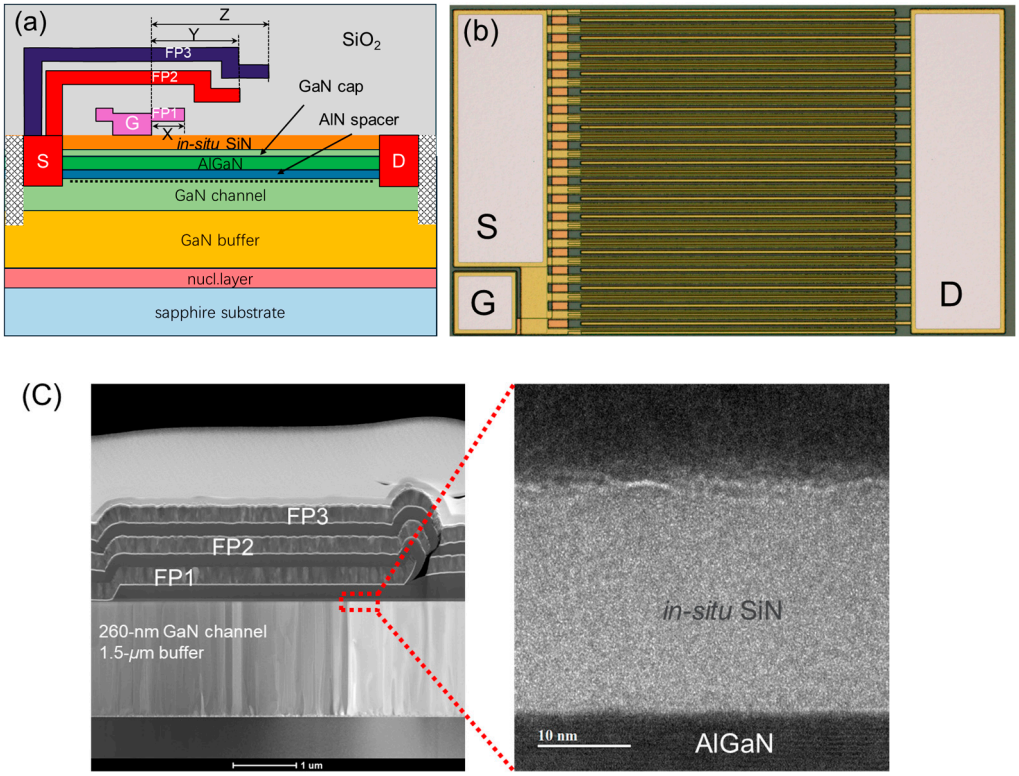

Figure 2. (**a**) Cross-sectional schematic of the fabricated GaN power HEMTs on 6-inch sapphire, (**b**) top view of the fabricated 36 mm GaN power HEMTs with in situ SiN as the gate dielectric, and (**c**) SEM and TEM images of the GaN power HEMTs on sapphire. The thickness of the field plate metal is approximately 300 nm.

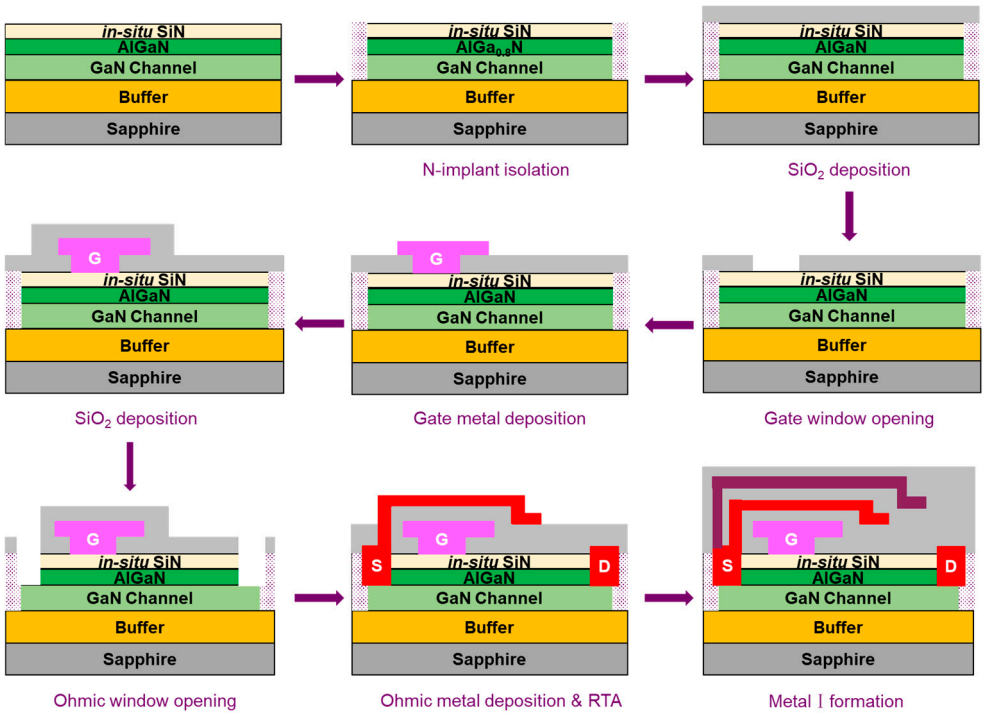

Figure 3. Processing flow of the GaN power HEMTs on 6-inch sapphire.

The fabricated power HEMTs have a gate width (W_G) of 36 mm, a gate length (L_G) of 4 μm, a gate–source distance (L_{GS}) of 1.5 μm, and various gate–drain distances (L_{GD})

ranging from 6 μm to 30 μm, as depicted in Figure 2b. The device includes three field plates, denoted as [X, Y, Z], which are formed by gate metal, Ohmic metal, and Metal I, as shown in Figure 2c. The electrical characterizations were performed using Keysight B1500A and B1505A (Keysight Technologies, one of the company's global core sites, is located in Santa Rosa, CA, USA).

3. Results

Figure 4a displays the typical transfer characteristics of the GaN power HEMTs with an L_{GD} of 6/16/22/30 μm, on which we can see the V_{TH} is concentrated around −9.5 V under the criterion of I_{DS} = 0.1 mA/mm, attributed to the uniformly deposited in situ SiN under the gate. It can also be observed that the curves exhibit almost no hysteresis. The SS value is 104 mV/decade, and the mobility is 1561 $cm^2/V{\cdot}s$.

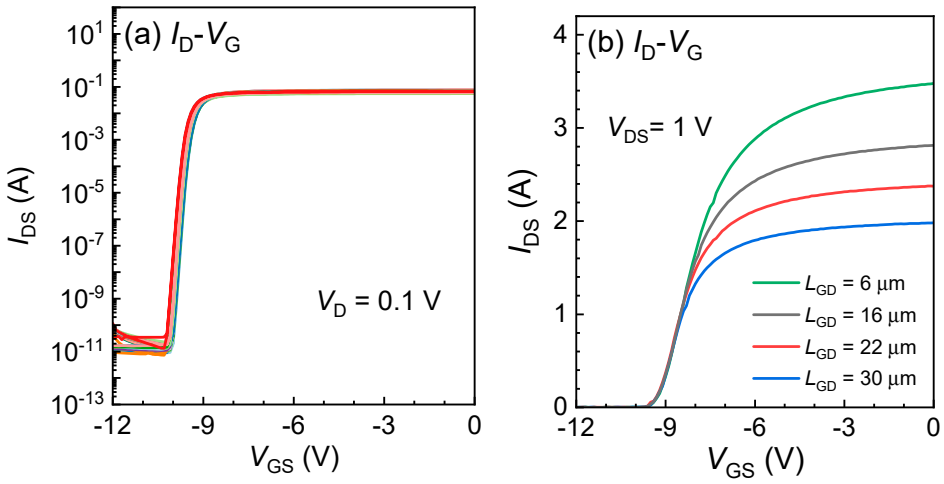

Figure 4. (**a**) The logarithmic and (**b**) linear transfer characteristics of the GaN power HEMTs with an L_{GD} of 6/16/22/30 μm on 6-inch sapphire.

Figure 5 displays the typical output characteristics of the fabricated GaN power HEMTs with various L_{GD} ranging from 6 to 30 μm. At V_{GS} = 0 V, the on-state saturation current is 15.4 A with an L_{GD} of 6 μm, as shown in Figure 5a. Figure 5b,c respectively show the on-state saturation current and R_{ON} for L_{GD} of 16 μm and 22 μm. The device exhibits an on-state saturation drain current of 355 mA/mm and an on-state resistance of 18.06 Ω·mm with an L_{GD} of 30 μm, as shown in Figure 5d.

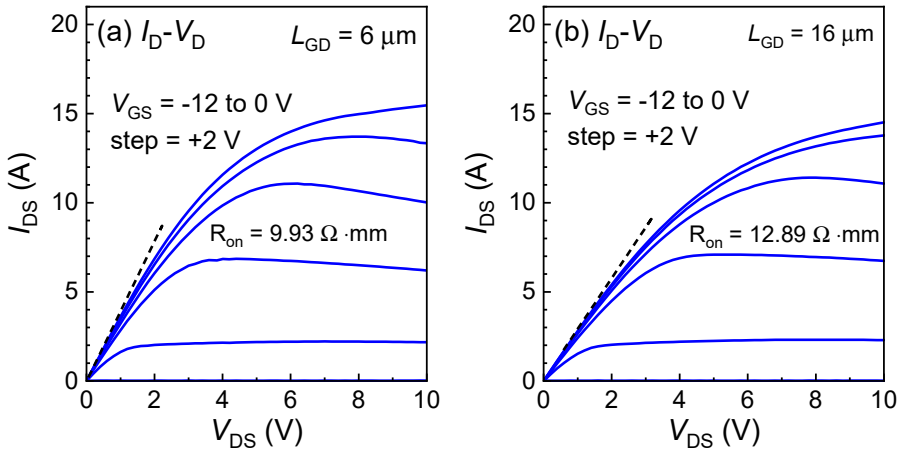

Figure 5. *Cont.*

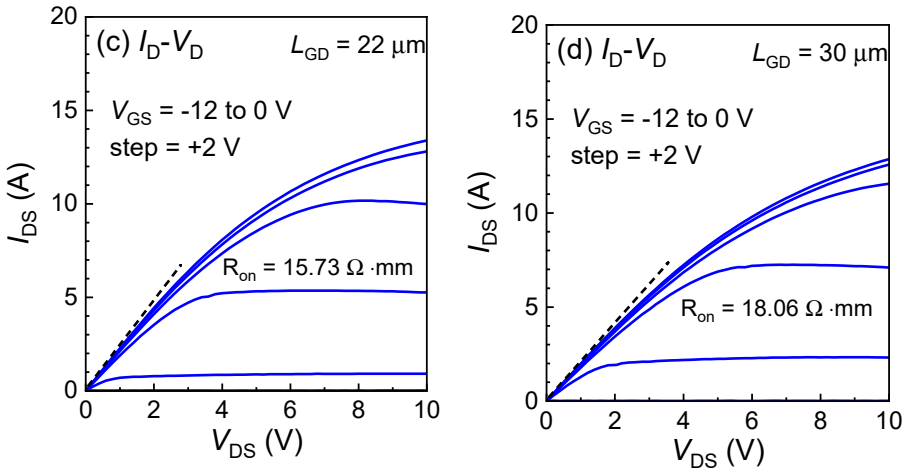

Figure 5. Output characteristics of the GaN power HEMTs with an L_{GD} of 6/16/22/30 μm on 6-inch sapphire.

The electrical mapping of V_{TH} and R_{ON} was summarized to verify the uniformity of the 6-inch wafer. As shown in Figure 6, the V_{TH} values are concentrated in the range of −10 to −9 V, and the R_{ON} values are concentrated in the range of 18 to 19 Ω·mm for the GaN power HEMTs with an L_{GD} of 30 μm. The relatively high uniformity can be attributed to the uniform in situ SiN and the precise etch-stop technique used during gate window opening.

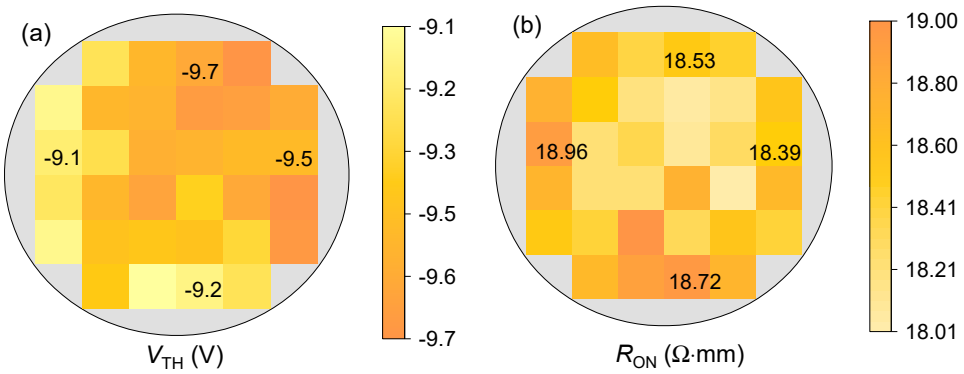

Figure 6. Electrical mapping of (**a**) V_{TH} and (**b**) R_{ON} of the fabricated GaN power HEMTs with an L_{GD} of 30 μm across the 6-inch sapphire wafer.

Next, the OFF-state breakdown characteristics of the fabricated GaN power HEMTs with various L_{GD} ranging from 16 to 30 μm were probed. As shown in Figure 7a, generally, GaN power HEMTs exhibit excellent blocking capability, with V_{BD} reaching 3 kV for an L_{GD} of 30 μm. The boxplots of OFF-state breakdown and R_{ON} are presented in Figure 7c,d, respectively. Devices with different L_{GD} values exhibit high breakdown voltages and excellent uniformity, which highlights the potential of the GaN power HEMTs on sapphire for future medium- to high-voltage applications. As shown in Figure 7b, the gate forward breakdown voltage (V_{GS}) reaches 16 V, owing to the high-quality and highly uniform in situ SiN. The successful fabrication of ≥3 kV GaN power HEMTs is of great significance for driving the revolution in power electronics.

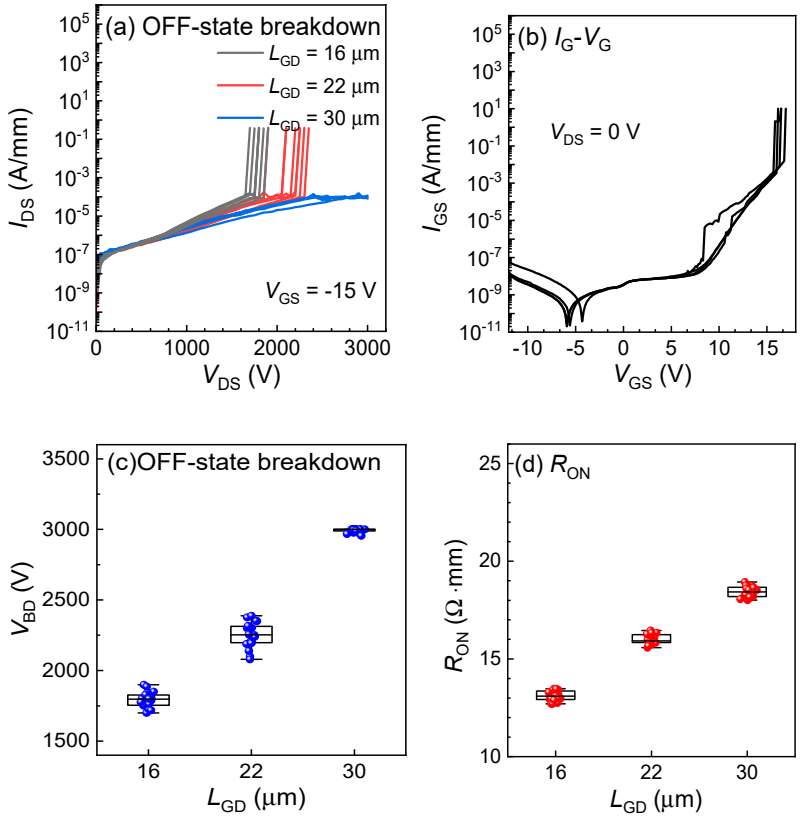

Figure 7. (**a**) OFF-state breakdown characteristics with various L_{GD} and (**b**) forward I_G-V_G measurement of the GaN power HEMTs on 6-inch sapphire. The statistical distribution of V_{BD} (**c**) and R_{ON} (**d**) versus L_{GD}.

The capacitance–voltage characteristics (C_{GD}) of GaN power HEMTs with different field plate structures in the OFF state were evaluated, as plotted in Figure 8. It can be seen from Figure 8a that the 0-FP HEMTs exhibit lower capacitance values, and the capacitance values remain consistent for different L_{GD}. As shown in Figure 8b, the capacitance values for different L_{GD} exhibit significant differences. Moreover, the capacitances are strongly modulated by the field plate structure. Three field plate structures, [2.25 3.75 6.75], [2.25 4.75 8.75], and [2.25 4.75 8.75], correspond to L_{GD} values of 16, 22, and 30 μm, respectively.

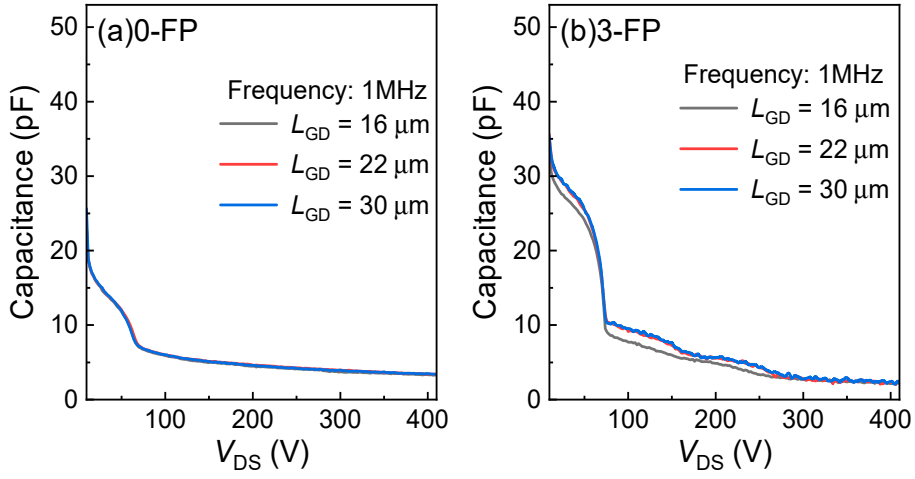

Figure 8. The C_{GD} characteristics of (**a**) the 0-FP GaN HEMTs and (**b**) the 3-FP GaN HEMTs with various structures. The measurement frequency is 1 MHz.

Bias Temperature Instability (BTI) is a crucial reliability issue, as it generates interface traps and oxide charges that degrade the performance of HEMTs, which could trigger malfunctions in the power system during operation.

In this work, BTI measurements were performed to examine the V_{TH} stability under gate stress using fast sweeping characterization with a Keysight B1530A WGFMU (Waveform Generator/Fast Measurement Unit). During the measurements, as shown in Figure 9a, the stress was periodically interrupted to measure the I_D-V_G curves by sweeping the V_{GS} from −10 to 0 V within 5 µs. For negative gate stress, V_{TH} decreases with stressing time and the magnitude of stress voltage, as shown in Figure 9b. Figure 9c summarizes the BTI performance of the GaN power HEMTs under various V_{GS}, and the V_{TH} shift was kept to as low as −0.36057 V corresponding to a V_{GS} of −10 V, thanks to the high-quality in situ SiN.

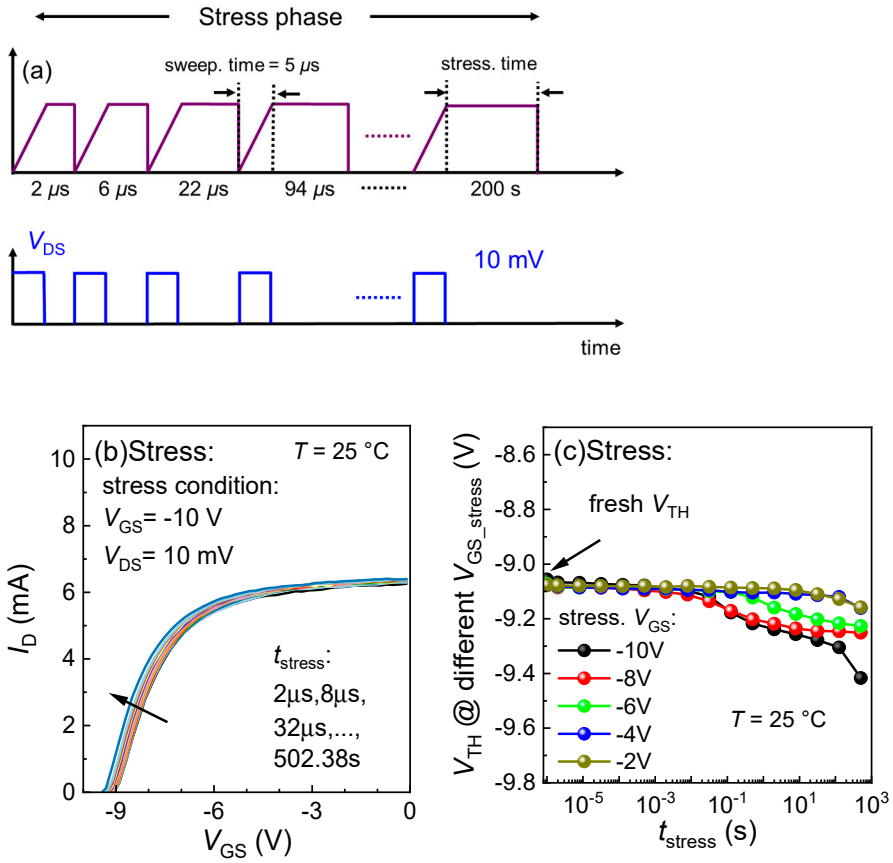

Figure 9. (**a**) Sketches of BTI measurement sequences using fast sweeping over 5 µs in this work, (**b**) I_D-V_G curves during the stressing phase by stressing V_{GS} of −10 V, and (**c**) V_{TH} evolution under different stress V_{GS} from −10 to −2 V during the stressing phase at 25 °C. The fast V_{GS} sweeps from −10 to 0 V in 5 µs. V_{TH} is extracted at I_{DS} = 0.1 mA/mm.

Figure 10 shows the schematic band diagram of the metal/in situ SiN/GaN/AlGaN/AlN/GaN gate stack under negative gate bias stress. The conduction band and the occupation of traps are shown in Figure 10a under thermal equilibrium, where all electrons below the Fermi level are filled. Open and filled circles indicate empty and filled traps, respectively. During BTI stress, part of the border traps in the SiN should be able to discharge, either by tunneling through the AlGaN barrier or via trap-assisted conduction, inducing a negative V_{TH} shift [27].

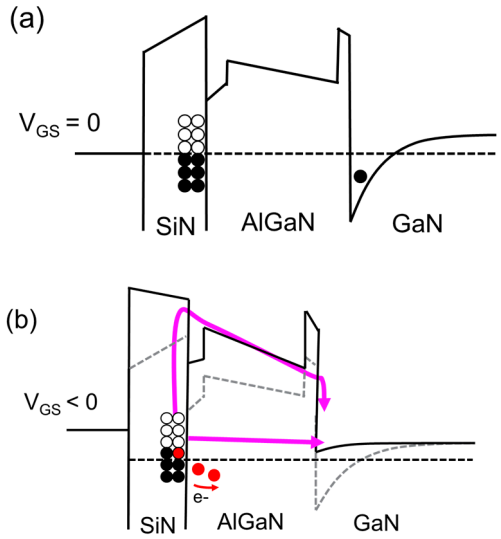

Figure 10. Schematic band diagram of the metal/in situ SiN//GaN/AlGaN/AlN/GaN gate stack under (**a**) V_{GS} = 0 V and (**b**) negative gate bias stress.

Table 1 shows a comparison of our GaN HEMTs on 6-inch sapphire substrates with other reported works. The devices in this work show excellent performance in terms of I_{ON}/I_{OFF}, SS, I_{DS}, $R_{ON,SP}$, R_{ON}, V_{BD}, and V_{BD}/L_{GD}. These results indicate their potential for high-power applications.

Table 1. Comparison of GaN HEMTs.

Ref.	I_{ON}/I_{OFF}	SS (mV/Decade)	I_{DS} (mA/mm)	I_{DS} (A)	$R_{ON,SP}$ (mΩ·cm^2)	R_{ON} (Ω·mm)	V_{BD} (V)	V_{BD}/L_{GD} (V/μm)
[20]	~10^8	-	~350	-	6.73	17.7	1412	52.29
[26]	-	-	-	-	-	-	1925	-
[28]	10^{10}	80	600	8	2.9	-	785	82.63
This work	10^{10}	104	355	15.4	-	18.06	>3000	>100

4. Conclusions

The GaN power HEMTs on 6-inch sapphire with an OFF-state breakdown voltage exceeding 3 kV have been successfully fabricated using a CMOS-compatible process in our pilot line. The 1.5 μm thin buffer and in situ SiN together guarantee high uniformity across the whole wafer. A preliminary evaluation of the device's gate threshold voltage instability was conducted. The fabricated power HEMTs exhibit a low R_{ON}, a low OFF state leakage current, and a high breakdown voltage, verifying the high quality and high uniformity of the 6-inch wafer. The remarkably simple epitaxy process and device structures, combined with the use of large-scale and low-cost sapphire substrates, can facilitate the application of GaN in the medium-voltage market in the future.

Author Contributions: Device design, X.L. and S.Y.; fabrication, J.J., X.L., L.C., L.W. and Z.L.; characterization, J.Z. and X.L.; writing—original draft preparation, J.Z., X.L., Y.H. and J.Z. (Jincheng Zhang). All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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Conflicts of Interest: Authors Long Chen, Lezhi Wang and Zilan Li were employed by the company Guangdong Ziener Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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