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A Novel 6500 V SiC Trench MOSFET with Integrated Unipolar Diode for Improved Third Quadrant and Switching Characteristics

Hao Wu [1], Xuan Li [1,*], Xiaochuan Deng [1], Yangyang Wu [1], Jiawei Ding [1], Wensong Peng [2] and Bo Zhang [1]

[1] State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China; jerrywhtc@163.com (H.W.); xcdeng@uestc.edu.cn (X.D.); wuyangyang_uestc@163.com (Y.W.); djfdjw@163.com (J.D.); zhangbo@uestc.edu.cn (B.Z.)

[2] Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen 518110, China; pengwensong_uestc@163.com

* Correspondence: xuanli@uestc.edu.cn

Abstract: A 6500 V SiC trench MOSFET with integrated unipolar diode (UD-MOS) is proposed to improve reverse conduction characteristics, suppress bipolar degradation, and reduce switching loss. An N type base region under the trench dummy gate provides a low barrier path to suppress hole injection during the reverse conduction operation. The reverse conduction voltage V_{ON} is reduced to 1.11 V, and the reverse recovery charge (Q_{RR}) is reduced to 1.22 μC/cm^2. The gate-to-drain capacitance (C_{GD}) and gate-to-source capacitance (C_{GS}) of the UD-MOS are also reduced to improve switching loss due to the thick oxide layer between the trench gate and dummy gate. The proposed device exhibits an excellent loss-related figure of merit (FOM). It provides a high-voltage SiC MOSFET prototype with potential performance advantages for voltage source converter-based high voltage direct current applications.

Keywords: SiC trench MOSFET; bipolar degradation; integrated unipolar diode; low switching loss

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1. Introduction

The voltage source converter-based high-voltage direct current (VSC-HVDC) transmission with high flexibility and controllability is a key approach to the construction of a high-proportion clean energy grid. The high-voltage (6500 V and above) SiC MOSFET is a promising candidate for VSC-HVDC transmission to increase power efficiency and reduce the volume of the system [1–3]. In the VSC, the freewheeling diode of SiC MOSFET operates during the dead time period. However, the utilization of the integrated PN body diode causes potential issues. Firstly, the reverse recovery charge Q_{RR} and reverse conduction voltage V_{ON} considerably increase loss. Secondly, the basic plane dislocations (BPDs) generate stacking faults (SFs) in the drift region by absorbing the energy from charge recombination [4], which degrades the V_{ON} and leakage current of SiC MOSFET [5]. For the 6500 V SiC MOSFET with a thicker drift region, many more SFs could be generated based on same initial BPDs density, spelling more serious bipolar degradation issues [6].

To prevent SiC MOSFET bipolar degradation issues, a common solution is utilizing the externally antiparallel Schottky barrier diode (SBD) for freewheeling operation [7], but this increases the parasitic parameters and size of the MOSFETs-based power module [8]. However, for the monolithic integrated diode schemes, SBD-integrated MOSFETs have been reported [9–11] and the source-controlled channel-diode-embedded SiC MOSFETs have been demonstrated [12,13], whereas Schottky contact and the uneven gate oxide layer-related reliability issues have yet to be introduced [14–17]. Gate-controlled channel-diode-embedded SiC MOSFETs have also been fabricated [18–20], which allow the forward and reverse conduction currents to share the same MOS-channel path. However, this brings

a huge challenge to achieving a better trade-off between low reverse conduction voltage and reasonable threshold voltage [18].

In this paper, a 6500 V SiC trench MOSFET with integrated unipolar diode (UD-MOS) is proposed to improve reverse conduction characteristics, suppress bipolar degradation issue, and reduce switching loss. Compared with the asymmetric trench MOSFET (C-MOS), the performance with its operation mechanism of UD-MOS is demonstrated by numerical simulations, involving doping-dependent mobility, high-field saturation mobility, Shockley–Read–Hall (SRH) recombination, Auger recombination, incomplete ionization of impurities, and impact ionization models.

2. Device Structure and Mechanism

The schematic cross-section view of the 6500 V SiC C-MOS and UD-MOS is shown in Figure 1. Compared with the C-MOS, the polysilicon gate of UD-MOS splits into two parts with a thick oxide layer. The left one is the true gate electrically connected to the gate electrode, while the right one is the dummy gate electrically connected to the source electrode. An N type region (i.e., N base region) beneath the dummy gate for electrons from the CSL region to N+ region, forms a unipolar diode (UD) as illustrated in Figure 1b.

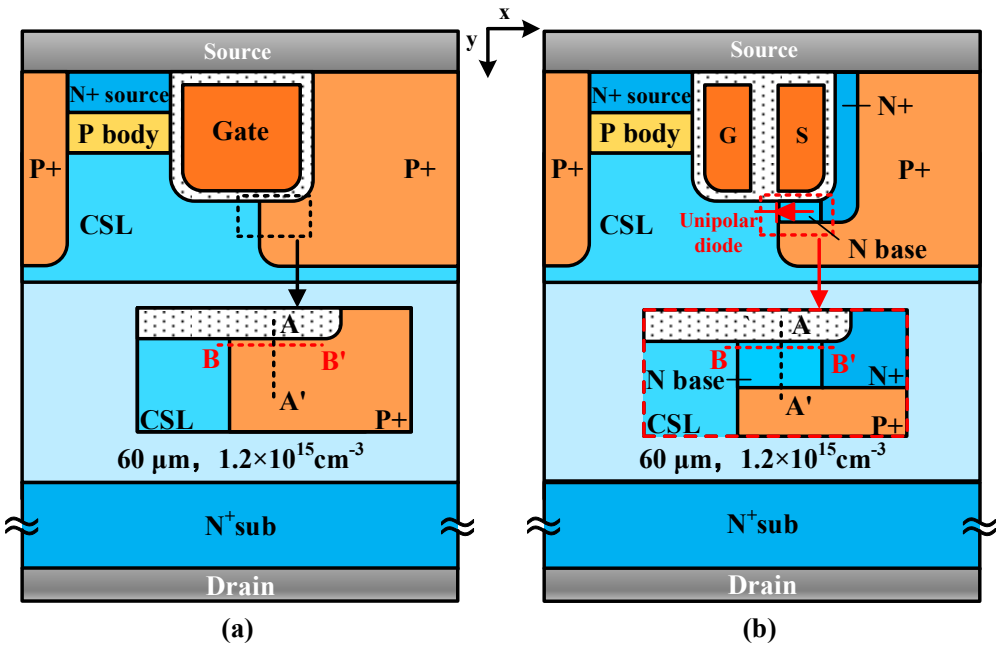

Figure 1. Schematic cross-section view of the 6500 V SiC (**a**) C-MOS and (**b**) UD-MOS.

For the zero-bias condition, the potential barrier distribution of the integrated unipolar diode of UD-MOS is shown in Figure 2. Compared with the body diode of C-MOS, the decrease of potential barrier from the P+ region to the SiC/SiO_2 interface (i.e., along line A′-A of Figure 1) makes a relatively low potential barrier (i.e., V_{UD}) for electrons transported from the CSL to N+ region. It should be noted that the V_{UD} is still relatively higher than the potential barrier of the CSL region and the N+ region as shown in Figure 2d. In other words, the electrons cannot flow through the N base region to the N+ region under this condition.

When in blocking condition, although the increasing V_{DS} lowers the barrier of the CSL region and N base region due to the drain-induced barrier lowering effect, the V_{UD} is still high enough to ensure blocking capability, as shown in Figure 3a. When in the reverse conduction condition, the potential barrier of the CSL region is raised by the negative V_{DS}. Once the potential barrier of the CSL region exceeds V_{UD}, the electrons from the CSL region can flow through the N base region to the N+ region, as shown in Figure 3b. Therefore, the potential height of the N base region determines both the blocking and reverse conduction

characteristics of UD-MOS. Furthermore, a barrier height analysis model is given here to inform the design of the V_{UD} as follows,

$$V_{UD} = V_P - \frac{\phi_{Si,SiC} + V_{GS} - \frac{qN_{CH}t_{CH}^2}{2\varepsilon_{SiC}}}{\frac{\varepsilon_{SiC}t_{ox}}{\varepsilon_{ox}t_{nch}} + 1} - \frac{qN_{CH}t_{CH}^2}{2\varepsilon_{SiC}} \quad (1)$$

where V_P is the potential barrier height of P+ region, $\phi_{Si,SiC}$ is the work function difference between N-type polysilicon and the P+ region, ε_{SiC} is the dielectric constant of SiC, ε_{ox} is the dielectric constant of oxide, q is the elementary charge, t_{CH} is the thickness of the N base region, and N_{CH} is the doping concentration of the N base region, respectively. According to (1), even though the negative V_{GS} can enhance blocking capability by increasing the V_{UD}, it also results in a high reverse conduction voltage V_{ON} of UD-MOS. Moreover, the positive V_{GS} even reduces the V_{UD} to make the unipolar diode turn on, causing the UD-MOS to lose gate control when in the forward conduction condition [17]. Therefore, the dummy gate not controlled by the gate electrode is introduced to guarantee both the forward and reverse conduction capability. Furthermore, the thickness t_{CH} and doping concentration N_{CH} of the N base region also affect the V_{UD}. With the increase of t_{CH} and N_{CH}, the V_{UD} decreases, as shown in Figure 4. The influence of breakdown voltage (BV) and V_{ON} on t_{CH} and N_{CH} is discussed further in the following section.

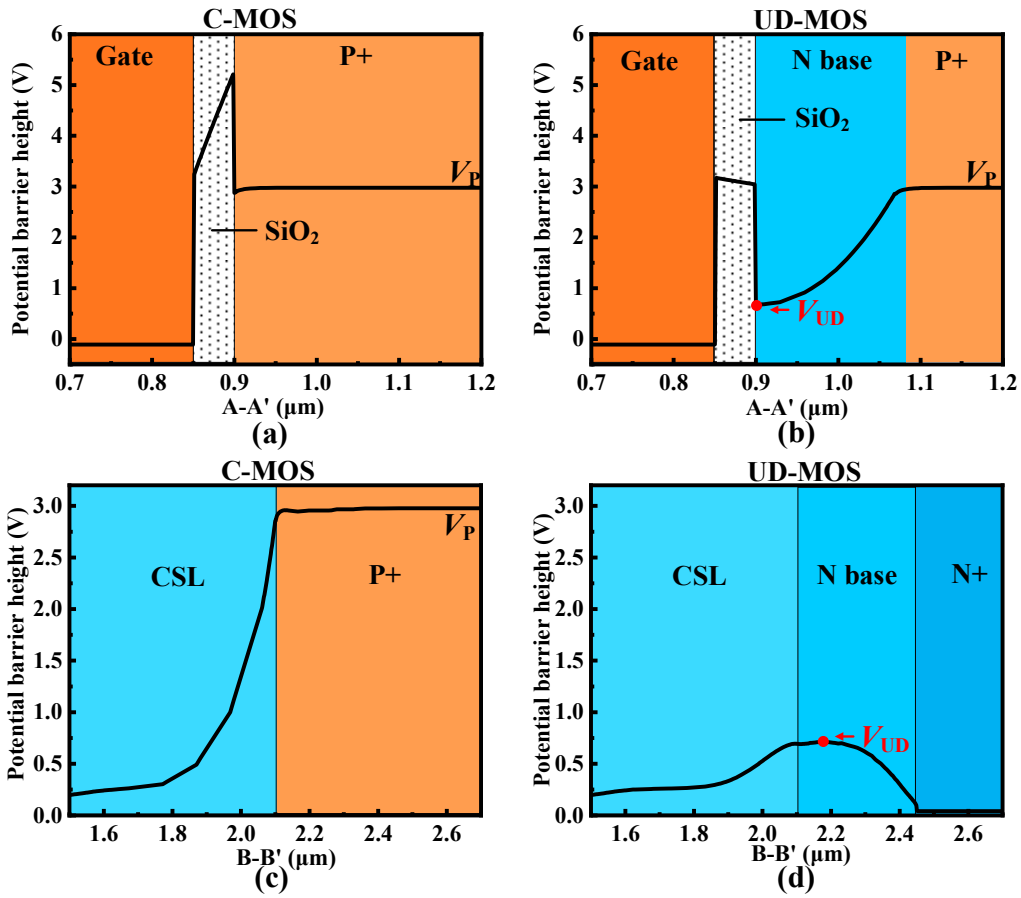

Figure 2. Potential barrier distribution at zero-bias (V_{GS} = 0 V and V_{DS} = 0 V) condition. (**a**) Along line A-A′ of the SiC C-MOS, (**b**) along line A-A′ of the SiC UD-MOS, (**c**) along line B-B′ of the SiC C-MOS, and (**d**) along line B-B′ of the SiC UD-MOS.

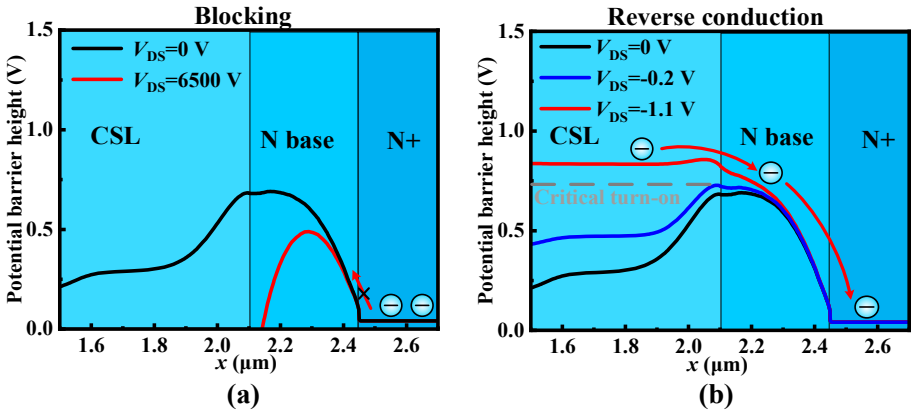

Figure 3. Potential barrier distribution along line B-B′ of the SiC UD-MOS. (**a**) The blocking condition and (**b**) the reverse conduction condition at V_{GS} = 0 V.

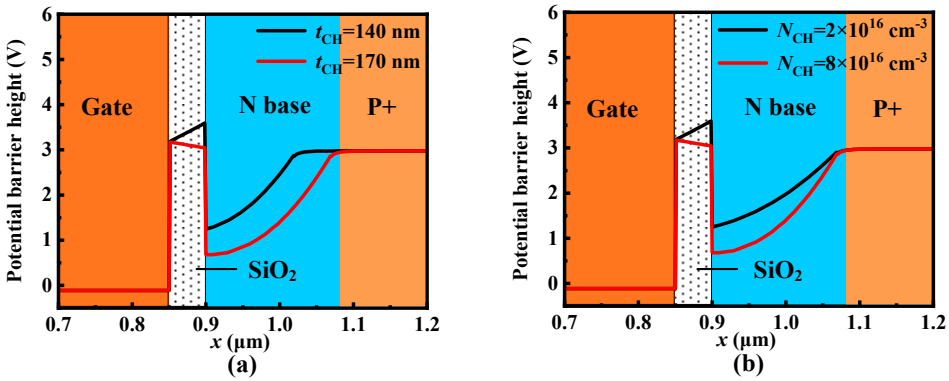

Figure 4. Effects of (**a**) N_{CH} and (**b**) t_{CH} on the potential barrier height along line A-A′ at zero-bias condition (V_{GS} = V_{DS} = 0 V).

3. Results and Discussion

With the increase of t_{CH} and N_{CH}, the V_{ON} (@V_{GS} = 0 V, I_{DS} = −3 A/cm^2) and BV (@I_{DS} = 1 × 10^{-8} A/cm^2) of UD-MOS decrease, as shown in Figure 5. It should be noted that the V_{ON} is mainly the voltage drop of the UD (i.e., V_{UD}) and the thick epi-layer. The thicker t_{CH} and higher N_{CH} bring lower V_{ON}, but also lead to premature breakdown. Therefore, considering both the V_{ON} and BV of the UD-MOS, the t_{CH} and N_{CH} are designed to be 170 nm and 8 × 10^{16} cm^{-3}, respectively. The key structural parameters of the C-MOS and UD-MOS are shown in Table 1.

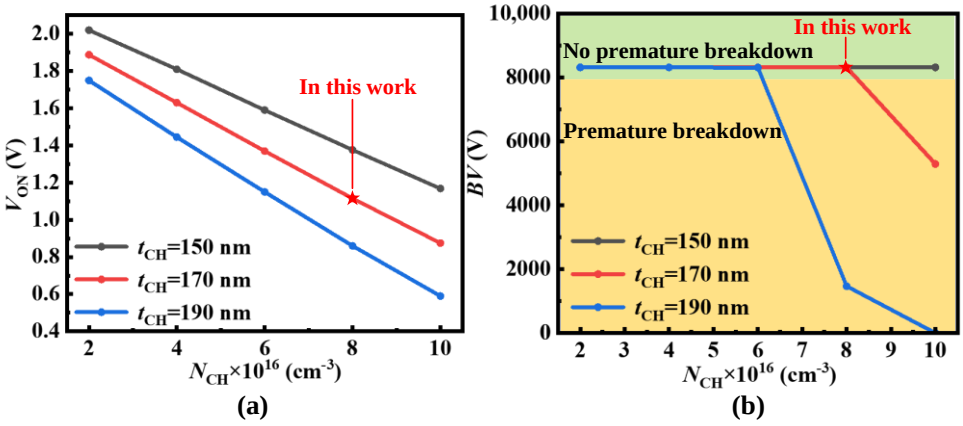

Figure 5. Effects of t_{CH} and N_{CH} on (**a**) V_{ON} and (**b**) BV of UD-MOS.

Table 1. Key Structure Parameters of the SiC C-MOS and UD-MOS.

Parameters	UD-MOS	C-MOS
cell pitch (μm)	3.35	3.15
drift region thickness (μm)	60	60
drift region doping (cm^{-3})	1.2×10^{15}	1.2×10^{15}
polysilicon width (μm)	0.8	0.8
trench depth (μm)	0.9	0.9
trench width (μm)	1.1	0.9
oxide thickness (nm)	50	50
CSL doping (cm^{-3})	3×10^{16}	3×10^{16}
JFET width (μm)	1.3	1.3
P+ region thickness (μm)	1.7	1.7
P+ region doping (cm^{-3})	1×10^{19}	1×10^{19}
N base length (μm)	0.35	–
N base thickness (nm)	170	–
N base doping (cm^{-3})	8×10^{16}	–

The effect of the N base length L_{CH} on V_{UD} is also discussed. With the narrowness of L_{CH}, the potential of the N+ region influences the potential barrier of the N base as shown in Figure 6a. Although the lower V_{UD} helps to reduce the V_{ON}, the BV is weakened at the same time, as shown in Figure 6b.

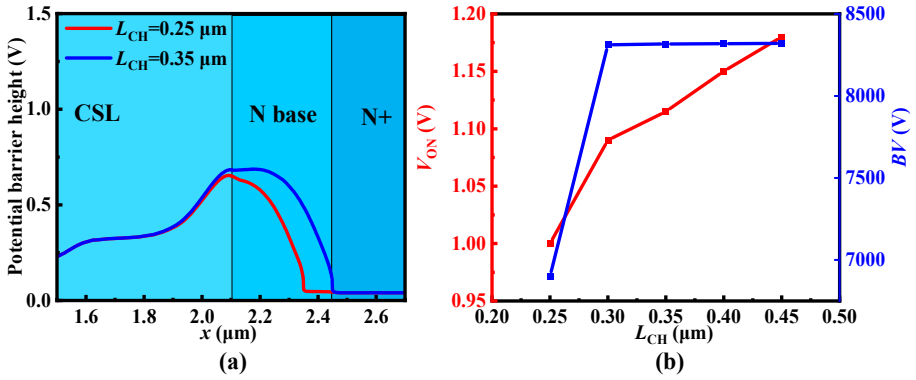

Figure 6. (**a**) Potential distribution in different L_{CH} and (**b**) effect of L_{CH} on V_{ON} and BV.

3.1. Static Characteristics

Based on optimized t_{CH} and N_{CH}, the SiC C-MOS and UD-MOS have a similar BV, as shown in Figure 7. The peak electric field in the gate oxide is less than 3 MV/cm, which ensures the long-term reliability of the gate oxide, as shown in the insets of Figure 7.

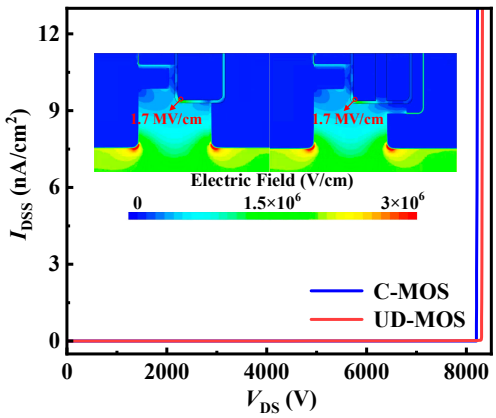

Figure 7. Blocking characteristics of the SiC C-MOS and UD-MOS. The insets show the electric field distributions in SiC MOSFET at V_{DS} = 6500 V.

Moreover, the V_{ON} of UD-MOS is −1.1 V, while the C-MOS is −2.8 V, as shown in Figure 8a. It should be noted that the integrated unipolar diode makes for lesser hole injection into the drift region when in the reverse conduction condition, as shown in Figure 8b, which effectively avoids the risk of bipolar degradation.

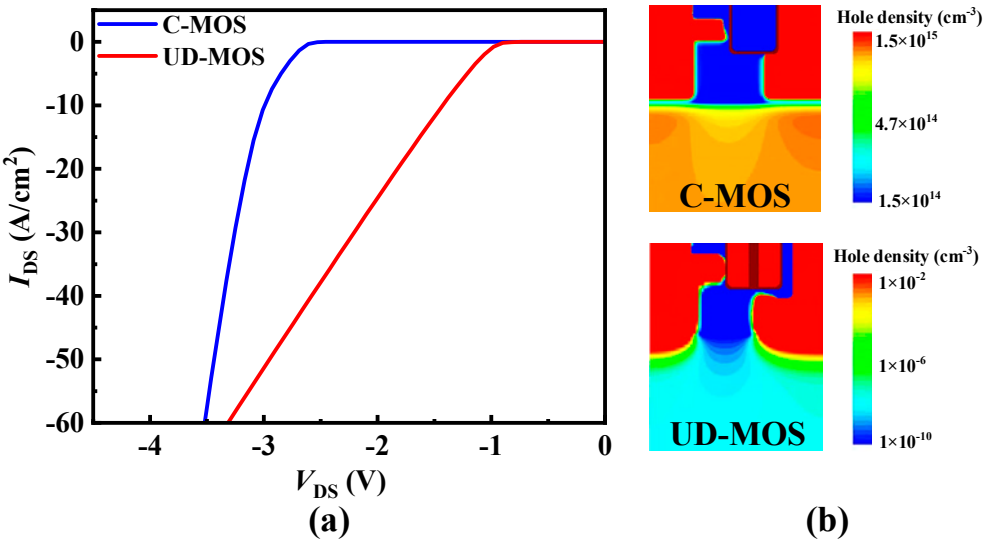

Figure 8. (**a**) Reverse conduction characteristics and (**b**) hole density distribution of the SiC C-MOS and UD-MOS at V_{GS} = 0 V and I_{SD} = 50 A/cm^2.

Even though the cell pitch of the UD-MOS is slightly larger than that of the C-MOS, the conduction capability of the UD-MOS is not degraded, because its channel density no longer dominates for high voltage SiC MOSFETs. The R_{ON} of UD-MOS and C-MOS are 35.48 mΩ·cm^2 and 35.00 mΩ·cm^2, respectively (@I_{DS} = 50 A/cm^2), as shown in Figure 9a. The transfer characteristic of the UD-MOS is also not degraded, which shows nearly the same V_{TH} as the C-MOS, as shown in Figure 9b.

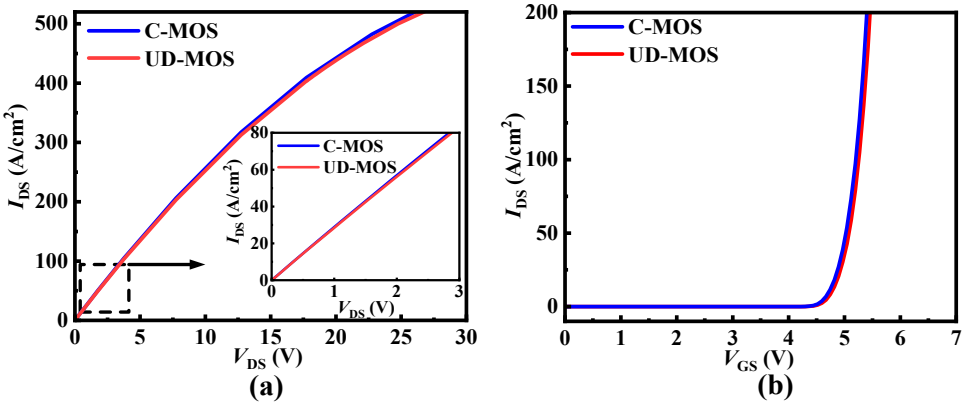

Figure 9. (**a**) Output characteristics at V_{GS} = 18 V and (**b**) transfer characteristics of the SiC C-MOS and UDMOS.

3.2. Dynamic Characteristics

The reverse recovery characteristics of the body diode in the SiC C-MOS and UD-MOS are compared, as shown in Figure 10. Thanks to no extraction of minority carrier during the reverse recovery process, the peak reverse recovery current (I_{RRM}) and reverse recovery charge (Q_{RR}) of UD-MOS are 54 A/cm^2 and 1.04 μC/cm^2, which are significantly reduced by 76% and 81%, respectively, compared to the C-MOS (I_{RRM} =176 A/cm^2 and Q_{RR} =5 μC/cm^2).

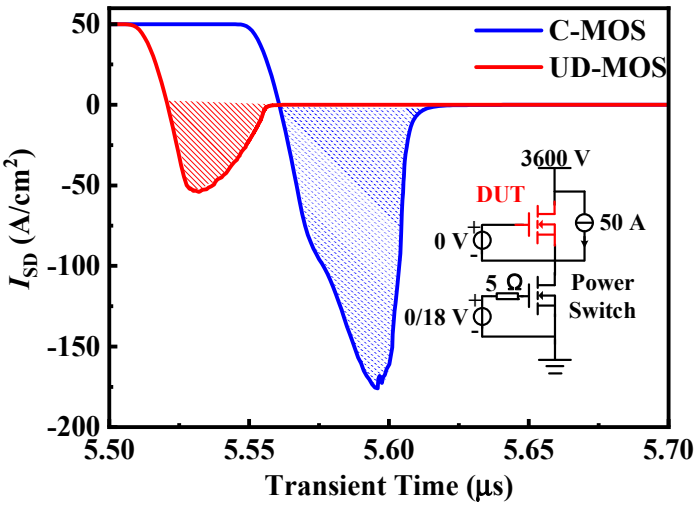

Figure 10. Reverse recovery characteristics of the body diode in the SiC C-MOS and UD-MOS.

Moreover, the dummy gate of the UD-MOS reduces the effective overlapping area between gate and drain terminals, so that the gate-to-drain capacitance (C_{GD}) is 4.01 pF/cm^2 (@V_{DS} = 3600 V), which is reduced by 9.5% compared with the C-MOS. Meanwhile, due to the thick oxide layer between the trench gate and dummy gate as well as a slightly smaller overlapping area, the gate-to-source capacitance (C_{GS}) of the UD-MOS is 18.1 nF/cm^2, which is reduced by 52%. Accordingly, thanks to the smaller C_{GD} and C_{GS}, the UD-MOS has a lower gate charge (Q_G) of 566 nC/cm^2 (@V_{GS} = 0 V–18 V) and gate-to-drain charge (Q_{GD}) of 109 nC/cm^2, as shown in Figure 11. Furthermore, considering conduction and dynamic capability, the UD-MOS exhibits a better loss-related figure of merit (FOM, i.e., $R_{ON} \times Q_{GD}$ [21]) of 3.87 mΩ·μC, which is 8.7% lower than that of the C-MOS.

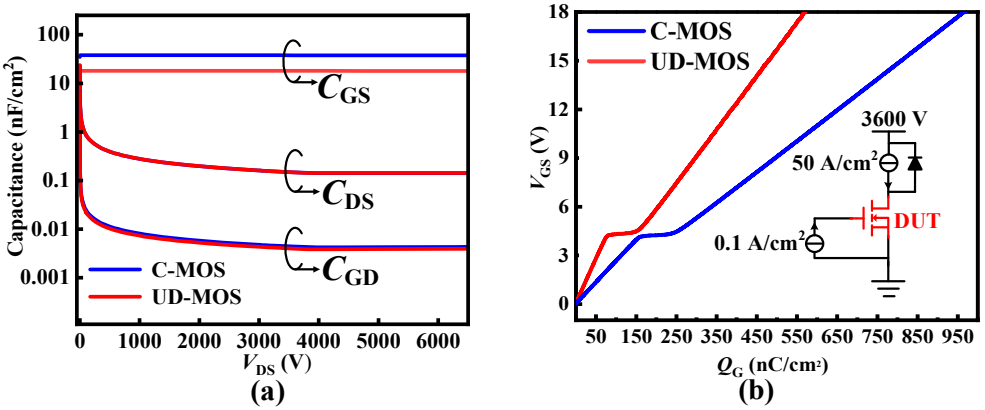

Figure 11. (**a**) Capacitance characteristics at V_{GS} = 0 V, f = 1 MHz and (**b**) Q_G for the SiC C-MOS and UD-MOS.

The switching waveforms of the SiC C-MOS and DP-MOS are as shown in Figure 12. Benefitting from the reduced capacitances, the UD-MOS has lower turn-on loss (E_{ON}) and turn-off loss (E_{OFF}) of 3.80 mJ/cm^2 and 3.36 mJ/cm^2, which are 34% and 17% lower than that of the C-MOS, respectively.

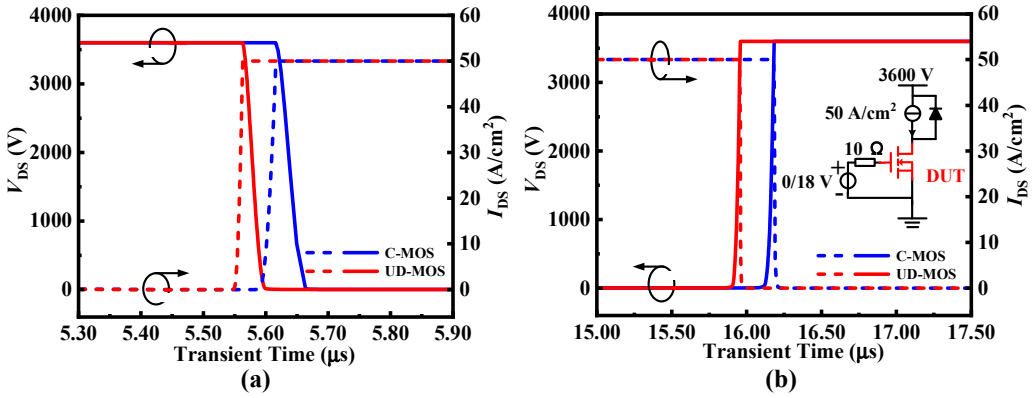

Figure 12. (**a**) Turn-on and (**b**) turn-off waveforms of the C-MOS and UD-MOS at V_{DS} = 3600 V and I_{DS} = 50 A/cm^2.

One feasible process flow of the UD-MOS is presented, including (a) epitaxial growing, P body implantation, N+ source region implantation, trench etch and P+ region implantation, (b) N+ region and N base region implantation, (c) thermal oxidation and polysilicon gate deposition, (d) polysilicon etch, (e) isolated oxidation deposition and (f) metallization, as shown in Figure 13. Finally, Table 2 compares the main characteristics of the SiC UD-MOS and the C-MOS. The SiC UD-MOS exhibits superior performance due to the unipolar diode.

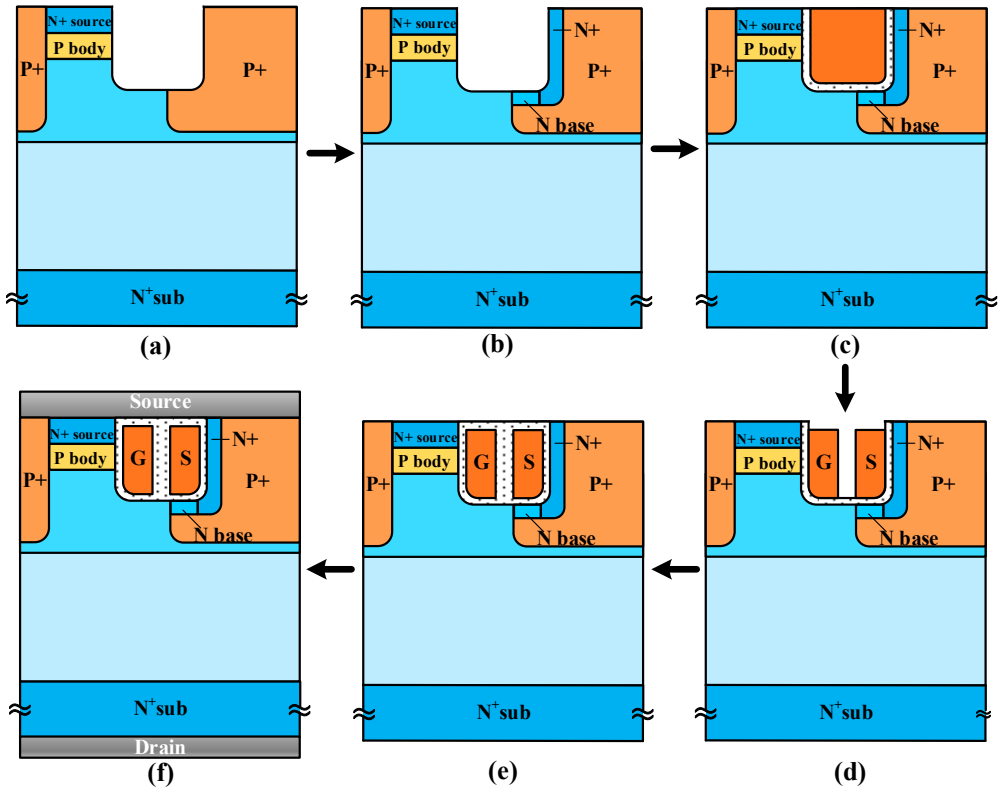

Figure 13. Brief fabrication process flow of the SiC UD-MOS. (**a**) Epitaxial growing, P body implantation, N+ source region implantation, trench etch and P+ region implantation, (**b**) N+ region and N base region implantation, (**c**) thermal oxidation and polysilicon gate deposition, (**d**) polysilicon etch by oxide sidewall spacer, (**e**) isolated oxidation deposition and (**f**) metallization.

Table 2. Performance Comparison of the SiC C-MOS and UD-MOS.

Parameters	UD-MOS	C-MOS
R_{ON} (mΩ·cm^2)	35.48	34.99
V_{ON} (V)	−1.11	−2.77
BV (V)	8317	8217
V_{TH} (V)	5.2	5.2
I_{RRM} (A/cm^2)	54	176
C_{GS} (nF/cm^2)	18.1	37.9
C_{DS} (pF/cm^2)	149	149
C_{GD} (pF/cm^2)	4.01	4.43
Q_{RR} (μC/cm^2)	1.22	5.01
Q_G (nC/cm^2)	566	970
Q_{GD} (nC/cm^2)	109	121
$R_{ON} \times Q_{GD}$ (mΩ·μC)	3.87	4.24
E_{ON} (mJ/cm^2)	3.8	5.71
E_{OFF} (mJ/cm^2)	3.36	4.38

4. Conclusions

A novel 6500 V SiC trench UD-MOS is proposed with improved reverse conduction and switching characteristics. The grounded dummy gate causes the unipolar diode of the SiC UD-MOS to reduce V_{ON} to 1.1 V, which avoids the risk of bipolar degradation and reduces the parasitic capacitances with lower switching loss. The proposed UD-MOS provides a promising device prototype in VSC applications for HVDC transmission.

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Conflicts of Interest: The authors declare no conflict of interest.

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