

Article

Improving Performance and Breakdown Voltage in Normally-Off GaN Recessed Gate MIS-HEMTs Using Atomic Layer Etching and Gate Field Plate for High-Power Device Applications

An-Chen Liu ¹, Po-Tsung Tu ^{1,2}, Hsin-Chu Chen ^{3,*} , Yung-Yu Lai ⁴ , Po-Chun Yeh ² and Hao-Chung Kuo ^{1,5,*} 

¹ Department of Photonics, Institute of Electro-Optical Engineering, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan; arsen.liou@gmail.com (A.-C.L.); itria30378@itri.org.tw (P.-T.T.)

² Electronic and Optoelectronic System Research Laboratories, Industrial Technology Research Institute, Zhudong 310401, Taiwan; a50164@itri.org.tw

³ Institute of Advanced Semiconductor Packaging and Testing, National Sun Yat-sen University, Kaohsiung 804201, Taiwan

⁴ Research Center for Applied Sciences, Academia Sinica, 128 Sec. 2, Academia Rd., Nankang, Taipei 115, Taiwan; loveriver031@gmail.com

⁵ Semiconductor Research Center, Hon Hai Research Institute, Taipei 114699, Taiwan

* Correspondence: chenhc@mail.nsysu.edu.tw (H.-C.C.); hckuo0206@nycu.edu.tw (H.-C.K.); Tel.: +886-7-525-2000 (ext. 6612) (H.-C.C.); +886-3-571-2121 (ext. 31986) (H.-C.K.)

Abstract: A typical method for normally-off operation, the metal–insulator–semiconductor–high electron mobility transistor (MIS-HEMT) has been investigated. Among various approaches, gate recessed MIS-HEMT have demonstrated a high gate voltage sweep and low leakage current characteristics. Despite their high performance, obtaining low-damage techniques in gate recess processing has so far proven too challenging. In this letter, we demonstrate a high current density and high breakdown down voltage of a MIS-HEMT with a recessed gate by the low damage gate recessed etching of atomic layer etching (ALE) technology. After the remaining 3.7 nm of the AlGaN recessed gate was formed, the surface roughness (Ra of 0.40 nm) was almost the same as the surface without ALE (no etching) as measured by atomic force microscopy (AFM). Furthermore, the devices demonstrate state-of-the-art characteristics with a competitive maximum drain current of 608 mA/mm at a V_G of 6 V and a threshold voltage of +2.0 V. The devices also show an on/off current ratio of 10^9 and an off-state hard breakdown voltage of 1190 V. The low damage of ALE technology was introduced into the MIS-HEMT with the recessed gate, which effectively reduced trapping states at the interface to obtain the low on-resistance (R_{on}) of 6.8 Ω ·mm and high breakdown voltage performance.

Keywords: atomic layer etching (ALE); MIS-HEMT; gate surface roughness



Citation: Liu, A.-C.; Tu, P.-T.; Chen, H.-C.; Lai, Y.-Y.; Yeh, P.-C.; Kuo, H.-C. Improving Performance and Breakdown Voltage in Normally-Off GaN Recessed Gate MIS-HEMTs Using Atomic Layer Etching and Gate Field Plate for High-Power Device Applications. *Micromachines* **2023**, *14*, 1582. <https://doi.org/10.3390/mi14081582>

Academic Editor: Niall Tait

Received: 17 June 2023

Revised: 1 August 2023

Accepted: 9 August 2023

Published: 11 August 2023



Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Owing to its excellent electrical properties, gallium nitride (GaN) power devices have received enormous attention for next-generation switching power devices [1]. Currently, the dominant structure of GaN devices that is commercially available is based on a lateral structure design, which is grown on large low-cost silicon (Si) wafers. GaN on Si can be fabricated using the existing fully mature 6 or 8 in silicon fabrication facilities, which further offers the advantages of the cost competitiveness of GaN on Si power technology. In addition, the rapid advance in device design, epitaxial growth, gate-driving techniques, processing, and packaging technology has made the possibility of the commercialization of GaN on Si power devices, which are commonly implemented in compact and efficient power converters [2].

The GaN devices are divided into two types according to the mode of operation, enhancement mode (E-mode), or normally-off, and depletion mode (D-mode), or normally-

on. For power applications, E-mode devices are preferred as this provides less power loss during switching, safer operation, and less-complex gate driver circuitry [3]. There are different varieties of approaches for designing E-mode GaN devices; among them, the most popular ones are by using the recessed gate GaN MIS-HEMT [4,5], the p-GaN HEMT [6–8], fluoride treatment [9], and the cascode configuration circuit [10,11]. In fluoride treatment, a negative charge is introduced under the gate electrode to adjust the threshold voltage (V_{TH}) of the device to make it a normally-off device. However, there is an issue regarding the stability of V_{TH} during high-temperature annealing [12]. In the p-GaN HEMT, a p-GaN cap is introduced below the Schottky gate, which lifts the conduction band and, thus, achieves a normally-off device. The device exhibits lower on-resistance and also has high mobility. However, the device suffers from the incapability of achieving high V_{TH} and also has various issues regarding gate reliability [13]. Among the above-mentioned methods, the implementation of the recessed gate GaN MIS-HEMT is more widely considered as it provides a larger gate swing, higher V_{TH} , and lower gate leakage. Methods available for performing gate recess are the dry etch process [14] and the chlorine-based dry etch process [15].

A procedure that is commonly used for performing the recessed gate structure is by using dry etching techniques, namely inductively coupled plasma-reactive ion etching (ICP-RIE) [16–20]. However, the UV photons present in the plasma discharged from the process cause serious damage to the surface of the semiconductor [21,22]. The damage on the surface causes an increase in leakage current, V_{TH} instability, and current collapse, hence degrading the performance of the device [23–26]. Furthermore, in the conventional method, the suppression of the remaining AlGaIn thickness variation is difficult to perform at the nanometric scale level, as the processing time controls the amount of etching [27]. An alternative etching process that provides high-quality interface engineering after etching is atomic layer etching (ALE). The ALE process is a type of dry etching technique that uses a series of self-limiting surface reactions to remove material layer by layer with high precision and control. In the case of GaN HEMT fabrication, the ALE process is used to create a recessed gate structure in the AlGaIn/GaN heterostructure and has low etching damage [28–34]. In this study, a high breakdown voltage of 1190 V of the normally-off AlGaIn/GaN MIS-HEMT with a recessed gate was successfully demonstrated. The ALE process was used instead of using ICP-RIE in order to reduce the roughness of the gate recess surface and further improve its trapping states at the interface.

The normally-off AlGaIn/GaN MIS-HEMT with a recessed gate was verified using the ALE process with the Cl_2/BCl_3 reaction gas to carefully control the gate recess process and minimize surface damage. Furthermore, atomic layer deposition (ALD) was used to create high-gate dielectric Al_2O_3 for reduced leakage current, lower interface trap density, and improved surface passivation. At an off-state current density of 1 mA/mm, an extremely low gate leakage of 10^{-7} mA/mm and a dramatically high breakdown voltage of 1190 V were achieved.

2. Devices' Fabrication

The fabricated normally-off AlGaIn/GaN MIS-HEMT with a recessed gate structure was grown on a 6 in commercial Si substrate by MOCVD, which consisted of the 1 nm GaN cap layer, a 25 nm $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer, a 1 nm AlN interlayer, a 300 nm undoped GaN channel layer, and a 4 μm AlGaIn buffer layer [35,36], as shown in Figure 1a. The normally-off MIS-HEMT with a recessed gate process started with mesa isolation, which was performed by the ICP-RIE to etch a specific region. Subsequently, the ohmic contact (S/D metal) based on Ti/Al/Ni/Au (25/125/45/75 nm) was formed by rapid thermal annealing (RTA) at 825 °C for 30 s in nitrogen (N_2) atmosphere to complete the source–drain ohmic connections. The ohmic contact resistance was 0.6 Ω mm. Then, a significant recessed gate structure was formed by the ALE technology. For a low-damage surface in the AlGaIn barrier by the ALE process, a recessed gate pattern was fabricated via Cl_2/BCl_3 hybrid etching.

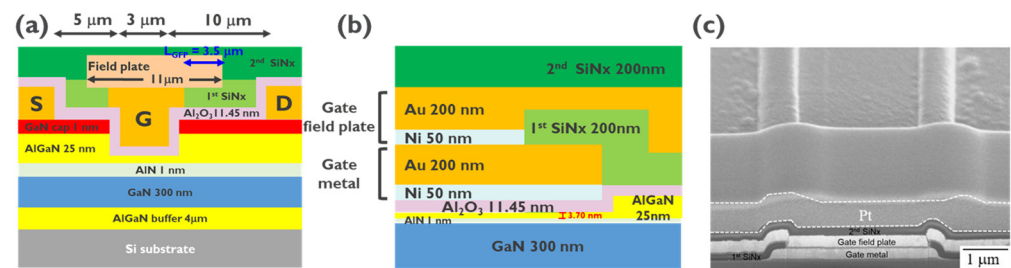


Figure 1. (a) Cross-section schematic view of the AlGaIn/GaN MIS-HEMT with a recessed gate. (b) MIS gate stack structure. (c) SEM image of the MIS-HEMT with a recessed gate.

In this case, the GaN cap and AlGaIn barrier were recessed by multiple cycles of oxidation and etching using inductively linked plasma, with each cycle consisting of generating a thin oxide layer on top and etching away using BCl₃ etching [37]. ALE employing two quasi-self-limiting steps (O₂ plasma modification and BCl₃ plasma removal) was used to fabricate the AlGaIn/GaN HEMT. This technique allows for the precise control of recessing and the suppression of leakage current, making it a promising alternative to the continuous dry etching method [38–40].

A wet cleaning process of HCl:DI = 1:10, BOE:DI = 1:10, and remote O₂ plasma pretreatment was applied to remove the metal impurities, carbides, and native oxide, followed by the ALD of the 11.45 nm Al₂O₃ high-dielectric layer synthesized using trimethylaluminum and H₂O as precursors at 350 °C. A gate metal with Ni/Au (50 nm/200 nm) was deposited by an E-Gun evaporator on the Al₂O₃ high-dielectric layer, followed by the first layer passivation of SiNx with 200 nm deposited by plasma enhanced chemical vapor deposition (PECVD). To suppress the high-electric-field effect between the gate-to-source/drain, a gate field plate with a width of 11 μm with field plate distance extending from the edge of the gate to the drain (L_{GFP}) of 3.5 μm was fabricated by lithograph patterning and a Ni/Au (50 nm/200 nm) metal stack deposited by the E-Gun. Then, the second layer passivation of SiNx with a 200 nm thickness was fabricated. For the final pad-contacting hole opening in the gate, source, and drain region defined by the lithograph process, the last pad metal stack of Ni/Au (50 nm/200 nm) was deposited by the E-Gun. The specific characteristic values (feature length) of the MIS-HEMT with the recessed gate were the gate length (L_G) of 3 μm, the gate width (W_G) of 100 μm, the gate-to-source length (L_{GS}) of 5 μm, the gate-to-drain length (L_{GD}) of 10 μm, as shown in Figure 1a,b. Figure 1c presents the SEM image of the single finger in the recessed gate region, clearly showing the gate metal, gate field plate, and SiNx passivation.

The gate metal Ni/Au (50 nm/200 nm) structure deposited by the E-Gun is a crucial component of the AlGaIn/GaN HEMT, and its design can significantly impact the device's performance. Typically, the gate metal structure consists of a thin layer of refractory metal, such as gold, deposited on the semiconductor surface to create the gate electrode. It affects critical parameters such as gate-to-channel capacitance, gate resistance, and gate-to-drain/source capacitance, which can significantly impact the device's performance. In this study, we found that using Ni/Au as the gate metal structure can lead to a low gate resistance and a low gate-to-channel capacitance, ultimately improving the device's transconductance.

The gate field plate structure is a crucial element in the AlGaIn/GaN HEMT. Typically, it consists of a thin layer of metal or doped semiconductor that connects to the gate contact and extends beyond the source and drain edge. This structure effectively increases the gate-to-source/drain distance and reduces the electric field at the gate edge, leading to an improvement in the device's breakdown voltage and a reduction in the gate leakage current. The gate field plate design significantly impacts the device's performance, affecting its breakdown voltage, gate leakage current, and parasitic capacitance. In this paper, Ni/Au was utilized as the gate field plate material, and a large-area structure with a width of 11 μm was designed to effectively reduce the gate leakage current and improve the device

reliability. However, this may increase parasitic capacitance, thereby degrading the high-frequency performance of the device. The selection of the gate metal and gate field plate structures should be carefully considered based on the specific application requirements to optimize the device's performance and reliability. Using Ni/Au as the gate metal in HEMT provides good electron transport performance, contributing to the high-frequency characteristics and fast switching speed of the device. The Ni/Au layer has good adhesion with HEMT materials, typically being semiconductor materials. This ensures a strong contact between the metal gate and the semiconductor, thereby improving the device's performance and reliability. Au is highly resistant to oxidation, meaning the metal gate is less prone to oxidation during long-term usage. This contributes to the device's longevity and stability. The common choices of the metal for the gate field plate are Ni/Au [41] or Ti/Au [42], both of which have excellent conductivity and adhesion.

Compared to other metals, the main differences of Ni/Au lie in their conductivity and adhesion properties. While other metals may have good conductivity, they may not adhere as well to semiconductors. Poor adhesion could lead to unstable performance or failure of the device. Additionally, some metals may be more susceptible to oxidation, reducing the device's reliability. Therefore, considering factors such as conductivity, adhesion, and oxidation resistance, Ni/Au is widely used in HEMT devices to ensure high performance and reliability. The gate field plate width designed at 11 μm effectively disperses the electric field, improving the breakdown voltage. As indicated in the reference, the lower the proportion of the L_{GFP} length to the L_{GD} length, the higher the maximum transconductance (G_m) value and the gain will be, which is mainly due to the reduction in the access resistance caused by the increase in available carriers in the channel. According to A. Mohanbabu et al. [43], when the $L_{\text{GFP}}/L_{\text{GD}}$ ratio is around 30%, it can achieve better G_m and breakdown voltage [43–45].

The V_{TH} for the AlGaIn/GaN MIS-HEMT with a recessed gate is expressed as Equation (1) [46,47].

$$V_{\text{TH}} = \frac{1}{e}(\varphi_B(x) + E_F(x) - \Delta E_{\text{C1}}(x) - \Delta E_{\text{C2}}(x)) - \sigma(x) \left(\frac{t_{\text{die}}}{\epsilon_0 \epsilon_{\text{Al}_2\text{O}_3}} + \frac{t_{\text{RB}}}{\epsilon_0 \epsilon_{\text{AlGaIn}}} \right) \quad (1)$$

In the equation, $\frac{t_{\text{RB}}}{\epsilon_0 \epsilon_{\text{AlGaIn}}}$ represents the layer thickness (t_{RB}) and dielectric constant (ϵ) of the AlGaIn layer, respectively. $\left(\frac{t_{\text{die}}}{\epsilon_0 \epsilon_{\text{Al}_2\text{O}_3}} \right)$ represents the layer thickness (t_{die}) and dielectric constant (ϵ) of the Al_2O_3 layer, respectively. $\sigma(x)$ is the polarization sheet charge amount. $E_F(x)$ is the difference between the Fermi level and the GaN conduction band edge level. $\Delta E_{\text{C1}}(x)$ and $\Delta E_{\text{C2}}(x)$ denote the conduction band discontinuity between Al_2O_3 and AlGaIn and between AlGaIn and GaN, respectively. $\varphi_B(x)$ is the Schottky barrier height.

The movement of V_{TH} in the positive direction is strongly correlated with the AlGaIn barrier thickness, as a decrease in thickness leads to a reduction in both the 2DEG concentration and electron mobility, ultimately resulting in a positive shift in V_{TH} . However, a high V_{TH} can negatively affect the drain current (I_{D}) due to the reduced 2DEG concentration. Therefore, the precise control of the AlGaIn layer etch depth is critical to optimize both V_{TH} and I_{D} current. To avoid potential dielectric (Al_2O_3) side effects, we investigated three different depths of 5 nm and 3 nm and over-etching of the AlGaIn gate recess in Schottky HEMT devices, and the reference device was without the gate recessed etching. By examining the correlation between the threshold voltage shift and AlGaIn depths, we found that AlGaIn with a 3 nm remaining thickness of the AlGaIn layer showed the realization of normally-off characteristics in the HEMT devices. Although the over-etching of the AlGaIn gate recess also had normally-off characteristics, the lowest drain current was 6 mA/mm. AlGaIn with 3 nm remaining showed a threshold voltage of +0.5 V and a drain current of 440 mA/mm at a gate voltage of 4 V, and the reference device without gate recessed etching showed a threshold voltage of −4.5 V and a drain current of 650 mA/mm. The 3 nm remaining thickness of the AlGaIn was inspired by a prior study, which yielded promising outcomes with this particular approach in the recessed gate MIS-HEMTs. The maximum

drain current density of a typical D-mode HEMT can reach 900 mA/mm. With the decrease in the AlGaIn thickness, the 2DEG concentration and electron mobility will also decrease. Theoretically, the critical value for generating a 2DEG is about 3 nm [48]. When AlGaIn is 0 nm, the current reaches its lowest, indicating very limited electrons in the channel. When there is little 2DEG in the channel under the gate, the scattering of electrons increases, and the electron mobility is very low. The V_{TH} in this paper is defined as the gate bias when the drain current reaches 1 mA/mm. The V_{TH} of a typical D-mode HEMT is about -4 V. When the thickness of AlGaIn decreases, the V_{TH} of the MIS-HEMT also rises. This indicates that V_{TH} can be determined by controlling the etching depth. Secondly, when the dielectric layer of Al_2O_3 is added, the capacitance between the dielectric layer and AlGaIn increases, further reducing the 2DEG concentration and electron mobility. Therefore, we can achieve the best device characteristics by adjusting the gate etching depth and the thickness of the dielectric layer [46].

The depth of the gate recess affects the carrier transport characteristics of the device. Typically, a deeper gate recess can increase the width of the carrier channel, reducing resistance, enhancing carrier mobility, and improving the current-carrying capacity, and the depth of the gate recess affects the V_{TH} of the device. Generally, a deeper gate recess leads to a higher threshold voltage, making the device more conducive to switching operations. Therefore, the depth of the gate recess requires a trade-off [46]. The ALE process is a promising technology for achieving nanoscale depth control and low surface damage in the fabrication of recessed gate MIS-HEMT devices, providing an excellent platform for further improving device performance.

Here, we discuss the characterization of a recessed gate structure in AlGaIn layers using different etching techniques. We also highlight the advantages of ALE over traditional plasma etching methods in terms of surface roughness and damage. Transmission electron microscopy (TEM) analysis was conducted on the recessed gate structure region, as shown in Figure 2a. The TEM profile revealed the thicknesses of the Al_2O_3 and AlGaIn layers to be 11.45 nm and 3.70 nm, respectively. This analysis provides important information about the dimensions of the layers in the structure. Conventionally, GaN-based materials are etched using the inductively coupled plasma-reactive ion etching (ICP-RIE) system, which is commonly employed for plasma etching processes such as gate recesses and ohmic recesses. However, one drawback of this technique is the potential lattice damage caused by the generation of free radicals, ions, and ultraviolet light during plasma discharge, as mentioned in [41].

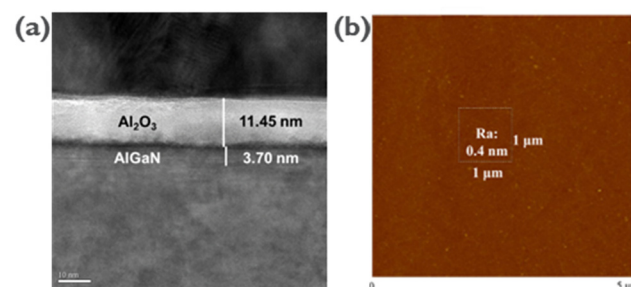


Figure 2. (a) The recessed gate structure from the TEM image and (b) the surface morphology of the recessed gate region; Ra of 0.4 nm by AFM inspection.

On the other hand, alternative etching processes such as ALE have been found to exhibit relatively low surface roughness compared to digital etching and continuous etching processes using Cl_2/BCl_3 . This means that ALE can potentially minimize the surface damage during the etching process. To demonstrate the low surface damage achieved through the ALE process on the AlGaIn layer, the surface roughness in the recessed gate region was measured using AFM. In Figure 2b, the arithmetic average roughness (Ra) is reported as 0.40 nm. This value indicates that the recess etching using ALE resulted in remarkably low surface damage, which was very similar to the surface without any

etching. This finding suggests that ALE can be a promising technique for achieving precise etching while minimizing surface roughness and damage in AlGaN layers. Overall, here, an overview of the TEM analysis of a recessed gate structure is given, comparing traditional plasma etching techniques with ALE in terms of lattice damage and surface roughness and providing evidence for the low surface damage achieved through the ALE process using AFM measurements.

3. Results and Discussion

In order to know the transfer and gate leakage characteristics of the normally-off AlGaN/GaN MIS-HEMT with the recessed gate, the device design with $L_G/L_{GS}/L_{GD}/W_G = 3/5/10/100 \mu\text{m}$ of the drain current–gate bias (I_D – V_G) measurement was performed. The fabricated device was a single-finger device, as shown in Figure 1c, with transfer characteristics in a linear scale, as shown in Figure 3a. According to the gate bias of the maximum transconductance curve, V_{TH} was determined to be +2.0 V by linear extrapolation or +0.7 V at a drain current extracted at $1 \mu\text{A}/\text{mm}$. The maximum drain current ($I_{D,max}$) of $608 \text{ mA}/\text{mm}$ at V_G of 6 V and G_m of $170 \text{ mS}/\text{mm}$ at V_G of 2 V were demonstrated, respectively. Figure 3b shows the semi-log scale of the I_D – V_G curve; the drain bias (V_D) was operated at 10 V, and the gate voltage (V_G) was swept from -2 V to 8 V . A subthreshold swing (SS) was found in $116 \text{ mV}/\text{dec}$. Even with a significant forward bias of 10 V, the I_D -to- I_G ratio was more than 10^9 , indicating that the high dielectric leakage current was negligible. This was due to the low-surface-damage etching on the AlGaN layer by the ALE process. A V_{TH} hysteresis of 0.6 V was found. The V_{TH} hysteresis phenomenon was produced by electrons caught in the AlGaN/ Al_2O_3 dielectric interface states or traps that remained in the Al_2O_3 dielectric bulk layer. Compared to other devices, the hysteresis of this device was relatively low [49,50].

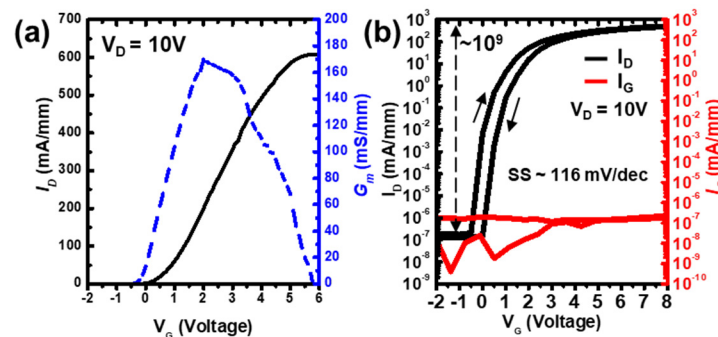


Figure 3. Transfer characteristic of normally-off AlGaN/GaN MIS-HEMT with the recessed gate: (a) I_D – V_G characteristic (black solid line) and G_m characteristic (blue dotted line) in a linear scale; (b) I_G – V_G sweeps characteristic (red solid line) and I_D – V_G sweeps characteristic (black solid line) in a semi-log scale.

Figure 4a shows the DC I_D – V_D output characteristics of a normally-off AlGaN/GaN MIS-HEMT with the recessed gate device with the feature design with $L_G/L_{GS}/L_{GD}/W_G$ of $3/5/10/100 \mu\text{m}$. V_G was applied from -1 V to 4 V , and the maximum output drain current density was $556 \text{ mA}/\text{mm}$ at a V_D of 10 V. Furthermore, the R_{on} of the recessed gate device was $6.8 \Omega \cdot \text{mm}$ (corresponding specifically to on-resistance, $R_{ON,SP}$ was $1.27 \text{ m}\Omega \cdot \text{mm}^2$). The three-terminal off-state breakdown voltage (BV) characteristics of the normally-off MIS-HEMT with the recessed gate device is shown in Figure 4b. The recessed gate device feature design with $L_G/L_{GS}/L_{GD}/W_G$ of $3/5/10/100 \mu\text{m}$ and V_G of -10 V was used as the BV measured condition. The BV was defined as the point at which the gate and drain leakage current reached $1 \mu\text{A}/\text{mm}$ and $1 \text{ mA}/\text{mm}$. The device's hard breakdown was dominated by the gate-to-drain leakage current (V_D) = 720 V at $1 \mu\text{A}/\text{mm}$. One Al_2O_3 gate dielectric design layer and the low-surface-damage recessed gate by the ALE process improved the gate leakage current. Compared to the study of Hsieh et al., using the $\text{Al}_2\text{O}_3/\text{AlN}$ stack

insulator reduced the interface trapping density between the $\text{Al}_2\text{O}_3/\text{GaN}$ interface for the gate recessed GaN MIS-HEMT made by low-power-plasma etching, for which the hard breakdown occurred at a gate-to-drain voltage (V_D) = 620 V at 2 $\mu\text{A}/\text{mm}$ [20]. The high gate-to-drain leakage current mechanism is due either to surface conduction or to the tunneling of electrons through the AlGaN barrier [51]. According to the gate-to-drain breakdown voltage results, there was a three-step breakdown behavior. The slight decrease of the I_G current before a V_D of 200 V in the initial stages indicated trapping, and the beginning of the increase of the I_G current from 200 V to 1100 V after that can be attributed to the stress-induced leakage current (SILC) [52]. When applied to the device, electrical stress can cause structural changes in surface conduction or the oxide layer, creating traps that can capture and release charge carriers. As a result, these traps can influence the current flow through the device, leading to leakage currents. Dielectric hard breakdown, the catastrophic breakdown, was observed to take place after 1100 V and was characterized by a very sharp vertical jump in the gate current of each device [53]. Therefore, a BV was exhibited of 720 V at 1 $\mu\text{A}/\text{mm}$ and another BV was exhibited of 1190 V at 1 mA/mm. Owing to the low-damage surface of the recessed gate, which can be well covered by the high-quality dielectric Al_2O_3 , the high critical breakdown field strength between the gate and the drain region can be effectively suppressed by the gate field plate design. A low surface gate leakage current was demonstrated to achieve a high breakdown voltage performance of 1190 V. Additionally, the gate field plate design also helped achieve a higher BV performance for the recessed gate devices.

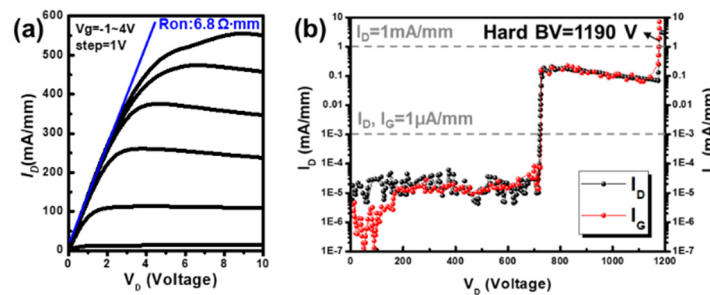


Figure 4. (a) DC I_D – V_D output characteristics of the normally-off AlGaN/GaN MIS-HEMT with the recessed gate. (b) Off-state breakdown characteristics of the recessed gate device with a gate–drain length of 10 μm measured at V_G of -10 V.

To further compare the trade-off between V_{TH} and $I_{D,max}$, Table 1 highlights the performance of the proposed MIS-HEMT with the recessed gate device and the state-of-the-art normally-off GaN devices. Compared to the device discussed in [54], our study exhibited a slightly higher BV of 720 V at 1 $\mu\text{A}/\text{mm}$. However, their $I_{D,max}$ exceeded this work by 200 mA/mm. This was due to the double-channel heterostructure design, which offered high 2DEG mobility by the lower channel heterostructure. The upper channel heterostructure achieved a fully recessed gate by completely etching away the AlGaN layer. This fully recessed gate structure aimed to obtain a normally-off operation with a positive V_{TH} requirement. Typically, when the gate recess is fully etched away, V_{TH} tends to be large, leading to a lower $I_{D,max}$. Therefore, the design of a double-channel heterostructure necessitates carefully considering the complex epitaxy process to attain high positive V_{TH} and $I_{D,max}$. In contrast, this work with a standard one-channel heterostructure and by ALE etching retains a remaining 3.7 nm of AlGaN after the gate recess, providing a simple process and controllable adjustment of V_{TH} and $I_{D,max}$.

Table 1. Comparison of state-of-the-art normally-off GaN devices [54–62].

Ref.	V_{TH} (V)	$I_{D,max}$ (mA/mm)	$R_{ON,SP}$ (m Ω ·cm ²)	BV (V)
This work	2.0	608	1.27	720 at 1 μ A/mm 1190 at 1 mA/mm
[54]	0.5	836	1.48	705 at 1 μ A/mm
[55]	1.35	500	1.56	1400 at 5 μ A/mm
[56]	0.4	356	2.79	880 at 5 μ A/mm
[57]	1.5	110	1.5	135 at 1 mA/mm
[58]	3.2	630	3.3	696 at 34 mA/mm
[59]	3.0	363	0.87	650 at 1 μ A/mm
[60]	1.2	825	0.63	810 at 1 mA/mm
[61]	0.8	312	2.73	852 at 1 μ A/mm
[62]	2.6	823	1.76	710 at 10 μ A/mm

The MIS-HEMT with the recessed gate formation using the novel low-damage ALE technology showed competitive performance, which featured both a high current density of 608 mA/mm and a controllable threshold voltage of +2.0 V. Another important factor for power GaN devices is the BV and $R_{ON,SP}$. The ALE-fabricated recessed gate devices demonstrated a very competitive BV of 1190 V at 1 mA/mm and $R_{ON,SP}$ of 1.27 m Ω ·cm² when compared to some state-of-the-art normally-off GaN devices. These results suggest that the normally-off device with the ALE recessed gate has significant potential for high-power device applications, such as in power converters and inverters.

4. Conclusions

Our study successfully showcased the exceptional performance of a normally-off GaN MIS-HEMT device with a recessed gate. Using the novel ALE technology allowed us to precisely control the recessed gate with normally-off characteristics with a remaining thickness of 3.7 nm, providing distinct advantages in nanoscale control and minimal surface damage. The device exhibited high-performance characteristics, including a high maximum drain current ($I_{D,max}$) of 608 mA/mm, a controllable threshold voltage (V_{TH}) of +2.0 V, and an outstanding on/off current ratio of 10^9 . Furthermore, the device demonstrated a remarkable off-state hard breakdown voltage (BV) of 1190 V at 1 mA/mm in the gate-to-drain of the I_G current. The superior BV performance can be attributed to the low surface roughness (Ra) of 0.40 nm in the recessed gate region, ensuring excellent coverage of the high-quality dielectric Al₂O₃. Additionally, incorporating a gate field plate with a width of 11 μ m in the design effectively suppressed the high critical breakdown field strength between the gate and drain regions, further enhancing the device performance. Based on these studies, we believe that normally-off GaN MIS-HEMTs with recessed gates, enabled by the innovative ALE technology, hold significant potential for applications in large-area high-power devices. These devices can achieve remarkable BV and $I_{D,max}$ values and maintain a controllable V_{TH} and a high on/off current ratio, making them up-and-coming candidates for next-generation power electronics applications.

Author Contributions: The detailed contributions are as follows: Front-end process of the MIS-HEMT and writing—original draft preparation, A.-C.L.; back-end process of the MIS-HEMT and measurement, P.-T.T.; integration process and writing—review and editing, H.-C.C.; data curation analysis and benchmarking of the novel technology, Y.-Y.L.; investigation mask layout and funding acquisition, P.-C.Y.; supervision and co-writing—review and co-editing, H.-C.K. All authors have read and agreed to the published version of the manuscript.

Funding: Ministry of Science and Technology, Taiwan (112-2218-E-008-007-).

Data Availability Statement: Not applicable.

Acknowledgments: The authors would like to thank Oxford Instruments Plasma Technology along with Sung-Jin Cho, Aileen O'Mahony, and Andrew Newton for the ALE valuable support and the Semiconductor Research Center, Hon Hai Research Institute, for the helpful discussion.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Mishra, U.K.; Parikh, P.; Wu, Y.-F. AlGaIn/GaN HEMTs—an overview of device operation and applications. *Proc. IEEE* **2002**, *90*, 1022–1031. [\[CrossRef\]](#)
2. Kevin, J.C.; Oliver, H.; Alex, L.; Chunlin, T.; Tetsuzo, U.; Yasuhiro, U.; Yifeng, W. GaN-on-Si power technology: Devices and applications. *IEEE Trans. Electron Devices* **2017**, *64*, 779–795.
3. Chen, K.J.; Zhou, C. Enhancement-mode AlGaIn/GaN HEMT and MIS-HEMT technology. *Phys. Status Solidi (A)* **2011**, *208*, 434–438. [\[CrossRef\]](#)
4. Oka, T.; Nozawa, T. AlGaIn/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications. *IEEE Electron Device Lett.* **2008**, *29*, 668–670. [\[CrossRef\]](#)
5. Zhou, Q.; Chen, B.; Jin, Y.; Huang, S.; Wei, K.; Liu, X.; Bao, X.; Mou, J.; Zhang, B. High-Performance Enhancement-Mode Al₂O₃/AlGaIn/GaN-on-Si MISFETs With 626 MW/cm² Figure of Merit. *IEEE Trans. Electron Devices* **2015**, *62*, 776–781. [\[CrossRef\]](#)
6. Greco, G.; Iucolano, F.; Roccaforte, F. Roccaforte. Review of technology for normally-off HEMTs with p-GaN gate. *Mater. Sci. Semicond. Process.* **2018**, *78*, 96–106. [\[CrossRef\]](#)
7. Yasuhiro, U.; Masahiro, H.; Hiroaki, U.; Hisayoshi, M.; Hidetoshi, I.; Manabu, Y.; Tetsuzo, U.; Tsuyoshi, T.; Daisuke, U. A Normally-off AlGaIn/GaN Transistor with R on A = 2.6 mΩcm² and BV_{ds} = 640V using conductivity modulation. In Proceedings of the 2006 International Electron Devices Meeting, San Francisco, CA, USA, 11–13 December 2006; pp. 1–4.
8. Hideyuki, O.; Masahiro, H.; Akihiko, N.; Takahiro, S.; Keiichi, M.; Hisayoshi, M.; Masaya, M.; Yasuhiro, U. Through recessed and regrowth gate technology for realizing process stability of GaN-GITs. In Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, Czech Republic, 12–16 June 2016; pp. 23–26.
9. Cai, Y.; Zhou, Y.; Chen, K.; Lau, K. High-performance enhancement-mode AlGaIn/GaN HEMTs using fluoride-based plasma treatment. *IEEE Electron Device Lett.* **2005**, *26*, 435–437.
10. Zhu, T.; Zhuo, F.; Wang, F.; Wang, H.; He, X.; Shi, S. A Novel Cascode GaN Switch Integrating Paralleled GaN DHEMTs for High-Power Applications. In Proceedings of the 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Xi'an, China, 16–18 May 2018; pp. 332–336.
11. Buetow, S.; Herzer, R. Characterization of GaN-HEMT in cascode topology and comparison with state of the art-power devices. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 196–199.
12. Lorenz, A.; Derluyn, J.; Das, J.; Cheng, K.; Degroote, S.; Medjdoub, F.; Germain, M.; Borghs, G. Influence of thermal anneal steps on the current collapse of fluorine treated enhancement mode SiN/AlGaIn/GaN HEMTs. *Phys. Status Solidi (C)* **2009**, *6*, S996–S998. [\[CrossRef\]](#)
13. Meneghini, M.; Hilt, O.; Wuerfl, J.; Meneghesso, G.J.E. Technology and reliability of normally-off GaN HEMTs with p-type gate. *Energies* **2017**, *10*, 153. [\[CrossRef\]](#)
14. Ren, F.; Lothian, J.; Chen, Y.; Karlicek, R.; Tran, L.; Schurmann, M.; Stall, R.; Lee, J.; Pearton, S. Recessed gate GaN field effect transistor. *Solid-State Electron.* **2006**, *41*, 1819–1820. [\[CrossRef\]](#)
15. Maroldt, S.; Haupt, C.; Pletschen, W.; Müller, S.; Quay, R.; Ambacher, O.; Schippel, C.; Schwierz, F. Gate-Recessed AlGaIn/GaN Based Enhancement-Mode High Electron Mobility Transistors for High Frequency Operation. *Jpn. J. Appl. Phys.* **2009**, *48*, 04C083. [\[CrossRef\]](#)
16. Saito, W.; Takada, Y.; Kuraguchi, M.; Tsuda, K.; Omura, I. Recessed-gate structure approach toward normally off high-voltage AlGaIn/GaN HEMT for power electronics applications. *IEEE Trans. Electron Devices* **2006**, *53*, 356–362. [\[CrossRef\]](#)
17. Chung, J.W.; Hoke, W.E.; Chumbes, E.M.; Palacios, T. AlGaIn/GaN HEMT With 300-GHz f_{max}. *IEEE Electron Device Lett.* **2010**, *31*, 195–197. [\[CrossRef\]](#)
18. Burm, J.; Schaff, W.J.; Martin, G.H.; Eastman, L.F.; Amano, H.; Akasaki, I. Recessed gate GaN MODFETs. *Solid-State Electron.* **2013**, *41*, 247–250. [\[CrossRef\]](#)
19. Schuette, M.L.; Ketterson, A.; Song, B.; Beam, E.; Chou, T.-M.; Pilla, M.; Tserng, H.-Q.; Gao, X.; Guo, S.; Fay, P.J.; et al. Gate-recessed integrated E/D GaN HEMT technology with f_T/f_{max} >300 GHz. *IEEE Electron Device Lett.* **2013**, *34*, 741–743. [\[CrossRef\]](#)
20. Hsieh, T.-E.; Chang, E.-Y.; Song, Y.-Z.; Lin, Y.-C.; Wang, H.-C.; Liu, S.-C.; Salahuddin, S.S.; Hu, C.C. Gate recessed quasi-normally OFF Al₂O₃/AlGaIn/GaN MIS-HEMT with low threshold voltage hysteresis using PEALD AlN interfacial passivation layer. *IEEE Electron Device Lett.* **2014**, *35*, 732–734.
21. Kinoshita, T.; Hane, M.; McVittie, J.P. Microelectronics, M. Nanometer Structures Processing, and Phenomena. Notching as an example of charging in uniform high density plasmas. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.* **1996**, *14*, 560–565.

22. Yonekura, K.; Goto, K.; Matsuura, M.; Fujiwara, N.; Tsujimoto, K. Tsujimoto. Low-damage damascene patterning using porous inorganic low-dielectric-constant materials. *Jpn. J. Appl. Phys.* **2005**, *44*, 2976. [\[CrossRef\]](#)
23. Cao, X.A.; Cho, H.; Pearton, S.J.; Dang, G.T.; Zhang, A.P.; Ren, F.; Shul, R.J.; Zhang, L.; Hickman, R.; Van Hove, J.M. Depth and thermal stability of dry etch damage in GaN Schottky diodes. *Appl. Phys. Lett.* **2019**, *75*, 232–234. [\[CrossRef\]](#)
24. Hashizume, T.; Nakasaki, R. Discrete surface state related to nitrogen-vacancy defect on plasma-treated GaN surfaces. *Appl. Phys. Lett.* **2002**, *80*, 4564–4566. [\[CrossRef\]](#)
25. Mouffak, Z.; Bensaula, A.; Trombetta, L. The effects of nitrogen plasma on reactive-ion etching induced damage in GaN. *J. Appl. Phys.* **2003**, *95*, 727–730. [\[CrossRef\]](#)
26. Tang, K.; Huang, W.; Chow, T.P. GaN MOS Capacitors and FETs on Plasma-Etched GaN Surfaces. *J. Electron. Mater.* **2009**, *38*, 523–528. [\[CrossRef\]](#)
27. Shrestha, N.M.; Li, Y.; Suemitsu, T.; Samukawa, S. Electrical Characteristic of AlGaIn/GaN High-Electron-Mobility Transistors With Recess Gate Structure. *IEEE Trans. Electron Devices* **2019**, *66*, 1694–1698. [\[CrossRef\]](#)
28. Kanarik, K.J.; Lill, T.; Hudson, E.A.; Sriraman, S.; Tan, S.; Marks, J.; Vahedi, V.; Gottscho, R.A. Overview of atomic layer etching in the semiconductor industry. *J. Vac. Sci. Technol. A Vol.* **2015**, *33*, 020802. [\[CrossRef\]](#)
29. Kanarik, K.J.; Tan, S.; Gottscho, R.A. Atomic layer etching: Rethinking the art of etch. *J. Phys. Chem. Lett.* **2018**, *9*, 4814–4821. [\[CrossRef\]](#)
30. Fang, C.; Cao, Y.; Wu, D.; Li, A. Thermal atomic layer etching: Mechanism, materials and prospects. *Prog. Nat. Sci. Mater. Int.* **2018**, *28*, 667–675. [\[CrossRef\]](#)
31. George, S.M.; Lee, Y. Prospects for thermal atomic layer etching using sequential, self-limiting fluorination and ligand-exchange reactions. *ACS Nano* **2016**, *10*, 4889–4894. [\[CrossRef\]](#)
32. Faraz, T.; Roozeboom, F.; Knoops, H.C.M.; Kessels, W.M.M. Atomic layer etching: What can we learn from atomic layer deposition? *ECS J. Solid State Sci. Technol.* **2015**, *4*, N5023. [\[CrossRef\]](#)
33. Ohba, T.; Yang, W.; Tan, S.; Kanarik, K.J.; Nojiri, K. Nojiri. Atomic layer etching of GaN and AlGaIn using directional plasma-enhanced approach. *Jpn. J. Appl. Phys.* **2017**, *56*, 06HB06. [\[CrossRef\]](#)
34. Yang, T.-Y.; Huang, H.-Y.; Liang, Y.-K.; Wu, J.-S.; Kuo, M.-Y.; Chang, K.-P.; Hsu, H.-T.; Chang, E.-Y. A Normally-Off GaN MIS-HEMT Fabricated Using Atomic Layer Etching to Improve Device Performance Uniformity for High Power Applications. *IEEE Electron Device Lett.* **2022**, *43*, 1629–1632. [\[CrossRef\]](#)
35. Liu, Y.; Yu, Q.; Du, J.-F. A novel high breakdown voltage and high switching speed GaN HEMT with p-GaN gate and hybrid AlGaIn buffer layer for power electronics applications. *Chin. Phys. B* **2020**, *29*, 127701. [\[CrossRef\]](#)
36. Liu, Y.; Yu, Q.; Du, J. Simulation design of a high-breakdown-voltage p-GaN-gate GaN HEMT with a hybrid AlGaIn buffer layer for power electronics applications. *J. Comput. Electron.* **2010**, *19*, 1527–1537. [\[CrossRef\]](#)
37. Burnham, S.D.; Boutros, K.; Hashimoto, P.; Butler, C.; Wong, D.W.S.; Hu, M.; Micovic, M. Gate-recessed normally-off GaN-on-Si HEMT using a new O₂-BCl₃ digital etching technique. *Phys. Status Solidi C* **2010**, *7*, 2010–2012. [\[CrossRef\]](#)
38. Hahn, H.; Lükens, G.; Ketteniss, N.; Kalisch, H.; Vescan, A. Recessed-Gate Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistors on Si with Record DC Performance. *Appl. Phys. Express* **2011**, *4*, 114102. [\[CrossRef\]](#)
39. Du, F.; Jiang, Y.; Wu, Z.; Lu, H.; He, J.; Tang, C.; Hu, Q.; Wen, K.; Tang, X.; Hong, H.; et al. The Atomic Layer Etching Technique with Surface Treatment Function for InAlN/GaN Heterostructure. *Crystals* **2022**, *12*, 722. [\[CrossRef\]](#)
40. Rocha, P.F.P.P.; Vauche, L.; Pimenta-Barros, P.; Ruel, S.; Escoffier, R.; Buckley, J. Recent Developments and Prospects of Fully Recessed MIS Gate Structures for GaN on Si Power Transistors. *Energies* **2023**, *16*, 2978. [\[CrossRef\]](#)
41. Chiu, H.C.; Yang, C.W.; Wang, H.C.; Huang, F.H.; Kao, H.L.; Chien, F.T. Characteristics of AlGaIn/GaN HEMTs With Various Field-Plate and Gate-to-Drain Extensions. *IEEE Trans. Electron Devices* **2013**, *60*, 3877–3882. [\[CrossRef\]](#)
42. Shi, N.; Wang, K.; Zhou, B.; Weng, J.; Cheng, Z. Optimization AlGaIn/GaN HEMT with Field Plate Structures. *Micromachines* **2022**, *13*, 702. [\[CrossRef\]](#)
43. Mohanbabu, A.; Mohankumar, N.; Raj, D.G.; Sarkar, P.; Saha, S.K. Efficient III-Nitride MIS-HEMT devices with high-κ gate dielectric for high-power switching boost converter circuits. *Superlattices Microstruct.* **2012**, *103*, 270–284. [\[CrossRef\]](#)
44. Lee, J.W.; Kumar, V.; Adesida, I. High-Power-Density 0.25 μm Gate-Length AlGaIn/GaN High-Electron-Mobility Transistors on Semi-Insulating 6H-SiC Substrates. *Jpn. J. Appl. Phys.* **2006**, *45*, 13. [\[CrossRef\]](#)
45. Mohanbabu, A.; Anbuselvan, N.; Mohankumar, N.; Godwinraj, D.; Sarkar, C.K. Modeling of sheet carrier density and microwave frequency characteristics in Spacer based AlGaIn/AlN/GaN HEMT devices. *Solid-State Electron.* **2014**, *91*, 44–52. [\[CrossRef\]](#)
46. Zhao, Y.; Wang, C.; Zheng, X.; Ma, X.; He, Y.; Liu, K.; Li, A.; Peng, Y.; Zhang, C.; Hao, Y. Effects of recess depths on performance of AlGaIn/GaN power MIS-HEMTs on the Si substrates and threshold voltage model of different recess depths for the using HfO₂ gate insulator. *Solid-State Electron.* **2020**, *163*, 107649. [\[CrossRef\]](#)
47. Ćapajna, M.; Kuzmík, J. A comprehensive analytical model for threshold voltage calculation in GaN based metal-oxide-semiconductor high-electron-mobility transistors. *Appl. Phys. Lett.* **2012**, *100*, 113509. [\[CrossRef\]](#)
48. Smorchkova, I.P.; Elsass, C.R.; Ibbetson, J.P.; Vetury, R.; Heying, B.; Fini, P.; Haus, E.; DenBaars, S.P.; Speck, J.S.; Mishra, U.K. Polarization-induced charge and electron mobility in AlGaIn/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy. *J. Appl. Phys.* **1999**, *86*, 4520–4526. [\[CrossRef\]](#)
49. Shenghou, L.; Shu, Y.; Zhikai, T.; Qimeng, J.; Cheng, L.; Maojun, W.; Chen, K.J. Al₂O₃/AlN/GaN MOS-Channel-HEMTs With an AlN Interfacial Layer. *IEEE Electron Device Lett.* **2014**, *35*, 723–725.

50. Sung-Wen, C.; De-Ren, Y.; Neng-Jie, Y.; Wen-Chieh, H.; Jerry, T.; Hao-Chung, K.; Jia-Min, S. Improving the GaN-on-GaN Schottky Barrier Diode by ALD-AlN Tunneling Barrier Layer and Multi-Fins Structure. *IEEE Trans. Nanotechnol.* **2021**, *20*, 489–494.
51. Meneghesso, G.; Meneghini, M.; Zanoni, E. Breakdown mechanisms in AlGaIn/GaN HEMTs: An overview. *Jpn. J. Appl. Phys.* **2014**, *53*, 100211. [\[CrossRef\]](#)
52. Degraeve, R.; Kauerauf, T.; Cho, M.; Zahid, M.; Ragnarsson, L.; Brunco, D.; Kaczer, B.; Roussel, P.; De Gendt, S.; Groeseneken, G. Degradation and breakdown of 0.9 nm EOT SiO₂/ALD-HfO₂/metal gate stacks under positive constant voltage stress. In Proceedings of the IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest, Washington, DC, USA, 5 December 2005; pp. 408–411.
53. Del Alamo, J.A.; Guo, A.; Warnock, S. Gate dielectric reliability and instability in GaN metal-insulator-semiconductor high-electron-mobility transistors for power electronics. *J. Mater. Res.* **2017**, *32*, 3458–3468. [\[CrossRef\]](#)
54. Wei, J.; Liu, S.; Li, B.; Tang, X.; Lu, Y.; Liu, C.; Hua, M.; Zhang, Z.; Tang, G.; Chen, K.J. Enhancement-mode GaN double-channel MOS-HEMT with low on-resistance and robust gate recess. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 9.4.1–9.4.4.
55. Jingnan, G.; Yufeng, J.; Yilong, H.; Bing, X.; Cheng, P.W.; Bo, S.; Maojun, W. Gate-Recessed Normally OFF GaN MOSHEMT With High-Temperature Oxidation/Wet Etching Using LPCVD Si₃N₄ as the Mask. *IEEE Trans. Electron Devices* **2018**, *65*, 1728–1733.
56. Ming, T.; Shaofer, L.; Bing, X.; Cheng, P.W.; Jinyan, W.; Yilong, H.; Wengang, W.; Kai, C.; Bo, S.; Maojun, W. Characterization of 880 V Normally Off GaN MOSHEMT on Silicon Substrate Fabricated With a Plasma-Free, Self-Terminated Gate Recess Process. *IEEE Trans. Electron Devices* **2018**, *65*, 1453–1457.
57. He, Y.; He, Q.; Mi, M.; Zhang, M.; Wang, C.; Yang, L.; Ma, X.; Hao, Y. High Breakdown Electric Field MIS-Free Fully Recessed-Gate Normally Off AlGaIn/GaN HEMT With N₂O Plasma Treatment. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 2163–2170. [\[CrossRef\]](#)
58. Ming, T.; Shaofer, L.; Bing, X.; Cheng, P.W.; Jinyan, W.; Yilong, H.; Wengang, W.; Kai, C.; Bo, S.; Maojun, W. A Novel 700 V Monolithically Integrated Si-GaN Cascoded Field Effect Transistor. *IEEE Electron Device Lett.* **2018**, *39*, 394–396.
59. Chiu, H.-C.; Liu, C.-H.; Huang, C.-R.; Chiu, C.-C.; Wang, H.-C.; Kao, H.-L.; Lin, S.-Y.; Chien, F.-T. Normally-Off p-GaN Gated AlGaIn/GaN MIS-HEMTs with ALD-Grown Al₂O₃/AlN Composite Gate Insulator. *Membranes* **2021**, *11*, 727. [\[CrossRef\]](#)
60. Huang, Y.P.; Huang, C.C.; Lee, C.S.; Hsu, W.C. High-Performance Normally-OFF AlGaIn/GaN Fin-MISHEMT on Silicon With Low Work Function Metal-Source Contact Ledge. *IEEE Trans. Electron Devices* **2020**, *67*, 5434–5440. [\[CrossRef\]](#)
61. Xing, W.; Xiaodong, Z.; Chi, S.; Wenxin, T.; Chunhong, Z.; Fu, C.; Tao, H.; Guohao, Y.; Liang, S.; Wenkui, L.; et al. Improvement of Breakdown Voltage and ON-Resistance in Normally-OFF AlGaIn/GaN HEMTs Using Etching-Free p-GaN Stripe Array Gate. *IEEE Trans. Electron Devices* **2021**, *68*, 5041–5047.
62. Hongyue, W.; Jinyan, W.; Mengjun, L.; Qirui, C.; Min, Y.; Yandong, H.; Wengang, W. 823-mA/mm Drain Current Density and 945-MW/cm² Baliga's Figure-of-Merit Enhancement-Mode GaN MISFETs With a Novel PEALD-AlN/LPCVD-Si₃N₄ Dual-Gate Dielectric. *IEEE Electron Device Lett.* **2018**, *39*, 1888–1891.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.