



Article Non-Buffer Epi-AlGaN/GaN on SiC for High-Performance Depletion-Mode MIS-HEMTs Fabrication

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Abstract: A systematic study of epi-AlGaN/GaN on a SiC substrate was conducted through a comprehensive analysis of material properties and device performance. In this novel epitaxial design, an AlGaN/GaN channel layer was grown directly on the AlN nucleation layer, without the conventional doped thick buffer layer. Compared to the conventional epi-structures on the SiC and Si substrates, the non-buffer epi-AlGaN/GaN structure had a better crystalline quality and surface morphology, with reliable control of growth stress. Hall measurements showed that the novel structure exhibited comparable transport properties to the conventional epi-structure on the SiC substrate, regardless of the buffer layer. Furthermore, almost unchanged carrier distribution from room temperature to 150 °C indicated excellent two-dimensional electron gas (2DEG) confinement due to the pulling effect of the conduction band from the nucleation layer as a back-barrier. High-performance depletion-mode MIS-HEMTs were demonstrated with on-resistance of 5.84 Ω ·mm and an output current of 1002 mA/mm. The dynamic characteristics showed a much smaller decrease in the saturation current (only ~7%), with a quiescent drain bias of 40 V, which was strong evidence of less electron trapping owing to the high-quality non-buffer AlGaN/GaN epitaxial growth.

Keywords: GaN; MIS-HEMTs; buffer layer; SiC substrate; current collapse

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs), as a representative of GaNbased wide-band gap semiconductor devices, are becoming one of the most promising candidates for next-generation high-density power conversion systems due to high breakdown voltage, low on-resistance, a wide range of operating temperatures, and high frequency switching [1,2]. Considering the advantages of substrate size and cost, GaN on Si technology has been widely used in AlGaN/GaN HEMTs fabrication [3]. However, large mismatches of lattice dimension and thermal expansion between Si and (Al)GaN will lead to high-density dislocation, poor crystalline quality, and even wafer cracks in the (Al)GaN epilayer due to the failure of stress control. To solve these problems, some strain management procedures have been developed such as AlN/GaN superlattice [4], gradient Al component from AlN to GaN [5,6], and an AlN insert layer [7].

Due to the presence of impurities as Si and O in the metal-organic chemical vapor deposition (MOCVD) chamber, *n*-type (Al)GaN has often been obtained for the buffer layer, even in the unintentional doping (UID) epitaxial process. Therefore, in order to reduce the



Citation: Zhang, P.; Wang, L.; Zhu, K.; Wang, Q.; Pan, M.; Huang, Z.; Yang, Y.; Xie, X.; Huang, H.; Hu, X.; et al. Non-Buffer Epi-AlGaN/GaN on SiC for High-Performance Depletion-Mode MIS-HEMTs Fabrication. *Micromachines* **2023**, *14*, 1523. https://doi.org/10.3390/ mi14081523

Academic Editor: Kun Li

Received: 30 June 2023 Revised: 22 July 2023 Accepted: 25 July 2023 Published: 29 July 2023



Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). vertical leakage and increase the breakdown voltage of devices [8], several methods have been proposed, such as a thicker buffer layer [9], optimized concentration of C-doping or Fe-doping, and so on [10–12]. It should be pointed out that a large number of deep-level traps will be introduced during compensation doping in the thick buffer layer, which is one of the main causes of the current collapse phenomenon of AlGaN/GaN HEMTs, leading to increasing dynamic on-resistance and a decreasing output current. In other words, the buffer layer on the Si substrate has both positive as well as negative effects on device performance.

Improving the epi-structure and substrate design is a promising method to enhance the dynamic performance of devices. For the 4H-SiC substrate, its lattice mismatch with (Al)GaN is much lower [13,14]; hence, there is no urgent need for the thick buffer layer to reduce dislocation. Compared with *p*-type doping Si, the 4H-SiC substrate is semiinsulating, which could suppress the vertical leakage current without the help of a highresistance buffer. In addition, the thermal conductivity of SiC (substrate thickness of 0.5 mm) is much higher than that of Si (substrate thickness of 1 mm), indicating that there is a significant advantage in its heat dissipation capability [13]. Recently, the growth technique of SiC has been rapidly developed due to the huge demand for electric vehicles. Thus, the cost of SiC substrates will come down gradually, causing GaN on SiC to become a potential solution for high-end power-switching applications, instead of GaN on Si.

Chen [15] and Hult [16] et al. proposed an epi-structure named QuanFINE based on a SiC substrate that skipped the thick buffer layer between the AlN nucleation layer and GaN channel layer, showing some superiority in their reports, respectively. However, the properties of the epitaxial wafer and the device performance based on this novel epistructure have not been studied in detail yet. In this work, a variety of characterization methods were employed to systematically evaluate the non-buffer epi-structure without a buffer layer compared with conventional epitaxial wafers based on SiC and Si substrates. Temperature-changing tests were performed for the Schottky diodes on the three epistructures to further investigate the surface and transport properties of two-dimensional electron gas (2DEG). Normally-on metal insulator semiconductor-HEMTs (MIS-HEMTs) were also fabricated. The DC and dynamic performances of the devices were studied and compared, and the advantages of the non-buffer structure were revealed.

2. Experimental Section

Three AlGaN/GaN hetero-structures epitaxially grown by MOCVD on 4-inch semiinsulating SiC substrates and 6-inch *p*-doping Si substrates were used in this paper. The novel epi-structure without a buffer layer was GaN (2 nm)/Al_{0.26}Ga_{0.74}N (17 nm)/AlN (1 nm)/UID GaN (150 nm)/AlN (200 nm)/SiC (0.5 mm). It should be pointed out that a unique epitaxy process of the AlN nucleating layer and interface treatment was developed to play an important role in the high crystal quality of the AlN growth. The other two conventional epitaxial wafers on SiC and Si substrates were grown simultaneously with the same structure: GaN (2 nm)/Al_{0.25}Ga_{0.75}N (18 nm)/AlN (1 nm)/UID GaN (150 nm)/Buffer (Fe-doping, 2.2 μ m)/AlN (200 nm)/SiC (0.5 mm) or Si (1 mm). They are referred to as Epi A, Epi B, and Epi C in the rest of this article. The schematic structures of the above epitaxial wafers are shown in Figure 1a–c.

Four characterization methods were performed to investigate the effects of the nonbuffer design on the heterojunction and surface properties. A WITec alpha300R Raman Imaging Microscope (WITec, Ulm, Germany) was used to study the growth stress with a 405 nm solid-state laser. Rigaku SmartLabII X-ray Diffraction (XRD) (Rigaku, Tokyo, Japan) was employed to characterize the crystalline quality of the epilayer through X-ray rocking curves of (002) and (102). The surface morphology was evaluated using a Park NX10 Atomic Force Microscope (AFM) (Park Systems Corp., Suwon, Republic of Korea) in no-contact mode (NCM). The carrier concentration and mobility in the heterojunction channel were measured by the Ecopia AHT55T3 (Ecopia, Anyang, Republic of Korea) Hall Effect Measurement System.



Figure 1. Schematic structures of (**a**) non-buffer epi-structure on SiC substrate, i.e., Epi A, (**b**) conventional epi-structure on SiC substrate, i.e., Epi B, and (**c**) conventional epi-structure on Si substrate, i.e., Epi C.

The fabrication of Schottky diodes on the three epi-structures started with mesa etch using an inductively coupled plasma (ICP) etcher with Cl-based gas. Ti/Al/Ni/Au (20/120/50/50 nm) metal stacks were deposited as the source/drain electrodes by electron beam evaporation (EBE). The ohmic contact was formed by rapid thermal annealing (RTA) at the temperature range of 790 °C to 860 °C for 30 s in N₂ ambient, according to the different crystalline quality in the AlGaN barrier layer on different substrates. The *I-V* results of the transmission line model (TLM) suggested that the contact resistance (R_c) of each epi-structure was 0.82 Ω ·mm, 0.73 Ω ·mm, and 0.77 Ω ·mm, sequentially. Finally, the gate electrodes of Ni/Au (40/60 nm) were deposited by EBE.

The process flow for MIS-HEMTs was similar with Schottky diodes, with the addition of a gate dielectric process between the ohmic contact formation and the gate metal deposition, as shown in Figure 2a. Before 20 nm Al₂O₃ deposition by thermal atomic layer deposition (ALD), in-situ remote NH₃/N₂ plasma treatment was carried out in a Sentech Si-500 PEALD system (Sentech, Berlin, Germany), which was applied to the gate region in sequence at an RF plasma power of 100/50 W, gas flow of 100/100 sccm, process time of 4/10 min, and substrate temperature of 300 °C. NH₃ plasma acted as a deoxidation step to remove the native oxide, while the subsequent N₂ plasma compensated the N vacancy beneath the surface and formed the nitridated interface. After the following ALD process, post-deposition annealing (PDA) was implemented at 450 °C in O₂ ambient for 3 min to reduce the defects in the film. Transmission electron microscopy (TEM) was performed on the Al₂O₃/GaN/AlGaN interface to examine the effect of in-situ remote plasma treatment, as shown in Figure 2b. The boundary of the interface without any treatment was rough, which tended to be sharp after the low-damage in-situ NH₃/N₂ plasma treatment.



Figure 2. (a) Schematic process flow of MIS-HEMTs fabrication. (b) Cross-sectional TEM micrographs of the $Al_2O_3/GaN/AlGaN$ interface with and without in-situ plasma treatment.

3. Results and Discussion

3.1. Epitaxial Wafer Quality Characterization

Figure 3a,b display the cross-section views of the non-buffer epi-structure, i.e., Epi A, and conventional epi-structure on the SiC substrate, i.e., Epi B, by scanning electron microscopy (SEM). The thickness of the total epilayer on Epi A was approximately 380 nm, which was only 1/7 compared with the conventional epilayer on Epi B, indicating a clear advantage of heat dissipation of the devices. However, the surface stress on Epi A should be investigated due to the absence of a buffer layer, which is considered to play a crucial role in stress control on conventional epi-structures. The scattering peaks of GaN in E2(TO) mode could be measured by Raman spectroscopy; Raman shift is sensitive enough to characterize the growth stress for a GaN epilayer. Figure 3c shows the Raman spectrum of the above three epi-structures. The peaks of SiC, Si, and GaN exhibited different strengths, consistent with the thickness of the respective epilayers and substrates. Figure 3d shows the Lorentz fitting results of the GaN E2(TO) peak for the above samples. The Raman shifts were 567.37 cm⁻¹, 567.44 cm⁻¹, and 567.29 cm⁻¹, respectively. Compared with the theoretical position of 567.6 cm⁻¹ [17,18], slight red shifts occurred in all samples, which suggests that there was tensile stress on the surface with intensities of 0.07 GPa, 0.10 GPa, and 0.13 GPa by calculation [19]. The peak positions of GaN E2(TO) for the three epi-structures were very close to the theoretical value, indicating that the epitaxial process on the SiC substrate without a buffer layer could still achieve effective stress control.



Figure 3. Cross-section views of (**a**) Epi A and (**b**) Epi B by SEM. (**c**) Room temperature Raman spectra of the three epi-structures on SiC and Si substrates under 405 nm laser line excitation. (**d**) Lorentz fitting curves of GaN E2(TO) for above samples.

The crystalline quality of the (Al)GaN epilayer could be characterized by the full width at half maximum (FWHM) in the XRD rocking curves of (002) and (102) planes, respectively. The FWHM of (002) and (102) represents the densities of helical and mixed dislocation [20], as shown in Figure 4a. The non-buffer epi-structure on the SiC substrate

had the lowest dislocation density, with FWHMs of (002) and (102) of only 145 arcsec and 267 arcsec, confirming that the growing doping buffer layer was not essential on the SiC substrate. For the conventional epi-structure on SiC, the FWHMs were 196 arcsec and 395 arcsec. The FWHMs of the conventional epi-structure on Si were measured as 433 arcsec and 681 arcsec. This result fully indicates that the epi-structures on the 4H-SiC substrate had a lower dislocation density and higher crystalline quality than that on the Si substrate.



Figure 4. X-ray rocking curves of (a) (002) and (b) (102) for the three epi-structures by XRD.

Figure 5 shows the surface morphology of the above three epi-structures measured by AFM ($5 \times 5 \ \mu m^2$). Atomic step-flow patterns were observed in all of them. The mean square root (RMS) roughness of two epi-structures on the SiC substrate was much less than those on the Si substrate. There were plenty of pits due to dislocation at both ends of the step flow curve on the surface of the epi-structure on the Si substrate. For comparison, no clear dislocation points could be observed on the surface of the other two epi-structures on the SiC substrate. Among these epi-structures, the non-buffer one had the smallest RMS roughness of 0.231 nm, indicating the lowest density of dislocation results and best surface morphology.



Figure 5. Surface morphology of (a) Epi A, (b) Epi B, and (c) Epi C by AFM.

Hall measurements were used to study the electrical performance of these heterojunction channels. The results are recorded in Table 1, where R_{sheet} is the sheet resistance of the heterojunction, μ_{2DEG} is 2DEG mobility, and n_{s} is electron density. The smallest R_{sheet} of 284 Ω /sq and largest n_{s} up to 9.8 × 10¹³ cm⁻² were measured on the conventional epi-structure on the SiC substrate. Although owning the same epilayer, R_{sheet} of the conventional epi-structure on Si was nearly 30% larger. The non-buffer epi-structure on the SiC substrate had the highest μ_{2DEG} of 1835 cm²/V·s and n_s of 9.3 × 10¹² cm⁻², and its R_{sheet} was slightly higher than that for the conventional epi-structure. These results indicate that the 2DEG properties were almost independent of the buffer design but strongly related to the crystalline quality of the (Al)GaN epilayer.

Table 1. Hall test results of the three epitaxial structures.

Epi-Structures	$R_{\rm sheet}$ ($\Omega/{ m sq}$)	$\mu_{2\text{DEG}}$ (cm ² /V·s)	$n_{\rm s}~(10^{12}~{\rm cm}^{-2})$
Non-buffer epi-structure on SiC	292	2287	9.4
Conventional epi-structure on SiC	284	2245	9.8
Conventional epi-structure on Si	365	1835	9.3

3.2. Temperature Changing Tests for Schottky Diodes

The *I-V* and *C-V* properties of the Schottky diodes on the three epi-structures were measured by an MPITS2000-SE probe platform at changing temperatures in the range of room temperature (RT) to 150 °C. The voltage scanning range on the anode was -8 V to 2 V, while the cathode was connected to the ground. As shown in Figure 6, while the temperature rose, the forward current and reverse leakage both increased on each diode. The forward current increased mainly because the high temperature improved the ability concerning 2DEG spilling over the AlGaN barrier. At 150 °C, the reverse leakage of the two epi-structures on the SiC substrate increased by approximately one order of magnitude, from $\sim 10^{-4}$ mA/mm to $\sim 10^{-3}$ mA/mm. The reverse current of the epi-structure on the Si substrate increased by more than 2 orders of magnitude, from $\sim 10^{-3}$ mA/mm to $\sim 10^{-1}$ mA/mm. The significant increase in reverse leakage at high temperatures was mainly due to the trap-assisted tunneling mechanism caused by helical dislocation [21]. The non-buffer epi-structure on the SiC substrate had the minimum reverse leakage increment at high temperatures, indicating the best quality of Schottky contact. These results prove the reliability of XRD whereby the novel epitaxial design had the smallest dislocation density.



Figure 6. Measured *I-V* characteristics for Schottky diodes at different temperatures of RT ~ 150 $^{\circ}$ C on (a) Epi A, (b) Epi B, and (c) Epi C.

C-V measurements of these Schottky diodes were also carried out. Carrier distribution at different temperatures could be obtained through further calculation, as shown in Figure 7. The highest carrier concentration was found at 20~22 nm beneath the surface of the three epi-structures, which was the location of the AlGaN/GaN heterojunction channel. For the conventional epi-structures on the SiC and Si substrates, the distribution of the carrier in the direction to the channel and buffer layers was clearly widened as the temperature increased, which indicated that the high temperature led to the degradation of 2DEG confinement, and a few electrons spilled out from the channel.



Figure 7. Calculated carrier distribution at different temperatures of RT ~150 °C on (**a**) Epi A, (**b**) Epi B, and (**c**) Epi C.

The following theory explains the effect of the non-buffer design on 2DEG confinement from the perspective of the energy band [15]. As shown in Figure 8, the GaN channel layer was located upon the AlN nuclear layer in the epi-structure without a buffer layer; thus, the energy band of the GaN channel layer was pulled up by AlN due to its larger band gap. AlN could serve as the back barrier of the AlGaN/GaN interface, making the back conduction band of the AlGaN/GaN heterojunction potential well very steep. However, for the conventional epi-structures, the pulling effect from the AlN nucleation layer was not clear due to the existence of a GaN buffer layer with the thickness of a micron order.



Figure 8. Conduction band (E_c) (black line) of a (**a**) novel non-buffer epi-structure and (**b**) conventional epi-structure.

3.3. Device Performance of the MIS-HEMTs

The fabricated MIS-HEMTs had a gate length (L_g) of 4 µm, gate-source distance (L_{gs}) of 4 µm, gate-drain distance (L_{gd}) of 6 µm, and gate width (W_g) of 50 µm. Transfer and output characteristics were measured with a parameter analyzer of Keithley 4200A (Keithley, Solon, OH, USA), as shown in Figure 9. The linear transfer characteristics were obtained for $V_{DS} = 10$ V in both forward and reverse sweep directions with V_{GS} steps of 0.1 V. After in-situ NH₃/N₂ remote plasma interface treatment, the Al₂O₃/GaN/AlGaN interfaces on the three epi-structures showed low interfacial state density with small hysteresis voltage ΔV_{th} . The ΔV_{th} of the MIS-HEMTs on the SiC substrate were both only 10 mV, which was only 1/10 of those on the Si substrate. The transconductance (G_m) of the two types of devices on the SiC substrates were ~120 mS/mm and 121 mS/mm, respectively, which was 25% higher than that on the Si substrate. MIS-HEMTs on the SiC substrate also had almost the same subthreshold swings (SSs), which were 97 mV/dec and 96 mV/dec, respectively, much less than those on the Si substrate of ~130 mV/dec.



Figure 9. DC transfer and output characteristics for MIS-HEMTs on (a) Epi A, (b) Epi B, and (c) Epi C.

The output characteristics were measured at $V_{\rm DS}$ up to 10 V, with $V_{\rm GS}$ in the range of -10 V to 2 V in steps of +1 V. The MIS-HEMTs on all the epi-structures exhibited kinkfree characteristics. MIS-HEMTs on the SiC substrate with a thick, doped buffer showed the highest maximum current $I_{\rm D,max}$ of 1007 mA/mm and lowest on-resistance ($R_{\rm on}$) of 5.51 Ω ·mm. The output characteristic of the devices with a novel non-buffer epi-structure was almost the same as that with the conventional structure, while the $I_{\rm D,max}$ and $R_{\rm on}$ of the MIS-HEMTs on the Si substrate were only 760 mA/mm and 6.46 Ω ·mm, respectively.

Pulsed-*I-V* measurements under slow switching were performed to characterize the degree of current collapse of the fabricated MIS-HEMTs. The dynamic characteristics were investigated using the Keithley 4200A PMU module with the drain quiescent bias voltage V_{DSQ} . The period of the square wave pulse signal was 1 ms, with a width of 10 µs, duty cycle of 1%, and time of pulse rising and falling of 500 ns. The device was synchronously switched from a quiescent bias of $V_{\text{GSQ}} = 0$ V, $V_{\text{DSQ}} = 0/10/20/30/40$ V to a measurement state of $V_{\text{GS}} = 2$ V and V_{DS} from 0 V to 10 V.

Figure 10 illustrates the current collapse phenomenon of the MIS-HEMTs on the different epi-structures under increasing V_{DSQ} . When $V_{\text{DSQ}} = 40$ V, the current collapse of the conventional epitaxial structure on the Si substrate was 29%, which was the most serious among all the structures. For the two types of devices on the SiC substrate, no significant current collapse was observed when V_{DSQ} was within 20 V, indicating that the "virtual gate" effect did not occur at a weak field. When the V_{DSQ} was up to 40 V, the degree of current collapse on the novel non-buffer epi-structure was only 7%, while approximately 15% of current decrement occurred on the conventional structure. The non-buffer epi-structure on the SiC substrate had the best dynamic performance, which was mainly due to the following reasons: First, the novel epi-structure had a better crystalline quality and surface morphology, lower dislocation density, and resulted in fewer surface and body defects. Second, the novel structure offered better 2DEG confinement, which effectively reduced the probability of hot electron tunneling. Third, there were no deep-level traps caused by the doped thick buffer; thus, there was no contribution to current collapse.



Figure 10. Pulsed-*I*-*V* measurements performed at different V_{DSQ} MIS-HEMTs on (**a**) Epi A, (**b**) Epi B, and (**c**) Epi C.

4. Conclusions

In this study, a novel AlGaN/GaN epitaxial growth without a conventional buffer layer on a SiC substrate was systematically investigated. The ultra-thin 380 nm Al-GaN/GaN/AlN had better crystalline quality, as characterized by AFM, XRD, and Hall measurements. Carrier distribution at high temperatures extracted from the *C-V* curves of Schottky diodes indicated that the non-buffer epi-structure could be favorable for improving 2DEG confinement. MIS-HEMTs on the non-buffer epi-structure almost exhibited the same performance in DC characteristics as the conventional epi-structure on the SiC substrates, which were much better than the current commercial structure on the Si substrate. The pulsed-*I-V* measurements demonstrated the advantage of the non-buffer design, which showed the lowest current collapse compared to the conventional structures on both the SiC and Si substrates. This was attributed to the improved crystalline quality, enhanced electron confinement, and significantly reduced deep-level traps induced by the thick buffer doping. These characteristics made the non-buffer epi-structure on the SiC substrate an excellent candidate in AlGaN/GaN power HEMTs applications.

Author Contributions: Conceptualization, P.Z. and L.W.; methodology, P.Z. and L.W.; validation, Z.H., K.Z., Q.W. and M.P.; formal analysis, L.W. and K.Z.; investigation, P.Z. and L.W.; resources, S.X. and C.W. (Chunlei Wu); data curation, P.Z. and L.W.; writing—original draft preparation, P.Z.; writing—review and editing, M.X. and C.W. (Chen Wang); visualization, Y.Y., X.X., X.H. and H.H.; supervision, M.X., C.W. (Chen Wang) and D.W.Z.; project administration, M.X. and C.W. (Chen Wang); funding acquisition, M.X., C.W. (Chen Wang) and D.W.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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