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A High-Precision Current-Mode Bandgap Reference with Nonlinear Temperature Compensation

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Abstract: A high-precision current-mode bandgap reference (BGR) circuit with a high-order temperature compensation is presented in this paper. In order to achieve a high-precision BGR circuit, the equation of the nonlinear current has been modified and the high-order term of the current flowing into the nonlinear compensation bipolar junction transistor (NLCBJT) is compensated further. According to the modified equation, two solutions are designed to improve the output accuracy of BGR circuits. The first solution is to divide the NLCBJT branch into two branches to reduce the coefficient of the nonlinear temperature compensation current. The second solution is to inject the nonlinear current into the two branches based on the first one to further eliminate the temperature coefficient (TC) of the current flowing into the NLCBJT. The proposed BGR circuit has been designed using the Semiconductor Manufacturing International Corporation (SMIC) 55 nm CMOS process. The simulation results show that the variations in currents flowing into NLCBJTs improved from 148.41 nA to 69.35 nA and 7.4 nA, respectively, the TC of the output reference current of the proposed circuit is approximately 3.78 ppm/°C at a temperature range of −50 °C to 120 °C with a supply voltage of 3.3 V, the quiescent current consumption of the entire BGR circuit is 42.13 µA, and the size of the BGR layout is 0.044 mm^2, leading to the development of a high-precision BGR circuit.

Keywords: bandgap current reference; high-order curvature-compensated technique; temperature coefficient (TC); current-mode reference

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1. Introduction

Bandgap reference (BGR) circuits are critical modules in most integrated circuit systems and are widely used in analog circuits, digital circuits, and mixed-signal circuits, such as memory circuits, A/D converters, and low dropout linear regulators. BGR circuits provide temperature-independent voltages or currents for the system-on-a-chip (SoC), and their performance determines the quality of the entire SoC. With the development of the CMOS process, the feature size of integrated circuits continues to decrease, and the operation voltage of the electronic system is becoming increasingly lower. Low-voltage and high-precision BGR circuits have received widespread attention.

The output voltage of conventional voltage-mode BGR circuits with first-order temperature compensation is 1.25 V approximately, which can achieve a TC of about a few tens of ppm/°C. In order to achieve more accurate reference voltages, higher-order temperature-compensated techniques are required for BGR circuits. Rincon-Mora et al. [1] adjusted the reference voltage by optimizing the temperature component with the trimming process and achieved high accuracy of the output voltage. Leung et al. [2] proposed that the ratio of resistors with the same type and size is independent of temperature, which can be used to reduce temperature drift. Ker et al. [3] used a subtraction circuit to cancel the convex curve or the concave curve of the output reference current of two BGR circuits. Exponential temperature compensation [4], quadratic temperature compensation [5], and third-order

compensation [6] were also used to cancel the high-order terms of the emitter-base voltage V_{EB}, eliminate the temperature drift, and obtain a reference voltage with a very small TC.

In modern CMOS technology, the operation voltage of CMOS devices is lower than 1.2 V, so a reference voltage should be lower than 1.2 V. Banba et al. [7] proposed a sub-1V BGR circuit in which the current-mode technique is adopted to scale down the output reference voltage, and a variety of high-precision BGR circuits are developed.

Compared to the first-order temperature compensation in [7], Malcovati [8] introduced a high-order temperature compensation, which is based on the theory that the current in the nonlinear compensation bipolar junction transistor (NLCBJT) is temperature-independent. However, high-order temperature residue terms still exist in the NLCBJT currents in this circuit, which require further rejection or elimination.

In this paper, the accuracy of the BGR is further improved on the basis of [8]. The rest of this paper is organized as follows: Section 2 describes the operation principle of a conventional current-mode BGR circuit; Section 3 describes the two proposed solutions for nonlinear compensation BGR circuits; Section 4 presents the simulation results that verify the accuracy of the proposed high-order terms compensated circuit; and the conclusions are provided in Section 5.

2. Principle of Conventional Current-Mode BGR Circuits

The low-voltage BGR circuit proposed by Banba et al. [7] is a current-mode BGR circuit whose output reference current I_{REF} is realized by the sum of two currents. One is complementary to the absolute temperature I_{CTAT}, and the other is proportional to the absolute temperature I_{PTAT}. First, a temperature-independent reference current was generated.

As presented in Figure 1, due to the effect of negative feedback, the relationship $V_A = V_B = V_{EB1}$ and a PTAT current I_{PTAT} proportional to V_T is achieved. With additional equal resistors R_1 and R_2 ($R_1 = R_2 = R_{1,2}$), the BGR circuit achieves a CTAT current I_{CTAT} proportional to V_{EB}. The currents I_1 and I_2 are the sum of the currents I_{PTAT} and I_{CTAT}, flowing through the current mirror that consists of the transistors M_0, M_1, and M_2 with the same aspect ratio. The currents can be expressed as follows:

$$I_1 = I_2 = I_{REF} = \frac{v_T \ln N}{R_0} + \frac{V_{EB1}}{R_{1,2}} = \frac{kT}{qR_0} \ln N + \frac{V_{EB1}}{R_{1,2}} \quad (1)$$

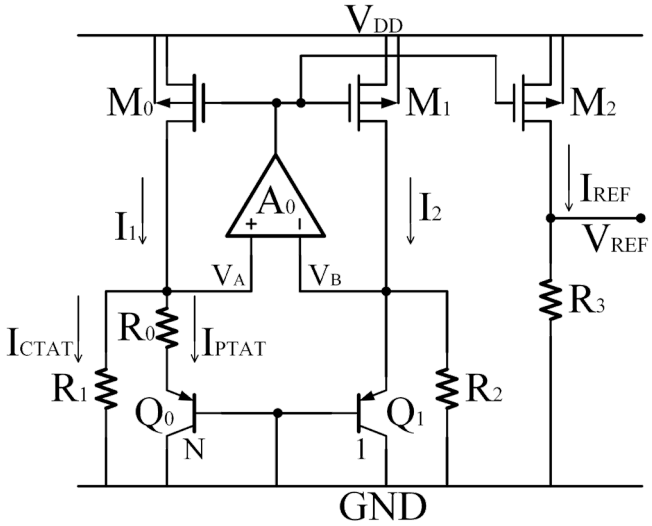

Figure 1. The BGR circuit proposed by Banba et al. [7].

Then, a low reference voltage V_{REF} can be generated and expressed as

$$V_{REF} = I_{REF}R_3 = I_1R_3 = I_2R_3 = \left(\frac{\Delta V_{EB}}{R_0} + \frac{V_{EB1}}{R_{1,2}}\right)R_3 \quad (2)$$

However, the current-mode BGR circuit shown in Figure 1 still belongs to first-order temperature compensation. A large high-order temperature current flows into the emitter of Q_1, which affects the accuracy of V_{REF}. According to the study by Tsividis et al. [9], an accurate analysis of the temperature effects on V_{EB}-T characteristics can be expressed as

$$V_{EB}(T) = V_{G0}(T_r) + \left(\frac{T}{T_r}\right)[V_{EB}(T_r) - V_{G0}(T_r)] - (n-\delta)\frac{kT}{q}ln\left(\frac{T}{T_r}\right) \quad (3)$$

where $V_{G0}(T_r)$ is the bandgap voltage of silicon at the reference temperature T_r, n is a temperature-independent and process-dependent constant around 4, and δ is a factor of the temperature dependent on the collector current, which is equal to 1 if the current in the BJT is PTAT and becomes 0 when the current is temperature-independent. V_T is the thermal voltage, k is Boltzmann's constant, and q is the electric charge.

In Equation (3), the second item has a first-order TC, whereas the third item is a high-order temperature nonlinear term that should be rejected or eliminated to achieve a high-precision BGR.

On the basis of [7], Malcovati et al. [8] presented a high-precision BGR circuit with a low supply voltage, where nonlinear currents were generated to compensate for the high-order errors, as shown in Figure 2.

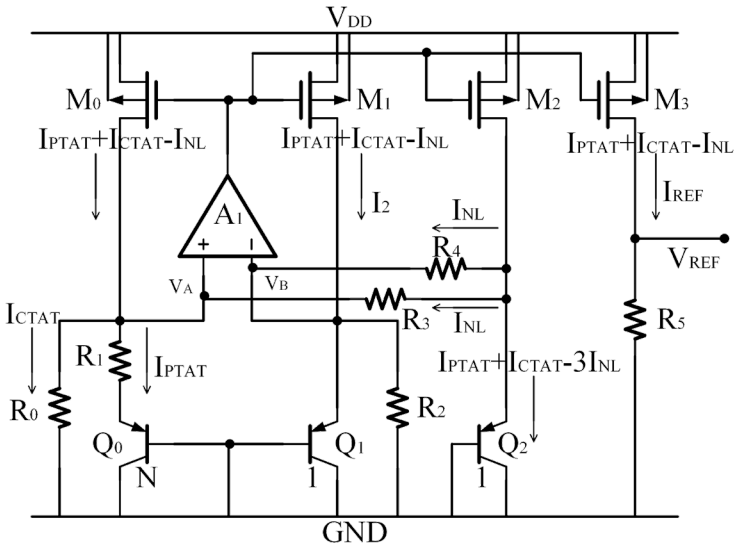

Figure 2. The high-accuracy BGR circuit proposed by Malcovati [8].

The currents flowing into Q_0 and Q_1 are proportional to the absolute temperature so that the parameter δ in the expression of V_{EB} is equal to 1. Since the currents flowing into Q_2 are temperature-independent, the parameter δ is equal to 0 [8].

The V_{EB} of Q_0 and Q_1 can be expressed as

$$V_{EB,Q0,1} = V_{G0}\left(1 - \frac{T}{T_r}\right) + V_{EB0}\left(\frac{T}{T_r}\right) - (n-1)\frac{kT}{q}ln\left(\frac{T}{T_r}\right) \quad (4)$$

The current in M_0 is

$$I_{REF} = I_{PTAT} + I_{CTAT} - I_{NL} \quad (5)$$

which is the current with a low TC after high-order temperature nonlinear compensation. The current is copied by M_2 and injected into a diode connected to NLCBJT Q_2, which is expressed by

$$I_{Q2} = I_{PTAT} + I_{CTAT} - 3I_{NL} \tag{6}$$

Because the nonlinear current I_{NL} is very small, its TC can be ignored [8]. Then, a V_{EB} with $\delta = 0$ is produced across Q_2, which can be expressed as

$$V_{EB,Q2} = V_{G0,Q2}\left(1 - \frac{T}{T_r}\right) + V_{EB0,Q2}\left(\frac{T}{T_r}\right) - n\frac{kT}{q}ln\left(\frac{T}{T_r}\right) \tag{7}$$

Equation (7) is subtracted from (4) and leads to a nonlinear voltage V_{NL}, which is expressed as

$$V_{NL} = V_{EB,Q2} - V_{EB,Q0,1} = -\frac{kT}{q}ln\left(\frac{T}{T_r}\right) + \Delta V_{EB,Q2,Q1}\left(\frac{T}{T_r}\right) \tag{8}$$

where the first term in the equation is the nonlinear term of temperature, and the second term is the error of the linear term of the V_{EB} of two BJT Q_1 and Q_2 with the same geometry; however, the emitter currents $I_{E,Q1}$ and $I_{E,Q2}$ are not equal, so the error of the linear term is not equal to zero. Equation (8) is then corrected.

The values of resistors R_3 and R_4 are equal, and the I_{NL}s generated on them are equal. Then, the current of $I_{PTAT} + I_{CTAT} - I_{NL}$ follows M_4 and R_5, as shown in Figure 3.

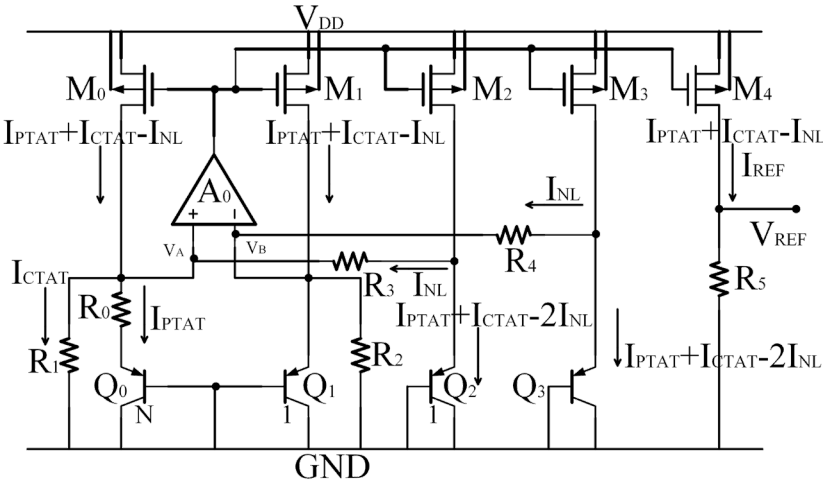

Figure 3. A solution for reducing the TC of current in NLCBJT.

The output reference voltage V_{REF} becomes

$$V_{REF} = V_T\frac{R_5 ln(N)}{R_0} + V_{EB,Q0,1}\frac{R_5}{R_{1,2}} + V_{NL}\frac{R_5}{R_{3,4}} = \frac{R_5}{R_{1,2}}\left(\frac{R_{1,2}ln(N)}{R_0}V_T + V_{EB,Q0,1} - \frac{R_{1,2}}{R_{3,4}}V_{NL}\right) \tag{9}$$

where the third term is the nonlinear part, and it can be used to effectively compensate for the nonlinear item of the second term, $V_{EB,Q0,1}$. By substituting (4) into (9) and setting n − 1 equal to $\frac{R_{1,2}}{R_{3,4}}$, the nonlinear temperature term in V_{REF} can be eliminated, and a high-precision reference voltage can be achieved.

This BGR circuit achieves an output reference voltage of 0.536 V and obtains a TC of 7.5 ppm/K over a wide temperature range of 80 °C (from 0 °C to 80 °C). Compared to the BGR circuit without the curvature correction technique, the BGR circuit is improved by about three times.

However, in this structure, the expression for the emitter current of Q_2 is actually

$$I_{E,Q2} = I_{PTAT} + I_{CTAT} - 3I_{NL} \tag{10}$$

where there are excess high-order temperature terms with a certain impact on I_{REF}. The coefficient of this current can be further reduced, and a more accurate I_{REF} can be achieved.

3. Proposed High-Precision Current-Mode BGR Circuit

In order to completely eliminate high-order temperature terms in the current flowing through Q_2, a novel high-precision compensation BGR structure is proposed in this paper.

On the basis of the conventional curvature-compensated BGR circuit, the transistor M_3 is first added to mirror the current in M_0 flowing into BJT Q_3 and then form a new branch, which can share the nonlinear current flowing into the same BJT, as shown in Figure 3.

At this time, the current flowing through Q_2 and Q_3 is

$$I_{E,Q2,3} = I_{PTAT} + I_{CTAT} - 2I_{NL} \tag{11}$$

The TC of the nonlinear compensation BJT current is reduced, which makes the output reference current more accurate.

In order to further eliminate high-order temperature terms, a BGR circuit with high-order temperature compensation was designed, as shown in Figure 4.

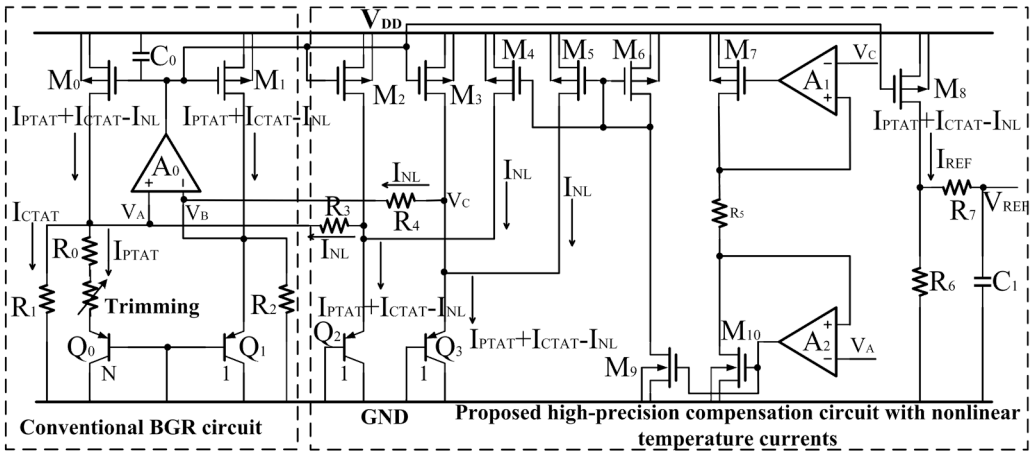

Figure 4. Proposed high-precision current-mode BGR circuit.

Let R_5 be equal to R_3 and R_4 ($R_3 = R_4 = R_5$). Based on the characteristics of the operational amplifier (OPAMP) A_1 and A_2, two branches, each with a nonlinear current similar to I_{NL}, are formed and injected into Q_2 and Q_3 to offset the excess high-order temperature terms.

The circuit of the OPAMP A_0, A_1, and A_2 is provided in Figure 5, where the input stage of this circuit mainly consists of a PMOS transistor differential pair M_{21} and M_{22} and an NMOS transistor differential pair M_{23} and M_{24} placed in parallel as a rail-to-rail differential input stage, whose range of input common-mode voltage can be from ground to V_{DD}. The dominant pole of the circuit is located at the output port. The product of the equivalent impedance and capacitance is large, so the position of the pole is close to the DC point. And the non-dominant pole of the circuit is located at the node between the drain of M_{32} and the source of M_{33}, and the other pole is located between the source of M_{34} and the drain of M_{35}. The output impedance and parasitic capacitance of these two nodes are both small so that their poles are far from the dominant pole. So this circuit can be regarded as only one pole approximately and is kept stable through simple compensation.

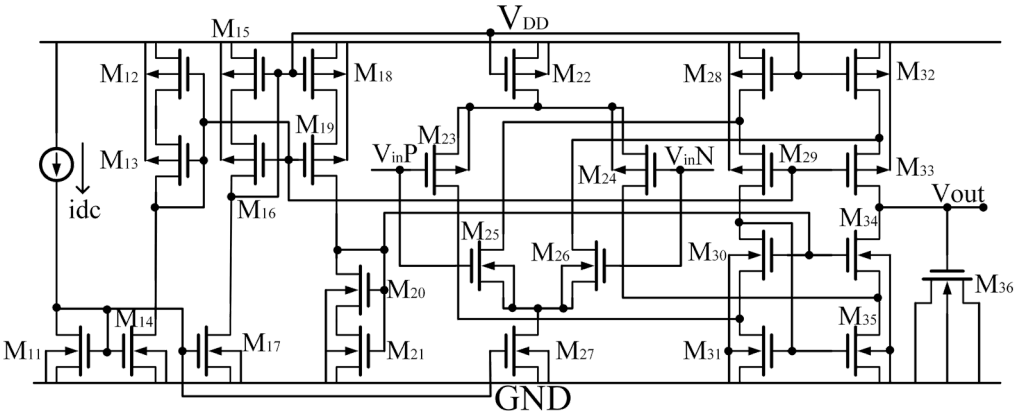

Figure 5. The OPAMP A_0, A_1, and A_2 of the circuit shown in Figure 4.

Finally, the current is

$$I_{E,Q2,3} = I_{PTAT} + I_{CTAT} - I_{NL} \tag{12}$$

This formation is theoretically completely independent of temperature.

The design details of the proposed high-precision current-mode BGR and OPAMP circuits A_0, A_1, and A_2 are provided in Table 1.

Table 1. Component sizes used in the proposed BGR circuit.

Component	Parameter
M_0, M_1, M_2, M_3 and M_8	W = 9 µm, L = 6 µm
M_4, M_5 and M_6	W = 6 µm, L = 6 µm
M_7	W = 3 µm, L = 6 µm
M_9 and M_{10}	W = 3 µm, L = 8 µm
M_{11}, M_{14} and M_{17}	W = 1 µm, L = 12 µm
M_{12}	W = 1.8 µm, L = 6 µm
M_{13}, M_{16}, M_{19}, M_{29} and M_{33}	W = 1.5 µm, L = 6 µm
M_{15} and M_{18}	W = 1.5 µm, L = 12 µm
M_{22}, M_{28} and M_{32}	W = 1.5 µm, L = 12 µm, m = 2
M_{23} and M_{24}	W = 3 µm, L = 6 µm, m = 4
M_{25} and M_{26}	W = 5 µm, L = 2.6 µm, m = 4
M_{20}	W = 1.5 µm, L = 8 µm
M_{21}, M_{30} and M_{34}	W = 1 µm, L = 12 µm
M_{27}, M_{31} and M_{35}	W = 1 µm, L = 12 µm, m = 2
Q_0	8 × (5.6 µm × 5.6 µm)
Q_1, Q_2 and Q_3	1 × (5.6 µm × 5.6 µm)
R_0	31.47 kΩ
R_1 and R_2	249.52 kΩ
R_3, R_4 and R_5	62.38 kΩ
R_6	160 kΩ

With the same power supply voltage, the same component sizes, and the same temperature range from −50 °C to 120 °C, the current $I_{PTAT} + I_{CTAT} - 3I_{NL}$ flowing into Q_2 in Figure 2, the current $I_{PTAT} + I_{CTAT} - 2I_{NL}$ flowing into Q_2 or Q_3 in Figure 3, and the current

$I_{PTAT} + I_{CTAT} - I_{NL}$ flowing into Q_2 or Q_3 in Figure 4 simulated in the SMIC 55 nm CMOS process are shown in Figure 6.

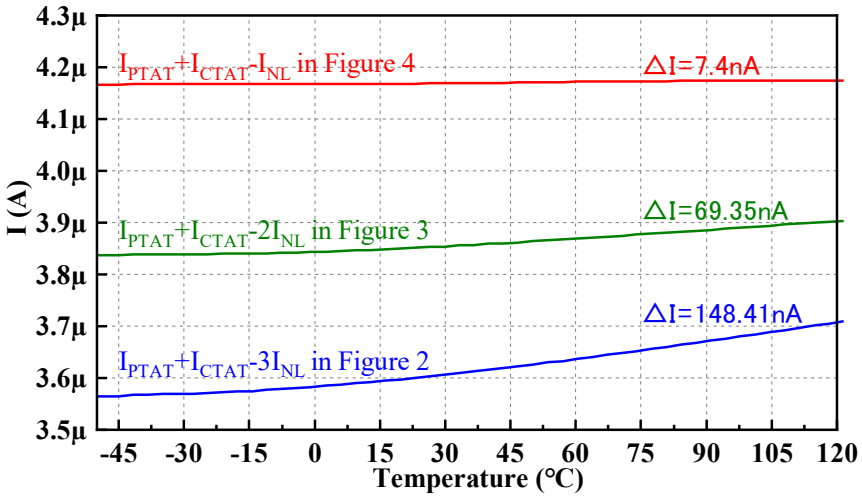

Figure 6. Currents flowing into Q_2 or Q_3 of the structures shown in Figures 2–4.

Compared to Figures 2 and 3, the current curve in Figure 4 is the most stable, and the variation is the smallest. In other words, the temperature stability is the best.

And the output reference currents I_{REF} of the structures in Figures 2–4 simulated in the SMIC 55 nm CMOS process are shown in Figure 7.

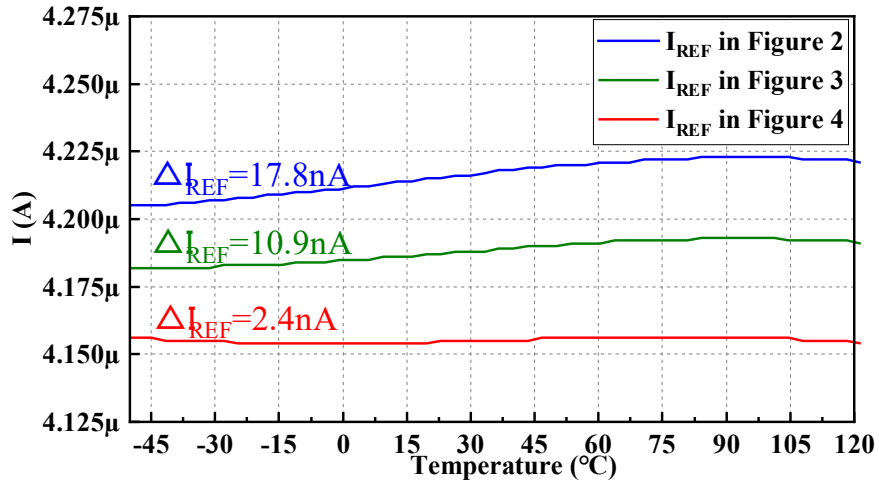

Figure 7. Measured I_{REF} of the structures shown in Figures 2–4.

The I_{REF} of the circuit in Figure 2 varies from the minimum of 4.2049 µA to the maximum of 4.2227 µA with a change of 17.8 nA, the I_{REF} in Figure 3 varies from the minimum of 4.1817 µA to the maximum of 4.1926 µA with a change of 10.9 nA, and the I_{REF} in Figure 4 varies from the minimum of 4.1539 µA to the maximum of 4.1563 µA with a change of 2.4 nA. It can be seen that the I_{REF} of the proposed high-precision current-mode BGR circuit is more stable significantly.

4. Simulation Results

The proposed current-mode BGR circuit with a high-order temperature compensation was designed using the SMIC 55 nm CMOS process. The size of the layout of the proposed circuit including dummies turned out to be 300.43 µm × 148.67 µm, which is illustrated in Figure 8.

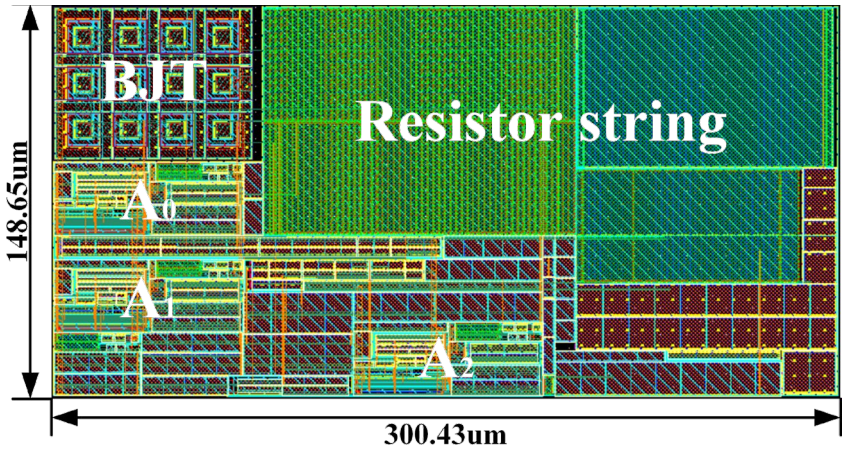

Figure 8. The layout of the proposed high-precision current-mode BGR circuit.

A. The output reference current

With a supply voltage of 3.3 V, the I_{REF} of the proposed circuit measured from −50 °C to 120 °C is presented in Figure 9.

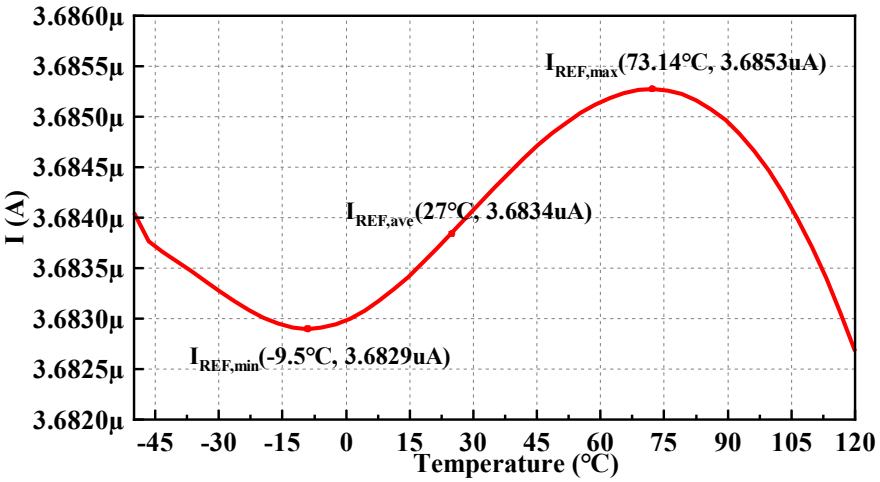

Figure 9. I_{REF} with temperature sweep at the process corner tt.

The equation of TC can be expressed as

$$TC = \frac{V_{REF,max} - V_{REF,min}}{V_{REF,ave} \times (T_{max} - T_{min})} \times 10^6 \quad (13)$$

In the current-mode BGR circuit, the V_{REF} in the above equation should be replaced by I_{REF}, while the rest remains unchanged. I_{REF} over the whole temperature range is about 2.4 nA, varying from 3.6829 µA to 3.6853 µA. So, the typical TC can be calculated as 3.78 ppm/°C.

B. Monte Carlo simulation

The Monte Carlo simulation is conducted to assess the circuit stability due to the influence of the process and mismatched variations. Three hundred iterations of the generated I_{REF} are shown in Figure 10.

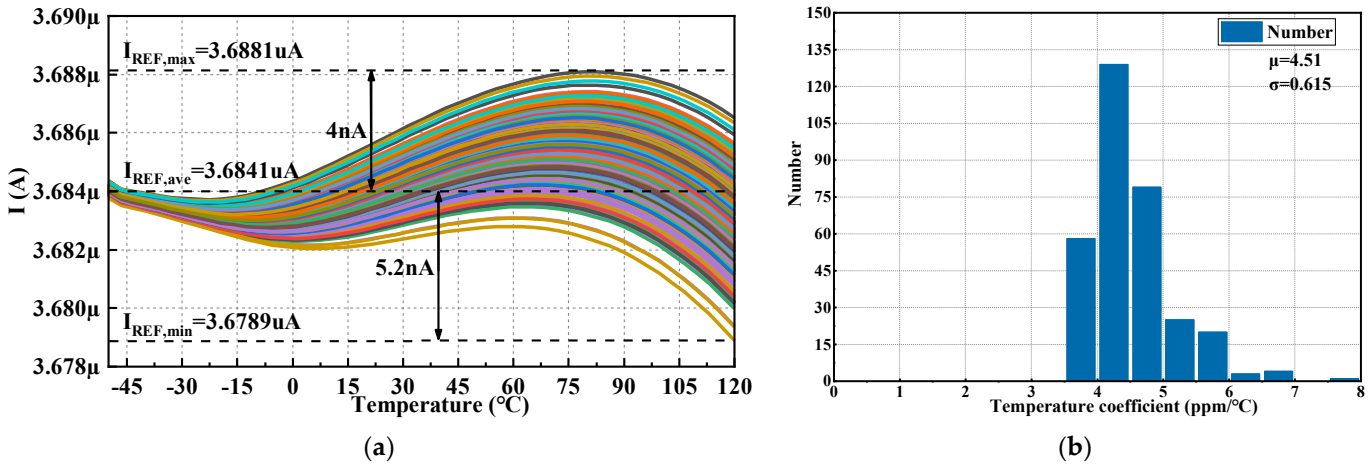

Figure 10. Monte Carlo simulation (300 iterations) for mismatch and process variations: (**a**) I_{REF} across temperature; (**b**) Temperature coefficient.

The simulation results show that I_{REF} varied from 3.6789 µA to 3.6881 µA under the worst-case scenario in Figure 10a, whose TC is about 7.64 ppm/°C. And it can be calculated that the mean value µ of TC is 4.51 ppm/°C, and the mean square error σ is 0.615 ppm/°C in Figure 10b.

The Monte Carlo simulation covers over 95% of the process corners and mismatches, which ensures a certain qualification rate for the product. However, the process corners have significant process variations under extreme conditions and require to be trimmed. Under the process corner of ss, there is a maximum deviation of 6 nA from the typical value in this paper. Due to the accuracy requirements of the BGR circuit, trims need to be made. Three-bit trimming is adopted, which means that there are eight trimming states. Three states greater than the typical value are set, and each state can be stepped by 3 nA, so a total of 9 nA can be stepped. Four trimming states below the typical value are set, and each state can be stepped by 3 nA, and a total of 12 nA can be stepped. Because trimming is an engineering implementation process, this paper does not provide detailed circuit implementation steps.

Figure 11 shows the simulation result of the output I_{REF} versus the temperature of the process corners, including ff, fs, sf, and ss, where the process corners of ss and fs are trimmed in one step to obtain better results, and those of ff and sf are maintained in the set state of tt without any trimming. At the worst process corner ff, the TC is about 7.97 ppm/°C.

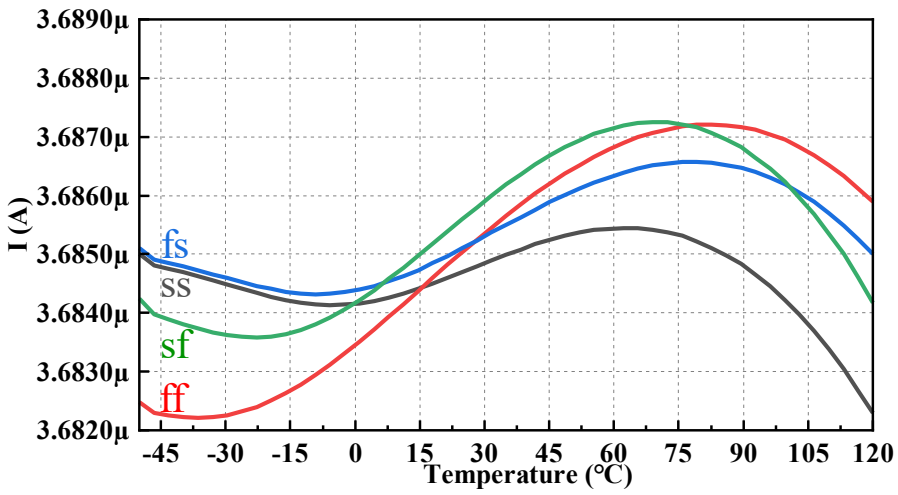

Figure 11. I_{REF} with temperature sweep of process corners including ff, fs, sf, and ss.

C. Stability

Figure 12 shows the AC analysis results of the BGR for the gain and phase frequency response of the process corners, including tt, ff, fs, sf, and ss of the proposed circuit.

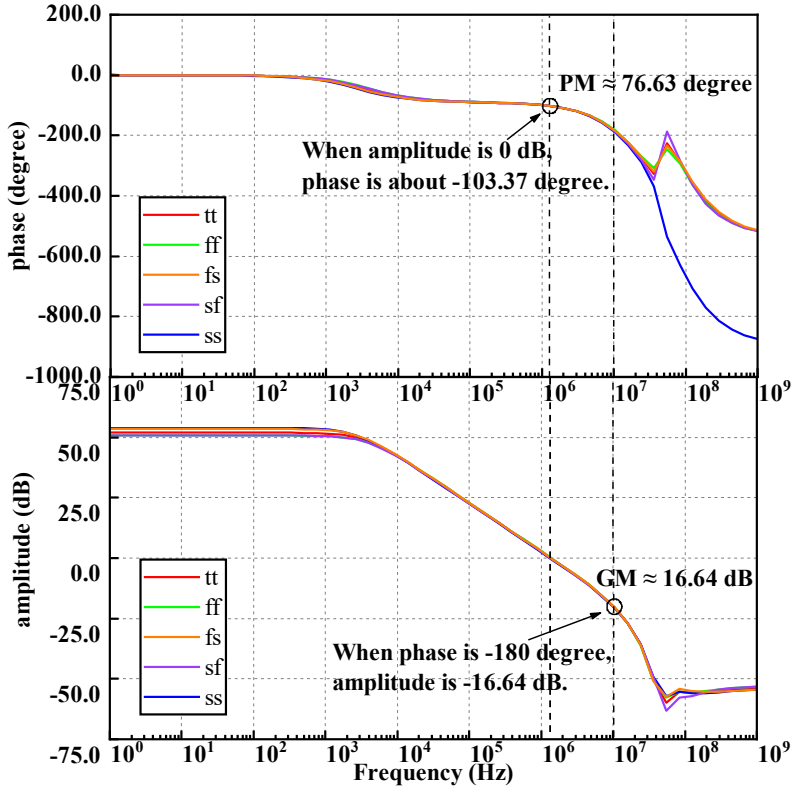

Figure 12. The gain and phase frequency response of every process corner.

It can be observed that the phase margin is better than 76.63 degrees, and the gain margin is about 16.64 dB. When the gain is 0 dB, the phase margin is much greater than 60 degrees, which is very stable.

D. Transient response

Figure 13 illustrates the start-up process of the proposed circuit with a supply voltage V_{DD} step from 0 V to 3.3 V at an edge time of 1 ms, and when I_{REF} flows through a high-precision resistor with a temperature compensation of 160 kΩ, the proposed BGR circuit takes 0.14 ms to reach the normal operating state.

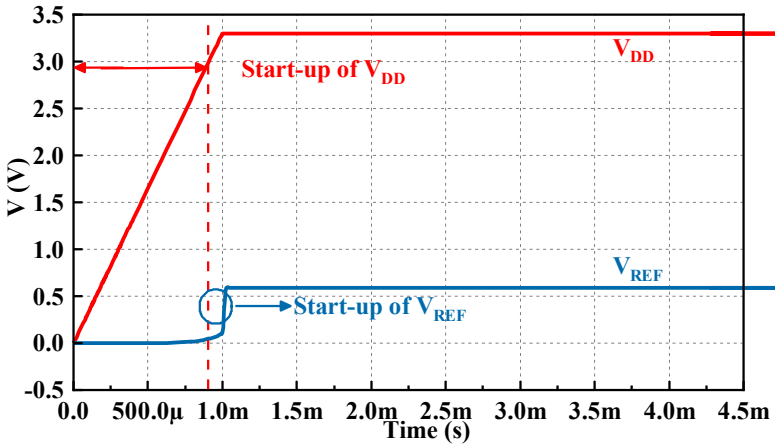

Figure 13. The transient response of the start−up process.

E. Comparison between the simulated characteristics of the proposed design and other works

The performance of the proposed BGR circuit is compared to that of other previous BGR circuits [10–14], as shown in Table 2.

Table 2. Performance summary and comparisons with other previous studies.

Parameters	This Work	Ref. [10]	Ref. [11]	Ref. [12]	Ref. [13]	Ref. [14]	Ref. [15]
Year	2023	2021	2019	2018	2012	2012	2010
Process	CMOS 55 nm	CMOS 65 nm	CMOS 0.18 µm	CMOS 0.5 µm	BiCMOS 0.5 µm	CMOS 0.35 µm	CMOS 0.5 µm
Supply voltage (V)	3.3	1.0–1.4	3.5–5	2.1–5	3.6	2.5	3.6
Layout area (mm^2)	0.044	(*)	0.2225	0.053	0.04	0.102	0.1
Temp range (°C)	−50 to 120	−40 to 100	−40 to 130	−5 to 125	−40 to 100	−15 to 150	−40 to 120
Best TC (ppm/°C)	3.78	5	4.6	3.98	5	3.9	11.8
Trimming	No	No	No	Yes	Yes	Yes	Yes
I_Q (µA)	42.13	5.2	108	38	25	38	18
PSR@27 °C	−63.1 dB @100 Hz	−28.8 dB @10 kHz	−92 dB @100 Hz	−84 dB @100 Hz	−70 dB @10 kHz	(*)	−31.8 dB @10 Hz
FOM	67.36	155.08	31.48	72.2	78.4	(*)	24

(*) Not listed.

It can be observed from Table 2 that due to more accurate high-order compensation, the TC of the proposed structure is superior to that of previous works over a wider range of temperatures, and there are also certain comprehensive advantages in layout area, current consumption, and PSR.

In order to evaluate the overall performance of the BGR circuits, an evaluation parameter figure-of-merit (*FOM*) defined in this paper can be expressed as

$$FOM = \frac{|PSR| \times Temp\ range}{Best\ TC \times I_Q} \tag{14}$$

Because the layout area is related to the process, for the purpose of a fair comparison, the parameter of the layout area is not used in *FOM*, which only uses the temperature range, best *TC*, quiescent current, and *PSR*. It can be seen from the results that the value of *FOM* in this paper is much higher than that in [11,15], almost similar to that in [12,13], but lower than that in [10]. However, the *FOM* of [10] is only because of the excellent parameter of I_Q, while the rest of the performance is ordinary. The most important parameter of the BGR circuit is the temperature coefficient, which is best identified in this paper.

F. Post-layout simulation

The results of the post-layout simulations are shown in Table 3.

Table 3. Post layout simulations of this work.

Specification	Parameter
Process	CMOS 55 nm
Supply voltage (V)	3.3
Temp range (°C)	−50 to 120
TC (ppm/°C)	6.02
Phase margin (degree)	63.5
I_Q (μA)	46.8
PSR (dB)	53.6 dB@DC

5. Conclusions

In this study, the equation of the nonlinear current was modified, the high-order term of the current flowing into the NLCBJT was compensated further, and a high-precision current-mode BGR circuit with a high-order temperature compensation was designed and simulated using Cadence SPECTRE with a SMIC CMOS 55 nm process. The simulation results verify that the output reference current has good temperature independence (TC ≈ 3.78 ppm/°C) with a supply voltage of 3.3 V, a better layout area, and power supply rejection ability (PSR ≈ −63.1 dB at 100 frequency). These results display an effective enhancement in the performance of the BGR circuit.

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