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A 0.6 V_{IN} 100 mV Dropout Capacitor-Less LDO with 220 nA I_Q for Energy Harvesting System

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Abstract: A fully integrated and high-efficiency low-dropout regulator (LDO) with 100 mV dropout voltage and nA-level quiescent current for energy harvesting has been proposed and simulated in the 180 nm CMOS process in this paper. A bulk modulation without an extra amplifier is proposed, which decreases the threshold voltage, lowering the dropout voltage and supply voltage to 100 mV and 0.6 V, respectively. To ensure stability and realize low current consumption, adaptive power transistors are proposed to enable system tropology to alter between 2-stage and 3-stage. In addition, an adaptive bias with bounds is utilized in an attempt to improve the transient response. Simulation results demonstrate that the quiescent current is as low as 220 nA and the current efficiency reaches 99.958% in the full load condition, load regulation is 0.0059 mV/mA, line regulation is 0.4879 mV/V, and the optimal PSR is −51 dB.

Keywords: low-dropout regulator; ultra-low-input voltage; high power efficiency; bulk modulation; energy harvesting

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1. Introduction

Energy harvesting (EH) technology converts weak energy harvested from the environment into electricity [1–3]. EH has been used in many fields, such as the Internet of Things (IoT), wearable devices, and wireless sensors [4–6]. The output voltage collected from energy harvesting is unstable. Therefore, the low-dropout regulators (LDOs) are used to provide a stable power supply for the loads, as they have the advantages of uncomplexity, a low cost, and being noise-immune.

A typical EH system is depicted in Figure 1. Considering the weakness of the energy source and low collection efficiency, energy collection suffers from a low supply voltage and high power consumption [7–9]. Consequently, new challenges and requirements are set forth for the supply voltage and power conversion efficiency of LDO.

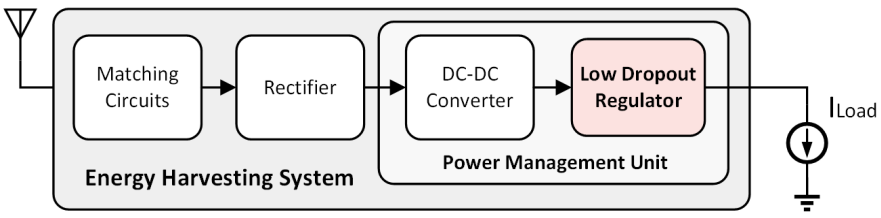

Figure 1. A typical EH system.

For the purpose of improving the integration and reducing the cost, [10–13] proposed the output-capacitor-less (OCL) LDOs consuming µA-level static currents. However, low-power equipment should consume as little electricity as possible during standby and

operation. To further reduce the current to nA levels, [14] adopts an adaptive bias solution based on the super-source follower (SSF) structure. Nevertheless, the minimum supply voltage is as high as 1.8 V, and struggles to meet the EH requirement. In addition, the large dropout voltage leads to large power loss.

Another approach to improving efficiency is to reduce the dropout voltage [15]. A dropout voltage can be defined as the product of the valid channel resistance of the component and the load current in non-regulatory conditions [16]. In [17], a large and wide ratio power transistor is proposed to reduce the equivalent resistance, but this requires a large area. One method to reduce the threshold voltage is the floating meter [18,19], and the other method is body bias [20–22]. Recent research has shown that the threshold voltage can be reduced using current-driven bulks [23]. Since V_B is less than V_S in the PMOS power transistor, the source-end bipolar crystal pipe can be turned on to reduce the threshold voltage. This extra adaptively biased current-driven loop generates a lot of static current, which cannot meet the low I_Q requirements.

This paper proposes a 100 mV-dropout and high-efficiency OCL-LDO with low supply voltage, which uses bulk modulation and adaptive bias technology with adaptive power transistors (APT). The bulk modulation without using the auxiliary amplifier has significantly reduced the dropout voltage to 100 mV. The adaptive bias can quickly detect the transient jumps to shorten the recovery times and reduce the quiescent current. Through the use of APT, the system is able to switch between 2-stage and 3-stage amplifiers under different load conditions, ensuring its stability in the full load range. Further, APT reduces power consumption by reducing unnecessary current consumption. On the one hand, ultra-low V_{IN} and V_{OUT} are suitable for weak EH systems, since they require a low input voltage and output voltage. On the other hand, by reducing the dropout voltage, high efficiency can be achieved with low power consumption.

In the rest of this paper, the operating principle of the proposed LDO is discussed in Section 2. Sections 3 and 4 describe the circuit implementation and stability analysis, respectively. The simulation results, along with comparisons with the state-of-the-art designs, are reported in Section 5. Finally, conclusions are drawn in Section 6.

2. Operation Principle

2.1. Bulk Modulation without Amplifier

The amount of energy collected by the EH system is extremely small. DC-DC Boost converter only produces a few hundred mV of output voltage, requiring a low V_{IN} in the LDO design. Generally, the V_{IN} can be expressed as:

$$V_{IN} = V_G + |V_{GSP}| \geq V_G + |V_{THP}|, \tag{1}$$

where V_G, V_{GSP}, and V_{THP} are the gate voltage, gate-source voltage, and threshold voltage of the power transistor, respectively. When there is a voltage difference between the bulk and source, V_{TH} decreases with V_{BS} due to the body effect and can be written as:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F| - V_{BS}} - \sqrt{|2\Phi_F|}), \tag{2}$$

where V_{TH0} is the threshold voltage when V_{BS} is zero, γ denotes the bulk-effect coefficient, and Φ_F is the Fermi potential. Generally, γ ranges from 0.3 $V^{1/2}$ to 0.4 $V^{1/2}$. This analysis was simplified by replacing source-bulk voltage V_{SB} with $-V_{BS}$. In the case of $a^2 >> b^2$, taking into account a mathematical formula [24]:

$$\sqrt{a+b} \approx \sqrt{a} + \frac{b}{2\sqrt{a}}. \tag{3}$$

In Equation (2), there is $(2\Phi_F)^2 >> V_{SB}^2$, and substitute them into a and b, and considering the relationship of [25,26]:

$$1 + \frac{\gamma}{2\sqrt{2\Phi_F}} = \eta, \tag{4}$$

where η ranges from 1.2 to 1.3. Part of Equation (2) can be approximately expressed as follows:

$$\gamma\left(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F}\right) \approx \frac{\gamma V_{SB}}{2\sqrt{2\Phi_F}} = (\eta - 1)V_{SB}. \tag{5}$$

Therefore, we can conclude that V_{TH} is linearly related to V_{SB}. Via the body effect approximation, Equation (2) can be simplified as [27]:

$$V_{TH} \approx V_{TH0} + (\eta - 1)V_B. \tag{6}$$

Previously, the bulk of the power transistor was connected to the source to prevent the conduction of the PN junction between the source and the bulk, as shown in Figure 2a. Thus $V_{TH} = V_{TH0}$. The minimum V_{IN} of this kind of LDO is larger than 1 V, which does not meet the criteria for low V_{IN}.

The bulk modulation is proposed to reduce V_{TH} and then V_{IN}, as illustrated in Figure 2b. This system imposes an additional amplifier to generate the bulk voltage V_{BODY}, which increases power consumption.

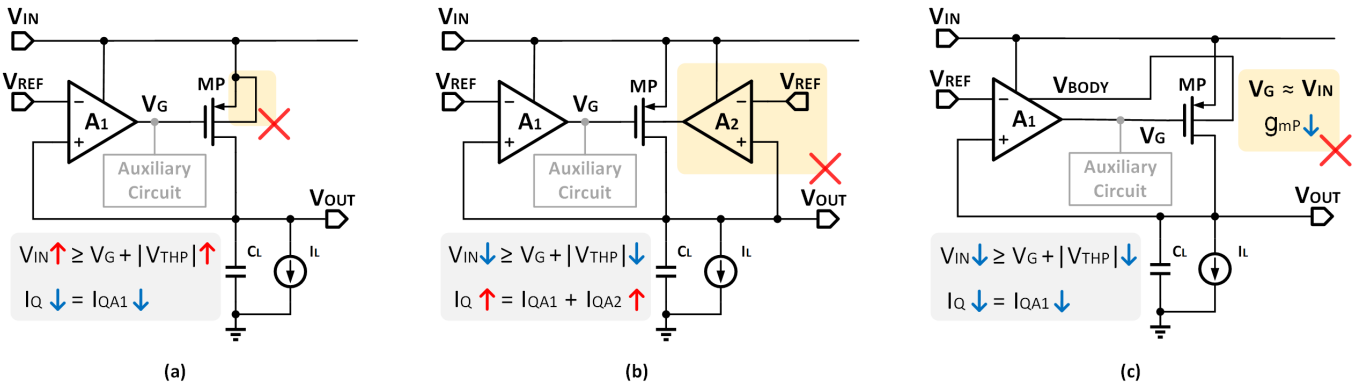

Figure 2. Structures of (**a**) conventional analog LDO, (**b**) bulk modulation with an extra amplifier, (**c**) bulk modulation without an extra amplifier.

Recently, bulk modulation without an extra amplifier was proposed in [28], which can better realize the balance between power consumption and low V_{IN}. Figure 2c shows its structural block diagram. However, the modulated V_G is close to V_{IN}, resulting in low gain and poor performance.

To solve the problems mentioned above, this paper proposes a voltage reuse scheme to generate V_{BODY}. In a typical three-stage structure of OCL-LDO, the buffer is used to increase the drive ability and enhance the load capacity of the power transistor due to the small output resistance. The buffer output is usually only connected to the gate of the power transistor V_G. In this paper, the bulk modulation is simplicity obtained by connecting the buffer output to not only the gate but also the bulk of the power transistor, as shown in Figure 3. V_{IN} in this paper can be expressed as:

$$V_{IN} = V_G + |V_{TH}| = V_{TH0} + V_G + (\eta - 1)V_G = V_{TH0} + \eta V_G. \tag{7}$$

From Equation (7) V_{IN} is determined only by V_{TH0} and V_G. The large value of V_{BODY} is replaced by V_G, resulting in a reduction in V_{IN} to 600 mV. In addition, a gain path is established from the bulk to V_{OUT}, and the body transconductance g_{mb} can enhance

the regulation gain. Consequently, V_{IN} is more effectively reduced without introducing additional power consumption, ensuring that the transistor performs normally in low V_{IN}.

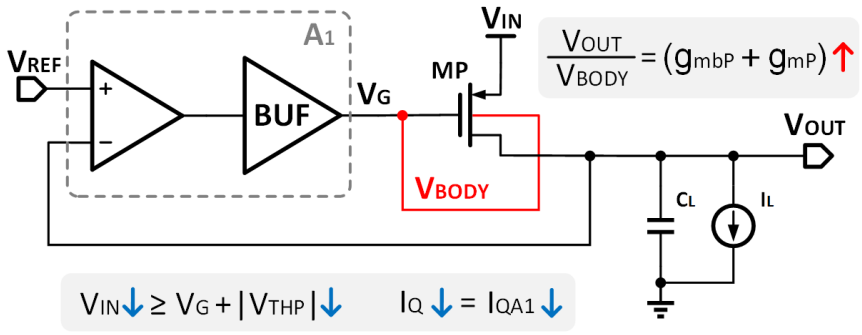

Figure 3. The structural diagram of the V_{BODY} reuse.

It is important to note that a forward-biased PN junction between bulk and source experiences very low voltage. An exceedingly high V_{SB} may lead to the forward breakdown of the MOS transistor, resulting in device damage. Lowering the bulk voltage appropriately, while ensuring that the PN junction does not undergo breakdown, can reduce V_{TH}. To validate the feasibility of the proposed approach, simulations of the circuit were conducted. Figure 4a shows that the value of V_{TH} as V_{IN} varies under different V_{BODY} when adopting the V_{BODY} reuse method. The simulation results show that V_{TH} increases as V_{IN} decreases, while V_{BODY} remains constant. However, V_{TH} can be effectively reduced by decreasing V_{BODY}. In the proposed design, the MOS transistor is protected from forward breakdown since the maximum value of V_{BODY} is 280 mV, which is less than the forward breakdown voltage. Additionally, Figure 4b shows the drain current with and without V_{BODY} reusing. There is evidence that, within a specific range, after adopting the reuse of V_{BODY}, I_Q can be effectively reduced. Therefore, the proposed bulk modulation without an amplifier reduces both V_{IN} and I_Q.

Despite this, bulk modulation also has some disadvantages, such as circuit instability due to the excessive modulation or reverse breakdown of PN junctions caused by a V_{BODY} that is too low. To solve the above problems, APT technology is proposed in the next section.

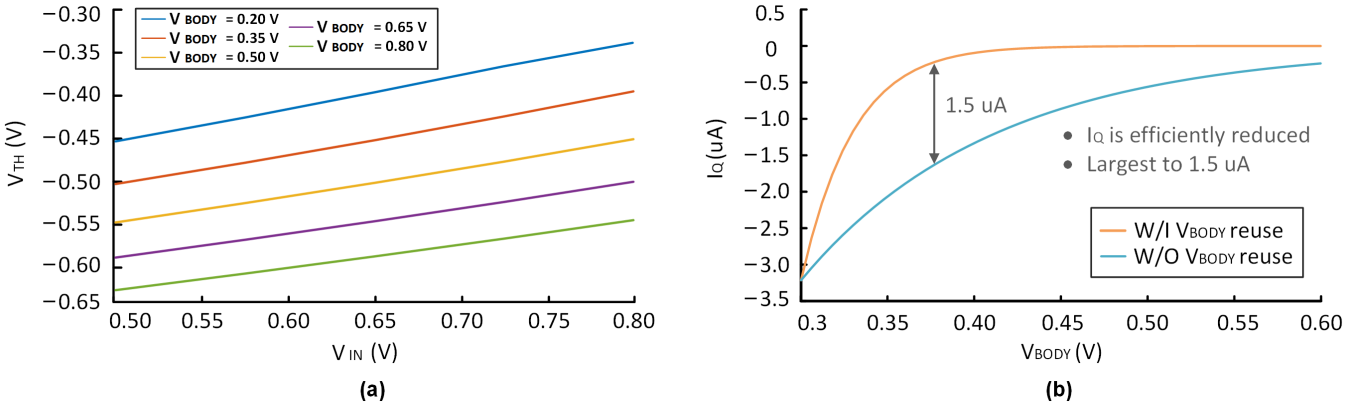

Figure 4. Simulation results of (**a**) the change of V_{TH} with V_{IN}, in the case of different V_{BODY}, (**b**) the I_Q with V_{BODY} reuse and without V_{BODY} reuse.

2.2. Adaptive Power Transistors

The drain current I_D of the power transistor working in the saturation region can be given by:

$$I_D = \frac{1}{2}\mu_P C_{OX}\frac{W}{L}(|V_{GS}| - |V_{TH}|)^2, \quad (8)$$

where μ_P is the mobility of the PMOS channel, C_{OX} is the capacitance of the gate oxide layer, and W/L is the transistor ratio.

As the load current I_{LOAD} gradually increases and V_{GS} increases, so V_G decreases accordingly. When employing V_{BODY} reuse, there is $V_G = V_{BODY}$. Reducing V_{BODY} too much will result in increased V_{BS}, which may lead to the forward breakdown of the PN junction.

As a preventative measure, this paper proposes the APT technology. This is based on the principle that, when the load changes, a feedback signal is used to adjust the use of the auxiliary and main power transistors (MP_1 and MP_2). Meanwhile, bulk modulation performs on MP_1 and MP_2. Specifically, the modulation effect will be enhanced as I_{LOAD} increases. The V_{BODY} reuse scheme being implemented for MP_2 will turn off under light loads, making V_{BODY} close to V_{IN}. The schematic diagram and working process of APT are shown in Figure 5.

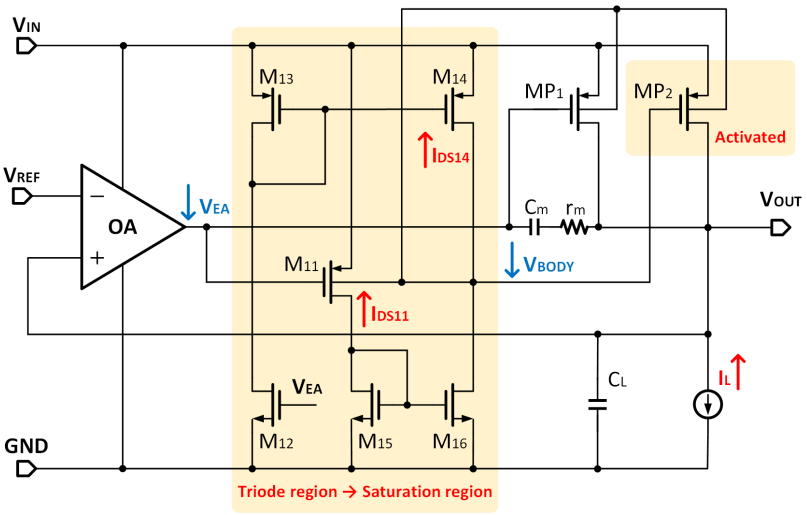

Figure 5. The schematic diagram and working process of APT.

The system works in a twp-stage amplifier topology when the load is light. Due to the second gain stage performing in the triode region, M_{14} pulls the output voltage closer to the supply. Therefore, the V_{GS} of MP_2 is minimal, and MP_2 is turned off. This was obtained by designing the aspect ratio of M_{14} and M_{16}. M_{14} is set to be small enough and M_{16} is set to be large enough; thus, M_{16} works in the saturation region, whereas M_{14} is forced into the deep linear region to sustain equilibrium in the light load. The gate of MP_1 is connected to the output of the first-stage amplifier, V_{EA}. MP_2 is forcibly disabled and all the load current flows through MP_1.

When the load current increases, the I_{DS} of MP_1 increases, as well as its V_{GS}. Therefore, V_{EA} decreases, as well as the V_G of M_{11}, which increases the current of M_{11} and provides a large current to M_{15}, as well as M_{16}. Thus, the drop-down ability of M_{16} becomes strong enough to pull M_{14} from the linear region into the saturation region. Hence, MP_2 is activated. The system works in a 3-stage amplifier topology.

To better distinguish the two operating states, we define a threshold current I_{ON} of approximately 350 µA. When the load current is less than I_{ON}, the second-stage amplifier is working in the triode region and turns off MP_2. When the load current increases to I_{ON}, the second-stage amplifier works in the saturation region and turns on MP_2.

It is worth mentioning that the proposed LDO can adaptively switch the power transistors according to the load current, allowing the system to transform itself between 2-stage and 3-stage topologies. In addition, simulation results have shown that V_{BODY} ranges between 350 mV and 550 mV with APT, and V_{BS} is less than the forward breakdown voltage, which ensures the safety of the device.

2.3. Structure of Proposed OCL-LDO

Figure 6 shows the LDO structure with the proposed bulk modulation and APT. The gain boost stage with an adaptive bias module (ABM) is used, which obtains a large bandwidth gain depending on the load current. The unity gain buffer (BUF) produces V_{BODY} to modulate the bulk voltages of MP_1 and MP_2, lowering the total current consumption via bulk modulation. The APT not only achieves satisfactory linearity but also improves the transient response. In an attempt to realize enough stability, the compensation module (CM) with an internal RC network is used.

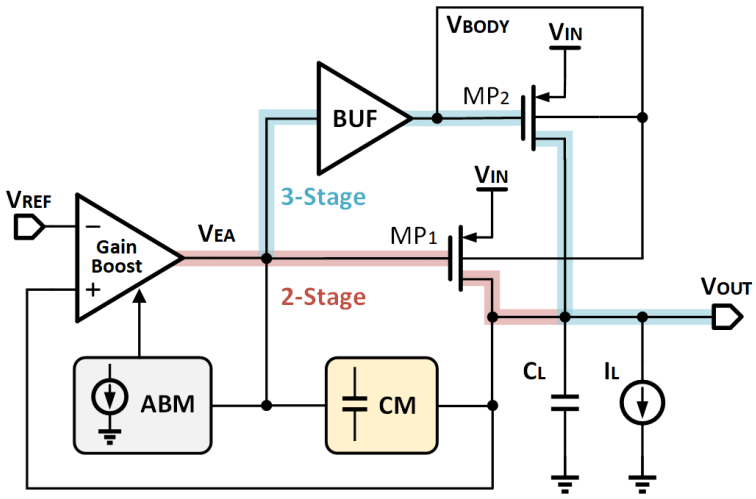

Figure 6. The black box schematic of the proposed LDO.

3. Circuit Implementation

This section will provide an overview of the OCL-LDO, including its structural realization and design consideration. The proposed OCL-LDO works under the condition of V_{IN} = 0.6 V, V_{REF} = 0.5 V, with V_{Drop} = 100 mV. The LDO's V_{REF} is ultra-low, which can be generated with a BJT-based Kuijk bandgap reference [29]. Figure 7 depicts the complete circuit diagram. The gain boost stage is a transconductance-boosted amplifier (M_1–M_{10}) and ABM provides adaptive tail current. The BUF consists of M_{11}–M_{16} in the form of a current mirror, which is capable of increasing the slew rate and improving the transient response. The CM is composed of a resistor r_m and a capacitor C_m.

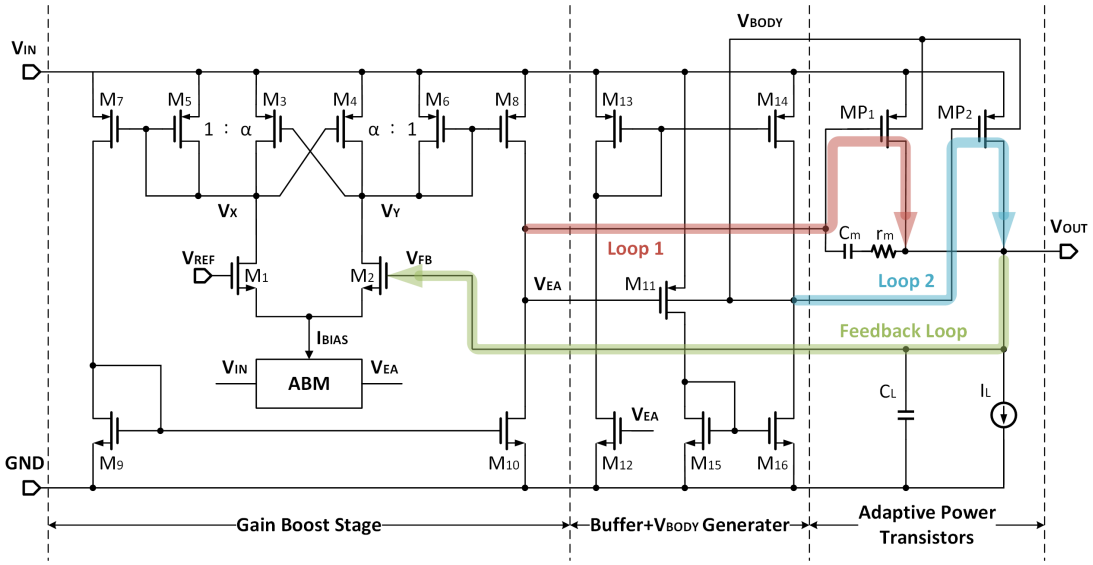

Figure 7. The schematic of the proposed LDO.

3.1. Maximize the Efficiency under Low V_{IN}

To maximize efficiency, it is necessary to reduce the dropout voltage. However, lowering the dropout voltage degenerates the DC gain of the power stage, which can be expressed as:

$$\begin{aligned} A_P &= g_{m,linear} R_{OUT} \\ &\approx \frac{\mu_n C_{OX} \frac{W}{L} V_{DS}}{\mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})} \\ &= \frac{V_{DS}}{V_{GS} - V_{TH}}, \end{aligned} \tag{9}$$

where $g_{m,linear}$ is the transconductance in the linear region. As V_{DS} in the design is merely 100 mV; it is highly possible for it to be smaller than $(V_{GS} - V_{TH})$, implying that the A_P is less than one. It is worth noting that this issue is not present for regular 200 mV dropout regulators, as their power stage can supply roughly 20 dB gain for the control loop. To address this problem, the proposed LDO introduces a gain boost stage with ABM.

From Figure 7, the gain boost stage employs a single-stage differential amplifier along with a cross-coupled PMOS pair to increase the gain. The cross-coupled pair generates negative resistance that can counteract the equivalent resistance of diode-connected transistors M_5 and M_6, which effectively increases the resistance of internal nodes V_X and V_Y. The amplifier gain is obtained as:

$$A_{EA} = \frac{(1+\alpha)g_m + g_{ds}}{(1-\alpha)g_m + g_{ds}} g_{m1}(r_{o8} || r_{o10}), \tag{10}$$

where g_m represents the transconductance of M_3, M_4, and g_{ds} denotes the total output conductance of node V_X or V_Y. The gain is amplified by a factor of $((1+\alpha)g_m + g_{ds})/((1-\alpha)g_m + g_{ds})$. To ensure that it works as an amplifier rather than a hysteresis comparator, the pairs M_3-M_4 and M_6-M_5 are set at a ratio of α:1, where α should be kept smaller than 1 to avoid the over-compensation of negative resistance, taking into account the random mismatch under the fabrication.

For the push-pull stage structure, the DC gain can be approximated at 1. As a result, the overall circuit gain can be expressed as follows:

$$A_{DC} = A_P \cdot A_{EA} = \frac{V_{DS}}{V_{GS} - V_{TH}} \cdot \frac{(1+\alpha)g_m + g_{ds}}{(1-\alpha)g_m + g_{ds}} g_{m1}(r_{o8} \| r_{o10}). \tag{11}$$

Thus, the DC performance of this LDO can be significantly improved by increasing A_{EA} when A_P is small.

3.2. Achieve Low I_Q and Transient Response

Realizing nA-level quiescent current is necessary to ensure ultra-high-power efficiency. The proposed LDO uses adaptive bias to ensure a low quiescent current while reducing transient response time and improving transient response.

Unlike traditional adaptive bias circuits, which mirror the current at the gate of the power transistor to bias the amplifier or buffer, the proposed ABM is driven by the first-stage amplifier itself and provides a bias current proportional to the load current, which can maintain a large enough gain of the first-stage amplifier over the entire load range.

Figure 8 illustrates the specific design of ABM. The ABM's input current is set by M_{23}, which is biased by V_{EA} and is proportional to the load current because V_{EA} is closely related to the load current. The output current of ABM is I_{BIAS}, which is used to bias the amplifier and equal to the sum current of M_1 and M_2. I_{MIN} and I_2 are used to define the bias upper and lower limit. The workflow of ABM can be summarized into the following three phases depending on the load current.

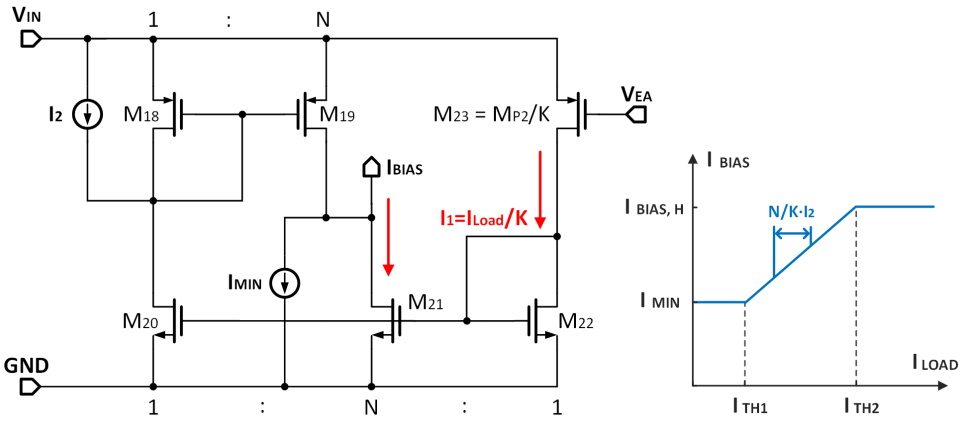

Figure 8. The schematic of ABM.

- Light load

During periods of low load current, the current in M_{23} is ultra-low and not sufficient to turn on the transistor. In this case, all devices are turned off, and I_{BIAS} is equal to I_{MIN}.

$$I_{BIAS,L} = I_{MIN}. \tag{12}$$

- Moderate load

As the load current increases, the transistors M_{20}, M_{21} and M_{22} in the ABM are turned on, and there are

$$\begin{aligned} I_{DM20} &= \frac{1}{K} \cdot I_{LOAD}, \\ I_{DM21} &= \frac{N}{K} \cdot I_{LOAD}. \end{aligned} \tag{13}$$

Considering that the current of M_{20} is less than I_2, I_{BIAS} is equal to the current sum of M_{21} and I_{MIN}, and can be expressed as:

$$I_{BIAS,M} = I_{MIN} + I_{DM21} = I_{MIN} + \frac{N}{K} \cdot I_{LOAD}, \tag{14}$$

where K and N are the current mirror ratios, as shown in Figure 8.

- Heavy load

Once the current of M_{20} increases to larger than I_2, the current mirror, made up of M_{18} and M_{19}, is activated. This threshold current I_{TH2} can be expressed in the following manner:

$$I_{LOAD} = I_{TH2} = K \cdot I_2. \tag{15}$$

I_{BIAS} stops increasing and reaches the upper limit, which can be expressed as:

$$I_{BIAS,H} = I_{MIN} + \frac{N}{K} \cdot I_{LOAD} = I_{MIN} + N \cdot I_2, \tag{16}$$

The bounds of I_{BIAS} ensures stable operation. In the actual design, I_{MIN} and I_2 are set at 7 nA, 18 nA, respectively. N and K are set at 6 and 5150, respectively. It is worth mentioning that ABM also contributes to improvements in gain. The equivalent transconductance g_{mEA} of the gain boost stage can be determined as follows:

$$g_{mEA} = \frac{g_{m1}}{\frac{g_{m3}}{g_{m5}} - 1}, \tag{17}$$

As I_{LOAD} increases, g_{m1} increases significantly; thus, g_{mEA} enlarges accordingly. Therefore, the bias current for the amplifier is proportional to the load current.

4. Stability Analysis

To analyze the stability of the proposed LDO, a small-signal transfer function needs to be derived. It can be seen from Figure 9 that the small-signal model switches between the two-stage amplifier and the three-stage amplifier. Due to the existence of the self-adaptive power transistor, MP_1, and MP_2 turn on and work sequentially under the condition of different load currents. Thus, the stability analysis of the circuit should be discussed according to the situation: (i) the second-stage amplifier and (ii) the third-stage amplifier.

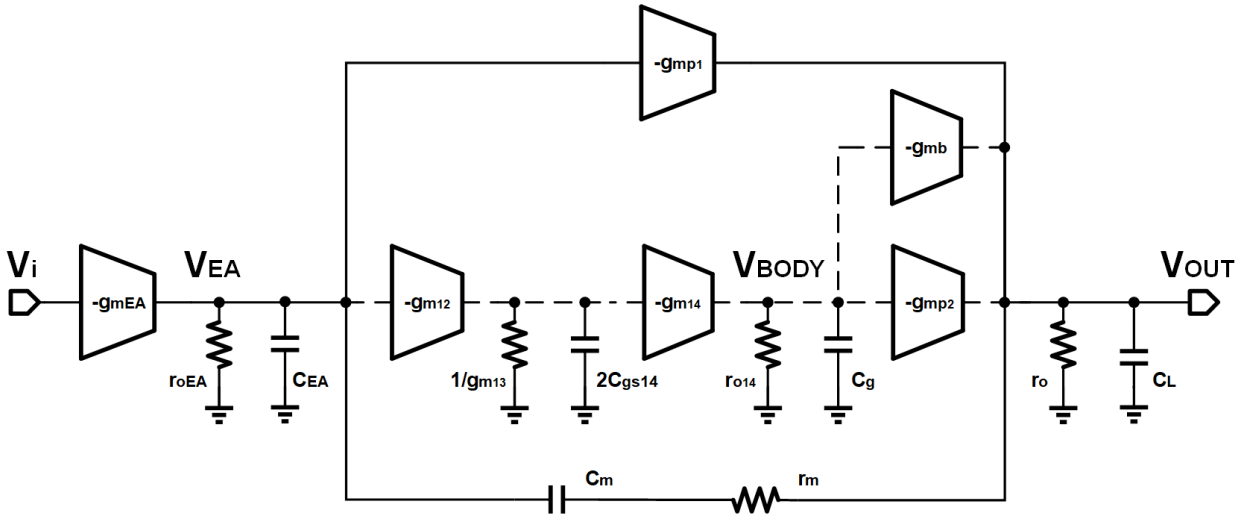

Figure 9. The small-signal model of the proposed LDO.

Due to the topology complexity, it is difficult to obtain the transmission function and analyze the stability. To simplify the derivation of the loop without reducing accuracy, the following assumptions are established.

The gains of the first-stage amplifier, the main power transistor, and the side power transistor are far larger than 1, that is, $g_{m<i>}r_{o<i>} >> 1$. In the case of the third-stage amplifier, $g_{mp2} >> g_{mp1}$. Since the g_{mb} of MP_1 is small, it was ignored in the analysis. The output capacitor C_L is larger than compensating capacitors C_M, C_{EA}.

4.1. Two-Stage Structure

In the case of a small load current, the LDO is equivalent to a secondary structure. There is a pole in V_{OUT} due to the output resistance and load capacitance. Since output resistance is closely related to the load size, a light load will have a relatively large output resistance, which results in the pole associated with the output terminal moving to the low frequency and becoming the dominant pole, P_1. The secondary pole P_2 is located at the output of the first stage because of the output resistance of the amplifier and the parasitic capacitance of the MP_1 gate. The poles' frequencies can be obtained by calculation as follows:

$$P_1 = -\frac{1}{r_{oEA}C_m g_{mp1} r_o}, \tag{18}$$

$$P_2 = -\frac{g_{mp1}}{C_{EA}}. \tag{19}$$

Maintaining stability by only allowing one pole to exist within the bandwidth is necessary. When the OCL-LDO is operated under the minimum load current condition, the pole frequency located in the output is close to zero. Therefore, LDO has a very poor phase margin (PM) and must adopt a compensation structure to produce a zero point. The compensation is performed by connecting the compensation Miller capacitor C_M between the output of the first-stage amplifier and V_{OUT}. However, the traditional Miller

compensation produces a zero point in the right half plane (RHP), which is converted to the left half plane (LHP) by adding the zeroing resistor r_m. Therefore, the zero point Z_1 can be expressed as:

$$Z_1 = -\frac{g_{mp1}}{C_m\left(g_{mp1}r_m - 1\right)}. \tag{20}$$

Therefore, the transfer function of the two-stage structure can be expressed as:

$$LG(s) = A_0\frac{\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}, \tag{21}$$

where A_0 is the DC gain under the condition of light load and can be calculated as:

$$A_0 = g_{mEA}r_{oEA}g_{mp1}r_o. \tag{22}$$

As shown in Figure 10, the LDO's open-loop frequency response and pole-zero distribution are plotted under the conditions of V_{IN} = 0.6 V with I_{LOAD} = 10 µA. Based on the simulation results, the PM is better than 45° for the worst-case scenario with the smallest load current, and the overall circuit is stable.

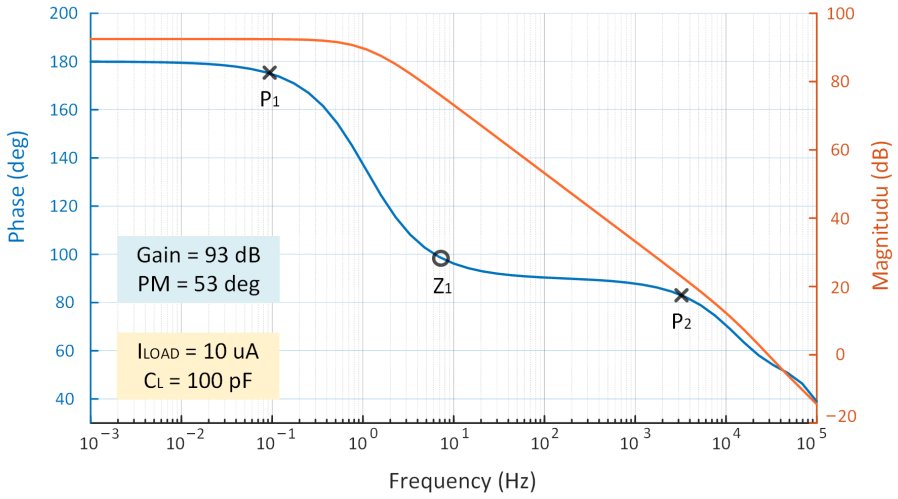

Figure 10. Open-loop gain simulation of the proposed LDO when I_{LOAD} = 10 µA.

4.2. Three-Stage Structure

During heavy load conditions, the output resistance of the circuit decreases, and the pole at the output becomes the secondary pole P_2 instead of the dominant pole P_1. Since the MP_2 main power transistor has a large size, its parasitic capacitance is relatively large. Therefore, the pole existing on the gate of the main power transistor becomes the main pole P_1. The poles under heavy load can be approximated as follows:

$$P_1 = -\frac{g_{m13}}{C_m g_{m12}g_{m14}r_{oEA}r_{o14}}, \tag{23}$$

$$P_2 = -\frac{1}{C_L\left(r_{mp2}\|r_o\right)}, \tag{24}$$

$$P_3 = -\frac{g_{m13}}{2C_{gs14}}, \tag{25}$$

$$P_4 = -\frac{1}{C_g r_{o14}}. \tag{26}$$

Because the output capacitance and equivalent resistance of other nodes in the small-signal diagram are small, other poles are outside the bandwidth, which will be canceled out by zeros and thus have no effect on the stability of the overall circuit.

Due to the relationship between the equivalent capacitance of the miller compensation and the gain of the amplifier, the zero frequency changes in response and moves to a higher frequency. This zero is given by:

$$Z_1 = -\frac{g_{mp1}}{C_m}, \tag{27}$$

$$Z_2 = -\frac{g_{m12}g_{m14}\left(g_{mb} + g_{mp2}\right)}{C_m g_{mp1}}. \tag{28}$$

As a consequence, the three-stage structure has the following transfer function:

$$LG(s) = A_0 \frac{\left(1 + \frac{s}{z_1}\right)\left(1 + \frac{s}{z_2}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right)\left(1 + \frac{s}{p_4}\right)}, \tag{29}$$

where A_0 is the DC gain under the condition of heavy load, which can be calculated as:

$$A_0 = \frac{g_{mEA}g_{m12}g_{m14}\left(g_{mp2} + g_{mb}\right)r_{oEA}r_{o14}r_o}{g_{m13}}. \tag{30}$$

Figure 11 depicts the specific poles and zeros with a bandwidth under the heavy load. The figure shows that the PM is 59°, which is greater than 45°, indicating that the circuit is stable overall.

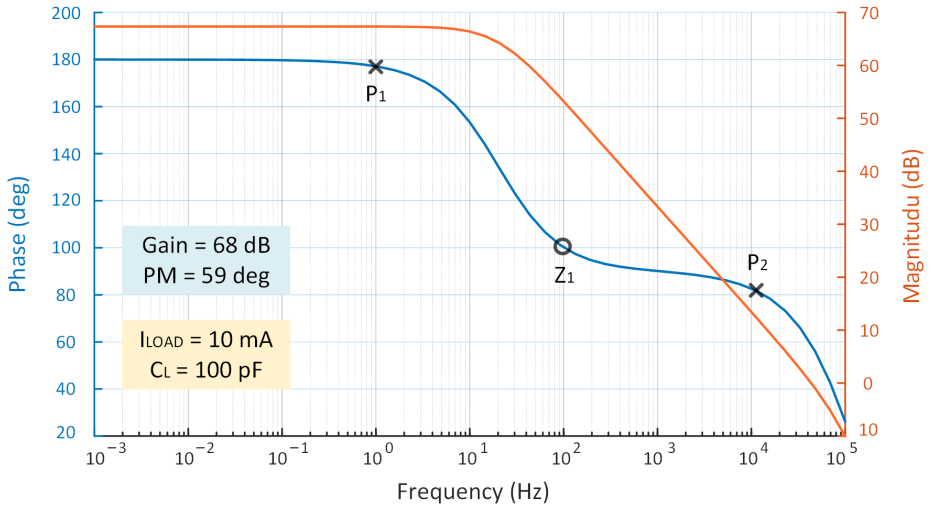

Figure 11. Open-loop gain simulation of the proposed LDO when I_{LOAD} = 10 mA.

5. Simulation Results and Discussion

The LDO proposed in this paper was implemented and verified in a 180 nm CMOS process, which supports 0.6–1.2 V supply voltage and 100 mV dropout voltage with a 10 mA maximum load current. The system can remain stable when C_L ranges between 0 and 1000 pF with a 10 pF on-chip compensation capacitor. When I_{LOAD} = 10 µA, V_{IN} varies from 0.6 V to 1.2 V, and I_Q changes from 226 nA to 219 nA. The devices' size and the most important parameter values for the proposed OCL-LDO are summarized in Table 1.

Table 1. Devices' size and parameters' value of proposed OCL-LDO.

Component	Size	Component	Size	Parameters	Value
M_1, M_2	5 µ/1 µ	M_{12}	500 n/5 µ	α	0.75
M_3, M_4	3 µ/1 µ	M_{13}	500 n/500 n	N	6
M_5, M_6, M_7	4 µ/1 µ	M_{14}	3.5 µ/500 n	K	5150
M_8, M_9	2 µ/1 µ	M_{16}	250 n/1 µ	I_{MIN}	7 nA
M_{10}, M_{15}	1 µ/1 µ	M_{P1}	70 µ/180 n	I_2	18 nA
M_{11}	1 µ/2 µ	M_{P2}	20 m/180 n		

Under the condition of V_{IN} = 600 mV, I_{LOAD} increases from 10 µA to 10 mA, I_Q changes from 220 nA to 1.2 µA. The changing trend of I_Q in the two cases is depicted in Figure 12.

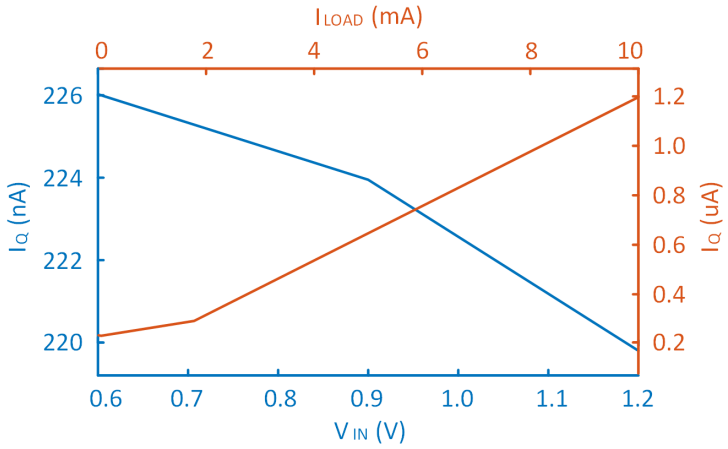

Figure 12. The I_Q of the proposed LDO when V_{IN} varies from 0.6 V to 1.2 V, I_{LOAD} changes from 10 µA to 10 mA.

Only 1.2 µA of quiescent current is consumed when the load current is 10 mA; thus, it achieves a maximum current efficiency of 99.96% when the load current is 10 mA. The current efficiency of the LDO under full load conditions is presented in Figure 13.

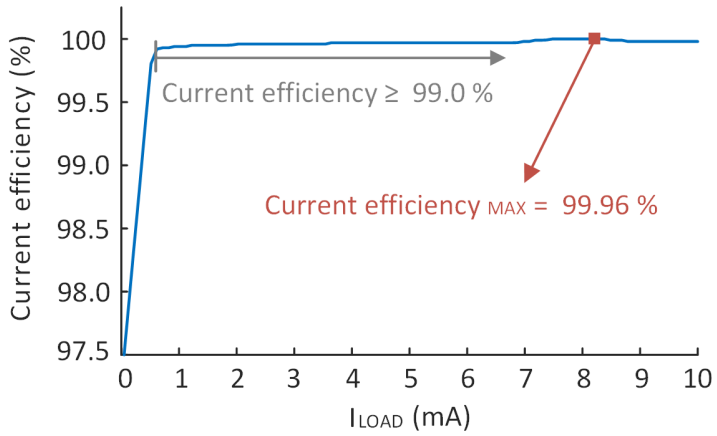

Figure 13. The current efficiency of the proposed LDO when I_{LOAD} changes from 10 µA to 10 mA.

The current of MP_1 and MP_2 are also shown in Figure 14. From the result, when the system works as a two-stage, system the current of MP_2 is almost equal to zero and MP_1 increases with I_{LOAD}. Once $I_{LOAD} > I_{ON}$, MP_2 is activated, its current increases with I_{LOAD} while the current of MP_1 remains unchanged.

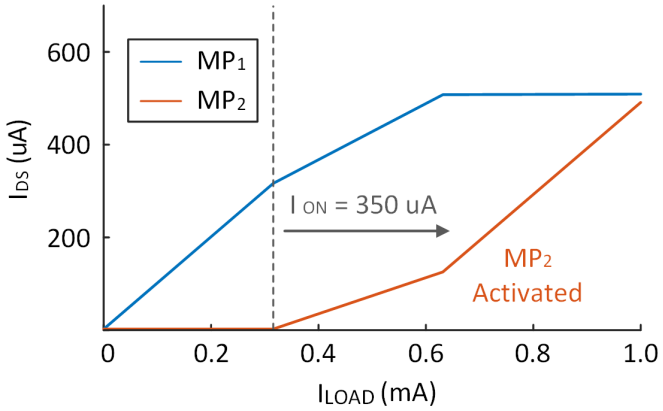

Figure 14. I_D of MP_1 and MP_2 when I_{LOAD} changes from 0 to 1 mA.

Additionally, we simulated the relationship between PM and load current under a variety of loop conditions. As shown in Table 2, PM decreases with an increase in I_{LOAD} when LDO works in a two-stage manner. However, PM in the three-stage is the opposite.

Table 2. PM with respect to I_{LOAD} in the two working conditions.

Loop	**2-Stage**			**3-Stage**		
I_{LOAD} (A)	100 µ	200 µ	300 µ	1 m	5 m	9 m
PM (deg)	49.1	47.8	44.5	51.1	55.4	58.2

The measured DC load regulation (LDR) is shown in Figure 15a; when the load current varies from 10 µA to 10 mA, the output voltage changes by 0.05857 mV. Therefore, the LDR of the LDO is 0.00585759 mV/mA. The simulation results depicted in Figure 15b indicate that the output voltage only changes to 0.292787 mV when the supply voltage changes linearly from 0.6 V to 1.2 V. According to the calculation formula, the DC line regulation (LNR) of LDO is 0.487978 mV/V.

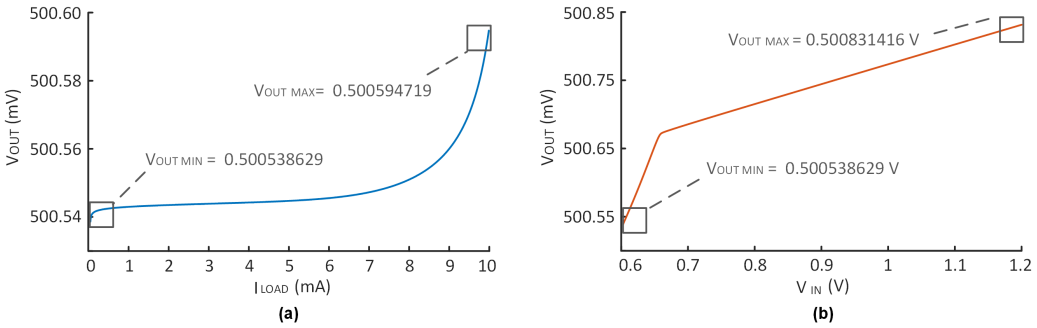

Figure 15. Simulation results of (**a**) DC load regulation, (**b**) DC line regulation.

Figure 16a,b show the measured transient response when the OCL-LDO supply voltage is set to 0.6 V and the load capacitor is set to 100 pF, respectively. For a 1 ns edge, the maximum transient response of $\triangle V_{OUT}$ is 230 mV, and the settling time is 5 µs. When the edge is 1 µs, the maximum $\triangle V_{OUT}$ is 140 mV, and the settling time is 3.5 µs, which represents a significant improvement. There is a minimum overshoot voltage of 95 mV and a undershoot voltage of 140 mV. However, the transient response is not entirely satisfactory. These results indicate that the circuit's performance is satisfactory and there is room for further improvement. Typically, an undershoot improvement circuit would be included to enhance the transient response. Nevertheless, due to the constraints of quiescent current, no improvement circuit has been incorporated.

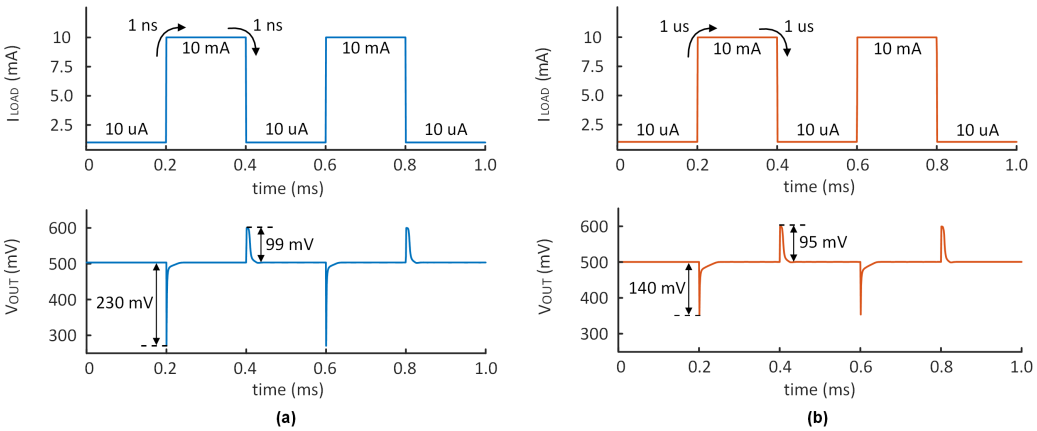

Figure 16. Measured dynamic response with a (**a**) 10 µA to 10 mA load step and 1 ns rising/falling edges, (**b**) 10 µA to 10 mA load step and 1 µs rising/falling edges.

The trend of the PSR with frequency can be plotted by analyzing the PSR at multiple frequencies over the course of one measurement. The simulated PSR performance at 10 µA load current, 0-pF C_L, and 100 mV dropout is shown in Figure 17. Hence, it can be seen that the minimum PSR is −51.40 dB, −49.17 dB at 1 Hz, and −43.97 dB at 1 k Hz.

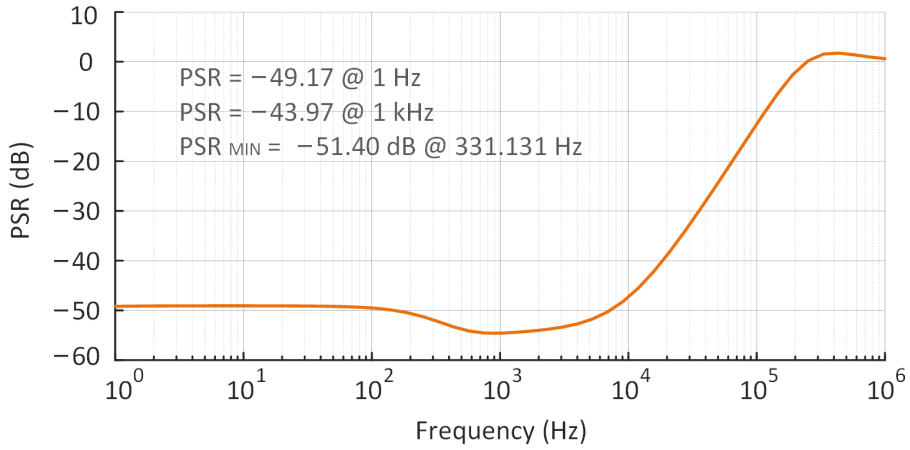

Figure 17. The simulated PSR performance of the proposed LDO at 10 µA load current, 0 pF C_L, and 100 mV dropout.

Simulations at different temperatures and process corners are conducted to demonstrate the robustness of the proposed design. The performance results, including minimum values of PM and GM, quiescent current, LDR, LNR, transient response, current efficiency, and PSR, are presented in Table 3. The minimum GM under different corners is greater than 50 dB, ensuring high regulation performance under different conditions. I_Q is generally within 500 nA, with the lowest value being 139 nA at the SS corner of −20 °C; the current efficiency is at least 99.95%, and the maximum is 99.99%. There is an excellent transient response at the FF corner of 27 °C, a 2.7 µs recovery time, and a maximum undershoot voltage of 320 mV. The worst PSR within 50 kHz is −51.4 dB at the TT corner of 27 °C. This shows that the proposed design can work steadily and perform as expected, even under extreme conditions. These results predict that the proposed LDO will work reliably after fabrication, even in the worst-case temperature and process corner.

Table 3. Performance summary under process and temperature corners.

Parameter	27 °C		−20 °C	80 °C	
Corner	TT	FF	SS	FF	SF
$Gain_{MIN}$ (dB)	68.4	65.1	78.51	71.1	53.4
PM_{MIN} (deg)	53.64	54.98	64.38	53.85	63.33
I_Q (nA)	220	370	139	870	424
LNR (mV/V)	0.48	0.78	0.60	0.83	0.73
LDR (μV/mA)	5.85	10.21	15.87	48.87	152.31
$\triangle V_{OUT}$ (mV)	230	320	346	465	428
Settling Time (μs)	3.8	2.7	7.1	5.3	13.1
Current Efficiency (%)	99.96	99.99	99.99	99.95	99.95
Min. PSR from DC to 50 kHz (dB)	−51.4	−63.4	−63.7	−55.9	−62.2

A merit map (FoM) is introduced to reflect the overall performance of the LDO, which has the following formula:

$$FoM = K\left(\frac{C_L I_Q \Delta V_{OUT}}{\Delta {I_{O,MAX}}^2}\right), \tag{31}$$

where I_Q is the minimum quiescent current, and ΔV_{OUT} is the maximum change in output during transient. Furthermore, K is the edge time ratio and defined by:

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among designs for comparison}}. \tag{32}$$

In this design, $K = 1$, bringing the above values into the calculation, the FoM value is 0.0506 ps. The comparison of the proposed LDO's performance with several state-of-the-art fully integrated LDOs is presented in Table 4 below. Based on the results of the analysis, the proposed LDO achieves the lowest dropout voltage, good load regulation, and lowest FoM.

Table 4. Performance comparison with other works.

Paper	TCAS-I [30]	TPE [31]	TPE [32]	AEU [33]	MDPI [11]	MDPI [10]	This Work
Year	2018	2018	2020	2021	2022	2022	2023
Technology (nm)	65	130	65	180	40	40	180
V_{IN} (V)	1	1	0.95	1.3	1.1	1.1	0.6
V_{OUT} (V)	0.8	0.8	0.8	1.1	0.9	0.9	0.5
Vdrop (mV)	200	200	150	200	200	200	100
Capacitor-less	Yes	Yes	Yes	Yes	Yes	Yes	Yes
$I_{LOAD(max)}$ (mA)	25	100	100	100	100	100	10
C_L (pF)	0–25 p	0–25 p	0–100 p	0–100 p	0–100 p	0–100 p	0–1000 p
I_Q (μA)	24.2	112	14	50.25	24.6-65	30	0.22
Line Reg. (mV/V)	0.7	2.25	12	0.75	N.A.	0.2	0.487
Load Reg. (mV/mA)	0.28	0.173	0.09	0.48	0.017	0.25	0.00585
Edge time (ns)	100	10	220	500	100	100	1
Edge time ratio K	100	10	220	500	100	100	1
$\triangle V_{OUT}$ (mV)	71	35	230	336	33	23.5	230
Min. PSR from DC to 50 kHz (dB)	−11	−22	−33	−22.5	−46	−70	−51.4
FoM (ps)	6.872	0.098	7.084	84.42	0.8118	0.705	0.0506

6. Conclusions

In this paper, an nA-level and 100 mV dropout LDO, combined with bulk modulation and adaptive power transistors is proposed and simulated in the 0.18 μm CMOS process. The operation principle, circuit implementation, stability analysis, and simulation results have been presented in detail. Particular attention has been paid to obtaining a low dropout and low supply voltage by the bulk modulation technology, without an auxiliary amplifier.

Adaptive power transistors are proposed to switch under different load conditions to ensure circuit stability while reducing circuit power consumption. In addition, the adaptive bias mirroring the current from the amplifier itself with bounds is utilized to improve the transient response. Due to the superiority of ultra-low-power consumption, low supply voltage, and a fast response, the proposed OCL-LDO is suitable for use as a point-of-load regulator in energy harvesting.

Author Contributions: Validation, writing—original draft preparation: Y.Z. (Yuting Zhang); sotfware, visualization, data curation, conceptualization, methodology, writing—review and editing, project administration, funding acquisition, Y.Z. (Yanhan Zeng); data Curation; visualization, Q.G. All authors have read and agreed to the published version of the manuscript.

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References

1. Bahramali, A.; Lopez-Vallejo, M. An RFID-Based Self-Biased 40 nm Low Power LDO Regulator for IoT Applications. *Micromachines* **2021**, *12*, 396. [CrossRef] [PubMed]
2. Wu, C.; Zhang, J.; Zhang, Y.; Zeng, Y. A 7.5-mV Input and 88%-Efficiency Single-Inductor Boost Converter with Self-Startup and MPPT for Thermoelectric Energy Harvesting. *Micromachines* **2023**, *14*, 60. [CrossRef] [PubMed]
3. He, Z.; Luo, P.; Wang, H.; Chen, J.; Song, H. A wide-input-range, low quiescent current LDO with ED reference for piezoelectric energy harvesting. *AEU-Int. J. Electron. Commun.* **2022**, *157*, 154419. [CrossRef]
4. Ruan, T.; Chew, Z.J.; Zhu, M. Energy-Aware Approaches for Energy Harvesting Powered Wireless Sensor Nodes. *IEEE Sens. J.* **2017**, *17*, 2165–2173. [CrossRef]
5. Paul, S.; Honkote, V.; Kim, R.G.; Majumder, T.; Aseron, P.A.; Grossnickle, V.; Sankman, R.; Mallik, D.; Wang, T.; Vangal, S.; et al. A Sub-cm3 Energy-Harvesting Stacked Wireless Sensor Node Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14-nm Tri-Gate CMOS for Always-ON Always-Sensing Applications. *IEEE J.-Solid-State Circuits* **2017**, *52*, 961–971. [CrossRef]
6. Reyes, A.C.; Abuellil, A.; Estrada-López, J.J.; Carreon-Bautista, S.; Sánchez-Sinencio, E. Reconfigurable System for Electromagnetic Energy Harvesting with Inherent Activity Sensing Capabilities for Wearable Technology. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1302–1306. [CrossRef]
7. Zou, Y.; Yue, X.; Du, S. A Nanopower 95.6% Efficiency Voltage Regulator with Adaptive Supply-Switching for Energy Harvesting Applications. In Proceedings of the 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 27 May–1 June 2022; pp. 3557–3561. [CrossRef]
8. Carreon-Bautista, S.; Huang, L.; Sanchez-Sinencio, E. An Autonomous Energy Harvesting Power Management Unit with Digital Regulation for IoT Applications. *IEEE J.-Solid-State Circuits* **2016**, *51*, 1457–1474. [CrossRef]
9. Park, S.-Y.; Cho, J.; Lee, K.; Yoon, E. A PWM Buck Converter With Load-Adaptive Power Transistor Scaling Scheme Using Analog-Digital Hybrid Control for High Energy Efficiency in Implantable Biomedical Systems. *IEEE Trans. Biomed. Circuits Syst.* **2015**, *9*, 885–895. [CrossRef]
10. Ni, S.; Chen, Z.; Hu, C.; Chen, H.; Wang, Q.; Li, X.; Song, S.; Song, Z. An Output-Capacitorless Low-Dropout Regulator with Slew-Rate Enhancement. *Micromachines* **2022**, *13*, 1594. [CrossRef]
11. Hu, C.; Chen, Z.; Ni, S.; Wang, Q.; Li, X.; Chen, H.; Song, Z. A Fully Integrated Low-Dropout Regulator with Improved Load Regulation and Transient Responses. *Micromachines* **2022**, *13*, 1668. [CrossRef]
12. Poongan, B.; Rajendran, J.; Yizhi, L.; Mariappan, S.; Parameswaran, P.; Kumar, N.; Othman, M.; Nathan, A. A 53-µA-Quiescent 400-mA Load Demultiplexer Based CMOS Multi-Voltage Domain Low Dropout Regulator for RF Energy Harvester. *Micromachines* **2023**, *14*, 379. [CrossRef] [PubMed]
13. Man, T.Y.; Mok, P.K.T.; Chan, M. A High Slew-Rate Push–Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement. *IEEE Trans. Circuits Syst. II Express Briefs* **2007**, *54*, 755–759. [CrossRef]
14. Pereira-Rial, Ó.; López, P.; Carrillo, J.M.; Brea, V.M.; Cabello, D. An 11 mA Capacitor-Less LDO With 3.08 nA Quiescent Current and SSF-Based Adaptive Biasing. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, *69*, 844–848. 2021.3130674. [CrossRef]
15. Ma, X.; Lu, Y.; Li, Q. A Fully Integrated LDO with 50-mV Dropout for Power Efficiency Optimization. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 725–729. [CrossRef]

16. Silverio, A.A. Forward Body Bias Technique for Low Voltage and Area Constrained LDO Design in Deep Submicron Technologies. In Proceedings of the 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Dubai, United Arab Emirates, 28 November–1 December 2021; pp. 1–4. [CrossRef]
17. Ming, X.; Zhou, Z.; Zhang, B. A low-power ultra-fast capacitor-less LDO with advanced dynamic push-pull techniques. In Proceedings of the 2011 IEEE/IFIP 19th International Conference on VLSI and System-on-Chip, Hong Kong, 3–5 October 2011; pp. 54–59. [CrossRef]
18. Gupta, M.; Srivastava, R.; Singh, U. Low Voltage Floating Gate MOS Transistor Based Differential Voltage Squarer. *Int. Sch. Res. Not.* **2014**, *2014*, 357184. [CrossRef]
19. Musa, F.A.S.; Nurulain, D.; Ahmad, N.; Mohamad Isa, M.; Ramli, M. Implementation of floating gate MOSFET in inverter for threshold voltage tenability. *Eur. Phys. J. Conf.* **2017**, *162*, 01069. [CrossRef]
20. Keikhosravy, K.; Mirabbasi, S. A 0.13-µm CMOS Low-Power Capacitor-Less LDO Regulator Using Bulk-Modulation Technique. *IEEE Trans. Circuits Syst. Regul. Pap.* **2014**, *61*, 3105–3114. [CrossRef]
21. Nagateja, T.; Kumari, N.; Chen, K.-H.; Lin, Y.-H.; Lin, S.-R.; Tsai, T.-Y. A 8-ns Settling Time Fully Integrated LDO with Dynamic Biasing and Bulk Modulation Techniques in 40nm CMOS. In Proceedings of the 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 10–21 October 2020; pp. 1–4. [CrossRef]
22. Koo, Y.S. A design of low-area low drop-out regulator using body bias technique. *Electron. Express Lett.* **2013**, *10*, 1–12. [CrossRef]
23. Wang, Y.; Shu, Z.; Zhang, Q.; Zhao, X.; Chen, S.; Tang, F.; Zheng, Y. A Low-Voltage and Power-Efficient Capless LDO Based on the Biaxially Driven Power Transistor Technique for Respiration Monitoring System. *IEEE Trans. Biomed. Circuits Syst.* **2022**, *16*, 1153–1165. [CrossRef]
24. Burington, R.S. *Handbook of Mathematical Tables and Formulas*; McGraw-Hill: New York, NY, USA, 1973.
25. Tsividis, Y.; McAndrew, C. *Operation and Modeling of the MOS Transistor*; Oxford University Press: New York, NY, USA, 1999.
26. Cheng, Y.; Hu, C. *MOSFET Modeling and BSIM3 User's Guide*; Springer: New York, NY, USA, 1999.
27. Zeng, Y.; Huang, Y.; Luo, Y.; Tan, H.-Z. An ultra-low-power CMOS voltage reference generator based on body bias technique. *Microelectron. J.* **2013**, *44*, 1145–1153. [CrossRef]
28. Adorni, N.; Stanzione, S.; Boni, A. A 10-mA LDO With 16-nA IQ and Operating From 800-mV Supply. *IEEE J. -Solid-State Circuits* **2020**, *55*, 404–413. [CrossRef]
29. Ria, A.; Catania, A.; Bruschi, P.; Piotto, M. A Low-Power CMOS Bandgap Voltage Reference for Supply Voltages Down to 0.5 V. *Electronics* **2021**, *10*, 1901. [CrossRef]
30. Bu, S.; Leung, K.N.; Lu, Y.; Guo, J.; Zheng, Y. A Fully Integrated Low-Dropout Regulator With Differentiator-Based Active Zero Compensation. *IEEE Trans. Circuits Syst. Regul. Pap.* **2018**, *65*, 3578–3591. [CrossRef]
31. Bu, S.; Guo, J.; Leung, K.N. A 200-ps-response-time output-capacitorless low-dropout regulator with unity-gain bandwidth >100 MHz in 130-nm CMOS. *IEEE Trans. Power Electron.* **2018**, *33*, 3232–3246. [CrossRef]
32. Li, G.; Qian, H.; Guo, J.; Mo, B.; Lu, Y.; Chen, D. Dual active-feedback frequency compensation for output-capacitorless LDO with transient and stability enhancement in 65-nm CMOS. *IEEE Trans. Power Electron.* **2020**, *35*, 415–429. [CrossRef]
33. Li, S.; Zhao, X.; Dong, L.; Yu, L.; Wang, Y. Design of a Capacitor-less Adaptively Biased Low Dropout Regulator Using Recycling Folded Cascode Amplifier. *AEU-Int. J. Electron. Commun.* **2021**, *135*, 153745. [CrossRef]