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Abstract: In this paper, a 4H-SiC lateral gate MOSFET incorporating a trench MOS channel diode at the source side is explored to improve the reverse recovery characteristics. In addition, a 2D numerical simulator (ATLAS) is used to investigate the electrical characteristics of the devices. The investigational results have demonstrated that the peak reverse recovery current is reduced by 63.5%, the reverse recovery charge is reduced by 24.5%, and the reverse recovery energy loss is decreased by 25.8%, with extra complexity in the fabrication process.

Keywords: LDMOS; MOS channel diode; reverse recovery

1. Introduction

Recently, laterally-diffused metal-oxide semiconductor (LDMOS) devices have been widely applied for AC-DC power supply [1–7]. With the superior physical properties, such as a higher critical breakdown electric field, higher saturated electron drift velocity, and wider band gap, silicon carbide LDMOS devices have lower specific on-resistance compared with a silicon LDMOS under the same breakdown voltage [8–12]. In the AC-DC power supply, LDMOS needs to be anti-parallel to an external freewheeling diode in order to suppress the voltage surge. There exists a parasitic body diode, consisting of the P-body and N-drift region, which can be used as a freewheeling diode [13].

However, this cost- and area-saving alternative is not feasible in silicon carbide devices for the following two reasons: one is the high built-in potential of PN junction (close to 3 V), leading to a high conduction loss; the other is that the recombination of minority carriers can cause a bipolar degradation issue [14]. In order to realize this alternative, the reverse recovery performance needs to be improved. In order to overcome the abovementioned two issues (high conduction loss and bipolar degradation), that is to say, improving the reverse recovery performance of the parasitic body diode, many solutions have been utilized, such as the introduction of a Schottky contact [15–17] and integrating a channel diode [18–21] in the SiC VDMOSFET. Compared with SiC VDMOSFET, LDMOS is better for integration and is beneficial to the miniaturization of the AC-DC electric system. However, research into the electrical performance of the 4H-SiC LDMOS has few reports [22–26], but the reverse recovery performance has not been reported in the 4H-SiC LDMOS.

When the C-LDMOS device serves as a freewheeling diode, reverse conduction takes place through the parasitic P-body/N-drift junction. This parasitic P-body/N-drift junction is a bipolar device that could cause an inferior reverse recovery performance. In this paper, in order to improve the reverse recovery of C-LDMOS, the concept of the MOS channel diode is introduced to a 4H-SiC LDMOS device (called TMCD-LDMOS), which has been reported in other 4H-SiC switches [18–20]. Compared to the parasitic P-body/N-drift junction, the TMCD has the following effects when the device serves as a freewheeling diode. On the one hand, the trench MOS channel diode has a smaller turn-on voltage than the parasitic P-body/N-drift junction and the two diodes are in a series connection. When a



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Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). LDMOS device works as a freewheeling diode, the TMCD diode turns on first, suppressing the turn-on of the parasitic body diode effectively. On the other hand, the TMCD diode is a unipolar device, which can reduce the injection of the minority carriers from the parasitic P-body/N-drift junction greatly and improve the reverse recovery performance.

In this paper, 4H-SiC LDMOS featuring a trench MOS channel diode is investigated in detail and compared with a conventional LDMOS. Note that due to the limitation of our present experimental conditions, we are unable to provide experimental results; however, simulation tools are generally used for the optimization and development of various semiconductor device structures in order to reduce the cost of device manufacturability and the development period and hence lower the risks associated with technology transfer in an industrial environment. Moreover, simulation tools are very useful to explore novel device architectural concepts for different material systems. So the aim of the simulation work is to compare the electrical characteristics of two different structures on the same terms while not revealing the physical devices' features.

2. Setup of Simulation Conditions

The structures of the investigated C-LDMOS and TMCD-LDMOS device are shown in Figure 1, which is not to scale and the distances are in micrometers. C-LDMOS and TMCD-LDMOS have the same region parameters, except that a trench MOS channel diode exists in TMCD-LDMOS, which is shown within the dashed box in Figure 1b. The gate oxide thickness is 50 nm and the trench oxide thickness of TMCD is 30 nm. The doping concentration of N+, P+, and n+ regions are set as 1×10^{19} cm⁻³.



Figure 1. Cross-sectional schematic of half-cells of (a) C-LDMOS (b) TMCD-LDMOS.

A possible fabrication process for TMCD-LDMOS is shown in Figure 2. The key fabrication steps are as follows: (a) forming the p-buffer, p-type, and n-drift regions on the n+ wafer by epitaxial growth technology; (b) forming the p-body layer by ion implantation and performing the ion implantation annealing; (c) forming the gate oxide by thermal growth, depositing and polishing polysilicon; (d) forming the n and p region by ion implantation; (e) forming the trench by etching; (f) depositing and polishing polysilicon, forming the gate, source and drain electrodes.

ATLAS, a 2D numerical simulator, is used to investigate and explore the device performances. The following simulation models are utilized: the bandgap narrowing model (BGN), which is important in heavily doped regions and critical for bipolar gain; AUGER, which describes the direct transition of three carriers and is important at high current densities; and Shockley–Read–Hall (SRH) for recombination and carrier lifetime models, which uses fixed minority carrier lifetimes, doping and temperature-dependent field mobility models (ANALYTIC) [27]; and Fermi Dirac statistics and Selberherr's impact ionization model. The actual effects of the used models on the electrical performance can be found in Ref. [27]. The material parameters and mobility are set to the same as in TABLE I and TABLE II shown in reference [28]. In addition, the lifetime in the N-drift region is set as 1 μ s.



Figure 2. A possible fabrication process of TMCD-LDMOS.

3. Analysis and Discussions of Performances

In this part, the electrical performances are explored and compared between C-LDMOS and TMCD-LDMOS, which includes the static performances (forward I–V, BV, reverse conduction of the body diode) and the reverse recovery characteristic of the body diode.

3.1. Static Performances

Figure 3 shows the current versus voltage characteristics of C-LDMOS and TMCD-LDMOS. From this figure, it can be seen that the introduction of TMCD has no effect on the specific on-resistance, which is 8.34 m $\Omega \cdot \text{cm}^2$ at $V_{\text{gs}} = 8$ V and $J_{\text{ds}} = 100$ A/cm² for C-LDMOS and TMCD-LDMOS. In addition, this figure presents the transfer characteristic at $V_{\text{ds}} = 5$ V, proving that the TMCD has no influence on the threshold voltage.



Figure 3. Comparison of output characteristics and transfer curves.

The electric field characteristic is presented in Figure 4 when the devices are at avalanche multiplication. Obviously, the breakdown voltage is the same for the two structures due to the same parameters of the N-drift region and the TMCD is far from the blocking region of the drain voltage.



Figure 4. Electric field distribution for (**a**) C-LDMOS and (**b**) TMCD-LDMOS when $V_{gs} = 0$ V and $V_{ds} = 1000$ V.

TMCD-LDMOS features a trench MOS channel diode, which has the following effects when the device serves as a freewheeling diode: on the one hand, it suppresses the turn-on of the PN junction diode effectively; however, it reduces the minority carrier concentration greatly, leading to a reduction in the power loss. Figure 5 shows the I—V characteristics of the parasitic body diode of the two structures. From this graph, we can see that the parasitic body diode, composed of the PN junction body diode, turns on at about 2.3 V in the C-LDMOS. However, for the TMCD-LDMOS, the parasitic body diode is composed of the PN junction body diode and the trench MOS channel diode and the TMCD turns on at ~1.5 V first.



Figure 5. I-V performances of the parasitic body diode of the C-LDMOS and TMCD-LDMOS devices.

At $J_{ds} = 100 \text{ A/cm}^2$, the conduction voltage of the parasitic body diode is 2.9 and 2.5 V for C-LDMOS and TMCD-LDMOS, respectively. The trench MOS channel diode has a lower conduction voltage than a PN junction diode, suppressing the turn-on of the PN junction diode effectively. Moreover, the TMCD is a unipolar structure (electron-type), resulting in a lower injection of the minority carriers (hole carriers) in TMCD-LDMOS. The electron and hole concentration distributions are presented in Figures 6 and 7 at $J_{ds} = 100 \text{ A/cm}^2$, proving that the TMCD-LDMOS has an extremely low hole concentration. The hole and electron concentration profiles along the cut-line A-A' shown in Figure 7 are plotted in Figure 8, intuitively demonstrating the turn-on of the parasitic PN junction diode is effectively suppressed by the TMCD. Moreover, the reduction in the minority carriers can result in a superior reserve recovery characteristic and a lower reverse recovery energy loss, which is discussed in the next part, allowing the parasitic body diode to be used as a freewheeling diode.



Figure 6. Electron concentration distribution of (**a**) C-LDMOS and (**b**) TMCD-LDMOS at $J_{ds} = 100 \text{ A/cm}^2$ when the device serves as a freewheeling diode.



Figure 7. Hole concentration distribution of (**a**) C-LDMOS and (**b**) TMCD-LDMOS at $J_{ds} = 100 \text{ A/cm}^2$ when the device serves as a freewheeling diode.



Figure 8. Carrier concentration distribution along cutline A-A' (shown in Figure 7) at $J_{ds} = 100 \text{ A/cm}^2$ when the device serves as a freewheeling diode.

3.2. Reverse Recovery Performance

When a MOSFET device works as a freewheeling diode, the reverse recovery performance of its parasitic body diode is very important and affects the system features. Thus, a MOSFET requires a superior reverse recovery characteristic when it is used as an AC-DC power supply.

The parasitic PN junction diode in C-LDMOS is a bipolar device and generates extensive hole carriers in the N-drift region working as a freewheeling diode. However, for the TMCD-LDMOS, a trench MOS channel diode is introduced, a unipolar device without an injection of the minority carrier when serving as a freewheeling diode. Moreover, the turn-on voltage of TMCD is lower and can suppress the turn-on of the parasitic PN junction diode. Thus, a LDMOS featuring a MOS channel diode can achieve a great improvement of the reverse recovery characteristic.

As can be seen in Figure 5, the TMCD-LDMOS structure outperforms the conventional one for current density of <250 A/cm² under this device's parameters, and the current density can be changed by adjusting the parameters of the TMCD diode. So, in this paper, the current density of 100 A/cm^2 is chosen to investigate the reverse recovery performance. The test circuit used for the reverse recovery performance and the simulation result is plotted in Figure 9 [29]. From this figure, it can be observed that the peak reverse recovery current density ($I_{\rm RM}$) is 136 and 373 A/cm² for TMCD-LDMOS and C-LDMOS, respectively. TMCD-LDMOS has a 63.5% improvement in I_{RM} compared with C-LDMOS. Integrating current over time, the reverse recovery charge (Q_{rr}) is 0.554 and 0.418 nC/cm² for C-LDMOS and TMCD-LDMOS, respectively, in which $Q_{\rm rr}$ is reduced by 24.5% in TMCD-LDMOS. This proves that the trench MOS channel diode can achieve a smaller Q_{rr} , which is beneficial for switching loss reduction. With the integration of the production of the drain voltage and source current with time, the reverse recovery energy loss ($E_{\rm RR}$) is 4.54×10^{-5} J/cm² in TMCD-LDMOS, which is 25.8% lower than that of C-LDMOS ($6.12 \times 10^{-5} \text{ J/cm}^2$). The hole carrier distribution at point A shown in Figure 9 is described in Figure 10, indicating that a lower hole carrier concentration exists in TMCD-LDMOS, which needs to be extracted during the reverse recovery process.



Figure 9. Comparison of the reverse recovery performances.



Figure 10. Hole concentration distribution of (**a**) C-LDMOS and (**b**) TMCD-LDMOS at point A shown in Figure 9 (J_{sd} = 100 A/cm² when the device serves as a freewheeling diode).

3.3. Parameter Influence

In this section, we investigate the effect of the tox of TMCD (shown in Figure 1) on the electrical characteristics, such as the I–V curve of the parasitic body diode and the reverse recovery performance.

Actually, the thickness of SiO₂ in TMCD may not be equal to 30 nm, but varied around 30 nm, so it is necessary to explore the influence of t_{ox} on the characteristics of TMCD. Figure 11 presents the I–V curves of TMCD at different t_{ox} . With decreasing t_{ox} , the TMCD-LDMOS has a lower voltage drop and lower hole concentration under the same drain current when the device works as a freewheeling diode. This leads to the relationship

between t_{ox} and reverse recovery curve presented in Figure 12. From Figures 11 and 12, it can be determined that the TMCD-LDMOS has superior electrical characteristics when the t_{ox} changes due to the fabrication process technology.



Figure 11. Influence of t_{ox} on reverse conduction performance.



Figure 12. Influence of t_{ox} on reverse recovery performance.

4. Conclusions

A 4H-SiC lateral MOSFET featuring a trench MOS channel diode at the source side is investigated in detail and compared with a conventional LDMOS. The drawback of the device is the extra complexity of the fabrication process. However, the research results have demonstrated that TMCD can effectively suppress the parasitic PN junction diode and significantly enhance the reverse recovery characteristic. Compared with C-LDMOS, TMCD-LDMOS has a 63.5% reduction in the peak reverse recovery current, a 24.5% reduction in the reverse recovery charge, and a 31.3% reduction in the reverse recovery energy loss, giving the device a significant advantage in high-frequency applications.

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References

- Hossain, Z.; Imam, M.; Fulton, J.; Tanaka, M. Double-RESURF 700 V n-channel LDMOS with best-in-class on-resistance. In Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics, Sante Fe, NM, USA, 7 June 2002; pp. 137–140.
- Qiao, M.; Jiang, L.; Zhang, B.; Li, Z. A 700 V BCD technology platform for high voltage applications. J. Semicond. 2012, 33, 044004. [CrossRef]
- Disney, D.R.; Paul, A.K.; Darwish, M.; Basecki, R.; Rumennik, V. A new 800 V lateral MOSFET with dual conduction paths. In Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216), Osaka, Japan, 7 June 2001; pp. 399–402.
- Lee, S.H.; Jeon, C.K.; Moon, J.W.; Choi, Y.C. 700V lateral DMOS with new source fingertip design. In Proceedings of the 2008 20th International Symposium on Power Semiconductor Devices and IC's, Orlando, FL, USA, 18–22 May 2008; pp. 141–144.
- Su, R.Y.; Yang, F.J.; Tsay, J.L.; Cheng, C.C.; Liou, R.S.; Tuan, H.C. State-of-the-art device in high voltage power ICs with lowest on-state resistance. In Proceedings of the 2010 International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; pp. 20.8.1–20.8.4.
- 6. Ludikhuize, A.W.; Weijland, I.M.; Strijker, J.W. Method of Manufacturing a Multi-Path Lateral High-Voltage Field Effect Transistor. U.S. Patent 2008/0 093 641 A1, 24 April 2008.
- Kim, S.; Kim, J.; Prosack, H. Novel lateral 700 V DMOS for integration: Ultra-low 85 mΩ·cm² on-resistance, 750 V LFCC. In Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs, Bruges, Belgium, 3–7 June 2012; pp. 185–188.
- 8. Hamada, K.; Nagao, M.; Ajioka, M.; Kawai, F. SiC—Emerging power device technology for next-generation electrically powered environmentally friendly vehicles. *IEEE Trans. Electron Devices* **2015**, *62*, 278–285. [CrossRef]
- Östling, M.; Ghandi, R.; Zetterling, C. SiC power devices—Present status, applications and future perspective. In Proceedings of the 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, USA, 23–26 May 2011; pp. 10–15.
- 10. Cooper, J.A.; Melloch, M.R.; Singh, R.; Agarwal, A.; Palmour, J.W. Status and prospects for SiC power MOSFETs. *IEEE Trans. Electron Devices* **2002**, *49*, 658–664. [CrossRef]
- 11. Mantooth, H.A.; Glover, M.D.; Shepherd, P. Wide bandgap technologies and their implications on miniaturizing power electronic systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2014**, *2*, 374–385. [CrossRef]
- 12. Zhou, X.; Wang, Y.; Yue, R.; Dai, G.; Li, J. Physics-based SPICE model on the dynamic characteristics of silicon carbide Schottky barrier diode. *IET Power Electron.* **2016**, *9*, 2803–2807. [CrossRef]
- 13. Zhang, M.; Wei, J.; Zhou, X.; Jiang, H.; Li, B.; Chen, K.J. Simulation study of a power MOSFET with built-in channel diode for enhanced reverse recovery performance. *IEEE Electron Device Lett.* **2019**, *40*, 79–82. [CrossRef]
- Ebihara, Y.; Uehara, J.; Ichimyra, A.; Mitani, S.; Noborio, M.; Takeuchi, Y.; Tsuruta, K. Suppression of bipolar degradation in deep-P encapsulated 4H-SiC trench MOSFETs up to ultra-high current density. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 35–38.
- Tominaga, T.; Hino, S.; Mitsui, Y.; Nakashima, J.; Kawahara, K.; Tomohisa, S.; Miura, N. Superior switching characteristics of SiC-MOSFET embedding SBD. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 27–30.
- Jiang, H.; Wei, J.; Dai, X.P.; Zheng, C.W.; Ke, M.; Deng, X.; Sharma, Y.; Deviny, I.; Mawby, P. SiC MOSFET with built-in SBD for reduction of reverse recovery charge and switching loss in 10-kV applications. In Proceedings of the 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Sapporo, Japan, 28 May–1 June 2017; pp. 49–52.
- Yen, C.T.; Hung, C.C.; Hung, H.T.; Lee, L.S.; Lee, C.-Y.; Yang, T.-M.; Huang, Y.-F.; Cheng, C.-Y.; Chuang, P.-J. 1700V/30A 4H-SiC MOSFET with low cut-in voltage embedded diode and room temperature boron implanted termination. In Proceedings of the 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong Kong, China, 10–14 May 2015; pp. 265–268.
- 18. Zhou, X.T.; Gong, H.; Jia, Y.G.; Hu, D.Q.; Wu, Y.; Xia, T.; Pang, H.; Zhao, Y. SiC planar MOSFETs with Built-in Reverse MOS-channel Diode for Enhanced Performance. *IEEE J. Electron Devices Soc.* **2020**, *8*, 619–625. [CrossRef]
- 19. Huang, M.; Li, R.; Yang, Z.; Li, Y.; Zhang, X.; Gong, M. A Multiepi Superjunction MOSFET with a Lightly Doped MOS-Channel Diode for Improving Reverse Recovery. *IEEE Trans. Electron Devices* **2021**, *68*, 2401–2407. [CrossRef]
- 20. Zhou, X.; Pang, H.; Jia, Y.; Hu, D.; Wu, Y.; Tang, Y.; Xia, T.; Gong, H.; Zhao, Y. SiC Double-Trench MOSFETs with Embedded MOS-Channel Diode. *IEEE Trans. Electron Devices* **2020**, *67*, 582–587. [CrossRef]
- 21. Li, X.; Jia, Y.; Zhou, X.; Zhao, Y.; Wu, Y.; Hu, D.; Fang, X.; Deng, Z. A Novel Split-Gate-Trench MOSFET Integrated with Normal Gate and Built-In Channel Diode. *IEEE J. Electron Devices Soc.* **2021**, *9*, 839–845. [CrossRef]
- 22. Bao, M.T.; Wang, Y.; Li, X.J.; Liu, C.M.; Yu, C.H.; Cao, F. Simulation Study of Single Event Effects in the SiC LDMOS with A Step Compound Drift Region. *Microelectron. Reliab.* **2018**, *91*, 170–178. [CrossRef]

- 23. Bao, M.T.; Wang, Y.; Yu, C.H.; Cao, F. A SiC LDMOS with Electric Field Modulation by A Step Compound Drift Region. *Superlattices Microstruct.* **2018**, *119*, 94–102. [CrossRef]
- 24. Wang, Y.L.; Duan, B.X.; Sun, L.C.; Yang, X.; Huang, Y.; Yang, Y. Breakdown Point Transfer Theory for Si/SiC Heterojunction LDMOS with Deep Drain Region. *Superlattices Microstruct.* **2021**, *151*, 106810. [CrossRef]
- Kong, M.F.; Duan, Y.M.; Gao, J.H.; Yan, R.H.; Zhang, B.; Yang, H. A Novel Optimum Variation Lateral Doping SiC Lateral Double-Diffused Metal Oxide Semiconductor with Improved. *Semicond. Sci. Technol.* 2022, *37*, 105022. [CrossRef]
- 26. Tahne, B.A.; Naderi, A.; Heirani, F. Reduction in Self-Heating Effect of SOI MOSFETs by Three Vertical 4H-SiC Layers in the BOX. *Silicon* 2020, 12, 975–986. [CrossRef]
- 27. Silvaco Int. Two-Dimensional Device Simulation Program; Silvaco Int.: Santa Clara, CA, USA, 2012.
- MUsman, M. Nawaz. Device design assessment of 4H–SiC n-IGBT—A simulation study. Solid-State Electron. 2014, 92, 5–11. [CrossRef]
- 29. Wang, Y.; Ma, Y.C.; Hao, Y.; Hu, Y.; Wang, G. Simulation Study of 4H-SiC UMOSFET Structure with p+-polySi/SiC Shielded Region. *IEEE Trans. Electron Devices* 2017, 64, 3719–3724. [CrossRef]

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