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A Novel Non-Isolated High-Gain Non-Inverting Interleaved DC–DC Converter

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Abstract: High-gain DC–DC converters are being drastically utilized in renewable energy generation systems, such as photovoltaic (PV) and fuel cells (FC). Renewable energy sources (RES) persist with low-level output voltage; therefore, high-gain DC–DC converters are essentially integrated with RES for satisfactory performance. This paper proposes a non-isolated high-gain non-inverting interleaved DC–DC boost converter. The proposed DC–DC converter topology is comprised of two inductors and these are charging and discharging in series and parallel circuit configurations. The voltage multiplier technique is being utilized to produce high gain. The proposed topology is designed to operate in three modes of operation. Three switches are operated utilizing two distinct duty ratios to avoid the extreme duty ratio while having high voltage gain. Owing to its intelligent design, the voltage stress on the switches is also significantly reduced where the maximum stress is only 50% of the output voltage. The proposed converter's steady-state analysis with two distinct duty ratios is thoroughly explored. Furthermore, a 160 W 20/400 V prototype is developed for performance analysis and validation. The converter topology can generate output voltage with a very high voltage gain of 20, which is verified by the prototype. Moreover, a high efficiency of 93.2% is attained by the proposed converter's hardware prototype.

Keywords: non-isolated DC–DC converter; non-inverting; high gain; switching stress; renewable energy

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1. Introduction

In recent years, energy generation using renewable energy sources (RES) has significantly contributed to sustainable development globally [1,2]. Photovoltaic (PV) has gained remarkable popularity among other renewable energy sources. PV systems have already outperformed with both on-grid and off-grid-connected systems [3,4]. Power generation systems utilizing RES generates a low-level output voltage; therefore, requisite effective DC–DC converters having higher voltage gain capability [5]. Other than renewable power conversion, numerous other applications utilize DC–DC converters, such as electric vehicles, electric traction systems, power back-up systems, surgical equipment, and lighting applications [6,7]. In earlier times, conventional DC–DC converters were opted for voltage-boosting applications. However, conventional DC–DC boost converters persist with high switching stress that is equivalent to the output voltage [8]. Therefore, it requires switches with higher power ratings that ultimately increase the conduction losses to cater to the higher switching stress. Furthermore, choosing higher duty ratios to acquire high voltage gain induces high voltage spikes, conduction losses, and generates diode reverse recovery issues [9].

Nowadays, various DC–DC converter topologies with high-gain capabilities are available as per the application requirements [10]. High-gain DC–DC converters are further distributed within two clusters, named as isolated and non-isolated converter topologies [11]. Numerous isolated converter topologies to acquire high voltage gain are elaborated in the literature [12]. However, isolated converter topologies have substantial problems that include thermal impact, high voltage ripples on the power switches, leakage inductance, core saturation, and their large size makes them more expensive [11,13]. Thus, non-isolated converter topologies are opted for instead, for higher voltage gain; these are smaller in size and cost-effective, considering that no galvanic isolation is required [14,15].

Non-isolated converter topologies are also designed for specific applications, such as electric vehicles (EV). In [16], three-phase interleaved parallel bi-directional converter topology is integrated with EV that offer multi-phase circuit topology, and the operation is based on multiple stages with different duty cycle ranges in order to fulfil the EV power requirements in a smooth manner. Another multi-phase interleaved boost converter topology using an auxiliary resonant circuit is presented in [17]; it has the capability of soft switching and high voltage gain. For fuel cell integration non-isolated interleaved high-gain converter topologies are presented in [18,19]; these interleaved topologies offer an improved DC bus regulation for the fuel cell irrespective of the intermittent source voltage. Furthermore, within the category of non-isolated high-gain converters most widely utilized, the topologies are quadratic boost [20], with a wide range of duty cycle ratios usually operated with a single switch; however, it has higher switching and diode stress in comparison to other non-isolated converter topologies. In [21], a cascaded boost converter utilizes the initial stage for voltage boosting with a higher duty ratio, whereas the second stage operates with a nominal duty ratio with lower switching stress in comparison to the first stage of the converter topology. Besides high-gain capability, it persists with some severe issues that include higher component count that results in poor efficiency, and it also possesses a diode reverse-recovery issue. Coupled inductor cascaded boost is presented in [22], and significantly high voltage gain could be attained by utilizing an extreme duty ratio for the operation of the converter or through increasing the coupled inductor's turns ratio; it is considered a design tradeoff. Due to excessive current stress across the switch, it is incompatible with the high-power applications. Another converter topology utilizing the voltage lifting approach is demonstrated in [23]; it overcomes the effect of parasitic elements in DC–DC converters and has improved power transfer efficiency. However, it has high switching stress and high passive component count, and is, therefore, not suitable for high-power applications. In [24], an active–passive inductor cell (APIC) converter topology is presented. Higher voltage gain along with optimal duty cycle are the highlighted merits for the proposed topology. In contrast, the high-power application requires higher active–passive inductor cells that will increase the complexity of the converter and will have high stress on the switches. However, with the addition of a switched-capacitor or switched-capacitor inductor, a power converter's complexity, along with the cost, increases significantly.

Various coupled inductor integrated DC–DC converter topologies are capable of generating higher gain factor along with less or optimum switching stress switches relying on the duty cycle ratio variation [25]. In certain cases, to attain the requisite voltage conversion set-point, the inductor turns ratio is increased; this results in an excessive input current ripple [26]. Therefore, the input current ripple requires optimization utilizing the filter at the input side, as depicted in [27]. In [28], a single-switch and single-inductor cascaded converter topology is presented, to acquire higher gain factor along with less input current ripple; however, it has quite a high component count and also possess harmonics due to capacitors; hence, it is not advisable for high-power loads. Furthermore, high-gain factor hybrid converter topologies are discussed in [24,29,30].

This paper presents, a high-gain non-inverting interleaved boost converter topology to resolve the aforementioned issues. By using appropriate component values and

suitable duty ratios, the proposed topology produces higher voltage gain. Furthermore, the proposed topology has these subsequent advantages:

(1) The proposed converter topology is operated utilizing two distinct duty cycle ratios to achieve higher voltage gain.
(2) The energy stored in the inductor is delivered to the voltage multiplier and supplied to the load.
(3) The proposed converter topology achieves significantly higher voltage gain factor in comparison to the conventional boost and other high-gain converter topologies proposed in [8,22,23,30–34].
(4) Voltage stress is significantly lower across the diodes and the switches as compared to the voltage output percentage.

Section 2 discusses the circuit arrangement of the proposed boost converter topology in detail. Steady-state analysis for the proposed DC–DC boost converter topology is illustrated in Section 3. Section 4 elaborates on the efficiency evaluation of the proposed topology. A performance evaluation of the proposed topology with respect to the voltage stress across the diodes, switches, and voltage gain is discussed in Section 5. Hardware results of the proposed converter topology is described in Section 6. Furthermore, a conclusion of the results for the proposed topology is highlighted in Section 7.

2. Circuit Configuration

The circuit of the proposed converter topology is demonstrated in Figure 1, which is comprised of three power switches, S_X, S_Y, and S_Z, two inductors, L_X and L_Y, four diodes, D_1, D_2, D_3, and D_4, and three capacitors, C_1, C_2, C_o. The power switches, S_X, S_Y, and S_Z, are operated with a switching frequency f_{sw}. The switches, S_X and S_Y, are operated with a duty ratio denoted as D_1, whereas S_Z is operated with a duty ratio D_2.

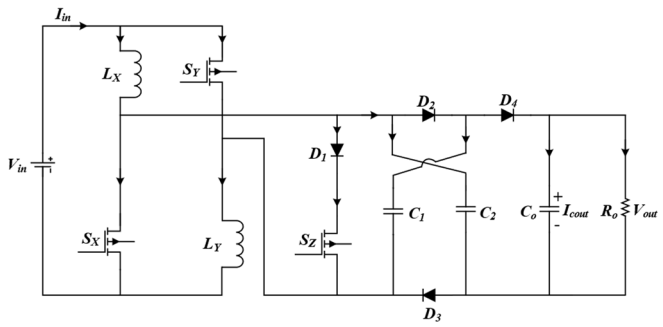


Figure 1. Proposed non-isolated high-gain non-inverting interleaved converter.

Some suppositions are considered while explaining the proposed converter topology's steady-state operation, including: (1) All of the components in the circuit are ideal. The impact of forward voltage drop, switch ON state resistance, and equivalent series resistance (ESR) for the capacitors and the inductors are ignored; (2) To maintain the stable output voltage, the output capacitor C_o is adequately large. Assume that the two inductors have an equivalent number of turn ratios.

$$L_X = L_Y = L \tag{1}$$

Therefore, a similar voltage is across both the inductors, V_{LX} and V_{LY}, depicted in Equations (2) and (3).

$$V_{LX} = L_X \frac{diL_X}{dt} = L \frac{diL_X}{dt} \tag{2}$$

$$V_{LY} = L_Y \frac{diL_Y}{dt} = L \frac{diL_Y}{dt} \tag{3}$$

3. Proposed Converter's Steady-State Analysis

This section elaborates on the operating modes in continuous conduction mode (CCM) of the proposed boost converter topology. There are three operational modes with two distinct duty ratios within a single switching period for the proposed converter. The output response in CCM for the proposed topology is illustrated in Figure 2.

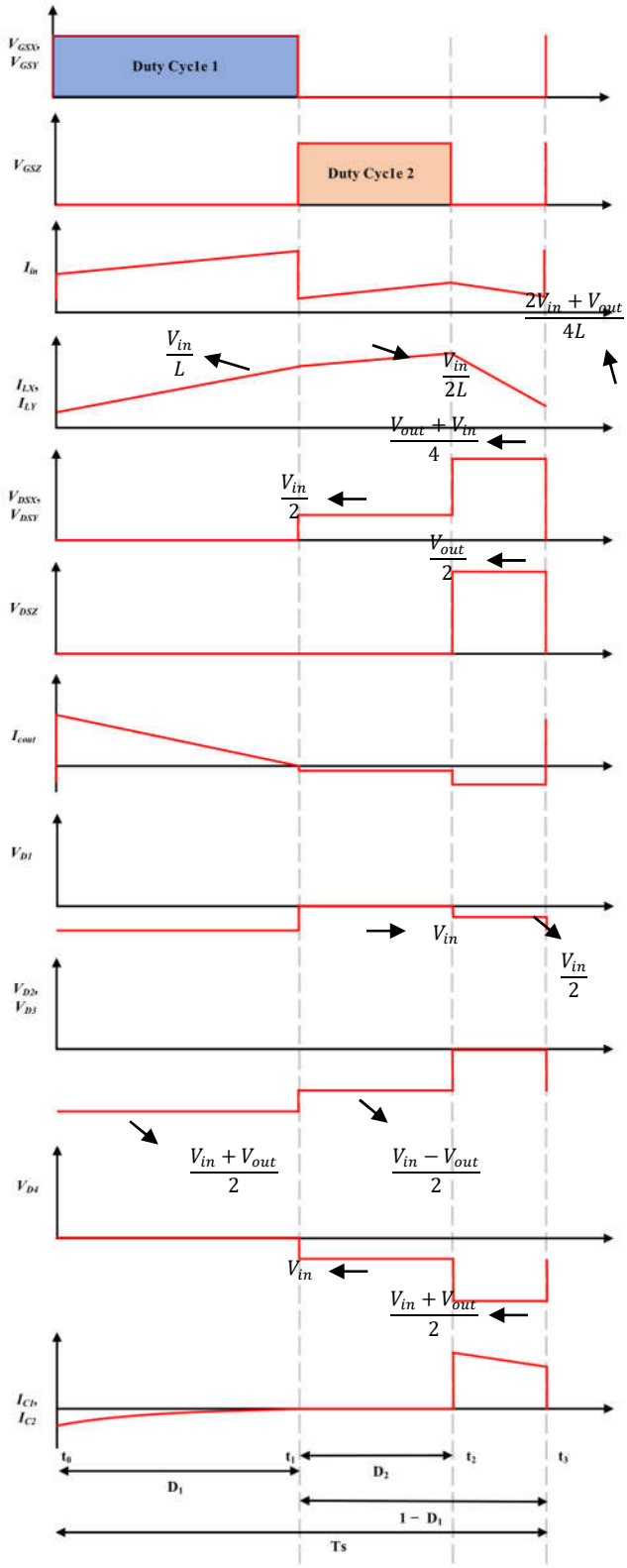


Figure 2. CCM operation of the proposed DC–DC boost converter topology.

3.1. Working in Continuous Conduction Mode

Mode I: The mode I time interval is [t_o − t_1]; switches S_X and S_Y are turned ON, whereas the third switch S_Z remains in the OFF state. Throughout this operation, the circuit's current direction is illustrated in Figure 3a. Here, the input energy will be supplied to the two inductors L_X and L_Y, and the capacitor C_o will supply stored energy at the output. The diodes D_1 and D_4 remains in reversed bias, whereas the inner diode of the third switch S_Z remains in the forward-biased state. Thus, even if the third switch S_Z remains in an OFF state, the conduction voltage will be present across it. As the inductors and the source are parallel to each other in this mode, the inductor voltages are presented as follows:

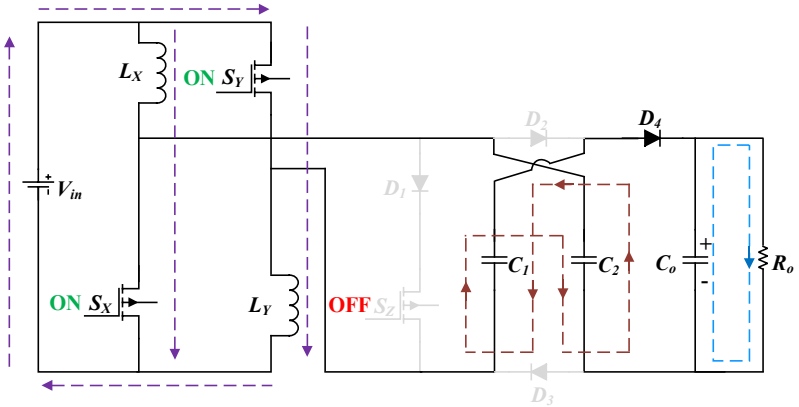
$$V_{LX} = V_{LY} = V_{in} \tag{4}$$

To obtain (5), (2) and (3) are substituted into (4)

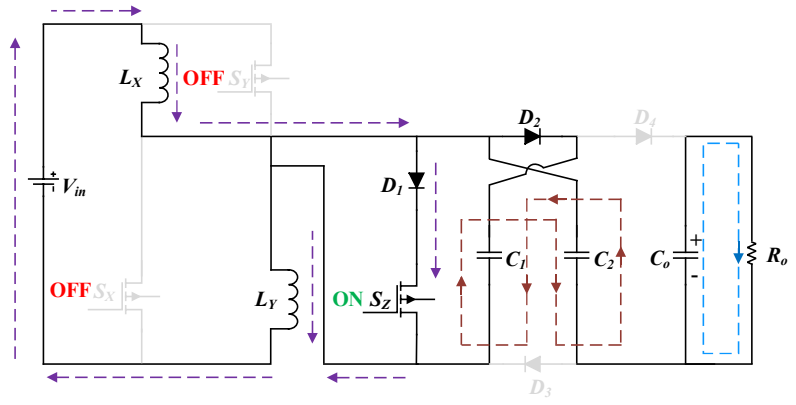
$$L\frac{diL_X}{dt} = L\frac{diL_Y}{dt} = L\frac{diL}{dt} = V_{in}, \quad t_o \le t \le t_1 \tag{5}$$

$$\frac{diL_X}{dt} = \frac{diL_Y}{dt} = \frac{diL}{dt} = \frac{V_{in}}{L} \tag{6}$$

$$\frac{diL}{dt} = \frac{V_{in}}{L} \tag{7}$$



(**a**)



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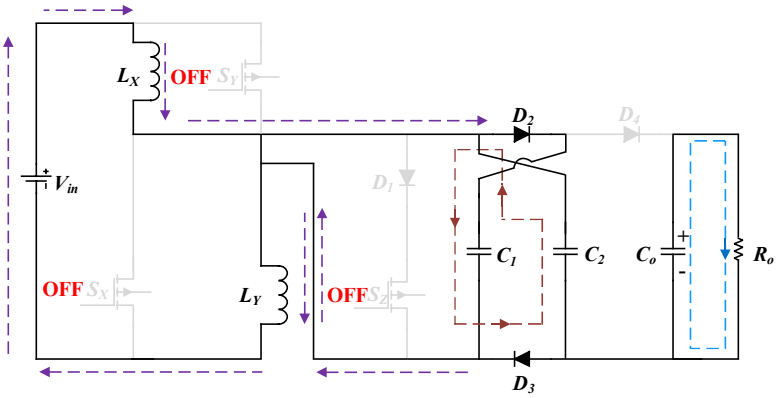


(**c**)

Figure 3. Operational modes in CCM: (**a**) mode I; (**b**) mode II; (**c**) mode III.

Mode II: The mode II time interval is [t_1 – t_2]; the third switch S_Z is turned ON, whereas the two switches S_X and S_Y remains in the OFF state. Thus, the current direction of the circuit in mode II is demonstrated in Figure 3b. The two inductors L_X, and L_Y are fed by the input source, and the circuit current flows through L_X, D_1, D_4, and L_Y. The switching stress on S_X and S_Y in this mode is half of the supplied voltage. Furthermore, the output capacitor C_o delivers the accumulated energy at the output load as D_4 is not in a forward-biased condition. The two inductors and the input source are connected in this mode. Expressions for calculating the inductor current and voltage are as follows:

$$iL_X = iL_Y = iL \tag{8}$$

$$V_{LX} + V_{LY} = V_{in} \tag{9}$$

$$L\frac{diL_X}{dt} + L\frac{diL_Y}{dt} = V_{in} \tag{10}$$

Since the two inductors L_X and L_Y are coupled in series to the source voltage V_{in}, and i_L current flowing through the inductors L_X and L_Y. By substitution of (2) and (3) into (8), the subsequent expression is attained:

$$\frac{diL}{dt} = \frac{V_{in}}{2L}, \quad t_1 \le t \le t_2 \tag{11}$$

Mode III: The mode III time interval is [t_2 – t_3]; and all three switches S_X, S_Y, and S_Z are in the OFF state. Figure 3c depicts the circuit's current path in mode III. Thus, in mode III, the input source together with the both inductors feed the output load. The diode D_1 is under the non-conduction state, being reverse-biased. Additionally, D_2 is in the forward-biased state that enables output capacitor C_o to be charged in this mode. The switching stress across S_X and S_Y is half of the average of source voltage and the output voltage, while for the voltage stress, the third switch S_Z is half related to the output voltage.

The two inductors L_X and L_Y are coupled in series to the input source in this mode. Expressions for calculating the inductor current and voltage are as follows:

$$iL_X = iL_Y = iL \tag{12}$$

$$VL_X + VL_Y = V_{in} - \frac{V_{out}}{2} \tag{13}$$

$$2L\frac{diL}{dt} = V_{in} - \frac{V_{out}}{2} \tag{14}$$

Where the converter's output voltage is V_{out}. By substitution of (2) and (3) into (13) and simplifying (14), the following expression (15) is attained: voltage. Both the inductors are coupled in a series connection to the input source in this mode. Expressions for calculating the inductor's current and voltage is attained as follows:

$$\frac{diL}{dt} = \frac{2V_{in} - V_{out}}{4L}, \quad t_2 \le t \le t_3 \tag{15}$$

By implying the state-space averaging technique, the subsequent expressions are attained from (7), (11), and (15):

$$\int_0^{D_1T_s} \left(\frac{diL}{dt}\right)^{I} dt + \int_0^{D_2T_s} \left(\frac{diL}{dt}\right)^{II} dt + \int_0^{(1-D_1-D_2)T_s} \left(\frac{diL}{dt}\right)^{III} dt = 0 \tag{16}$$

Simplifying (16), the voltage gain expression is obtained:

$$\frac{V_{out}}{V_{in}} = \frac{2(D_1 + 1)}{(1 - D_1 - D_2)} \tag{17}$$

3.2. Switching Stress

The switching stress on all three switches V_{DSX}, V_{DSY}, and V_{DSZ} is depicted in Figure 2, correspondingly, and is expressed as follows:

$$\begin{cases} V_{DS1} = V_{DS2} = \dfrac{V_{in} + V_{out}}{4} \\ V_{DS3} = \dfrac{V_{out}}{2} \end{cases} \tag{18}$$

3.3. Diode Voltage Stress

The diode voltage stress V_{D1}, V_{D2}, V_{D3}, and V_{D4} on the diodes D_1, D_2, D_3, and D_4 is expressed as follows:

$$\begin{Bmatrix} V_{D1} = V_{in} \\ V_{D2} = V_{D3} = V_{D4} = \dfrac{V_{in} + V_{out}}{2} \end{Bmatrix} \tag{19}$$

3.4. Component Selection

To obtain the appropriate performance of converter topology, adequate component selection is critical. The proposed converter topology's component selection comprises suitable inductor and capacitor calculations.

3.4.1. For Inductor

The appropriate inductor selection [35] relies on the input voltage V_{in}, duty ratio D_1, ripple current Δi_L, and the switching frequency fsw. For the optimum operation of proposed converter topology in CCM mode, an appropriate inductor value is determined by the following equation:

$$L_X = L_Y = \frac{V_{in} * D_1}{\Delta iL * f_{sw}} \tag{20}$$

3.4.2. For Capacitor

Obtain optimum values for the selection of the output capacitor C_o relies on the output voltage V_{out}, ripple voltage ΔV_c, switching frequency f_{sw}, and the output power of the converter P_{out}. These are attained by using the following expression:

$$C_{out} = \frac{P_{out}}{V_{out} * \Delta V_c * f_{sw}} \tag{21}$$

Respectively, the capacitance value for C_1 and C_2 are similar in order to avoid voltage distortions.

4. Efficiency Evaluation

The efficiency evaluation of the proposed converter topology is discussed with details for each of the operational modes. Figure 4. depicts the proposed converter's equivalent circuit. Thus, equivalent series resistance (ESR) for both of the inductors L_X and L_Y are denoted as r_{LX} and r_{LY}. Furthermore, ESR for the two capacitors C_1 and C_2 are denoted by r_{C1}, r_{C2}. Correspondingly, for the diodes D_1, D_2, D_3, and D_4, their internal resistances are represented by r_{D1}, r_{D2}, r_{D3}, and, r_{D4} and the voltage drop on the diodes are denoted by V_{D1}, V_{D2}, V_{D3}, and V_{D4}. Similarly, ON-state resistance for all the three switches S_X, S_Y, and S_Z are indicated by r_{SX}, r_{SY}, and, r_{SZ}.

MODE I: The time interval for mode I is D_1T_S; the two switches S_X and S_Y are in an ON state while the third switch S_Z remains in an OFF state; the average capacitor current I_{cout} and the inductor voltage V_{LX} are expressed as:

$$I_{cout}^{I} = iL_X - \frac{V_{out}}{R_o} \tag{22}$$

$$V_{LX}^{I} = V_{in} - i_{LX}(r_{LX} + r_{SX}) \tag{23}$$

MODE II: The time interval for mode II is D_2T_S; the two switches S_X and S_Y are in an OFF state, whereas the third switch S_Z is in an ON state; the average capacitor current I_{cout} and the inductor voltage V_{LX} are expressed as:

$$I_{cout}^{II} = -\frac{V_{out}}{R_o} \tag{24}$$

$$V_{LX}^{II} = \frac{V_{in} - I_{LX}(r_{LX} + r_{LY}) - I_{in}(r_{D2} + r_{SZ}) - V_{D1}}{2} \tag{25}$$

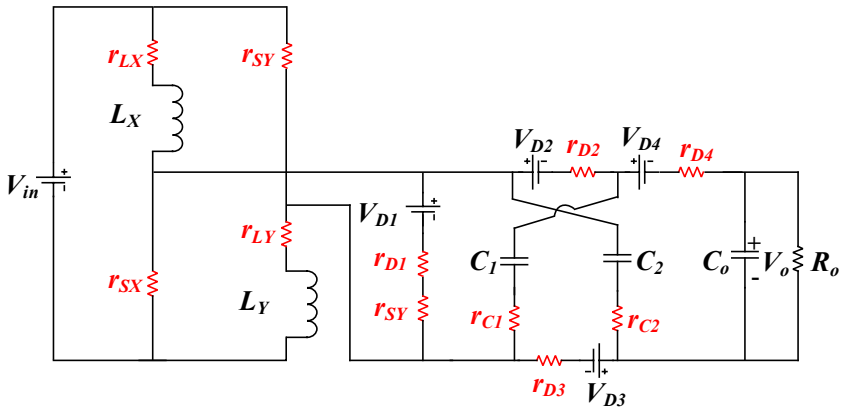


Figure 4. Proposed converter's equivalent circuit.

MODE III: The time interval for mode III is $(1 - D_1 - D_2)$; all the switches S_X, S_Y, and S_Z are in an OFF state, while the average capacitor current I_{cout} and the inductor voltage V_{LX} are expressed as:

$$I_{cout}^{III} = -\frac{V_{out}}{R_o} \tag{26}$$

$$V_{LX}^{III} = \frac{V_{in} - I_{LX}(r_{LX} + r_{LY}) - \frac{V_{out}}{2} - \frac{V_{out}}{2}(r_{C2} + r_{D3}) - V_{D3}}{2} \tag{27}$$

To obtain (28), an ampere-second balance approach is implemented for the output capacitor C_o.

$$\int_0^{D_1T_S} I_{co}^{I}\, dt + \int_0^{D_2T_S} I_{co}^{II}\, dt + \int_0^{(1-D_1-D_2)T_S} I_{co}^{III}\, dt = 0 \tag{28}$$

Inductor current through I_{LX} is obtained by simplifying (28):

$$I_{LX} = -\frac{V_{out}}{R_o D_1} \tag{29}$$

By implementing a volt-second balance approach to the inductor L_X, expression (30) is attained.

$$\int_0^{D_1 T_s} V_{LX}^{I}\, dt + \int_0^{D_2 T_s} V_{LX}^{II}\, dt + \int_0^{(1-D_1-D_2)T_s} V_{LX}^{III}\, dt = 0 \tag{30}$$

The output voltage obtained in (31) is achieved by simplifying (30).

$$V_{out} = \frac{2[V_{in}(1+D_1) - (V_{D1}D_2) - (V_{D3}(1-D_1-D_2))]}{\left(\frac{D_1X_1 + D_2X_2 + X_3}{R_o D_1}\right) + (1-D_1-D_2)} \tag{31}$$

where,

$$\begin{gathered} X_1 = 2r_{LX} + 4r_{SX} - r_{C2} - r_{D3} - r_{D4} - 2r_{LY} \\ X_2 = \frac{2(r_{D2} - r_{SZ})(r_{D2} - r_{C1})(r_{D3} - r_{C2})}{(r_{D1} - r_{SZ})(r_{D2} + r_{C1} + r_{D3} + r_{C2}) + (r_{D2} - r_{C1})(r_{D3} - r_{C2})} - 2r_{C2} \\ - 2r_{D3} - 2r_{D4} \\ X_3 = 2r_{LX} + 2r_{LY} + r_{C2}\& + r_{D3} + r_{D4} \end{gathered} \tag{32}$$

The expressions for the input and output powers are as follows:

$$P_{in} = 2V_{in}I_{LX}D_1 + V_{in}I_{LX}D_2 + V_{in}I_{LX}(1-D_1-D_2) \tag{33}$$

The input power is attained by substituting (29) into (33).

$$P_{in} = \frac{V_{in}V_{out}(1+D_1)}{R_o(1-D_1-D_2)} \tag{34}$$

$$P_{out} = \frac{V_{out}^2}{R_o} \tag{35}$$

The efficiency evaluation of the proposed converter topology related to conduction losses is expressed in (37), and calculated by using (31), (34), and (35).

$$\eta = \frac{P_{out}}{P_{in}} \tag{36}$$

$$\eta = \frac{2[V_{in}(1+D_1) - V_{D1}D_2 - V_{D3}(1-D_1-D_2)]D_1}{V_{in}(1+D_1)(1-D_1-D_2) + \left[\frac{(D_1X_1 + D_2X_2 + X_3)}{R_o D_1}\right]} \tag{37}$$

Considering the switching losses (P_{sw}), expression (38) is derived for the output power for the proposed converter topology.

$$P_{out} = \frac{V_{out}^2}{R_o} - P_{SW} \tag{38}$$

$$P_{SW} = V_{DS}I_D(t_{rise} + t_{fall})f_{SW} \tag{39}$$

Thus, V_{DS} is the MOSFET's voltage from drain to source, I_D represents the drain current of the MOSFET, f_{sw} represents switching frequency, and t_{rise} and t_{fall} are the MOSFET's rise time and fall time. The proposed converter's efficiency is expressed in (40), which is calculated by using (31), (32), (34), and (39).

$$\eta = \frac{\left[\frac{V_{out}^2}{R_o} - P_{SW}\right]}{\left[\frac{V_{in}V_{out}(1+D_1)}{R_o D_1}\right]} \tag{40}$$

Considering the capacitor losses for the proposed converter, the output power is attained as:

$$P_{out} = \frac{V_{out}^2}{R_o} - P_{rc} \tag{41}$$

$$P_{rc1} = \left\{\frac{D_1 + (A-1)D_2(1+D_1)}{(1-D_1-D_2)}\right\}^2 \frac{P_o}{R} r_C \tag{42}$$

$$P_{rc2} = \left\{\frac{D_1 + (A-1)D_2(1+D_1)}{(1-D_1-D_2)}\right\}^2 \frac{P_o}{R} r_C \tag{43}$$

$$P_{rco} = \left\{\frac{D_1(1+3D_1+D_2)}{(1-D_1-D_2)}\right\}^2 \frac{P_o}{R} r_C \tag{44}$$

$$A = \frac{2(r_D + r_{S3})}{2r_D + 2r_{S3} + r_D + r_C} \tag{45}$$

$$P_{rc} = P_{rc1} + P_{rc2} + P_{rco} \tag{46}$$

$$P_{rc} = \frac{2\{D_1 + (A-1)D_2(1+D_1)\}^2 + \{D_1(1+3D_1+D_2)\}^2}{(1-D_1-D_2)^2} * \frac{P_o}{R} \tag{47}$$

Power losses for all the three capacitors C_1, C_2, and C_o are expressed in (42), (43), and (44), respectively, whereas the total capacitor power losses P_{rc} is expressed in (48). The proposed converter's efficiency considering the capacitor losses is expressed in (47).

$$\eta = \frac{\left[\frac{V_{out}^2}{R_o} - P_{rc}\right]}{\left[\frac{V_{in}V_{out}(1+D_1)}{R_o D_1}\right]} \tag{48}$$

5. Comparative Performance Analysis

The proposed converter's characteristics comparison is determined in Table 1 with conventional and high-gain converter topologies. Comparative performance analysis of the proposed converter topology is mainly dependent on the fundamental parameters: voltage gain, switching stress, diode stress, and the quantity components. Table 1 includes converter topologies with one power switch and single duty ratio D presented in [22] and [8] and two power switches and double duty ratios D_1 and D_2 [33], whereas [34] is based on two power switches and single duty ratio D, and three power switches and double duty ratio D_1 and D_2 are included in [23,30–32]. Table 1 depicts the voltage gain equation of the proposed converter topology. It is evident that converter topologies with double duty ratios have higher gain factor and satisfactory switching stress. Similarly, the proposed topology utilizes three power switches that are operated by two distinct duty ratios, and it has a higher voltage gain, as depicted in Table 1. The calculated value of duty ratios $D_{new[p]}$ is 85% where D_1 = 50% and D_2 = 35%. By splitting the duty ratio into two, it becomes convenient to operate the converter topology utilizing a higher duty cycle ratio within optimum operational limits; converter topologies with a single duty ratio cannot be operated by using extreme duty ratios. Moreover, the switching stress and diode stress for the proposed converter topology is less in contrast to converter topologies depicted in [23,30–32]. Furthermore, Figure 5 depicts the assessment of the proposed converter topology and the established converter topologies with respect to voltage gain versus duty ratio. The plot depicted in Figure 5 determines the output response of the proposed topology by iterating the duty ratio D_1, whereas another duty ratio D_2 remains fixed at 0.35. The proposed converter has achieved a higher voltage gain factor of 50 with a duty ratio of D_1 0.6 and D_2 0.35. Whereas, converter topologies in [8,22,30,34] have acquired a voltage gain of less than 15, and converter topologies in [23,31,32] have obtained a voltage gain between 3 and 11. However, all the converter topologies were tested with a similar duty cycle ratio

of 0.6. Moreover, Figure 6 illustrates the voltage gain response for the proposed converter topology under multiple variations in both duty ratios D_1 and D_2. Thus, it is shown that by applying suitable duty ratios D_1 and D_2, the proposed converter topology is competent for generating significant voltage gain.

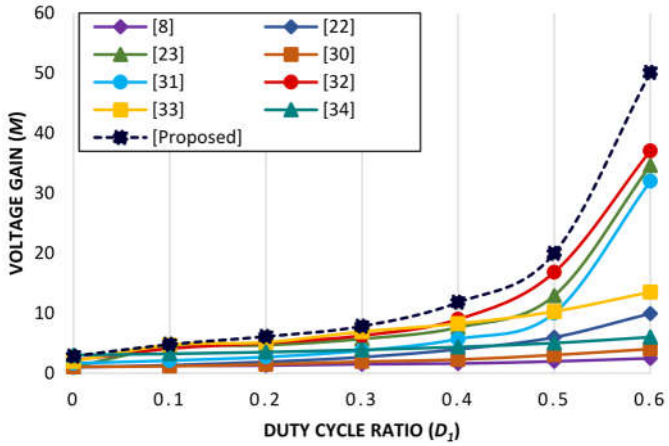


Figure 5. Voltage gain comparison among various recently proposed DC–DC converters.

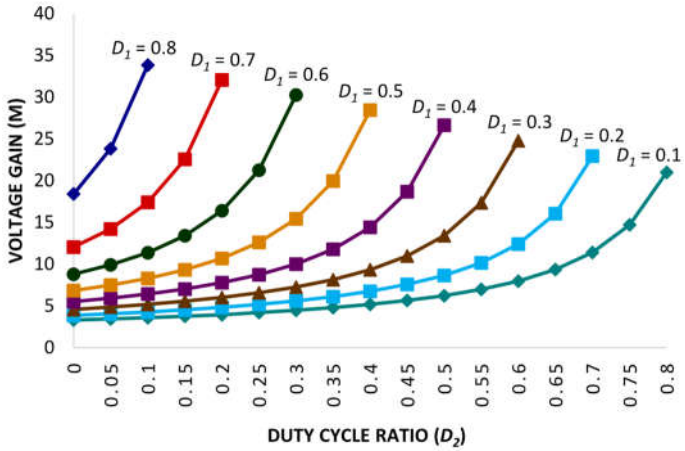


Figure 6. Voltage gain response under varying duty ratios D_1 and D_2 for the proposed converter.

Table 1. Steady-state analysis and the component count comparison.

Converter Topologies	Voltage Gain	Voltage Gain (%)	Switching Stress	Diode Stress	Switches	Inductors	Diodes	Capacitors
Conventional Boost Converter [8]	$\frac{1}{(1-D)}$	10	$V_{DS} = V_{out}$	V_0	1	1	1	1
Converter in [22]	$\frac{1+D}{(1-D)^2}$	12	$V_{DS} = V_{out}$	$V_{D1} = V_{C1}$ $V_{D2} = \frac{V_{out} + V_{C1}}{1+n_2}$ $V_{D3} = V_{out} + nV_{C1}$ $V_{D4} = V_{C2}$ $V_{D5} = V_{out} - V_{C2}$ $V_{D6} = V_{out} - V_{C3}$	1	4	6	4
Converter in [23]	$\frac{(3D_1 - 2D_2)}{(1-D_1-D_2)}$	11.11	$V_{DSX} = V_{DSY} = \frac{V_{out} - V_i}{2}$ $V_{DSZ} = V_{out} - 2V_{in}$	$V_{D1} = V_2 = -(V_{out} - V_{in})$ $V_{D3} = \frac{-(V_{out} - V_{in})}{2}$	3	2	3	3

Converter in [30]	$\frac{1+D}{1-D}$	3	$V_{DSX} = V_{DSY} = \frac{V_{out}+V_i}{2}$ $V_{DSZ} = V_{out} + V_{in}$	-	3	2	0	1
Converter in [31]	$\frac{(1+D_1)}{(1-D_1-D_2}$	10	$V_{DSX} = V_{DSY} = \frac{V_{out}+V_{in}}{2}$ $V_{DSZ} = V_{out}$	$V_{D1} = V_{in}$ $V_{D2} = V_{in} + V_{out}$	3	2	2	2
Converter in [32]	$\frac{(2-D_1)}{(1-D_1-D_2}$	10.52	$V_{DSX} = V_{DSY} = \frac{V_{out}}{2}$ $V_{DSZ} = V_{out}$	$V_{D1} = V_{D2} = \frac{V_{out}}{2}$ $V_{D3} = V_{out}$	3	2	3	2
Converter in [33]	$\frac{2}{(1-D_1-D_2}$	13.33	$V_{DSX} = V_{DSY} = \frac{V_{out}}{2}$	$V_{D1} = V_{D2} = V_{D3}$ $= V_{D4} = \frac{V_{out}}{2}$	2	2	4	4
Converter in [34]	$\frac{(1+D)}{(1-D)}$	8.3	$V_{DSX} = V_{DSY}$ $= \frac{V_{in}+V_{out}}{2}$	$V_D = V_{in} + V_{out}$	2	2	1	1
Proposed Converter	$\frac{2(1+D_1)}{(1-D_1-D_2}$	20	$V_{DSX} = V_{DSY} = \frac{V_{in}+V_{ou}}{4}$ $V_{DS3} = \frac{V_{out}}{2}$	$V_{D1} = V_{in}$ $V_{D2} = V_{D3} = V_{D4}$ $= \frac{V_{in}+V_{out}}{2}$	3	2	4	3

Hence, the overall voltage stress for the proposed converter topology remains relatively low; for the power switches S_X and S_Y, the voltage stress is 25% with respect to the output voltage, whereas the power switch S_Z has 50% voltage stress with respect to the output voltage. Moreover, the switching stress for the converters presented in [8,22] is 100% of the output voltage. For converters presented in [33,34], the voltage stress for switches S_X and S_Y is 50% of the output voltage. Whereas, the converter topologies presented in [23,30–32] persist with a different switching voltage stress pattern; two of the switches S_X and S_Y have 50% voltage stress of the output voltage, and the switch S_Z has 100% voltage stress of the output voltage. However, it is evident for the proposed converter topology that it has significantly low switching voltage stress related to the converter topologies discussed in Table 1. Similarly, the voltage stress on the diodes is also low related to the converter topologies discussed in Table 1. Furthermore, the number of component counts for the converter topologies includes the quantity of switches, inductors, diodes, and capacitors. The measure of component counts for the converter topologies is between 4 and 15, since conventional and high-gain converter topologies are considered to persist with a slightly higher number of component counts. However, the component count for the proposed topology is 12, which includes three switches, three inductors, four diodes, and three capacitors. Whereas in [22], the component count is 15, and the similar high-gain converter topology presented in [33] has a component count of 12, equivalent to the proposed converter topology. Theoretical efficiency under varying duty ratios D_1 and D_2 is demonstrated in Figure 7. Thus, the efficacy of the proposed converter topology is evaluated, and remained higher than 90%. Additionally, the voltage gain for the proposed converter topology is higher than the converter topologies discussed in Table 1. Moreover, to acquire high voltage gain with optimum efficiency, the duty cycle ratio must be adequately selected considering the following limitations: (1) both the duty ratios D_1 and D_2 must not be equivalent to 0.5, and (2) the total duty ratios D_1 and D_2 must be less than 1.

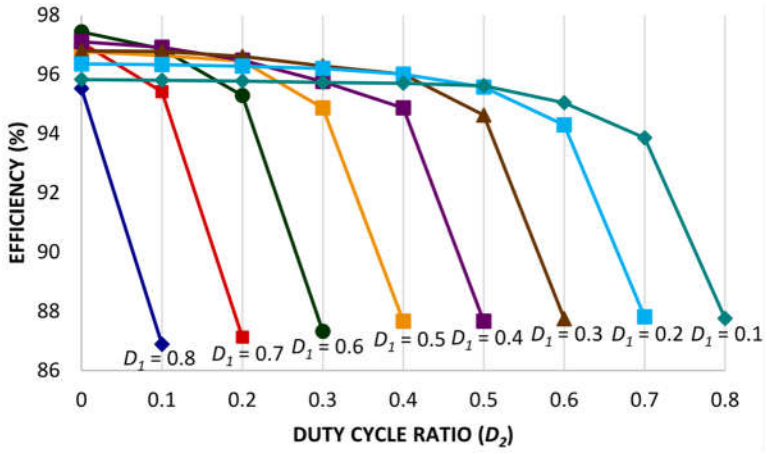


Figure 7. Proposed converter's theoretical efficiency under varying duty cycle ratios D_1 and D_2.

6. Experimental Results

To verify and evaluate the theoretical results of the proposed converter topology, a 160 W prototype has been developed, as depicted in Figure 8. The design parameters and component specifications are illustrated in Table 2. To operate the proposed converter topology with appropriate switching gate pulses, phase delay, and duty ratio, an Arduino UNO is integrated in the hardware setup. The gate pulses V_{GSX}, V_{GSY}, and V_{GSZ} to regulate the switches S_X, S_Y, and S_Z are depicted in Figure 9a. The two switches S_X and S_Y are operated by gate pulses V_{GSX} and V_{GSY} using a switching frequency of 50 kHz with a duty ratio D_1 of 0.5. The switch S_Z is operated by gate pulse V_{GSZ} with a 180° phase shift, a similar switching frequency of 50 kHz, and a duty ratio D_2 of 0.35. The input voltage and input current results V_{in} and $I_{in,}$ along with the gate pulses are shown in Figure 9b. The proposed converter topology achieved a voltage gain of 19.7 and a voltage ripple of 2.2% while the input voltage is 20 V. During the converter operation, the average input is observed to be 10 A. Furthermore, the theoretical calculation of voltage gain is substantiated by the experimental setup. Figure 9c depicts the output response of the voltage and output current V_o and $i_{o,}$ along with the gate pulses. The observed average output current is 400 mA. Additionally, the current ripple for both the inductors L_X and L_Y is observed to be 8%. Figure 9d illustrates the voltage stress across the S_X and S_Y along with the gate pulse; it is evident that the switching stress is 25% related the output voltage. Whereas, for the switch S_Z, switching stress is half or 50% related the output voltage. Figure 9e depicts the response of inductor currents I_{LX} and I_{LY} along with the gate pulses; the inductor currents are observed to be continuous. For the ON-state duration of the two switches S_X and $S_{Y,}$ the source current is almost double the inductor current I_{LX} or $I_{LY,}$ and for the OFF-state duration of the two switches S_X and $S_{Y,}$ the inductor current I_{LX} or I_{LY} is similar to the input current. Considering the topologies presented in Table 1, the proposed converter topology persists with a significantly low switching stress percentage in comparison to the output voltage. Diode stress V_{D1} and V_{D2} are shown in Figure 9f. For the diode D_1, the maximum voltage stress is similar to the input voltage; for diode D_2 the maximum voltage stress is equivalent to the average source voltage and the output voltage. Figure 10 depicts the output power and efficiency comparison. The analysis is based on the theoretical and experimental setup; the observed deviation is about 1.08%, between the theoretical and experimental investigation. The hardware prototype results validate the efficacy of the proposed converter; it is capable of generating high voltage gain with minimum voltage stress on the diodes and the switches.

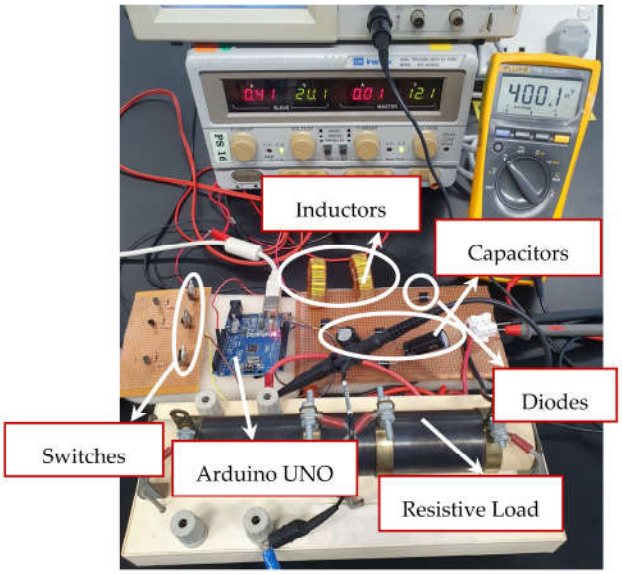
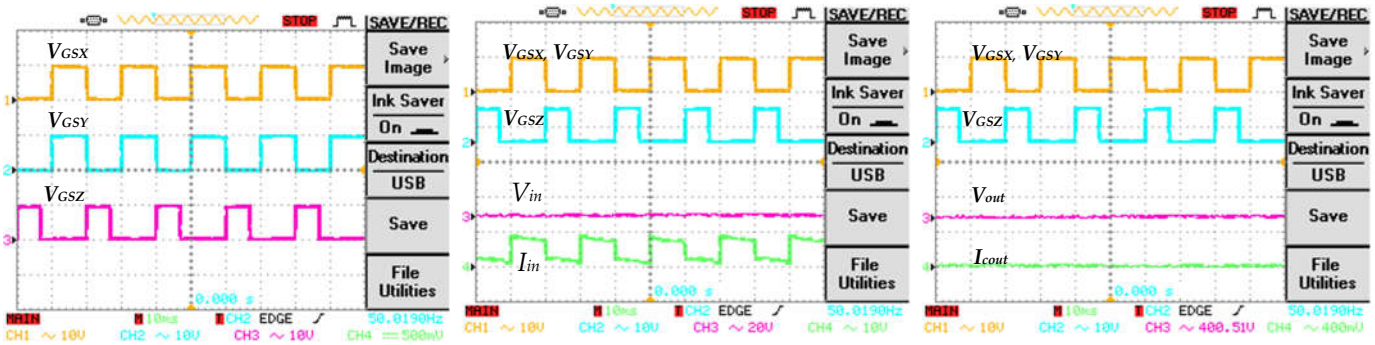


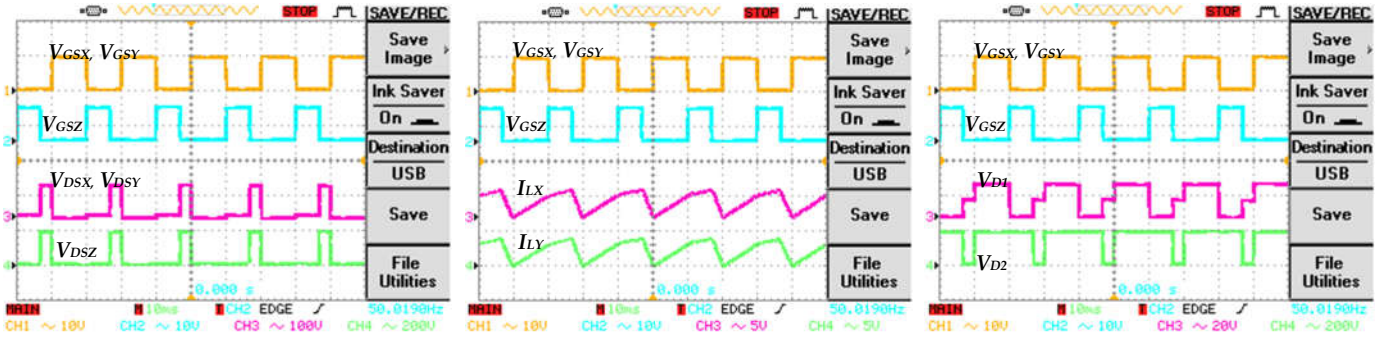
Figure 8. Proposed converter's hardware prototype setup.

Table 2. Proposed converter's design parameter.

Parameters	Ratings (Units)
Rated Power	160 W
Source Voltage	20 V
Output Voltage	400 V
Duty Cycle Ratio (D_1)	50 %
Duty Cycle Ratio (D_2)	35 %
Switching Frequency (f_{sw})	50 kHz
Inductors (L_X, L_Y)	360 µH
Capacitor (C_1, C_2, C_o)	100 µF
Switches (S_X, S_Y, S_Z)	600 V MOSFET FCP20N60
Diodes (D_1, D_2, D_3, D_4)	10A10 Power Diodes



(**a**) (**b**) (**c**)



(**d**) (**e**) (**f**)

Figure 9. Experimental results for the proposed converter. (**a**) Gate pulse voltages (V_{GS1}, V_{GS2}, and V_{GS3}); (**b**) input voltage and input current (V_{in} and, I_{in}); (**c**) output voltage and output current (V_{out} and i_{cout}); (**d**) switch voltages (V_{DSX}, V_{DSY}, and V_{DSZ}); (**e**) inductor currents (I_{LX} and I_{LY}); (**f**) diode voltages (V_{D1} and V_{D2}).

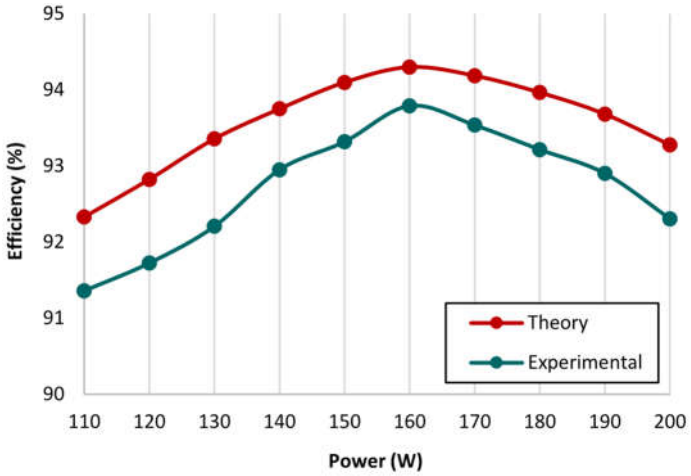


Figure 10. Output power versus efficiency comparison related to theoretical and experimental results.

7. Conclusions

A novel non-isolated high-gain non-inverting interleaved converter topology is proposed in this paper. DC–DC converters utilizing a single duty ratio *D* persist with implications while operating at excessive duty cycle ratios. Considering this issue, the proposed converter includes three switches and these switches are operated with two distinct duty ratios, avoiding excessive duty cycle ratios. The proposed converter topology also has some limitations that include: a slightly higher component count, and it is not recommended for applications that require lower voltage gain or lower loads that operate the converter in discontinuous conduction mode (DCM). However, in contrast, the proposed converter topology is designed to generate a higher voltage gain with a nominal voltage stress, and it is suitable for high power applications and to operate in continuous conduction mode (CCM). Theoretical and practical analyses for the proposed converter topology were carried out considering the crucial parameters, such as voltage stress, on the diodes and switches, voltage gain, and efficiency. Thus, to validate the performance analysis practically, a prototype model 160 W 20/400 V of the proposed converter was built for experimental setup. The voltage gain percentage for the proposed converter is significantly higher with lower voltage stress on the switches and diodes with respect to the recently developed DC–DC converter topologies. The maximum efficiency of the proposed converter is well above 90%. Therefore, the pivotal features of the proposed converter determine it to be an appropriate choice for voltage boosting applications, such as

renewable energy applications, energy management of the microgrid, fuel cell-based energy generation, and electric automobiles. Further improvements can be made in the proposed converter topology by designing it for low power applications by changing the positions of the switches and their operation, provided that if offers low voltage stress on the components, as compared to established converter topologies.

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Nomenclature

V_{in}	Input voltage	r_{D2}	Parasitic resistance of diode D_2
V_{out}	Output voltage	r_{D3}	Parasitic resistance of diode D_3
I_{in}	Input current	r_{D4}	Parasitic resistance of diode D_4
I_{cout}	Output capacitor current	V_{LX}	Inductor voltage L_X
L_X	Inductor L_X	V_{LY}	Inductor voltage L_Y
L_Y	Inductor L_Y	I_{LX}	Inductor current L_X
C_1	Capacitor C_1	I_{LY}	Inductor current L_Y
C_2	Capacitor C_2	V_{GSX}	Switching voltage for switch S_X
C_o	Output Capacitor C_o	V_{GSY}	Switching voltage for switch S_Y
S_X	Switch S_X	V_{GSZ}	Switching voltage for switch S_Z
S_Y	Switch S_Y	V_{DSX}	Voltage stress at switch S_X
S_Z	Switch S_Z	V_{DSY}	Voltage stress at switch S_Y
D_1	Diode 1	V_{DSZ}	Voltage stress at switch S_Z
D_2	Diode 2	V_{D1}	Voltage stress at diode D_1
D_3	Diode 3	V_{D2}	Voltage stress at diode D_2
D_4	Diode 4	V_{D3}	Voltage stress at diode D_3
R_o	Load resistance	V_{D4}	Voltage stress at diode D_4
fsw	Switching frequency	I_{C1}	Capacitor current C_1
r_{LX}	Parasitic resistance of inductor L_X	I_{C2}	Capacitor current C_2
r_{LY}	Parasitic resistance of inductor L_Y	P_{in}	Input power
r_{SX}	Parasitic resistance of switch S_X	P_o	Output power
r_{SY}	Parasitic resistance of switch S_Y	P_{sw}	Switching power losses
r_{SZ}	Parasitic resistance of switch S_Z	P_{rc}	Capacitor power losses
r_{D1}	Parasitic resistance of diode D_1	η	Efficiency

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