

Article

Linearity Enhancement Techniques for PGA Design

Yujun Wang ^{1,2,3}, Yi Wang ⁴ , Lixi Wan ² and Zhi Jin ^{1,*}

¹ Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China
² University of Chinese Academy of Sciences, Beijing 100029, China
³ Chengdu Tiger Microelectronics Research Institute Co., Ltd, Chengdu 610000, China
⁴ School of Integrated Circuits, Tsinghua University, Beijing 611731, China
* Correspondence: jinzhi@ime.ac.cn

Abstract: This paper presents some techniques to improve the linearity of traditional resistive feedback PGAs. By utilizing the switched op-amp in the PGA, the MOS switches in the feedback resistor array can be eliminated and thus the PGA's linearity can be improved. The PGA's linearity is further improved with an additional capacitor, which is used for pre-charging the sampling capacitor to strengthen its capability to drive the sampling capacitor without any extra power consumption. The pre-charge technique is especially suitable for the case where the PGA drives a large sampling capacitance. Implemented in SMIC 0.18 um CMOS technology, the proposed PGA can achieve a gain of 0.5 or 1 and consumes 4.68 mW at a single 5 V supply with the switched output stage enabled. When driving a 20 pF sampling capacitor at a sampling frequency of 200 kHz, the simulation results show that the proposed PGA can give a 9 dBc improvement in SFDR of the sampled signal compared to the traditional PGA design and the SFDR can reach up to 114 dBc.

Keywords: PGA; class AB; pre-charge; linearity



Citation: Wang, Y.; Wang, Y.; Wan, L.; Jin, Z. Linearity Enhancement Techniques for PGA Design. *Micromachines* **2023**, *14*, 356. <https://doi.org/10.3390/mi14020356>

Academic Editors: Yiqiang Chen, Yi Liu and Changqing Xu

Received: 18 December 2022
 Revised: 12 January 2023
 Accepted: 16 January 2023
 Published: 31 January 2023

Correction Statement: This article has been republished with a minor change. The change does not affect the scientific content of the article and further details are available within the backmatter of the website version of this article.



Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The programmable-gain amplifier (PGA) is one of the fundamental building blocks in most analog front-ends and is widely used in wireless communication [1–4], bioelectronic signal processing [5] and data acquisition systems [6–8], whose main function is to provide a relatively constant input level to optimize the dynamic range of these systems. Figure 1 shows the block diagram of a typical analog front-end, which is composed of a sensor, an anti-aliasing filter, an AD converter, a digital signal processor and an automatic gain control loop in addition to a PGA. Additionally, the gain control of the PGA is performed by a DSP through the automatic gain control loop.

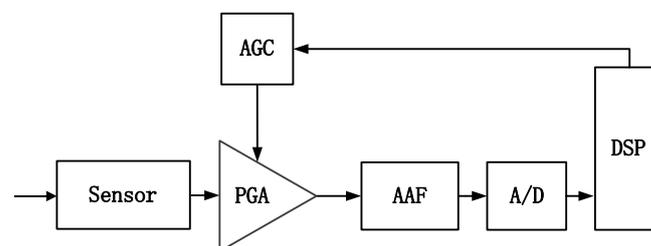


Figure 1. Block diagram of a typical analog front-end.

There exist mainly two topologies for the implementation of the PGA: the negative feedback closed-loop architecture [2] and the open-loop architectures [9,10]. The gain of the closed-loop PGA is dependent on the ratio of the feedback resistance to the input resistance and is insensitive to PVT variations. However, implementing such a PGA demands an op-amp with an extremely high gain and sometimes also requires a wide bandwidth which

means that a power hungry op-amp is needed. On the other hand, open-loop PGAs implement the programmable gain by using the variable input transconductance [9] or output load [10], and the requirements on op-amps are quite relaxed. However, open-loop PGAs suffer a lot from PVT variations. Additionally, the latest research about the PGA has been mainly focused on its applications in wireless communication systems [11–15]. Wide bandwidth and wide gain tuning range are usually required for PGAs utilized in these systems, while the linearity may be limited. For example, the THD performance in reference [11] is only about -50 dB and is not suitable for some applications requiring high linearity. Traditional resistive feedback PGAs are still widely employed in the cases [8,9,16,17]. However, the linearity of the traditional closed-loop resistive feedback PGAs is limited by the non-idealities of the MOS switches utilized in the feedback resistor array network. Meanwhile, another issue in traditional closed-loop PGAs is their lack of capability to drive sampling circuits. In order to obtain a high precision sample to the input signal, the traditional solution is to give more of a power consumption budget to the PGA or spend more time on the sampling phase, which means that a trade-off between power consumption and speed has to be made. It is really a challenging job to design a high linear PGA without experiencing losses in power efficiency and speed.

In this paper, a novel PGA architecture is proposed. A switched op-amp is introduced into PGA design, and the MOS switches used in the feedback resistor array are eliminated. In doing so, the linearity of the PGA can be enhanced. A capacitor used to pre-charge the sampling capacitor is also employed in the proposed PGA to strengthen its capability to drive sampling circuits, and thus the linearity is further improved.

The remainder of this paper is organized as follows. Section 2 gives a detailed analysis of traditional closed-loop PGAs and points out the nonideal factors that limit their linearity. Both the switched op-amp and pre-charge techniques used in the proposed PGA are introduced in Section 3. Simulation results are given in Section 4 and, finally, some conclusions are given in Section 5.

2. Analysis of the Traditional Closed-Loop PGA

The traditional closed-loop PGA architectures are shown in Figure 2. As can be seen, the control switches can be placed at the input or output ends of the op-amp, and the PGAs shown below also perform a single to differential conversion. To simplify, the feedback resistor array network here only consists of two switched resistors. By adding more switched resistors, the gain range of the PGA can be extended. Assuming the gain of the op-amp is infinite, and only SW1 is closed, the closed-loop gain of the PGA in Figure 2a is expressed as:

$$Gain1 = \frac{R_1}{R_0} \quad (1)$$

The gain control is realized by different combinations of feedback resistors; tuning the switches in series with the resistors in the feedback resistor array will achieve the programmable gain. However, in Equation (1), the on-resistance of the MOS switches has been neglected. Indeed, the gain in (1) should be rewritten as

$$Gain1 = \frac{R_1 + ron1}{R_0} \quad (2)$$

where $ron1$ is the on-resistance of SW1. This will not bring any nonlinearity to the gain but only a constant gain shift if $ron1$ holds a constant value. Such a switch can be implemented with an NMOS transistor; then, the on-resistance of SW1 can be expressed as

$$ron1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{TH} - V_{OUT})} \quad (3)$$

where μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, V_{TH} is the threshold voltage and V_{OUT} is the output voltage of the PGA, where all of which are

constant values except for V_{OUT} . V_{OUT} is dependent on the input of the PGA; thus, $ron1$ is related to the input of the PGA and nonlinearity is introduced in Equation (2). Even though SW1 can be implemented through a transmission gate, the on-resistance of SW1 is still slightly related to the input of the PGA, which still results in degradation in the linearity.

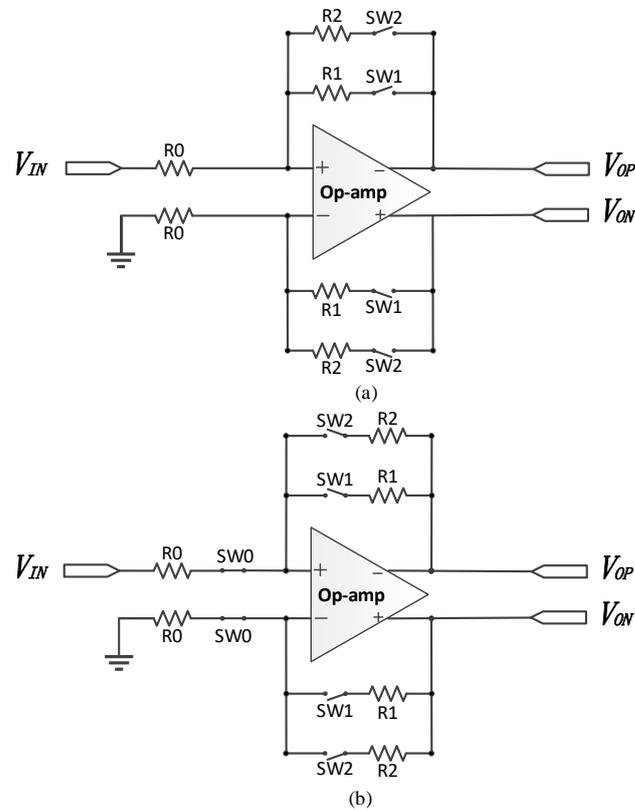


Figure 2. PGA architectures with (a) control switches at the output of the op-amp and (b) control switches at the input of the op-amp.

By placing the switches at the input end of the op-amp and proper sizing arrangements, the linearity of the PGA can be kept free from the varying on-resistance of the switches as shown in Figure 2b.

In Figure 2b, SW0 is an always-on dummy switch and the switches are sized according to Equation (4).

$$\left(\frac{W}{L}\right)_0 : \left(\frac{W}{L}\right)_1 : \left(\frac{W}{L}\right)_2 = \frac{1}{R_0} : \frac{1}{R_1} : \frac{1}{R_2} \quad (4)$$

Then, Equation (5) can be derived, where $ron0$, $ron1$ and $ron2$ are the on-resistances of SW0–SW2, respectively.

$$\frac{R_0}{ron0} = \frac{R_1}{ron1} = \frac{R_2}{ron2} \quad (5)$$

It should be noted that Equation (5) is established, unrelated to the input of the PGA. Hence, the gain with SW1 being closed can only be expressed as

$$Gain1 = \frac{R_1 + ron1}{R_0 + ron0} = \frac{R_1 + \frac{R_1}{R_0}ron0}{R_0 + ron0} = \frac{R_1}{R_0} \quad (6)$$

where $ron0$ – $ron1$ are the on-resistances of SW0–SW1, as previously mentioned. As can be seen, the nonlinear on-resistances of SW0 and SW1 are canceled out. The gain is now precise and highly linear compared to Equation (2). However, the switches have introduced

nonlinear parasitic capacitances at the input nodes of the op-amp, which will lead to the degradation in linearity at high-frequency inputs.

There comes another problem when the PGA is driving a large sampling capacitance in some particular applications [16,17], as shown in Figure 3.

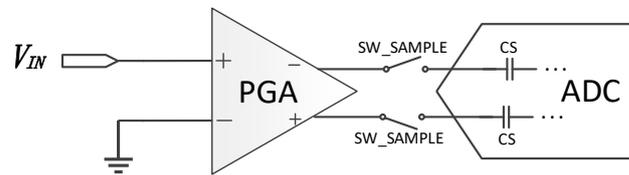


Figure 3. Typical block diagram of a data acquisition system.

At the beginning of the sampling phase, the sampling capacitor CS will be connected to the output node of the PGA and acts as a load to the PGA. The sudden load of the sampling capacitor CS to the PGA will cause the slewing of the op-amp inside the PGA especially when the initial PGA output voltage differs a lot from the last sampled voltage on the sampling capacitor, which will reduce the settling speed of the output voltage. In other words, the settling speed is dependent on the previously sampled signal, which will also cause degradation in linearity with a fixed sampling duration. Whether giving more power consumption budget to the PGA to speed up the settling of the sampling signal or prolonging the sampling duration, neither are a perfect solution.

From the above analyses, the linearity of traditional closed-loop PGAs is limited by the nonideality of MOS switches in the feedback resistor array network and the sudden load of sampling capacitor CS to the PGA during the sampling duration.

3. The Proposed PGA Architecture

In this section, a novel PGA architecture is proposed. Firstly, the op-amp in the traditional closed-loop PGA is replaced by a switched op-amp (SC-OPA), and the MOS switches in the feedback loop are eliminated. As a result, the gain linearity is improved. Furthermore, an additional capacitor used to pre-charge the sampling capacitor is also employed to speed up the settling of sampling signal, which further improves the linearity of the PGA. A detailed description about these techniques will be given below.

3.1. PGA Design Based on a Switched Op-Amp

Figure 4a displays the block diagram of the proposed PGA architecture and Figure 4b shows the block diagram of the switched op-amp. As can be seen, the switched op-amp has two output stages that share the same input stage. Additionally, each output stage corresponds to a feedback resistor array. When the EN signal is enabled, both R_1 and R_2 participate in the signal amplification process, and the gain is expressed as follows:

$$Gain1 = \frac{R_1 \parallel R_2}{R_0} \quad (7)$$

Additionally, when the second output stage of the second stage is disabled, only R_1 participates in the signal amplification process; thus, the gain now turns into

$$Gain2 = \frac{R_1}{R_0} \quad (8)$$

Because the MOS switches presented in the feedback loop of the traditional PGA now disappear, a more linear gain can be obtained compared to traditional closed-loop PGAs.

Different from the conventional design, the resistor array is directly connected to the output stage without any serial MOS switches. The control of the feedback resistor array is realized by controlling the corresponding output stage; when we do not want some resistor to participate in the signal amplification process, we can simply disable the corresponding

output stage and vice versa. In such a manner, the programmable gain can be achieved. Additionally, the gain range can be extended by adding more switched output stages and feedback resistor arrays.

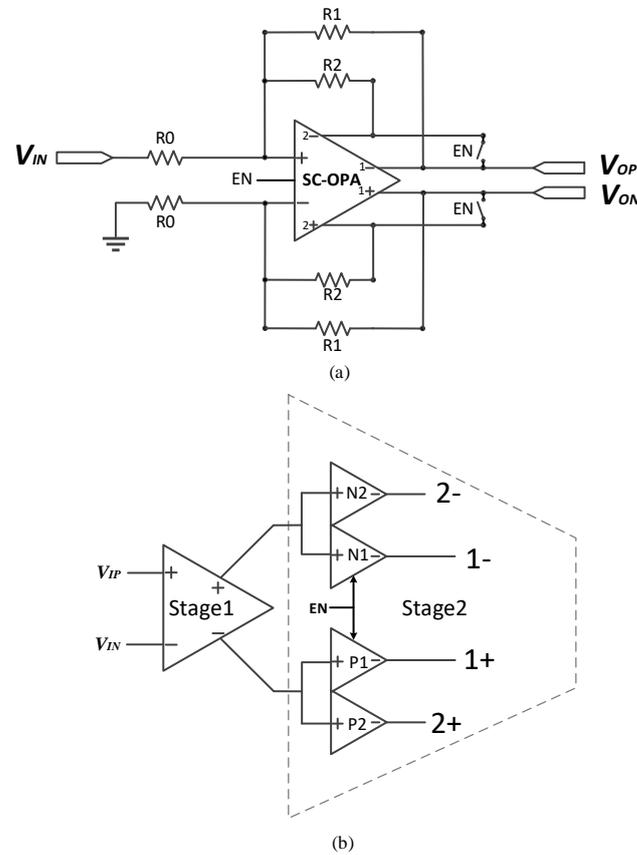


Figure 4. Block diagram of (a) the proposed PGA and (b) SC-OPA.

3.2. The Proposed Pre-Charge Technique in the PGA

Figure 5 shows the proposed pre-charge technique and the timing diagram, respectively. A third phase is added between the tracking phase and sampling phase, which is called the pre-charge phase. Additionally, an additional capacitor is also added to the output of the PGA. During the tracking phase, the switches between the PGA and this additional capacitor are closed; hence, the capacitor is charged by the PGA in this phase. This charge operation ends at the end of the tracking phase; then, the switches between this additional capacitor and the sampling capacitors are closed during the pre-charge phase to pre-charge the sampling capacitors and thus they perform a coarse sample to the input signal. Finally, during the sampling phase, the sampling capacitors are connected to the PGA to realize a fine sample to the input signal. In this way, two-step sampling to input signal is achieved. The slewing effect of the op-amp has been weakened thanks to the pre-charge to the sampling capacitors and thus this speeds up the settling of the sampling signal. In other words, the linearity of the sampled signal will be improved with the same sampling duration.

The speed of the system is not affected by the additional pre-charge phase, because the duration of the pre-charge phase can be taken from the original sampling phase duration and is short. In addition, the linearity of the PGA can be improved without any extra power consumption.

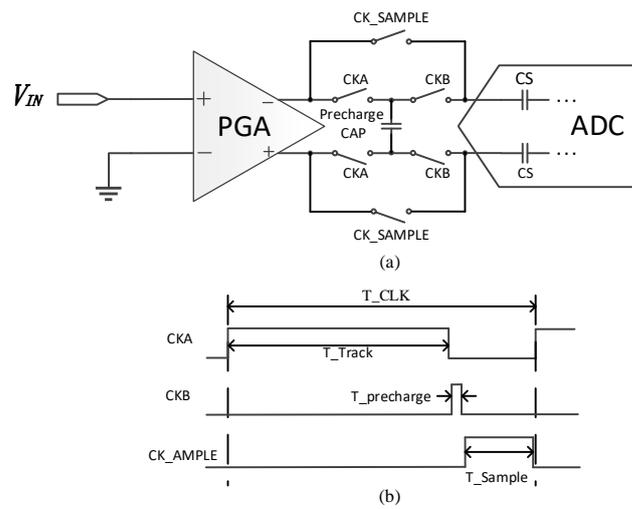


Figure 5. (a) Block diagram of the pre-charge technique used in the PGA. (b) Timing diagram of the pre-charge technique.

3.3. The Circuit Implementation

Figure 6 shows the final block diagram of the proposed PGA and the circuit schematic of the switched op-amp. Each resistance of the feedback resistor array is set to be identical to the input resistance of the PGA ($R_0 = R_1 = R_2$); thus, the proposed PGA can realize a gain of 0.5 or 1. The feedback resistor along with the parallel capacitor form a first-order anti-aliasing filter.

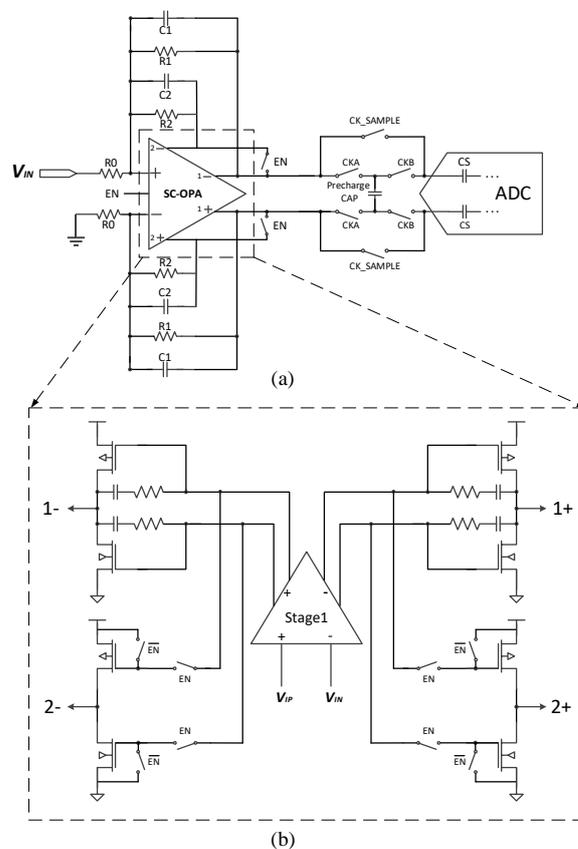


Figure 6. (a) The proposed PGA design. (b) Schematic of the SC-OPA.

The switched op-amp is a two-stage amp consisting of a shared input stage and two class ab output stages. In Figure 6b, the upper output stage is the main output stage and is kept always-on, while below is the auxiliary switched output stage. By placing some switches at the gates of the auxiliary output stage, a switched amp is realized. The switched amp can be enabled with its input connected to the input stage or disabled with its input connected to the VDD or GND. This way, we can determine whether the corresponding feedback resistor participates in the signal amplification or not, and gain control is realized in this way. Additionally, note that in Figure 6b the miller compensation is only realized between the first stage and the main output stage to save the chip area.

Generally speaking, the additional capacitance should be set as large as possible to perform an efficacy pre-charge to the sampling capacitor. Yet, a too-large capacitance may introduce a stability issue in the feedback loop. So, the ratio of the additional capacitance to the sampling capacitance is set to two to guarantee the stability of the feedback loop without too much loss in pre-charge efficacy.

4. Simulation Results

The prototype PGA is implemented in SMIC 180 nm technology using the proposed techniques and the layout is shown in Figure 7. The proposed PGA occupies a die area of 0.17 mm² including a switched op-amp and a pre-charge capacitor. The performance of the switched op-amp is summarized in Table 1. Operating at a 5 V supply voltage, the power consumption at room temperature is 4.68 mW with the switched output stage enabled.

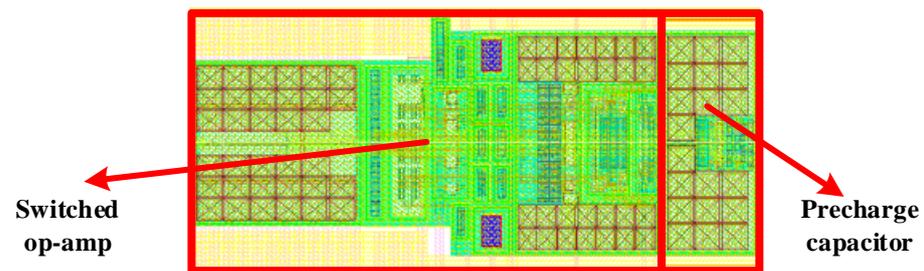


Figure 7. Layout of the proposed PGA.

Table 1. Performance of the switched op-amp with its switched output stage enabled and disabled.

	Open-Loop Gain (dB)	GBW (MHz)	Phase Margin (deg)	Power (mW)
Enabled	101.1	11.2	91	4.68
Disabled	100.9	10.94	87.1	4.39

The measured voltage gain versus frequency is shown in Figure 8a. The proposed PGA can realize a gain of 0.5 or 1 by controlling the switched output stage. To verify the linearity enhancement effects of the proposed techniques, the linearities of the proposed PGA and traditional closed-loop PGAs are simulated. The gain of all of the PGAs is set to be 0.5 and each output of the PGAs drives a 20 pF sampling capacitance during the simulation. Figure 8b,c shows the measured SFDR versus input amplitude and frequency, respectively. The SFDR here is defined as the ratio of the signal power to the power of the largest undesired harmonic or spur.

As can be seen in Figure 8b, while the linearity of the traditional PGA with switches at the output of the op-amp suffers a lot from the nonlinear effects of MOS switches, placing these MOS switches at the inputs of the op-amp will keep the linearity free from the above nonlinear effects. However, the linearity is still limited due to its poor capability to drive large sampling capacitances. The proposed PGA can give a maximum SFDR performance improvement thanks to the proposed techniques. As depicted in Figure 8c,

there is little degradation in linearity in the proposed PGA as input frequency increases while the measured SFDR with the traditional PGAs degrades a lot. There is a significant SFDR degradation in the conventional PGA with control switches at the inputs of the op-amp because of the introduced nonlinear parasitic capacitance. The SFDR is at least improved by 9 dBc with the proposed techniques and can reach up to 114 dBc.

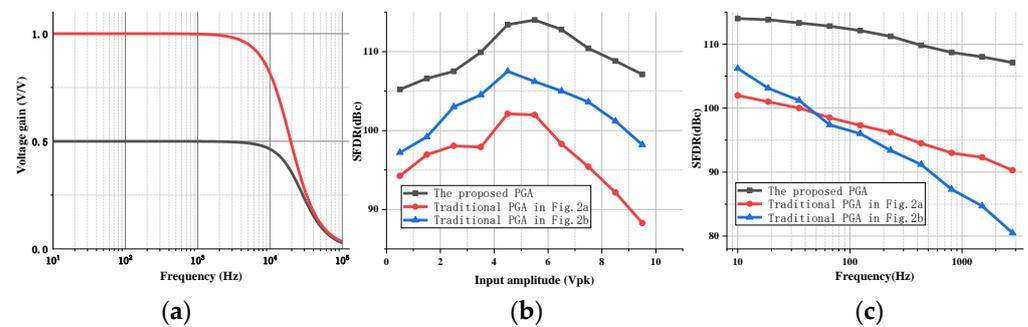


Figure 8. (a) The closed-loop gain verse frequency. (b) The simulated SFDR versus input amplitude. (c) The simulated SFDR versus frequency.

Figure 9a shows the simulated THD versus the output swing for different gain settings. Figure 9b displays the simulated THD versus the frequency. Both pre-simulations and post-simulations on different PVT corners (tt, ss and ff) with temperatures of $-40\text{ }^{\circ}\text{C}$, $27\text{ }^{\circ}\text{C}$ and $85\text{ }^{\circ}\text{C}$ are carried out. Results are summarized in Table 2. As can be seen, the proposed PGA design is robust and the linearity degrades little in post-simulations. The main performances and comparisons with some existing works are summarized in Table 3.

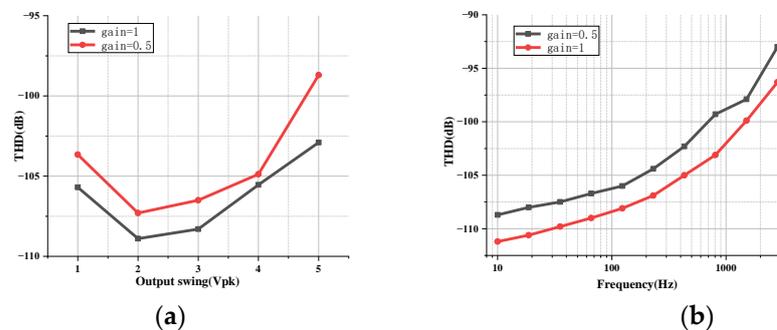


Figure 9. The simulated THD versus (a) the output swing at 1 KHz and (b) the frequency when the output swing = 5 Vpk.

Table 2. Summarization of simulation results.

Input amplitude = 5 Vpk at 1 KHz gain = 1		Typical	Min	Max
Pre-simulation	SFDR (dB)	105.2	91.7	108.6
	THD (dB)	-103.2	-105.8	-87.2
Post-simulation	SFDR (dB)	104.7	92.2	108.8
	THD (dB)	-102.9	-105.1	-88.3
Input amplitude = 10 Vpk at 1 KHz gain = 0.5		Typical	Min	Max
Pre-simulation	SFDR (dB)	103.2	101	108.7
	THD (dB)	-98.8	-105.8	-95.8
Post-simulation	SFDR (dB)	103.8	101	107.3
	THD (dB)	-98.4	-105.8	-96.9

Table 3. Performance summary and comparison.

Reference	[11]	[13]	[14]	[15]	This Work
Technology (nm)	180	180	180	180	180
Supply (V)	5	1.8	1.8	1.2	5
Bandwidth (MHz)	30	10–25	14	11–78	0.02
Gain range (dB)	0–14	–12–24	3.39–43.79	19.5–42.5	0.5/1 V/V
Gain error (dB)	<0.5	N/A	0.07	N/A	0.0013 V/V
THD (dB)	–50.5	<–56 ^a	N/A	–40.7 ^a	–98.4
Power (mW)	1.044	3.6	7.02	0.1968	4.68
Area (mm ²)	0.052	0.32	0.283	0.0007	0.17

^a HD3.

5. Conclusions

This paper presents a PGA design with high linearity performance. Firstly, the switches in the feedback loop of the traditional closed-loop PGA are eliminated by introducing a switched op-amp into the PGA design which is beneficial to the linearity of the PGA. The PGA's driving capability is enhanced with the proposed pre-charge technique and thus this leads to a further improvement in linearity. Moreover, this would not consume any extra power. Implemented in SMIC 180 nm technology, the proposed PGA can provide a gain of 0.5 or 1 and gain error of less than 0.0013 V/V. It occupies a die area of 0.17 mm² and the total power consumption at a 5 V supply is 4.68 mW with its switched output stage enabled. Compared with previously published works as displayed in Table 3, the proposed PGA has obvious advantages in terms of the THD and gain error. The THD performance is still better than –98 dB at a 5 Vpk 1 KHz sinusoidal input. Thus, it can be applied to systems where high linearity is required.

Author Contributions: Writing—original draft preparation, Y.W. (Yujun Wang); writing—review and editing, Y.W. (Yi Wang); supervision, L.W.; project administration, Z.J. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

References

- He, L.; Li, L.; Zhao, D.; Wang, Z. A Low-Power Wide Gain Range Digitally Controlled Variable Gain Amplifier with a Wide Tuning Bandwidth for 60 GHz Applications. In Proceedings of the 2016 IEEE 17th Annual Wireless and Microwave Technology Conference (WAMICON), Clearwater, FL, USA, 11–13 April 2016; pp. 1–4.
- Giannini, V.; Craninckx, J.; D'Amico, S.; Baschiroto, A. Flexible Baseband Analog Circuits for Software-Defined Radio Front-Ends. *IEEE J. Solid-State Circuits* **2007**, *42*, 1501–1512. [[CrossRef](#)]
- Wu, W.; Zhang, L.; Wang, Y. A PVT-Robust Analog Baseband with DC Offset Cancellation for FMCW Automotive Radar. *IEEE Access* **2019**, *7*, 43249–43257. [[CrossRef](#)]
- Barin, F.; Zencir, E. Gain and Bandwidth Programmable Fourth-Order Multiple Feedback Butterworth Low-Pass Filter for C-V2X Applications. *J. Circuits Syst. Comput.* **2022**, *31*, 2250164. [[CrossRef](#)]
- Cha, J.-H.; Park, J.-H.; Park, Y.; Shin, H.; Hwang, K.S.; Cho, I.-J.; Kim, S.-J. A CMOS Microelectrode Array System with Reconfigurable Sub-Array Multiplexing Architecture Integrating 24,320 Electrodes and 380 Readout Channels. *IEEE Trans. Biomed. Circuits Syst.* **2022**. [[CrossRef](#)]
- Subramanian, A.; Halder, T.; Kannan, A. Programmable Gain Amplifier with Programmable Resistance. U.S. Patent 11152904B2, 19 October 2021.
- Agarwal, U.K.; Kannan; Vishweshwara, R.; Subramanian, A.; Gelabert, P.R.; Thodi, D.M.; Patki, A.A. Analog-to-Digital Converter with Dynamic Range Enhancer. U.S. Patent 20200304139A1, 1 September 2020.
- Chao, Y.J. Programmable Gain Amplifier (PGA) Embedded Pipelined Analog to Digital Converters (ADC) for Wide Input Full Scale Range. U.S. Patent 10686459B2, 16 June 2020.
- Calvo, B.; Celma, S.; Aznar, F.; Alegre, J. Low-voltage CMOS programmable gain amplifier for UHF applications. *Electron. Lett.* **2007**, *43*, 1087–1088. [[CrossRef](#)]
- Kim, T.W.; Kim, B. A 13-dB IIP3 Improved Low-Power CMOS RF Programmable Gain Amplifier Using Differential Circuit Transconductance Linearization for Various Terrestrial Mobile D-TV Applications. *IEEE J. Solid-State Circuits* **2006**, *41*, 945–953. [[CrossRef](#)]

11. Bai, C.; Wu, J.; Chen, C.; Deng, X. A 35-dBm OIP3 CMOS Constant Bandwidth PGA With Extended Input Range and Improved Common-Mode Rejection. *IEEE Trans. Circuits Syst. II Express Briefs* **2016**, *64*, 922–926. [[CrossRef](#)]
12. Bhamra, H.; Lynch, J.; Ward, M.; Irazoqui, P. A Noise-Power-Area Optimized Biosensing Front End for Wireless Body Sensor Nodes and Medical Implantable Devices. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 2917–2928. [[CrossRef](#)]
13. Bhattaru, P.; Krishnapura, N. A 36dB Gain Range, 0.5dB Gain Step Variable Gain Amplifier with 10 to 25MHz Bandwidth Third-Order Filter for Portable Ultrasound Systems. In Proceedings of the 2020 33rd International Conference on VLSI Design and 2020 19th International Conference on Embedded Systems (VLSID), Bangalore, India, 4–8 January 2020; pp. 96–100.
14. Wang, L.S.; Ku, P.C.; Ko, P.T.; Chung, C.J.; Lu, L.H. A 40.4-dB Range, 0.73-dB Step, and 0.07-dB Error Programmable Gain Amplifier Using Gain Error Shifting Technique. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1109–1113. [[CrossRef](#)]
15. Firouz, S.; Najafiaghdam, E.; Jafarnejad, R. A low power CMOS programmable gain amplifier employing positive feedback technique. *Int. J. Circuit Theory Appl.* **2022**, *50*, 2982–2996. [[CrossRef](#)]
16. Xu, Z.; Hu, B.; Wu, T.; Yao, Y.; Chen, Y.; Ren, J.; Ma, S. A 12-Bit 50 MS/s Split-CDAC-Based SAR ADC Integrating Input Programmable Gain Amplifier and Reference Voltage Buffer. *Electronics* **2022**, *11*, 1841. [[CrossRef](#)]
17. Kevin, Z. *System-Driven Circuit Design for ADC-Based Wireline Data Links*; Stanford University: Stanford, CA, USA, 2018.

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.