

Article

Controlling Drain Side Tunneling Barrier Width in Electrically Doped PNP Tunnel FET

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Abstract: In this paper, we propose and investigate an electrically doped (ED) PNP tunnel field effect transistor (FET), in which the drain side tunneling barrier width is effectively controlled to obtain a suppressed ambipolar current. We present that the proposed PNP tunnel FETs can be realized without chemically doped junctions by applying the polarity bias concept to a doped N⁺/P[−] starting structure. Using numerical device simulations, we demonstrate how the tunneling barrier width on the drain side can be influenced by several design parameters, such as the gap length between the channel and the drain (L_{gap}), the working function of the polarity gate, and the dielectric material of the spacer. The simulation results show that an ED PNP tunneling FET with an ED drain, which has been explored for the first time, exhibits a low ambipolar current of 5.87×10^{-16} A/ μm at a gap length of 20 nm. The ambipolar current is reduced by six orders of magnitude compared to that which occurs with a conventional ED PNP tunnel FET with a uniformly doped drain, while the average subthreshold slope and the ON state and OFF state currents remained nearly identical.

Keywords: electrically doping; PNP tunnel FET; ambipolar current; tunneling barrier width; TCAD simulation



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1. Introduction

Tunnel field effect transistors (TFETs) are promising low power devices that can replace metal oxide semiconductor field effect transistors (MOSFETs) in ultra low power circuits applications due to the subthreshold swing (SS) of less than 60 mV/decade at room temperature and a lower OFF state current [1–6]. However, due to the inherent band-to-band tunneling and ambipolar mechanism, TFETs also have their own drawbacks in terms of a low drive current and a high ambipolar current. Ambipolarity refers to the device conducting both positive and negative gate voltages. In complementary circuit applications, the TFET's ambipolar conduction limits its usefulness [7–9]. PNP tunnel FETs, which have a narrow N⁺ pocket between the source and the channel, have been intensively investigated to improve their electrical performances [10–14]. Compared to the conventional TFETs, PNP tunnel FETs have shown their advantages such as a higher drive current, an enhanced SS, and an improved device reliability. However, realizing this narrow N⁺ doped pocket is a technological challenge [15–18]. Based on the polarity bias concept, we have recently reported a theoretical device structure of an in-built N⁺ pocket electrically doped (ED) tunnel FET, which provides a possible technique to overcome the difficulties in realizing a highly doped narrow pocket [19].

By using the polarity bias concept [20–22], a conventional in-built N⁺ pocket electrically doped tunnel FET is presented, as shown in Figure 1b. With a starting NPN structure (shown in Figure 1a), a polarity gate electrode is set on the source side of the device to achieve the PNP TFET structure. Therefore, the narrow N⁺ pocket is built in the device and without the need for any additional doping processes, which simplifies the manufacturing complexity. Furthermore, 2D Technology Computer Aided Design (TCAD)

simulations have demonstrated that the introduction of the in-built N^+ pocket yields a higher drive current and a steeper average SS when they are compared to those of a conventional ED-TFET. However, the ambipolar characteristics of the in-built N^+ pocket ED-TFET have not been discussed yet.

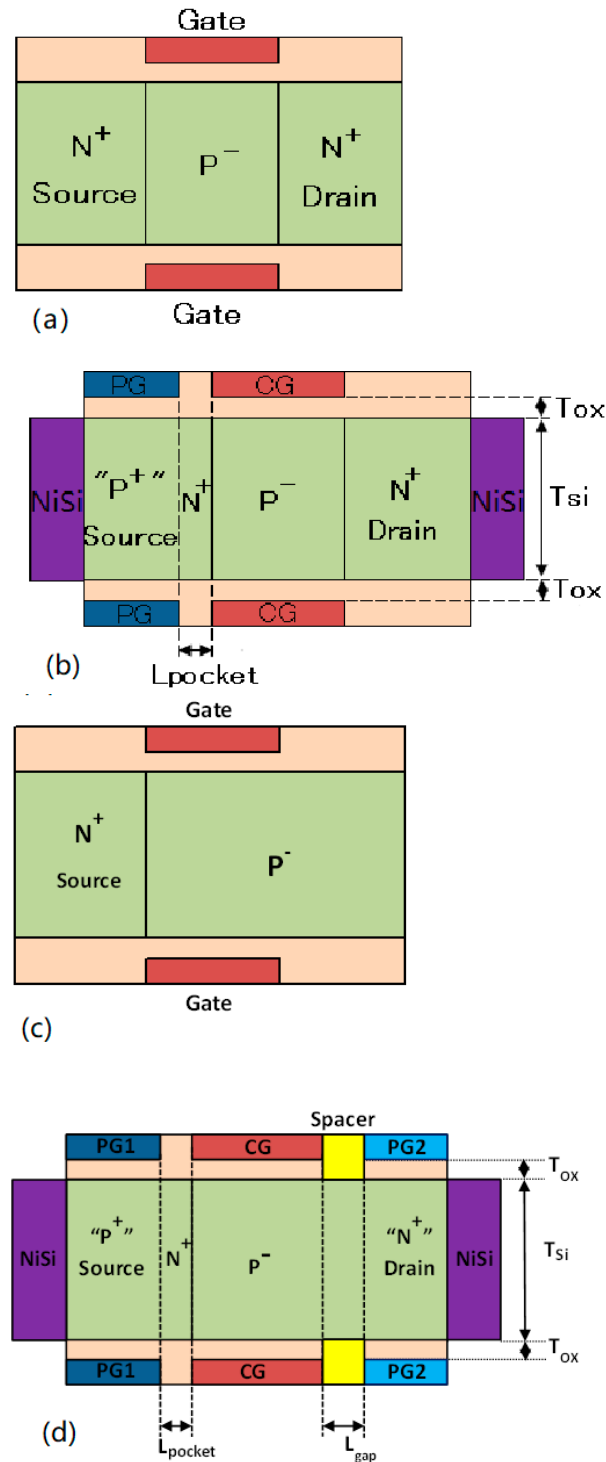


Figure 1. Cross-sectional views of (a) initial NPN structure used to realize conventional in-built N^+ pocket ED-TFET, (b) conventional in-built N^+ pocket ED-TFET, (c) initial NP structure used to realize in-built N^+ pocket ED-TFET with an ED drain, and (d) in-built N^+ pocket ED-TFET with an ED drain.

In this paper, in order to perform a further analysis on the ambipolar characteristics and suppress the ambipolar current by controlling the tunneling barrier width at channel–drain

junction, we propose and investigate an in-built N^+ pocket ED-TFET with an electrically doped drain. To realize the proposed device, first, a PN junction structure is depicted, as shown in Figure 1c. The proposed device is composed of three sets of gate electrodes: a control gate (CG) and two polarity gates (PG). Then, one polarity gate electrode (marked as PG1) is embedded on the source side of the device to convert part of the N^+ doped source into a “P⁺” region. Another polarity gate electrode (marked as PG2) is embedded on the drain side to convert part of the p-doped region into an “N⁺” drain [21]. Therefore, an in-built N^+ pocket ED-TFET with an ED drain is realized, as shown in Figure 1d. To create a P⁺ source region, the PG1 terminal is biased at -0.7 V to increase the hole concentration to $1 \times 10^{19} \text{ cm}^{-3}$ in the TCAD simulations. Meanwhile, to create an N⁺ drain region, the PG2 terminal is biased at 0.7 V to increase the electron concentration to $5 \times 10^{18} \text{ cm}^{-3}$. The source and drain contacts are composed of nickel silicide (NiSi) with a Schottky barrier height of 0.45 eV. Band bending at the source/drain contact indicates a low PG bias, thereby making the holes become the majority carriers, and a high PG bias makes the electrons become the majority carriers, as well [23]. Thus, to create a P⁺ source region with a hole concentration that is similar to that of the reference device, PG1 is biased sufficiently negative. Furthermore, PG2 is sufficiently positively biased for an N⁺ drain region with an electron concentration that is equivalent to that of the reference device.

We can see from Figure 1b,d that the main difference between these two structures is the formation of the drain region. In the conventional in-built N^+ pocket ED-TFET, the N⁺ drain region is uniformly doped by ion implantation [19]. However, in the proposed device with an ED drain, the drain region is electrically doped based on the polarity bias concept, and it introduces a new design parameter L_{gap} , which is the length of the gap between the channel and the drain. Table 1 is presented to compare the proposed device with the conventional in-built N⁺ pocket ED-TFET and the conventional ED-TFET structures. The quotation marks “P⁺” and “N⁺” in the doping profile of the final structure indicate that this region is formed by electrical doping using the polarity bias concept, rather than ion implantation. The simulation results show that the tunneling barrier width at the channel–drain junction can be controlled by choosing an appropriate L_{gap} for the proposed device. Thus, the ambipolar current of the device can be effectively suppressed by introducing a gap on the drain side by using an electrical doping technique based on the concept of polarity bias.

Table 1. Comparison of device design.

Device Design	Conventional ED-TFET	Conventional In-Built N^+ Pocket ED-TFET with Uniform Doped Drain [19]	Proposed In-Built N^+ Pocket ED-TFET with an ED Drain
Doping Profile of Beginning Structure (From Source to Drain)	$N^+-N^+-N^+$	$N^+-P^--N^+$	N^+-P^-
Doping Profile of Final Structure (From Source to Drain)	“P ⁺ ”- $N^+-N^+-N^+$	“P ⁺ ”- N^+-P^- - N^+	“P ⁺ ”- N^+-P^- -“N ⁺ ”
Number of Polarity Gate	1	1	2
Location of Polarity Gate	Source Region	Source Region	Source and Drain Region

2. Simulation Parameters and Approach

The device parameters used in our simulations are shown in Table 2. In order to study the effect of the gap length on the tunneling barrier width and ambipolar current, L_{gap} varies from 5 nm to 25 nm. Making the layer underneath the polarity gate intrinsic, the

working functions of PG1 and PG2 in the proposed device with an ED drain were chosen to be 4.33 eV and 4.5 eV, which refer to the Ti and Mo materials, respectively [24]. An HfO_2 gate dielectric with a physical thickness of approximately 4.5 nm and an equivalent oxide thickness (EOT) of 0.8 nm was used in the simulations. The source terminals were set to be grounded ($V_S = 0$) in all of the simulations. Hence, we have regarded $V_{CG} = V_{CGS}$ and $V_{PG} = V_{PGS}$ in all of the devices.

Table 2. Parameters used for device simulation.

Parameter	Conventional In-Built N ⁺ Pocket ED-TFET [19]	In-Built N ⁺ Pocket ED-TFET with an ED Drain
Effective Gate Oxide Thickness (EOT)	0.8 nm	0.8 nm
Silicon Film Thickness (T_{Si})	10 nm	10 nm
Control Gate Length	50 nm	50 nm
Length of pocket (L_{pocket})	5 nm	5 nm
Length of gap (L_{gap})	-	5~25 nm
Source Doping	$4 \times 10^{19} \text{ cm}^{-3}$ (N ⁺)	$4 \times 10^{19} \text{ cm}^{-3}$ (N ⁺)
Channel Doping	$1 \times 10^{17} \text{ cm}^{-3}$ (P ⁻)	$1 \times 10^{17} \text{ cm}^{-3}$ (P ⁻)
Drain Doping	$1 \times 10^{17} \text{ cm}^{-3}$ (P ⁻)	$5 \times 10^{18} \text{ cm}^{-3}$ (N ⁺)
CG Work function	4.74 eV	4.74 eV
PG1 Work function	4.33 eV	4.33 eV
PG2 Work function	-	4.5 eV

All of the simulations were performed using the Silvaco Atlas device simulation tool, version 5.19.20.R [25]. The non-local band-to-band tunneling (BTBT) model was used to take into account the tunneling along the lateral direction. We used the Lombardi mobility model in our simulation in order to include the mobility degradation effect owing to the electric field. The Shockley–Read–Hall (SRH) recombination model and Fermi Dirac statistics were also used. The band-gap narrowing (BGN) model was used for the high doping concentration in the devices. Quantum mechanical effects were not considered when the T_{Si} exceeded 7 nm [5,26]. Thus, quantum mechanical effects are not included in our simulations since T_{Si} was designed to be 10 nm. Based on [4], we validated our simulation model using a nonlocal band-to-band tunneling (BTBT) model. Non-local BTBT computed the tunneling probability along the lateral direction of the device by analyzing the energy band diagrams. In the simulations, non-local BTBT was performed using a fine mesh across the region where tunneling occurs. A careful application of the Wentzel–Kramers–Brillouin method was used by Atlas for approximating the evanescent wavevector. There was no consideration of the gate leakage in these simulations, which can be expected to limit the OFF current. The bias condition is that the voltage of PG1 is fixed at -0.7 V, the voltage of PG2 is fixed at 0.7 V, and the drain voltage is fixed at 1 V. V_{CG} increased from -1 V to 1 V.

3. Results and Discussion

Figure 2 shows the transfer characteristics of the proposed in-built N⁺ pocket ED-TFET with an ED drain and a conventional device with uniform doped drain. The effect of changing the gap length L_{gap} on the ambipolar conduction is also shown in Figure 2. Accordingly, this gap corresponds to the channel-to-drain depletion region in the conventional TFETs. The drain side depletion region should be wide enough to minimize the ambipolar currents. We can see from Figure 2 that for the proposed ED drain device, the ambipolar current is significantly suppressed for the control gate voltage that is as large as -1.0 V, and the gap length reaches 10 nm. It can be seen that the bipolar current is effectively controlled whenever the gap length increases, as the gap length determines the tunneling barrier width in the drain region. A larger L_{gap} is equivalent to a wider depletion width, and thus, it increases the tunneling barrier width at the channel–drain junction. Therefore, by choosing an appropriate gap length, the ambipolar current can be effectively suppressed.

As shown in Figure 3, we present the energy band profiles of the proposed device below the Si–oxide interface at 1 nm and 5 nm with different gap lengths to explain the reduction in the ambipolar current with gap length. According to Figure 3, with a gap length of 20 nm, the tunnel barrier width is larger due to a wider depletion region between the channel and drain, resulting in a suppressed ambipolar conduction. The electron concentration contour plot of the proposed in-built N^+ pocket ED-TFET with an ED drain for L_{gap} values of 5 nm and 20 nm is shown in Figure 4 at $V_{CG} = -1$ V. We observe that the electron concentration varies drastically at the gaps. When the gap length is 5 nm, the electron concentration of the drain region near the channel side is higher, which is consistent with the performance of the energy band diagram in Figure 3. For different PG2 working functions, the transfer characteristics of the proposed in-built N^+ pocket ED-TFET with an ED drain is shown in Figure 5. The gap length is fixed at 5 nm. The working functions of PG2 are set to 4.33 eV, 4.5 eV, and 4.74 eV, referring to Ti, Mo, and Sb, respectively [24]. In Figure 5, we observe that the ambipolar current continuously decreases, while the OFF state current remains nearly constant with an increasing Φ_{PG2} . The ambipolar current (I_{AMB}) is extracted at $V_{CG} = -0.8$ V, and the OFF state current (I_{OFF}) is extracted at $V_{CG} = 0.0$ V. To understand this decrease in the ambipolar current, the energy band profile of the proposed in-built N^+ pocket ED-TFET with an ED drain with a different Φ_{PG2} is shown in Figure 6. As Φ_{PG2} increases, the induced electron concentration in the drain region decreases due to the polarity bias concept. Thus, a wider tunnel barrier width is seen in Figure 6 for Φ_{PG2} of 4.74 eV, which results in a suppressed ambipolar current. Figure 7 shows transfer characteristic curves of the proposed in-built N^+ pocket ED-TFET with an ED drain for different spacer materials at the drain side. As it can be seen from Figure 7, the spacer material has a small effect on the ambipolar conduction of the device, and it does not affect the electrical characteristics in the OFF state and ON state at all. The effect on the ambipolar conduction is that the higher the dielectric constant of the spacer is, the lower the ambipolar current is. To further explain the reason, we present the energy band diagrams for both Air and HfO_2 spacer material devices, as shown in Figure 8. The widths of the tunneling barrier corresponding to the two spacer materials are shown in the enlarged image in Figure 8, which are 6 nm for the Air spacer and 7 nm for the HfO_2 spacer. Additionally, this explains the results mentioned above. Therefore, this study indicates that the in-built N^+ pocket ED-TFET with an ED drain offers a new method of suppressing the ambipolar currents in TFETs, as well as a low thermal budget process since the drain region does not need to be chemically doped.

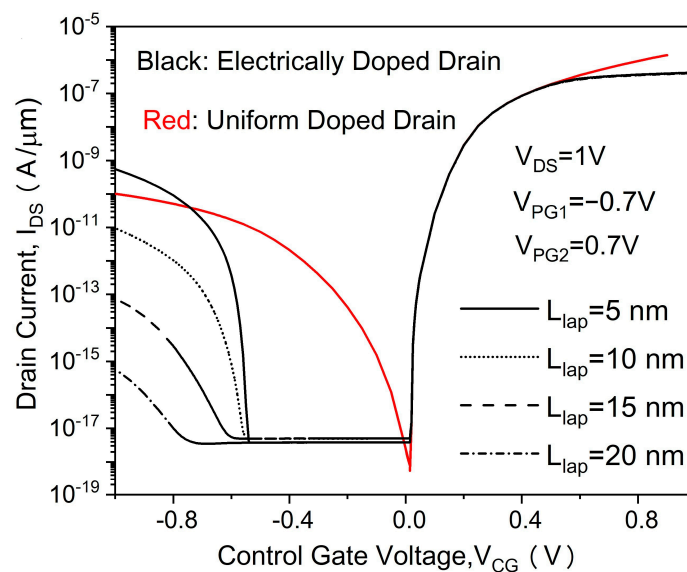


Figure 2. Transfer characteristics of proposed in-built N^+ pocket ED-TFET with an ED drain and conventional in-built N^+ pocket ED-TFET with uniformly doped drain.

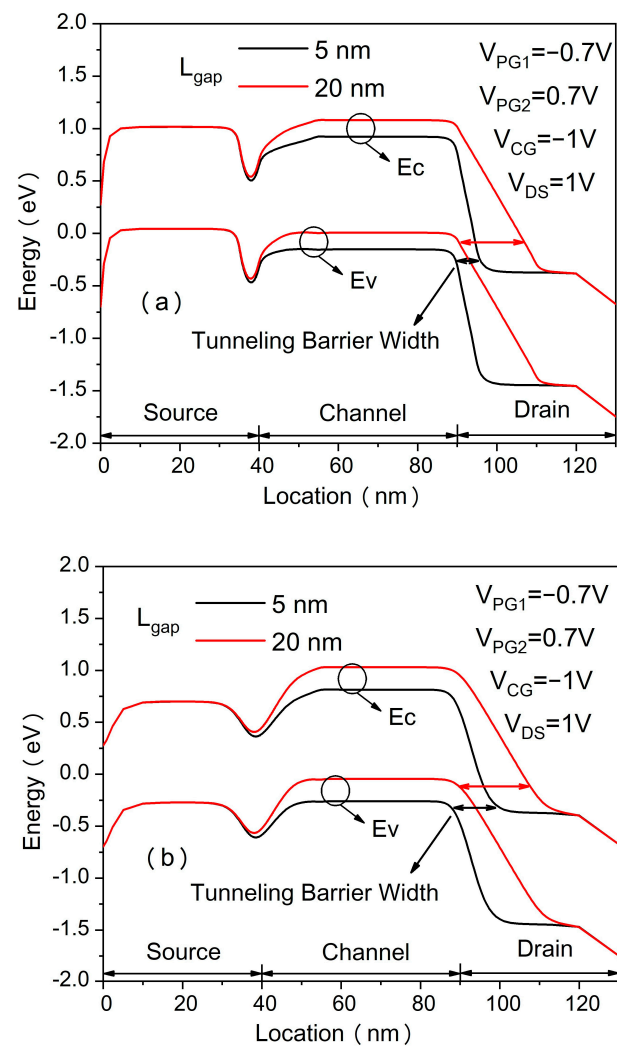


Figure 3. Energy band diagrams at (a) 1 nm and (b) 5 nm below the Si-oxide interface of the proposed ED-TFET with an ED drain at OFF state with L_{gap} of 5 nm (black) and 20 nm (red).

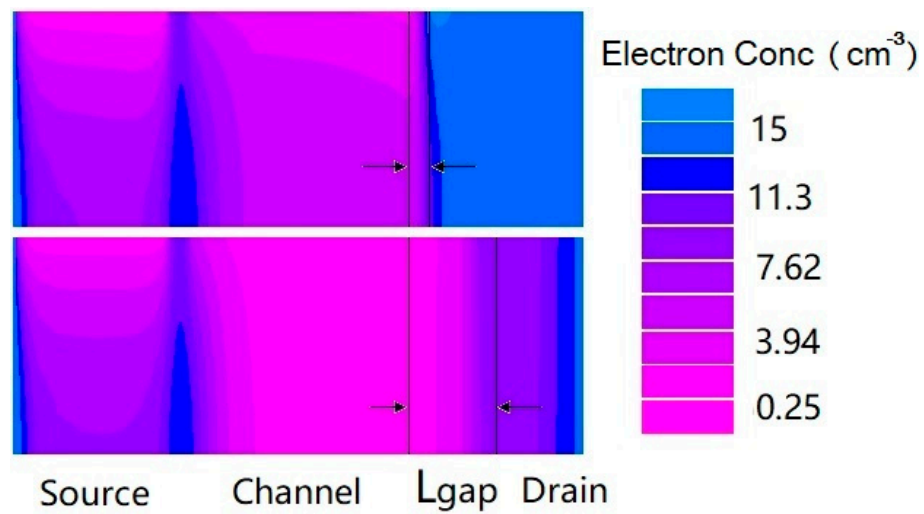


Figure 4. Electron concentration contour of proposed in-built N^+ pocket ED-TFET with an ED drain for L_{gap} of 5 nm (up) and 20 nm (down) at OFF state.

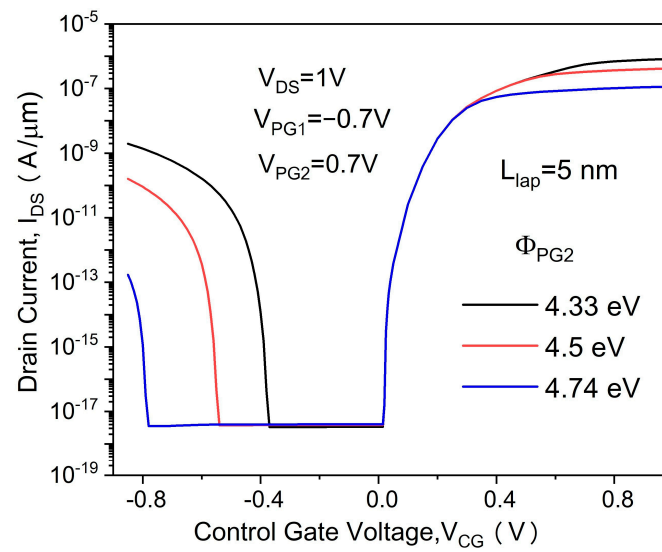


Figure 5. Transfer characteristics of proposed in-built N^+ pocket ED-TFET with an ED drain for different PG2 working functions.

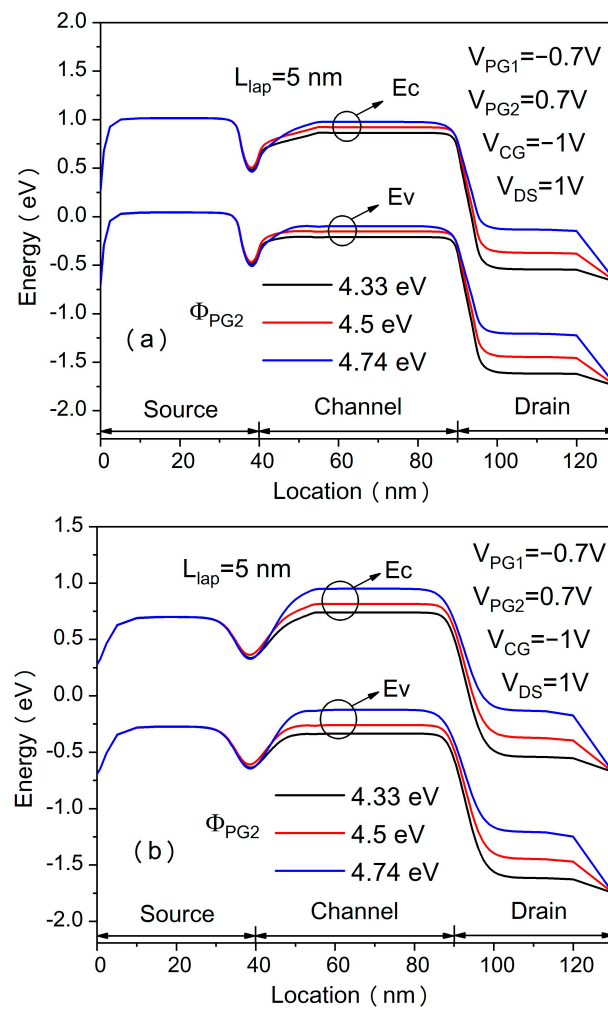


Figure 6. Energy band diagrams at (a) 1 nm and (b) 5 nm below the Si-oxide interface of the proposed ED-TFET with an ED drain at OFF state with Φ_{PG2} of 4.33 eV (black), 4.5 eV (red) and 4.74 eV (blue).

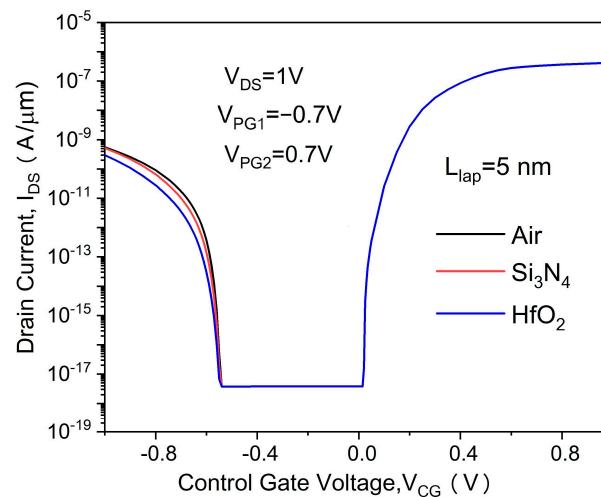


Figure 7. Transfer characteristics of proposed in-built N^+ pocket ED-TFET with an ED drain for different spacer materials at the drain side.

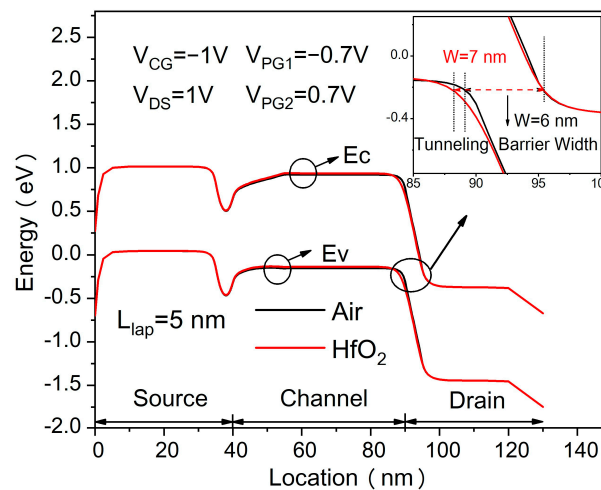


Figure 8. Energy band diagrams of the proposed ED-TFET with an ED drain with Air and HfO_2 spacer at the drain side.

4. Conclusions

In this paper, with the help of 2D TCAD simulations, we present an approach that can be used to realize an in-built N^+ pocket ED-TFET with an electrically doped drain. Based on polarity bias concept, we have shown that the tunneling barrier width at the drain side can be effectively controlled by several design parameters. The simulation results reveal that a PNPN tunneling FET with an ED drain, which has been presented for the first time, exhibits a low ambipolar current of 5.87×10^{-16} A/ μ m over a gap length of 20 nm. As compared to the conventional ED PNPN tunneling FETs with uniformly doped drains, the ambipolar current is reduced by six orders of magnitude, while the average subthreshold slope, ON state current, and OFF state current remain nearly the same. As a result, the ambipolar current of the proposed device can be effectively suppressed by choosing appropriate design parameters.

Author Contributions: Conceptualization, C.S.; methodology, Z.-M.L.; Software Y.L.; validation, H.Z.; investigation, C.S.; Writing—review and editing, L.Y. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Saurabh, S.; Kumar, M.J. Basics of Tunnel Field-Effect Transistors. In *Fundamentals of Tunnel Field-Effect Transistors*, 1st ed.; CRC Press: Boca Raton, USA, 2016; Volume 3, pp. 44–45. [\[CrossRef\]](#)
2. Vishnoi, R.; Kumar, M.J. An accurate compact analytical model for the drain current of a TFET from subthreshold to strong inversion. *IEEE Trans. Electron Dev.* **2015**, *62*, 478–484. [\[CrossRef\]](#)
3. Ma, W.C.Y.; Luo, S.M. Impacts of stress voltage and channel length on hot-carrier characteristics of tunnel field-effect thin-film transistor. *IEEE Trans. Electron Dev.* **2020**, *67*, 5243–5246. [\[CrossRef\]](#)
4. Boucart, K.; Ionescu, A.M. Double-gate tunnel FET with high- k gate dielectric. *IEEE Trans. Electron Dev.* **2007**, *54*, 1725–1733. [\[CrossRef\]](#)
5. Kumar, M.J.; Janardhanan, S. Doping-less tunnel field effect transistor: Design and investigation. *IEEE Trans. Electron Dev.* **2013**, *60*, 3285–3290. [\[CrossRef\]](#)
6. Liu, K.M.; Cheng, C.P. Investigation on the effects of gate-source overlap/underlap and source doping gradient of n-type Si cylindrical gate-all-around tunnel field-effect transistors. *IEEE Trans. Nanotechnol.* **2020**, *19*, 382–389. [\[CrossRef\]](#)
7. Krishnamohan, T.; Kim, D.; Raghunathan, S.; Saraswat, K. Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and $\ll 60$ mV/dec subthreshold slope. In Proceedings of the IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2008. [\[CrossRef\]](#)
8. Vladimirescu, A.; Amara, A.; Anghel, C. An analysis on the ambipolar current in Si double-gate tunnel FETs. *Solid State Electron.* **2012**, *70*, 67–72. [\[CrossRef\]](#)
9. Abdi, D.B.; Kumar, M.J. Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain. *IEEE J. Electron Dev. Soc.* **2014**, *2*, 187–190. [\[CrossRef\]](#)
10. Nagavarapu, N.V.; Jhaveri, R.; Woo, J.C.S. The tunnel source (PNPN) n-MOSFET: A novel high performance transistor. *IEEE Trans. Electron Dev.* **2008**, *55*, 1013–1019. [\[CrossRef\]](#)
11. Narang, R.; Saxena, M.; Gupta, R.S.; Gupta, M. Impact of temperature variations on the device and circuit performance of tunnel FET: A simulation study. *IEEE Trans. Nanotechnol.* **2013**, *12*, 951–957. [\[CrossRef\]](#)
12. Cui, N.; Liang, R.; Wang, J.; Zhou, W.; Xu, J. A PNPN tunnel field-effect transistor with high- k gate and low- k fringe dielectrics. *J. Semicond.* **2012**, *33*, 084004. [\[CrossRef\]](#)
13. Cao, W.; Yao, C.J.; Jiao, G.F.; Huang, D.; Yu, H.Y.; Li, M.F. Improvement in reliability of tunneling field-effect transistor with p-n-i-n structure. *IEEE Trans. Electron Dev.* **2011**, *58*, 2122–2126. [\[CrossRef\]](#)
14. Cho, S.; Kang, I.M. Design optimization of tunneling field-effect transistor based on silicon nanowire PNPN structure and its radio frequency characteristics. *Curr. Appl. Phys.* **2012**, *12*, 673–677. [\[CrossRef\]](#)
15. Jhaveri, R.; Nagavarapu, N.V.; Woo, J.C.S. Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor. *IEEE Trans. Electron Dev.* **2011**, *58*, 80–86. [\[CrossRef\]](#)
16. Tura, A.; Zhang, Z.; Liu, P.; Xie, Y.H.; Woo, J.C.S. Vertical silicon p-n-p-n tunnel nMOSFET with MBE-grown tunneling junction. *IEEE Trans. Electron Dev.* **2011**, *58*, 1907–1913. [\[CrossRef\]](#)
17. Chang, H.Y.; Adams, B.; Chien, P.Y.; Li, J.; Woo, J.C.S. Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing. *IEEE Trans. Electron Dev.* **2013**, *60*, 92–96. [\[CrossRef\]](#)
18. Zhang, Y.; Chu, H. Tunneling Field Effect Transistor (TFET) with Ultra-Shallow Pockets Formed by Asymmetric ion Implantation and Method of Making Same. U.S. Patent 20140158990, June 2014.
19. Li, J.; Liu, Y.; Wei, S.F.; Shan, C. In-Built N+ Pocket Electrically Doped Tunnel FET With Improved DC and Analog/RF Performance. *Micromachines* **2020**, *11*, 960. [\[CrossRef\]](#) [\[PubMed\]](#)
20. De Marchi, M.; Zhang, J.; Frache, S.; Sacchetto, D.; Gaillardon, P.E.; Leblebici, Y.; De Micheli, G. Configurable logic gates using polarity-controlled silicon nanowire gate-all-around FETs. *IEEE Electron Device Lett.* **2014**, *35*, 880–882. [\[CrossRef\]](#)
21. Lahgere, A.; Sahu, C.; Singh, J. PVT-aware design of dopingless dynamically configurable tunnel FET. *IEEE Trans. Electron Dev.* **2015**, *62*, 2404–2409. [\[CrossRef\]](#)
22. Kondekar, P.N.; Nigam, K.; Pandey, S.; Sharma, D. Design and analysis of polarity controlled electrically doped tunnel FET with bandgap engineering for analog/RF applications. *IEEE Trans. Electron Dev.* **2016**, *64*, 412–418. [\[CrossRef\]](#)
23. De Marchi, M.; Sacchetto, D.; Frache, S.; Zhang, J.; Gaillardon, P.-E.; Leblebici, Y.; De Micheli, G. Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs. In Proceedings of the IEEE Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012. [\[CrossRef\]](#)

24. Haynes, W.M. Electron Work Function of the Elements. In *CRC Handbook of Chemistry and Physics*, 95th ed.; Lide, D.R., Bruno, T.J., Eds.; CRC Press: New York, NY, USA, 2008; pp. 12–1014.
25. *ATLAS Device Simulation Software*, version 5.19.20.R; Silvaco: Santa Clara, CA, USA, 2018.
26. Musalgaonkar, G.; Sahay, S.; Saxena, R.S.; Kumar, M.J. A line tunneling field-effect transistor based on misaligned Core–Shell gate architecture in emerging nanotube FETs. *IEEE Trans. Electron Dev.* **2019**, *66*, 2809–2816. [[CrossRef](#)]

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