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Fabrication and Characterization of $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ Composite Channel Metamorphic HEMTs (mHEMTs) on a GaAs Substrate

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Abstract: In this work, we successfully demonstrated $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel metamorphic high electron mobility transistors (mHEMTs) on a GaAs substrate. The fabricated mHEMTs with a 100 nm gate length exhibited excellent DC and logic characteristics such as $V_T = -0.13$ V, $g_{m,max}$ = 949 mS/mm, subthreshold swing (SS) = 84 mV/dec, drain-induced barrier lowering (DIBL) = 89 mV/V, and I_{on}/I_{off} ratio = 9.8×10^3 at a drain-source voltage (V_{DS}) = 0.5 V. In addition, the device exhibited excellent high-frequency characteristics, such as f_T/f_{max} = 261/304 GHz for the measured result and well-matched modeled f_T/f_{max} = 258/309 GHz at V_{DS} = 0.5 V, which is less power consumption compared to other material systems. These high-frequency characteristics are a well-balanced demonstration of f_T and f_{max} in the mHEMT structure on a GaAs substrate.

Keywords: mHEMT; HEMT; InAs HEMT; InGaAs HEMT; Mo-based Ohmic contact; $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel; GaAs; InGaAs/InAs/InGaAs composite channel

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Citation: Shin, S.H.; Shim, J.-P.; Jang, H.; Jang, J.-H. Fabrication and Characterization of $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ Composite Channel Metamorphic HEMTs (mHEMTs) on a GaAs Substrate. *Micromachines* **2023**, *14*, 56. https://doi.org/10.3390/mi14010056

Academic Editor: Han Eol Lee

Received: 29 November 2022
Revised: 20 December 2022
Accepted: 23 December 2022
Published: 25 December 2022

1. Introduction

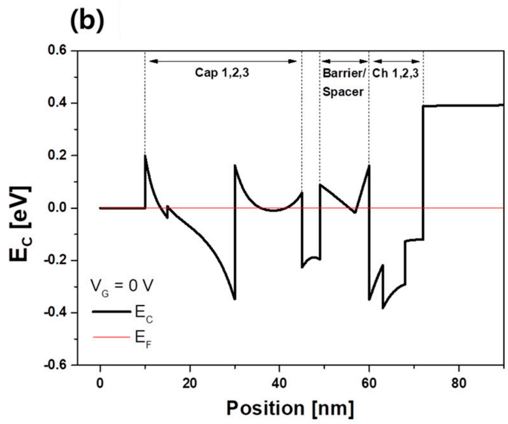
High electron mobility transistors (HEMTs) based on indium-rich $In_xGa_{1-x}As$ channel materials on an InP substrate have demonstrated excellent high-frequency and logic characteristics. In terms of high-frequency characteristics of the InGaAs channel HEMT, H. -B. Jo et al. demonstrated 738 GHz unity current gain cutoff frequency (f_T) in a 19 nm $In_{0.8}Ga_{0.2}As$ composite-channel HEMT on a InP substrate [1], D. -H. Kim et al. showed excellent logic performance and a f_T of 644 GHz in 30 nm InAs Pseudomorphic HEMTs (pHEMTs) [2], and Northrop Grumman Corporation exhibited an f_T of 610 GHz/f_{max} of 1.5 THz by using an $In_{0.53}GaAs/InAs/In_{0.53}GaAs$ composite channel with a L_g of 25 nm [3]. These remarkable performances have been achieved through downscaling of device feature size, an optimized fabrication process, and optimized InGaAs channel materials for excellent transport properties. In addition, InGaAs channel MOSFETs have shown outstanding logic performance on various substrates, such as InP and flexible substrates, with extensive efforts to enhance their capability in new device structures, S/D Ohmic contacts, and optimization of the gate stack [4–7]. Meanwhile, large-size and cheaper-cost substrates will be essential for large-volume manufacturing from a mass production point of view, but an InP substrate is more expensive than a GaAs substrate, and the size to date is limited to 6 inches. To overcome these limitations of the InP substrate, many groups have demonstrated many outstanding results for mHEMTs on a GaAs substrate [8–11]. In particular, Teledyne demonstrated excellent results of a 688 GHz f_T by utilizing an $In_{0.7}GaAs$ mHEMT structure with dual Si δ-doping and an InAs-rich $In_{0.7}Al_{0.3}As$ spacer on a GaAs substrate in 2011 [9]. Fraunhofer showed a maximum oscillation frequency (f_{max}) exceeding 1000 GHz by using an $In_{0.8}GaAs$ mHEMT structure on a GaAs substrate in 2013 [11]. Among various HEMT structures, an InGaAs/InAs/InGaAs composite channel was used to enhance high-frequency characteristics in HEMT structures because of its excellent electron transport properties, such as electron velocity and mobility [2,3,12]. However, an $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel structure on a GaAs substrate has not been demonstrated yet. In this work, we fabricated an $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel HEMT on a GaAs substrate incorporating a molybdenum (Mo)-based Ohmic contact using blanket Mo deposition and investigated its electrical performance, such as DC, logic, and RF characteristics, with an L_g of 100 nm.

2. Layer Structure and Experiments

The mHEMT heterostructures consisted of a 500 nm $In_{0.52}Al_{0.48}As$ buffer, a 12 nm $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ (4/5/3 nm) channel, a 3 nm $In_{0.52}Al_{0.48}As$ spacer, Si δ-doping (4.1×10^{12} cm^{-2}), an 8 nm $In_{0.52}Al_{0.48}As$ barrier, a 4 nm InP etch stop layer, and a 35 nm heavily doped $In_{0.53}Ga_{0.47}As$/$In_{0.52}Al_{0.48}As$ multi-layer cap from the bottom to the top as shown in Figure 1a. The energy band diagram of the epitaxial structure is shown in Figure 1b. From this structure, sheet carrier density and electron hall mobility were measured to be 2.92×10^{12} cm^{-2} and 10,000 cm^2/V·s at room temperature, respectively, with four-point probe measurement methods (Van der Pauw measurement method). Device fabrication began with a 30 nm blanket molybdenum (Mo) deposition for ohmic contact to prevent surface contamination and improve the contact resistance (R_c), then mesa isolation down to an InAlAs buffer layer by Mo dry etching and wet etching. After Ti/Au/Ni (20/150/30 nm) metallization for source and drain, dry etching in an SF_6/Ar plasma was performed to etch Mo in the gate region using the Ni metal etch mask of the source and drain [13]. A 30 nm thick layer of SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD), and then the pad patterns with Ti/Au (20/300 nm) were defined for ground-signal-ground probing. After e-beam exposure, the defined e-beam resist pattern was transferred to define the T-gate by using reactive ion etching based on CF_4 plasma. Gate recessing was performed in two different step stages, followed by anisotropic reactive ion etching of the InP etch stop layer in an Ar-based plasma [14]. After InP etching, Schottky gate metallization of Ti/Pt/Au (20/30/300 nm) was deposited on top of the InAlAs layer. Finally, the mHEMT with a width of 2 × 50 μm was fabricated, and a schematic of the fabricated mHEMT is shown in Figure 1c. Figure 1d shows the SEM image of the fabricated t-gate, whose foot and head sizes are 100 nm and 470 nm, respectively.

(a)

Comment	Material	Thickness	Doping Level
Cap.1	$In_{0.65}GaAs$	5 nm	2×10^{19} cm^{-3}
Cap.2	$In_{0.53}GaAs$	15 nm	2×10^{19} cm^{-3}
Cap.3	$In_{0.52}AlAs$	15 nm	1×10^{19} cm^{-3}
Etch-stop	InP	4 nm	
Barrier	$In_{0.52}AlAs$	8 nm	-
Doping	Si	-	4.1×10^{12} cm^{-2}
Spacer	$In_{0.52}Al_{0.48}As$	3 nm	-
Ch.1	$In_{0.53}Ga_{0.47}As$	3 nm	-
Ch.2	InAs	5 nm	-
Ch.3	$In_{0.53}Ga_{0.47}As$	4 nm	-
Buffer	$In_{0.52}AlAs$	500 nm	-
Substrate	3-inch GaAs	-	-



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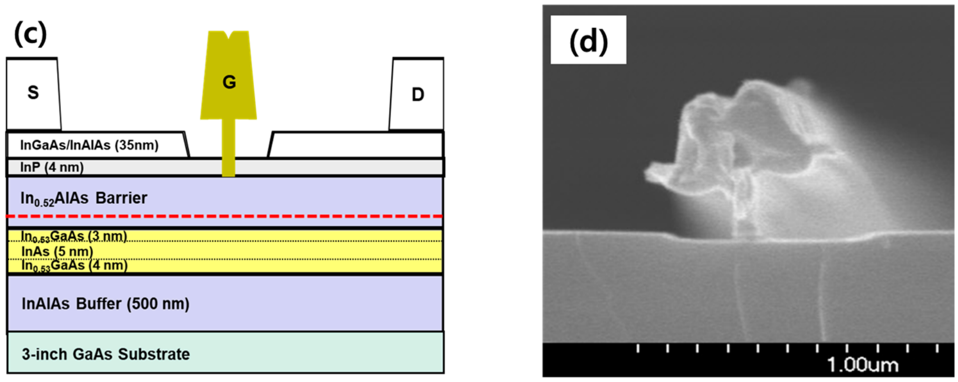

Figure 1. (**a**) Epitaxial structure of the $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel HEMT structure on a GaAs substrate. (**b**) Energy band diagram of the epitaxial structure (**c**) Schematic of the $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel HEMT on a GaAs substrate (**d**) SEM image of the fabricated T-gate.

3. Results and Discussion

The transfer characteristic and output characteristic of the mHEMTs are shown in Figure 2. The maximum transconductance ($g_{m,max}$) and maximum drain current density ($I_{D,max}$) were 949 mS/mm and 413 mA/mm at V_{DS} = 0.5 V, respectively. The output characteristics presented in Figure 2b show good pinch-off characteristics, but the measured R_{on} was 733 Ω-μm, which is a higher value than the lift-off Mo/Ti/Mo/Au metal scheme with an InAs rich InAlAs barrier spacer [15]. The ohmic contact resistance (R_c) and sheet resistance (R_{sh}) measured by the transmission line method (TLM) was as low as 0.01 Ω-mm and 75.5 Ω/sq as shown in Figure 2c. When compared to the lift-off method using a Mo/Ti//Mo/Au scheme (30/20/20/150 nm) on the same multi-cap layer, the blanket Mo method shows a higher R_{sh} value of 75.5 Ω/sq than the lift-off method of 69.2 Ω/sq because of SF_6/Ar plasma damage in the active region during Mo etching to define the active gate region. However, the blanket Mo method shows a Rc of 0.011 Ohm-mm, which is lower than that of 0.026 Ohm-mm with the lift-off method because it is beneficial to protect the surface underneath the metal contact region from contaminants during the device process. Due to the lower R_c of the Mo blanket method, a lower R_{on} value could be achieved if the S/D distance was reduced, as in the self-aligned gate scheme.

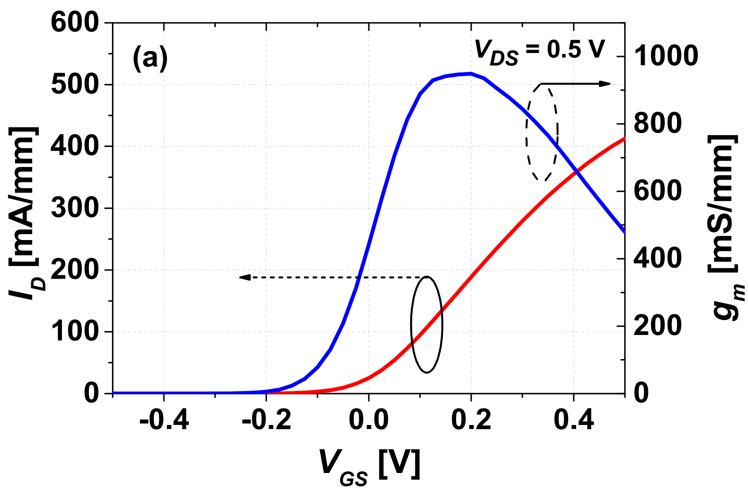

Figure 2. *Cont.*

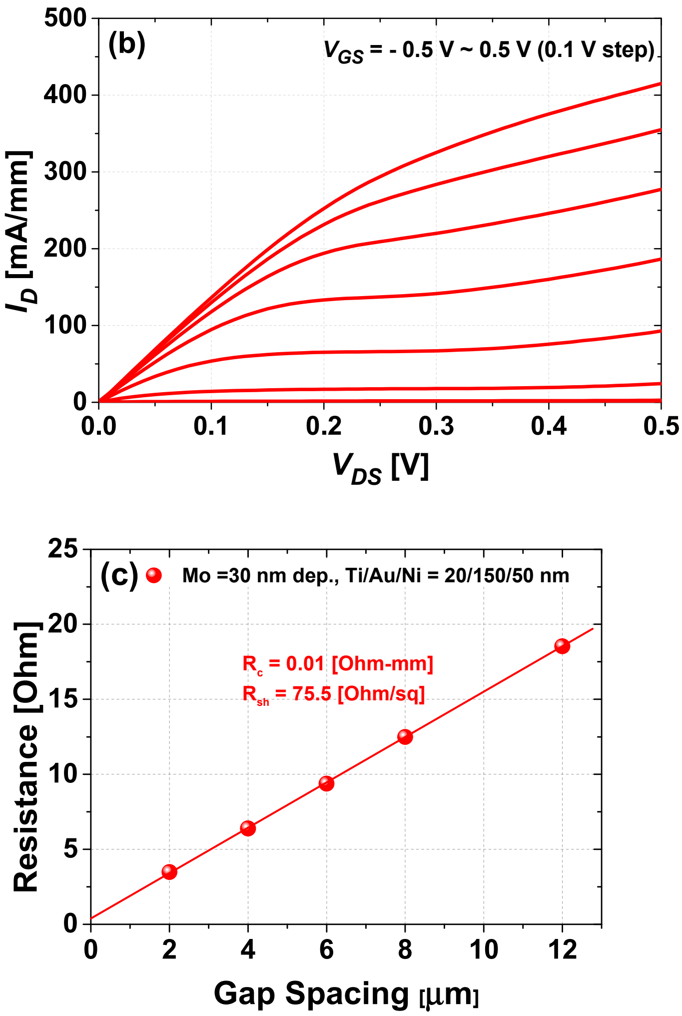

Figure 2. (**a**) Typical transfer characteristics of the mHEMTs measured at V_{DS} = 0.5 V. (**b**) Typical output characteristics of the mHEMTs (V_{GS} = −0.5 V ~ 0.5 V). (**c**) TLM result of the Mo-based Ohmic contact.

Figure 3 shows the subthreshold characteristics at V_{DS} = 0.5 V and 0.05 V, respectively. At V_{DS} = 0.5 V, the threshold voltage (V_T) is −0.13 V, defined as the value of V_{GS} that yields at I_D = 1 mA/mm, and a V_T of −0.13 V indicates that the fabricated mHEMT operated in depletion mode (D-mode). The fabricated device shows excellent electrostatic integrity, such as the subthreshold swing (SS) of 84 mV/dec, the drain-induced barrier lowering (DIBL) of 89 mV/V, and the I_{on}/I_{off} ratio of 9.8 × 10^3, respectively. Additionally, the gate leakage current of the fabricated mHEMT was measured at V_{DS} = 0.5 V and shows that the gate Schottky metallization is in good contact with the $In_{0.52}Al_{0.48}As$ barrier layer. These outstanding logic performances are due to the well-designed heterostructure and optimized fabrication process on the GaAs substrate.

To verify the high-frequency RF characteristics of the mHEMT, S-parameters were measured from 0.5 to 40 GHz using a vector network analyzer (VNA). In addition, small-signal modeling was performed by using a small-signal equivalent circuit [16], and we found that small-signal modeling and measured S-parameters are well matched, as shown in Figure 4a. Figure 4b shows the unity current gain cutoff frequency (f_T), maximum oscillation frequency (f_{max}), and maximum stable gain (MSG)/maximum available gain (MAG) against frequency for the measured results (symbols) and modeled results (solid lines) at V_{DS} = 0.5 V and V_{GS} = 0.2 V with a L_g of 100 nm mHEMT device. The de-embedding method was done by using open and short patterns to extract parasitic pad capacitance and inductance. We obtained 261 GHz/304 GHz for f_T/f_{max} by extrapolation (dashed lines) and 258 GHz/309 GHz for f_T/f_{max} by small-signal modeling, respectively. This excellent high-frequency response is due to the high value of the intrinsic transconductance (g_{mi}) of 2.0 mS/µm. The extracted intrinsic parameters of the mHEMT are summarized in Table 1 and are well-matched to the measured results. The difference between $g_{m,ext}$ (0.95 mS/µm) and g_{mi} (2.0 mS/µm) is due to the R_s and g_o values according to equation (1) [17].

$$g_{m,ext} = g_{mi}(1 - 2R_s \cdot g_o)/(1 + R_s \cdot g_{mi}) \quad (1)$$

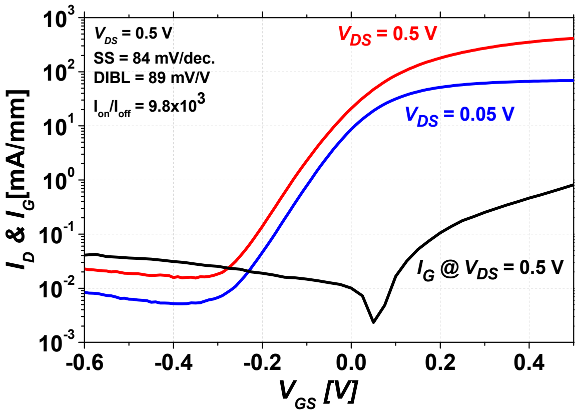

Figure 3. Subthreshold characteristics of the mHEMT were measured at V_{DS} = 0.5 V and V_{DS} = 0.05 V, and the gate leakage current was measured at V_{DS} = 0.5 V, respectively.

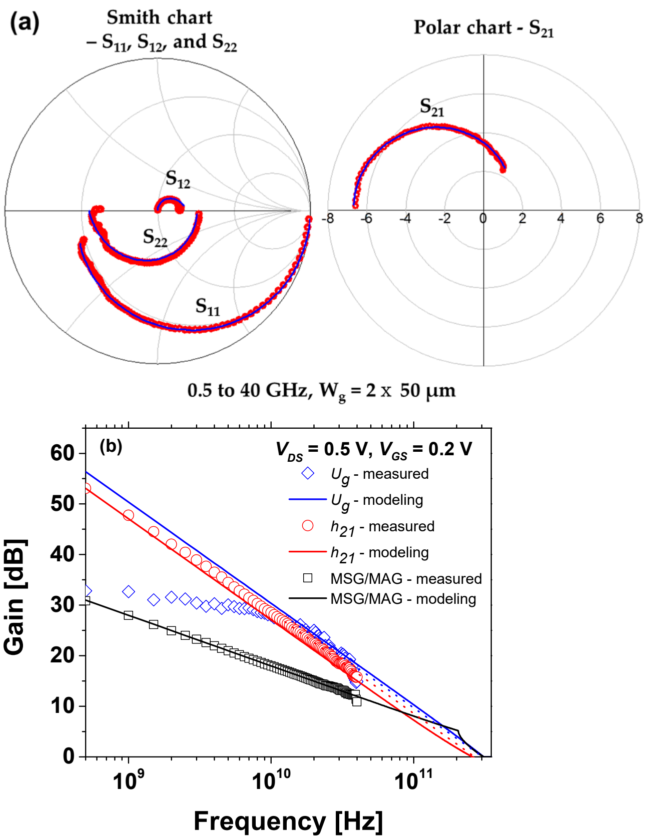

Figure 4. (**a**) Comparison of small-signal modeling and measured S-parameters at V_{DS} = 0.5 V and V_{GS} = 0.2 V. A Smith chart of S_{11}, S_{12}, and S_{22} (left) and a polar chart of S_{12} (right). (**b**) Measured (symbols) and modeled (solid lines) of RF gains-Maximum oscillation frequency (f_{max}), maximum stable gain (MSG)/maximum available gain (MAG), and unity current gain cutoff frequency (f_T) of the mHEMTs at V_{DS} = 0.5 V and V_{GS} = 0.2 V.

Table 1. Extracted intrinsic small-signal parameters.

Intrinsic Parameters	Measured f_T	Modeling f_T
g_{mi} = 2.0 mS/µm	261 GHz	258 GHz
g_{ds} = 0.22 mS/µm		
R_g = 70 Ω-µm		
R_s = 360 Ω-µm		
R_d = 360 Ω-µm	**Measured f_{max}**	**Modeling f_{max}**
R_i = 100 Ω-µm	304 GHz	309 GHz
C_{gs} = 0.65 fF/µm		

Figure 5 shows f_T and f_{max} as functions of I_D at V_{DS} = 0.5 V and 0.4 V. Around an I_D of 75 mA/mm, our device had already exhibited an f_T and f_{max} value of over 200 GHz and was confirmed to operate stably for the fabricated mHEMT.

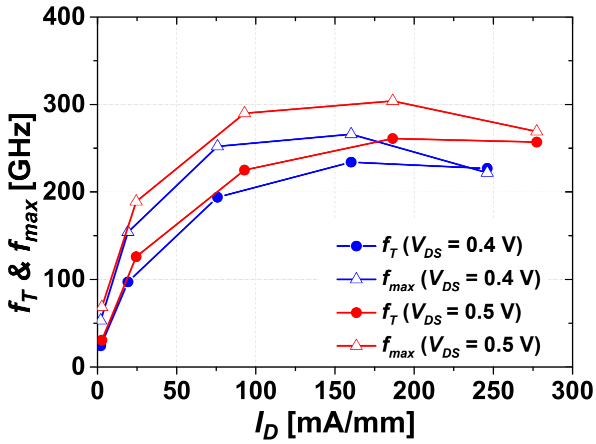

Figure 5. Maximum oscillation frequency (f_{max}) and unity current gain cutoff frequency (f_T) of the mHEMTs against drain current density (I_D) at a V_{DS} = 0.5 and 0.4 V, respectively.

Table 2 shows the benchmark high-frequency characteristics of the published state-of-the-art pHEMT and mHEMT results with an L_g of 100 nm. Among various HEMT structures, the $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel HEMT on an InP substrate shows excellent high-frequency characteristics such as an f_T of 421 GHz and an f_{max} of 620 GHz because of the well-optimized fabrication process and improved carrier transport properties of the $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel [18]. Our fabricated mHEMT exhibits an excellent $L_g f_T$ of 26.1 GHz-µm, which is related to carrier transport properties [19], and an outstanding f_T/f_{max} of 261/304 GHz with a L_g of 100 nm at a V_{DS} = 0.5 V. Although the performance of the fabricated mHEMT is not comparable to that of the $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel HEMT on an InP substrate, our fabricated mHEMT shows outstanding high-frequency characteristics compared to a single InGaAs channel HEMT on an InP substrate and other mHEMT structures because of the excellent transport properties of the composite channel on a GaAs substrate. Additionally, our fabricated device is operated at a V_{DS} = 0.5 V, which has a lower power consumption than other group devices' operational voltage. These excellent performances are mainly attributed to the well-grown $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel structure by using an $In_{0.52}AlAs$ buffer layer on a GaAs substrate, and a fabricated mHEMT would be a good candidate for the high-frequency device in both 5G and 6G communications through further scaling-down of device feature size.

Table 2. Performance parameters of the pHEMTs and mHEMTs with a L_g of 100 nm.

	[20]	[18]	[21]	[22]	**This Work**
Substrate	InP	InP	GaAs	GaAs	GaAs
Channel	$In_{0.68}Ga_{0.32}As$	$In_{0.53}Ga_{0.47}As$ /InAs/ $In_{0.53}Ga_{0.47}As$	$In_{0.65}Ga_{0.35}As$/ $In_{0.53}Ga_{0.47}As$	$In_{0.6}Ga_{0.4}As$	$In_{0.53}Ga_{0.47}As$ /InAs/ $In_{0.53}Ga_{0.47}As$
Buffer layer	InAlAs buffer	InAlAs buffer	Linear $In_xAl_{0.48}Ga_{0.52-x}As$	Graded InAlAs	500 nm $In_{0.52}AlAs$
L_g [nm]	100	100	100	100	100
f_T [GHz]	183	421	220	210	261
f_{max} [GHz]	230	620	300	252	304
$L_g f_T$ [GHz-µm]	18.3	42.1	22.0	21.0	26.1
V_{DS} [V]	0.5	0.7	1	1	0.5
Passivation	100 nm SiN_x	-	250 nm SiN_x	50 nm SiN_x	-

4. Conclusions

The 100 nm $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel metamorphic high electron mobility transistors (mHEMTs) on a GaAs substrate exhibited excellent logic characteristics as well as high-frequency RF performances. These outstanding performances are due to the excellent carrier transport properties of the well-grown $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel mHEMT structure on a GaAs substrate and an optimized fabrication process. The proposed mHEMT structure on a GaAs substrate, together with optimized source/drain and gate technologies, will potentially improve logic and high-frequency characteristics. Furthermore, the proposed mHEMT structure grown on a large-size GaAs substrate could be indispensable for large-volume manufacturing.

Author Contributions: Conceptualization, S.H.S. and J.-H.J.; methodology, S.H.S., H.J. and J.-P.S.; validation, S.H.S., H.J. and J.-P.S.; formal analysis, S.H.S. and J.-P.S.; investigation, S.H.S., H.J. and J.-P.S.; resources, S.H.S. and J.-H.J.; data curation, S.H.S. and J.-P.S.; writing—original draft preparation, S.H.S., H.J. and J.-P.S.; writing—review and editing, S.H.S. and J.-P.S.; visualization, S.H.S. and J.-P.S.; supervision, S.H.S. and J.-H.J.; funding acquisition, S.H.S. and J.-P.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the National R&D Program through the National Research Foundation of Korea (NRF), funded by the Ministry of Science and ICT (2022M3I8A1078437), and the Nanomaterial Technology Development Program through the National Research Foundation of Korea (NRF), funded by the Ministry of Science, ICT, and Future Planning (2009-0082580).

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

References

1. Jo, H.-B.; Yun, S.-W.; Kim, J.-G.; Yun, D.-Y.; Lee, I.-G.; Kim, D.-H.; Kim, T.-W.; Kim, S.-K.; Yun, J.; Kim, T.; et al. Lg = 19 nm $In_{0.8}Ga_{0.2}As$ composite-channel HEMTs with ft = 738 GHz and fmax = 492 GHz. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 12–18 December 2020.
2. Kim, D.-H.; del Alamo, J.A. 30-nm InAs PHEMTs With f_T = 644 GHz and f_{max} = 681 GHz. *IEEE Electron Device Lett.* **2010**, *31*, 806–808.
3. Mei, X.; Yoshida, W.; Lange, M.; Lee, J.; Zhou, J.; Liu, P.-H.; Leong, K.; Zamora, A.; Padilla, J.; Sarkozy, S.; et al. First Demonstration of amplification at 1 THz using 25-nm InP high electron mobility transistor process. *IEEE Electron Device Lett.* **2015**, *36*, 327–329. [CrossRef]

4. Shin, C.-S.; Park, W.-K.; Shin, S.H.; Cho, Y.D.; Ko, D.H.; Kim, T.-W.; Koh, D.H.; Kwon, H.M.; Hill, R.J.; Kirsch, P.; et al. Sub-100 nm regrown S/D gate-last $In_{0.7}Ga_{0.3}As$ QW MOSFETs with $\mu_{n,\,eff}$ > 5,500 cm^2/v-S. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014.
5. Jo, H.-B.; Lee, I.-G.; Baek, J.-M.; Lee, S.T.; Choi, S.-M.; Kim, H.-J.; Jeong, H.-S.; Park, W.-S.; Yoo, J.; Lee, H.-Y.; et al. Lg = 130 nm GAA MBCFETs with three-level stacked $In_{0.53}Ga_{0.47}As$ nanosheets. In Proceedings of the 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 12–17 June 2022.
6. Kim, T.-W.; Kim, D.-H.; Koh, D.H.; Kwon, H.M.; Baek, R.H.; Veksler, D.; Huffman, C.; Matthews, K.; Oktyabrsky, S.; Greene, A.; et al. Sub-100 nm InGaAs quantum-well (QW) tri-gate MOSFETs with Al_2O_3/HfO_2 (EOT < 1 nm) for low-power logic applications. In Proceedings of the 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 9–11 December 2013.
7. Park, S.; Kim, D.-K.; Cho, Y.-D.; Shim, J.-P.; Shin, C.-S.; Shin, S.H. Demonstration of high performance flexible $In_{0.7}Ga_{0.3}As$ MOSFETs using liquid polyimide (LPI) transfer. *IEEE Electron Device Lett.* **2022**, *43*, 858–861. [CrossRef]
8. Leuther, A.; Weber, R.; Dammann, M.; Schlechtweg, M.; Mikulla, M.; Walther, M.; Weimann, G. Metamorphic 50 nm InAs-channel HEMT. In Proceedings of the International Conference on Indium Phosphide and Related Materials, Glasgow, UK, 8–12 May 2005.
9. Kim, D.-H.; Brar, B.; del Alamo, J.A. Ft = 688 GHz and Fmax = 800 GHz in Lg = 40 nm $In_{0.7}Ga_{0.3}As$ MHEMTs with Gm_max > 2.7 ms/µm. In Proceedings of the 2011 International Electron Devices Meeting, Washington, DC, USA, 5–7 December 2011.
10. Komiak, J.J.; Smith, P.M.; Duh, K.H.; Xu, D.; Chao, P.C. Metamorphic HEMT technology for microwave, millimeter-wave, and submillimeter-wave applications. In Proceedings of the 2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Monterey, CA, USA, 13–16 October 2013.
11. Leuther, A.; Tessmann, A.; Dammann, M.; Massler, H.; Schlechtweg, M.; Ambacher, O. 35 nm mHEMT technology for THz and Ultra Low Noise Applications. In Proceedings of the 2013 International Conference on Indium Phosphide and Related Materials (IPRM), Kobe, Japan, 19–23 May 2013.
12. Akazaki, T.; Arai, K.; Enoki, T.; Ishii, Y. Improved InAlAs/InGaAs HEMT characteristics by inserting an InAs layer into the InGaAs channel. *IEEE Electron Device Lett.* **1992**, *13*, 325–327. [CrossRef]
13. Baraskar, A.K.; Wistey, M.A.; Jain, V.; Singisetti, U.; Burek, G.; Thibeault, B.J.; Lee, Y.J.; Gossard, A.C.; Rodwell, M.J. Ultralow resistance, nonalloyed ohmic contacts to N-InGaAs. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.* **2009**, *27*, 2036. [CrossRef]
14. Suemitsu, T.; Yokoyama, H.; Ishii, T.; Enoki, T.; Meneghesso, G.; Zanoni, E. 30-nm two-step recess gate InP-based InAlAs/InGaAs HEMTs. *IEEE Trans. Electron Devices* **2002**, *49*, 1694–1700. [CrossRef]
15. Kim, T.-W.; Kim, D.-H.; del Alamo, J.A. InGaAs HEMT with InAs-rich InAlAs barrier spacer for reduced source resistance. *Electron. Lett.* **2011**, *47*, 406. [CrossRef]
16. Dambrine, G.; Cappy, A.; Heliodore, F.; Playez, E. A new method for determining the FET small-signal equivalent circuit. *IEEE Trans. Microw. Theory Tech.* **1988**, *36*, 1151–1159. [CrossRef]
17. Yun, S.-W.; Kim, D.-H. Comprehensive study of components affecting extrinsic transconductance in $In_{0.7}Ga_{0.3}As$ quantum-well high-electron-mobility transistors for image sensor applications. *J. Sens. Sci. Technol.* **2021**, *30*, 441–445. [CrossRef]
18. Kim, D.-H.; Chen, P.; Kim, T.-W.; Urteaga, M.; Brar, B. LG = 100 nm InAs pHEMTs on InP substrate with record high frequency response. *Electron. Lett.* **2012**, *48*, 1352. [CrossRef]
19. Geum, D.M.; Shin, S.H.; Kim, M.S.; Jang, J.H. 75 nm t-shaped gate for $In_{0.17}Al_{0.83}N$/GaN HEMTs with minimal short-channel effect. *Electron. Lett.* **2013**, *49*, 1536–1537. [CrossRef]
20. Liu, L.; Alt, A.R.; Benedickter, H.; Bolognesi, C.R. InP-HEMT X-band low-noise amplifier with Ultralow 0.6-mW power consumption. *IEEE Electron Device Lett.* **2012**, *33*, 209–211. [CrossRef]
21. Tessmann, A. 220-GHz metamorphic HEMT amplifier MMICS for high-resolution imaging applications. *IEEE J. Solid-State Circuits* **2005**, *40*, 2070–2076. [CrossRef]
22. Lee, J.M.; Chang, W.J.; Kang, D.M.; Min, B.G.; Yoon, H.S.; Chang, S.J.; Jung, H.W.; Kim, W.; Jung, J.; Kim, J.; et al. W-band MMIC chipset in 0.1-um mHEMT technology. *ETRI J.* **2020**, *42*, 549–561. [CrossRef]