



# Article Optimization of the Field Plate Design of a 1200 V p-GaN Power High-Electron-Mobility Transistor

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**Abstract:** This study optimized the field plate (FP) design (i.e., the number and positions of FP layers) of p-GaN power high-electron-mobility transistors (HEMTs) on the basic of simulations conducted using the technology computer-aided design software of Silvaco. Devices with zero, two, and three FP layers were designed. The FP layers of the HEMTs dispersed the electric field between the gate and drain regions. The device with two FP layers exhibited a high off-state breakdown voltage of 1549 V because of the long distance between its first FP layer and the channel. The devices were subjected to high-temperature reverse bias and high-temperature gate bias measurements to examine their characteristics, which satisfied the reliability specifications of JEDEC.

**Keywords:** dynamic on-state resistance (R<sub>on</sub>); field plate (FP); high-temperature gate bias (HTGB); high-temperature reverse bias (HTRB); normally off operation; off-state breakdown voltage; p-GaN high-electron-mobility transistor (HEMT)

## 1. Introduction

GaN power transistors have become key devices in high-power and high-efficiency power conversion systems because of their suitable material properties, such as a wide band gap, high electron mobility, and high critical breakdown field. Various approaches such as using a gate-recessed structure [1-3], fluorine ion treatment [4], and adopting a p-type GaN cap layer—have been reported for enabling these devices to exhibit normally off operation [5–7]. Next-generation, high-power, and high-frequency switching systems are expected to be used in GaN power devices because of the superior characteristics of these systems. In particular, p-GaN power devices could be accepted in the market because the normally off operation offers a fail-safe requirement [8]. However, device reliability is a crucial factor that must be considered when GaN power devices are applied in high-power circuits. Many studies have examined the reliability of p-GaN high-electronmobility transistors (HEMTs), using methods such as the high-thermal reverse bias test (HTRB) [9–11], high-temperature gate bias (HTGB)-stress-induced instability [12–14], hardswitching robustness [15], and short-circuit safe operating area [16–18]; however, further comprehensive research is still required on the long-term reliability of GaN HEMTs. The reliability of p-GaN HEMTs depends on their  $V_{\text{TH}}$  shifts [19], gate stress [20], and dynamic performance [21] as well as temperature [22].

In power switching applications, the devices are repetitively switched between ON and OFF states at high frequency. When the device is operated in OFF states, a high drain bias stress might affect the device breakdown voltage and  $V_{\text{TH}}$  shifts [23]. These shifts are caused by a strong electric field, electron trapping and detrapping, and hole deficiencies.



Citation: Liu, C.-H.; Huang, C.-R.; Wang, H.-C.; Kang, Y.-J.; Chiu, H.-C.; Kao, H.-L.; Chu, K.-H.; Kuo, H.-C.; Chen, C.-T.; Chang, K.-J. Optimization of the Field Plate Design of a 1200 V p-GaN Power High-Electron-Mobility Transistor. *Micromachines* 2022, *13*, 1554. https://doi.org/10.3390/mi13091554

Academic Editor: Peng Song

Received: 29 August 2022 Accepted: 15 September 2022 Published: 19 September 2022

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**Copyright:** © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). This can be explained by the existence of a charge storage mechanism. When a high drain bias  $V_{\text{DSQ}}$  is applied to a p-GaN gate HEMT, the gate-to-drain capacitance ( $C_{\text{GD}}$ ) is charged to  $Q_{\text{GD}}$  ( $V_{\text{DSQ}}$ ). The net-positive charges at the drain-side access region are provided by the depletion of a two-dimensional electron gas. Therefore, drain-induced  $V_{\text{TH}}$  instability and large  $V_{\text{TH}}$  shifts are observed for p-GaN gate HEMTs when they are operated under a high drain voltage [24]. Another problem observed when p-GaN power devices are used for power switching is the dynamic on-state resistance ( $R_{\text{on}}$ ), which is measured immediately after the device is switched from the off state to the on state under a high drain stress. However, when a high drain stress is applied during the off state of the device, an electric field peak occurs at the gate edge, and some electrons might be accelerated and trapped in the surface or epitaxial layer of the device [25].

Some researchers have explored the failure mechanisms of normally off p-GaN HEMTs [26]. However, further research is required on this topic. According to Li, the  $V_{\text{TH}}$  shifts of a p-GaN gate HEMT under high-temperature reverse bias (HTRB) and NBTI stress occur because of hole emission in the p-GaN layer induced by the reverse bias. Li speculated that high temperatures can suppress the emission of holes or accelerate the detrapping of holes in experiments conducted under HTRB [27].

This study designed p-GaN power devices with different field plate (FP) setups (in terms of the number and positions of FP layers) and simulated the operation of these devices by using the technology computer-aided design (TCAD) software of Silvaco to examine their electric field between the gate and drain regions. The devices were then subjected to DC, off-state breakdown voltage, pulse, HTRB, and HTGB measurements.

#### 2. Simulation Results

Three devices with different numbers of FP layers (zero, two, and three) located at different distances from the channel were designed. In this paper, the terms FP1, FP2, and FP3 denote the first, second, and third FP layers, respectively. The distributions of the electric fields of the devices under high drain bias were simulated using the TCAD software of Silvaco (Figure 1a–c). For the p-GaN HEMT without an FP (Figure 1a), most of the potential lines were concentrated around the drain side of the gate, which indicates that a high electric field peak can form for this device. For the p-GaN HEMTs with FP layers, high potential line density was observed at the drain side of the gate edge and the edges of FP1, FP2, and FP3. These results can be attributed to the modulation effect of the FPs, which disperse the electric field peak between the gate and drain regions.



**Figure 1.** Electric field simulation results for a (**a**) p-GaN HEMT without an FP, (**b**) p-GaN HEMT with three FP layers, and (**c**) p-GaN HEMT with two FP layers.

### 3. Device Structure

p-GaN HEMTs were grown on 6-inch-diameter (15.24 cm-dia.) Si substrates through metal–organic chemical vapor deposition (MOCVD). A 300-nm-thick undoped GaN channel was deposited on top of a 4-µm-thick undoped GaN buffer transition layer. A 12-nm-thick Al<sub>0.17</sub>Ga<sub>0.83</sub>N layer, 1-nm-thick AlN etching stop layer, and 70-nm-thick p-GaN layer were then deposited in the channel. Finally, the wafer was annealed in an MOCVD chamber at 720 °C for 10 min in a N<sub>2</sub> atmosphere, and the activated Mg concentration was determined to be  $1 \times 10^{18}$  cm<sup>-3</sup> through Hall effect measurement.

First, p-GaN island etching was achieved through ICP with Cl<sub>2</sub>/BCl<sub>3</sub>/SF<sub>6</sub>, and the device was isolated through Ar<sup>+</sup> ion implantation. Subsequently, a Ti/Al/Ni/Au layer was deposited as an ohmic metal and then annealed at 875 °C for 30 s in a N<sub>2</sub> atmosphere. A SiN layer was then deposited on the device as a passivation layer, and a Mo/Au layer was stacked as the gate metal after the gate through etching. To disperse the electric field between the gate and drain regions, the first FP layer was deposited after the stacking of SiN. The second and third FP layers were then stacked on the device (Figure 2a,b). Table 1 presents the distances from FP1 to the gate, from FP1 to the channel, from FP2 to the gate, from FP3 to the gate, and from FP3 to the channel. The p-GaN power devices with FP layers had  $L_{GS}$ ,  $L_G$ ,  $L_{GD}$ , and  $W_G$  values of 1.5 µm, 2 µm, 17.5 µm, and 100 mm, respectively.



Figure 2. Cross-sectional schematics of the devices with (a) two and (b) three FP layers.

**Table 1.** Distances in the devices with two and three FP layers.

(Unit=µm)	L <sub>SD</sub>	L <sub>GD</sub>	L <sub>GS</sub>	FP1~Gate	FP1~Channel	FP2~Gate	FP2~Channel	FP3~Gate	FP3~Channel
Device with 2 FP layers	21	17.5	1.5	3	0.5	7	1.2	×	×
Device with 3 FP layers				2	0.3	4.75	0.7	10.5	1.7

#### 4. Experimental Results and Discussion

The  $I_{DS}-V_{GS}$ ,  $I_{DS}-V_{DS}$ , and  $I_{GS}-V_{GS}$  characteristics of the devices with two and three FP layers are presented in Figure 3a–c, respectively. These characteristics were measured using the Agilent B1505A power device analyzer at room temperature, and the maximum current compliance was set to 20 A. No large differences were observed in the DC characteristics of the devices under a low gate bias and drain bias because the epitaxial structure of the devices was the same. Both devices exhibited a  $V_{TH}$  value of 2.2 V and an  $I_{DS\_Leakage}$  value of  $1 \times 10^{-6}$  A (Figure 3a). They exhibited a dynamic on-state resistance (R<sub>on</sub>) of 200 m $\Omega$ , an  $I_{DS\_saturation}$  value of 15 A (@ $V_{DS} = 10$  V,  $V_{GS} = 6$  V), and an  $I_{GS\_Leakage}$  value of 600  $\mu$ A (@ $V_{GS} = 6$  V) (Figure 3b,c). To demonstrate the function of the FPs, the off-state breakdown voltage was measured (Figure 3d). The devices with two and three FP layers

exhibited off-state breakdown voltages of 1549 and 1353 V, respectively. Thus, both devices exhibited the same leakage level between 0 and 1000 V, and the device with two FP layers exhibited a lower leakage current than the device with three FP layers when the  $V_{DS}$  bias was higher than 1000 V. The highest off-state breakdown voltage can be attributed to the electric field in the vertical direction, which was highly dispersed at the gate edges. In general, FPs disperse the electric field at the gate edge effectively; thus, they can be used to improve the horizontal electric potential line. However, the vertical electric potential line is always ignored. As displayed in Figure 1b, when FP1 was closer to the channel, the potential line density between FP1 and the channel was higher. By contrast, when the distance between FP1 and the channel was longer, the potential line density between FP1 and the channel was longer in the device breakdown voltage under a high drain bias (Figure 1c).



**Figure 3.** (a)  $I_{DS}$ - $V_{GS}$ , (b)  $I_{DS}$ - $V_{DS}$ , (c)  $I_{GS}$ - $V_{GS}$ , and (d) off-state breakdown voltage characteristics of the devices with two and three FP layers.

For comparison with the international company, the measurement conditions were a pulse width of 10  $\mu$ s and a period of 2000  $\mu$ s. The time waveform of the device under a  $V_{\text{DSQ}}$  value of 600 V is displayed in Figure 4a. As displayed in Figure 4b, R<sub>on</sub> was measured under different  $V_{\text{DSQ}}$  values from 0 to 600 V in 100 V increments. The R<sub>on</sub> values of the devices with two and three FP layers were 1.36 and 1.31 times (@ $V_{\text{DSQ}} = 600$  V), respectively. The R<sub>on</sub> values of these devices increased as  $V_{\text{DSQ}}$  was increased from 0 to 400 V. As  $V_{\text{DSQ}}$  was further increased from 400 to 600 V, R<sub>on</sub> values of the devices decreased. The aim of this study was to design an FP setup that can suppress the hot electron injection behavior at the gate edge under a high drain stress bias [28]. The results can be attributed to the electron trapping and detrapping as well as the two-dimensional hole gas (2DHG) in the devices when they were operated at different  $V_{\text{DSQ}}$  values. Therefore, the increase in R<sub>on</sub> was caused by hot electron injection and the trapping and detrapping of electrons at the device surface or epitaxial interface during off-state operation, and then it could not be released

when the device was turned on in the extremely short switching time. However, enhanced vertical leakage was observed in the entire area between the source and the drain [29,30], electron trapping was observed at donor defects [31], and the 2DHG formed at the interface of C-doped GaN. The formation of a strain relief layer [32] under a high  $V_{DSQ}$  value results in a decrease in the number of trapped electrons, which causes a reduction in R<sub>on</sub> [33]. The energy band diagram for the substrate region under a high  $V_{DSQ}$  bias is displayed in Figure 4c.



**Figure 4.** (a) Waveform of operating time during pulse measurement, (b) normalized  $R_{on}$  values under different  $V_{DSQ}$  values, and (c) energy band diagram for the substrate region under a high  $V_{DSQ}$  bias.

The devices with two and three FP layers were subjected to HTRB and HTGB measurements. For commercial GaN power devices, the stress bias in HTRB measurement is set to 80% of the off-state breakdown voltage, and the stress bias in HTGB measurement is set to 100% of the gate turn-on voltage (reference from JEDEC). In this study, during the HTGB measurement, the drain and source were always grounded, the gate stress bias was 5 V, the chamber temperature was 150 °C, and the devices were under bias stress for 168 h. Figure 5a presents the time tracks of the gate leakage currents (@ $V_{GS} = 5$  V) of both devices. The results indicate that the gate leakage currents of both devices were distributed between 200 and 600 µA, and the devices did not break down after 168 h under bias stress. During the HTRB measurement, the gate and source were always grounded, the drain stress bias was 600 V, the chamber temperature was 150 °C, and the devices were under bias stress for 168 h. Figure 5b displays time tracks of the drain leakage currents of both devices.



drain leakage currents of both devices were distributed between 50 and 200  $\mu$ A, and the devices did not break down after 168 h under bias stress.

**Figure 5.** Time tracks of I<sub>DS</sub> for the devices with two and three FP layers in the (**a**) HTGB measurement and (**b**) HTRB measurement.

After HTGB measurement, the  $I_{DS}-V_{GS}$ ,  $I_{DS}-V_{GS}$ , and  $I_{GS}-V_{GS}$  characteristics of the devices with two and three FP layers were measured again to observe the changes in these parameters. After HTGB measurement, the device with two FP layers exhibited a  $V_{TH}$  shift of 15%, a 7% increase in R<sub>on</sub>, and a 15% increase in the gate leakage current. The device with three FP layers exhibited a  $V_{TH}$  shift of 14%, a 4% increase in R<sub>on</sub>, and a 6% increase in the gate leakage current. After HTRB measurement, the DC characteristics of the devices with two and three FP layers were remeasured to observe the changes in these characteristics. After HTRB measurement, the device with two FP layers exhibited a  $V_{TH}$  shift of 4%, a 4% increase in R<sub>on</sub>, and a 4% increase in the gate leakage current. The device with three FP layers exhibited a  $V_{TH}$  shift of 4%, a 4% increase in R<sub>on</sub>, and a 4% increase in the gate leakage current. The device with three FP layers exhibited a  $V_{TH}$  shift of 4%, a 4% increase in R<sub>on</sub>, and a 4% increase in the gate leakage current. The device with three FP layers exhibited a  $V_{TH}$  shift of 4%, a 4% increase in R<sub>on</sub>, and a 4% increase in the gate leakage current. The device with three FP layers exhibited a  $V_{TH}$  shift of 4%, a 4% increase in R<sub>on</sub>, and a 4% increase in the gate leakage current. The characteristics of the devices with two and three FP layers are presented in Table 2.

H	TGB	V <sub>TH</sub>	Ron	$I_{\rm GS}@V_{\rm GS} = 5 \rm V$	
Temperature = $150 \degree C$	Device with 2 FP layers	15%	7%	15%	
Time = 168 h	Device with 3 FP layers	14%	4%	6%	
H	TRB	V <sub>TH</sub>	Ron	$I_{\rm GS}@V_{\rm GS} = 5 \text{ V}$	
Temperature = $150 \degree C$ Vpc = $600 \text{ V}$ Vpc = $0 \text{ V}$	Device with 2 FP layers	<4%	<4%	<4%	
$V_{DS} = 000 V, V_{CS} = 0 V$ Time = 168 h	Device with 3 FP layers	<4%	<4%	<4%	

Table 2. Characteristics of the devices with two and three fp layers after the htrb and htgb measurements.

The results indicate that the device performance degraded after HTRB measurement. After subjecting a p-GaN HEMT to HTRB, surface defects and negative charges are generated, which can result in a negative potential. Consequently, the channel is depleted of electrons, and the gate depletion region is thus extended [34,35]. However, after a p-GaN HEMT is subjected to HTGB, a strong electric field can favor the generation of defects in p-GaN (similar to that observed in an AlGaN barrier under a negative bias), which leads to the generation of leakage paths and consequently the failure of the gate junction [36].

#### 5. Conclusions

We compared the electrical characteristics of p-GaN HEMTs with different FP setups using the TCAD software of Silvaco. The DC characteristics of p-GaN HEMTs with two and three FP layers did not differ under low voltage operation. However, when these devices were operated under a high drain bias, the device with two FP layers exhibited a higher off-state breakdown voltage (1549 V) than the device with three FP layers (1353 V), which can be attributed to the higher dispersion of the vertical electric field for the device with two FP layers. Both devices exhibited low R<sub>on</sub> values under high  $V_{DSQ}$  values because of the leakage current from the substrate region. The device with two FP layers had a lower manufacturing cost than that with three FP layers. Thus, the device with two FP layers was superior to that with three FP layers.

Author Contributions: Conceptualization, C.-H.L. and H.-C.W.; Methodology, C.-R.H. and H.-C.W.; Formal analysis, C.-R.H. and Y.-J.K.; Data curation, Y.-J.K. and K.-H.C.; Investigation, K.-H.C. and C.-T.C.; Writing—original draft preparation, C.-H.L.; Supervision, H.-C.C., H.-L.K., H.-C.K., and K.-J.C.; Project administration, H.-C.C.; Resources, H.-L.K., H.-C.K., C.-T.C., and K.-J.C. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the Ministry of Science and Technology (MOST), Taiwan, R.O.C., grant numbers MOST 111-2221-E-182-060 and MOST 111-2218-E-008-005; and the Chang Gung Memorial Hospital, Taiwan, R.O.C., grant number BMRP828.

Conflicts of Interest: The authors declare no conflict of interest.

#### References

- Lanford, W.; Tanaka, T.; Otoki, Y.; Adesida, I. Recessed-gate enhancement-mode GaN HEMT with high threshold voltage. *Electron.* Lett. 2005, 41, 449–450. [CrossRef]
- Oka, T.; Nozawa, T. AlGaN/GaN Recessed MIS-Gate HFET With High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications. *IEEE Electron. Device Lett.* 2008, 29, 668–670. [CrossRef]
- Wang, H.-C.; Chiu, H.-C.; Huang, C.-R.; Kao, H.-L.; Chien, F.-T. High Threshold Voltage Normally off Ultra-Thin-Barrier GaN MISHEMT with MOCVD-Regrown Ohmics and Si-Rich LPCVD-SiNx Gate Insulator. *Energies* 2020, 13, 2479. [CrossRef]
- Cai, Y.; Zhou, Y.; Chen, K.; Lau, K. High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment. *IEEE Electron. Device Lett.* 2005, 26, 435–437. [CrossRef]
- Uemoto, Y.; Hikita, M.; Ueno, H.; Matsuo, H.; Ishida, H.; Yanagihara, M.; Ueda, T.; Tanaka, T.; Ueda, D. Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation. *IEEE Trans. Electron. Devices* 2007, 54, 3393–3399. [CrossRef]
- Kaneko, S.; Kuroda, M.; Yanagihara, M.; Ikoshi, A.; Okita, H.; Morita, T.; Tanaka, K.; Hikita, M.; Uemoto, Y.; Takahashi, S.; et al. Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain. In Proceedings of the IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD), Hong Kong, China, 10–14 May 2015; pp. 41–44. [CrossRef]
- Marcon, D.; Saripalli, Y.N.; Decoutere, S. 200 mm GaN-on-Si epitaxy and e-mode device technology. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), IEDM Technical Digest, Washington, DC, USA, 7–9 December 2015; pp. 16.2.1–16.2.4. [CrossRef]
- Chen, K.J.; Häberlen, O.; Lidow, A.; Tsai, C.L.; Ueda, T.; Uemoto, Y.; Wu, Y. GaN-on-Si power technology: Devices and applications. IEEE Trans. Electron Devices 2017, 64, 779–795. [CrossRef]
- Hu, J.; Stoffels, S.; Zhao, M.; Tallarico, A.N.; Rossetto, I.; Meneghini, M.; Kang, X.; Bakeroot, B.; Marcon, D.; Kaczer, B.; et al. Time-Dependent Breakdown Mechanisms and Reliability Improvement in Edge Terminated AlGaN/GaN Schottky Diodes Under HTRB Tests. *IEEE Electron. Device Lett.* 2017, *38*, 371–374. [CrossRef]
- Azam, F.; Lee, B.; Misra, V. Optimization of ALD high-k gate dielectric to improve AlGaN/GaN MOS-HFET DC characteristics and reliability. In Proceedings of the IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 30 October–1 November 2017; pp. 39–43. [CrossRef]
- 11. Dalcanale, S. GaN-based MIS-HEMTs: Impact of cascodemode high temperature source current stress on NBTI shift. In Proceedings of the 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2–6 April 2017.
- 12. Lidow, A. Enhancement mode gallium nitride transistor reliability. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS 2015), Monterey, CA, USA, 19–23 April 2015.
- 13. Lidow, A.; Strydom, J.; Strittmatter, R.; Zhou, C. GaN: A Reliable future in power conversion: Dramatic performance improvements at a lower cost. In *IEEE Power Electronics Magazine*; IEEE: Piscataway, NJ, USA, 2015; Volume 2, pp. 20–26. [CrossRef]
- 14. Wong, K.-Y.; Lin, Y.S.; Hsiung, C.W.; Lansbergen, G.P.; Lin, M.C.; Yao, F.W.; Yu, C.J.; Chen, P.C.; Su, R.Y.; Yu, J.L.; et al. AlGaN/GaN MIS-HFET with improvement in high temperature gate bias stress-induced reliability. In Proceedings of the IEEE

26th International Symposium on Power Semiconductor Devices IC's (ISPSD), Waikoloa, HI, USA, 15–19 June 2014; pp. 55–58. [CrossRef]

- Bahl, S.R.; Joh, J.; Fu, L.; Sasikumar, A.; Chatterjee, T.; Pendharkar, S. Application reliability validation of GaN power devices. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), IEDM Technical Digest, San Francisco, CA, USA, 3–7 December 2016. [CrossRef]
- Fernández, M. P-GaN HEMTs drain and gate current analysis under short-circuit. *IEEE Electron. Device Lett.* 2017, 38, 505–508. [CrossRef]
- 17. Fernández, M. Short-circuit study in medium-voltage GaN cascodes, p-GaN HEMTs, and GaN MISHEMTs. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9012–9022. [CrossRef]
- Fernandez, M.; Perpina, X.; Vellvehi, M.; Jorda, X.; Roig, J.; Bauwens, F.; Tack, M. Short-circuit capability in p-GaN HEMTs and GaN MISHEMTs. In Proceedings of the 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Sapporo, Japan, 28 May–1 June 2017.
- Hua, M. Gate reliability and VTH stability investigations of p-GaN HEMTs. In Proceedings of the IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT), Kunming, China, 3–6 November 2020.
- He, J.; Wei, J.; Yang, S.; Hua, M.; Zhong, K.; Chen, J.K. Temperature-dependent gate degradation of p-GaN gate HEMTs under static and dynamic positive gate stress. In Proceedings of the 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019.
- Tang, X.; Li, B.; Moghadam, H.A.; Tanner, P.; Han, J.; Dimitrijev, S. Mechanism of Threshold Voltage Shift in p-GaN Gate AlGaN/GaN Transistors. *IEEE Electron. Device Lett.* 2018, 39, 1145–1148. [CrossRef]
- 22. He, J. Frequencyand temperature-dependent gate reliability of Schottky-type p-GaN gate HEMTs. *IEEE Trans. Electron Devices* **2019**, *66*, 3453–3458. [CrossRef]
- 23. Wang, H.; Wei, J.; Xie, R.; Liu, C.; Tang, G.; Chen, K.J. Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON characterization and circuit design considerations. *IEEE Trans. Power Electron.* **2017**, *32*, 5539–5549. [CrossRef]
- Wei, J.; Xie, R.; Xu, H.; Wang, H.; Wang, Y.; Hua, M.; Zhong, K.; Tang, G.; He, J.; Zhang, M.; et al. Charge Storage Mechanism of Drain Induced Dynamic Threshold Voltage Shift in p-GaN Gate HEMTs. *IEEE Electron. Device Lett.* 2019, 40, 526–529. [CrossRef]
- 25. Hu, Q. Reducing dynamic on-resistance of p-GaN gate HEMTs using dual field plate configurations. In Proceedings of the IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 20–23 July 2020.
- Meneghini, M.; Rossetto, I.; Borga, M.; Canato, E.; de Santi, C.; Rampazzo, F.; Meneghesso, G.; Zanoni, E.; Stoffels, S.; van Hove, M.; et al. Degradation of GaN-HEMTs with p-GaN gate: Dependence on temperature and on geometry. In Proceedings of the 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2–6 April 2017; pp. 4B-5.1–4B-5.5.
- Li, S.; He, Z.; Gao, R.; Chen, Y.; Chen, Y.; Liu, C.; Huang, Y.; Li, G. Time-Dependent Threshold Voltage Instability Mechanisms of p-GaN Gate AlGaN/GaN HEMTs Under High Reverse Bias Conditions. *IEEE Trans. Electron. Devices* 2021, 68, 443–446. [CrossRef]
- 28. Hwang, I.; Kim, J.; Chong, S.; Choi, H.-S.; Hwang, S.-K.; Oh, J.; Shin, J.K.; Chung, U.-I. Impact of Channel Hot Electrons on Current Collapse in AlGaN/GaN HEMTs. *IEEE Electron. Device Lett.* **2013**, *34*, 1494–1496. [CrossRef]
- 29. Uren, M.J.; Karboyan, S.; Chatterjee, I.; Pooth, A.; Moens, P.; Banerjee, A.; Kuball, M. "Leaky Dielectric" Model for the Suppression of Dynamic RON in Carbon-Doped AlGaN/GaN HEMTs. *IEEE Trans. Electron. Devices* **2017**, *64*, 2826–2834. [CrossRef]
- 30. Cornigli, D.; Reggiani, S.; Gnani, E.; Gnudi, A.; Baccarani, G.; Moens, P.; Vanmeerbeek, P.; Banerjee, A.; Meneghesso, G. Numerical investigation of the lateral and vertical leakage currents and breakdown regimes in GaN-on-Silicon vertical structures. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015.
- 31. Zhou, C.; Jiang, Q.; Huang, S.; Chen, K.J. Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices. *IEEE Electron*. *Device Lett.* **2012**, *33*, 1132–1134. [CrossRef]
- 32. Wang, W.; Liang, Y.; Zhang, M.; Lin, F.; Wen, F.; Wang, H. Mechanism Analysis of Dynamic On-State Resistance Degradation for a Commercial GaN HEMT Using Double Pulse Test. *Electronics* **2021**, *10*, 1202. [CrossRef]
- Xu, H.; Wei, J.; Xie, R.; Zheng, Z.; He, J.; Chen, K.J. Incorporating the Dynamic Threshold Voltage into the SPICE Model of Schottky-Type p-GaN Gate Power HEMTs. *IEEE Trans. Power Electron.* 2021, 36, 5904–5914. [CrossRef]
- Chihani, O.; Theolier, L.; Deletage, J.-Y.; Woirgard, E.; Bensoussan, A.; Durier, A. Temperature and voltage effects on HTRB and HTGB stresses for AlGaN/GaN HEMTs. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; IEEE: Piscataway, NJ, USA, 2018. ISBN 978-1-5386-5479-8.
- 35. Vetury, R.; Zhang, N.Q.; Keller, S.; Mishra, U.K. The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs. *IEEE Trans. Electron. Devices* 2001, *48*, 560–566. [CrossRef]
- 36. Meneghini, M.; Rossetto, I.; Rizzato, V.; Stoffels, S.; van Hove, M.; Posthuma, N.; Wu, T.-L.; Marcon, D.; Decoutere, S.; Meneghesso, G.; et al. Gate Stability of GaN-Based HEMTs with P-Type Gate. *Electronics* **2016**, *5*, 14. [CrossRef]