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On-Chip Temperature Compensation for Small-Signal Gain Variation Reduction

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Abstract: Power amplifier (PA) specifications are closely related to changes in temperature; thus, the small-signal gain (S21) of PA decreases with the temperature increase. To compensate for the degradation caused by the decrease in S21, we present a compensation circuit that consists of two diodes and four resistors. At the same time, a differential stacked millimeter-wave wideband PA was designed and implemented based on this compensation circuit and 55 nm CMOS process. The post-layout simulation results showed that the fluctuation of S21 reduced from 2.4 dB to 0.1 dB in the frequency range of 25−40 GHz over the temperature range of −40 °C to 125 °C. Furthermore, the proposed on-chip temperature compensation circuit also applies to multi-stage cascaded microwave/mm-wave power amplifiers.

Keywords: millimeter-wave; CMOS; power amplifier; specification degradation; temperature compensation

1. Introduction

In today's highly developed communication industry, the spectrum resources for the low-frequency band are becoming increasingly scarce, which seriously restricts the development of the wireless communication industry. The millimeter-wave band has received much attention because of the abundant and unexplored spectrum resources. A PA is a key module of a millimeter-wave wireless communication system [1–3], and its performance directly determines the quality of a wireless communication system. Millimeter-wave communication systems, for example, wireless communication [4–7], radars [8–10], satellites [11,12], and navigation [13], usually operate in outdoor or extremely harsh places with significant temperature variations, and the specifications of PAs are closely related to the temperature variation. Temperature variation leads to the specification degradation of PAs [14–16], which makes the millimeter-wave wireless communication system unable to meet the normal operation requirements or even fail [17–20]. Therefore, reducing the effect of temperature change on the PA's specification degradation under the dynamic, temperature-changing operating environment has become an urgent problem.

To address the above issues, a lot of fruitful work has been carried out by domestic and international researchers. For example, in 2017, Javed S. Gaggatur et al. from the Indian Institute of Science and Technology proposed a technique for the performance compensation of integrated CMOS power amplifiers based on non-invasive temperature sensing, which is expected to compensate for degradation due to self-heating [21]. A new method for the temperature compensation of on-chip differential logarithmic amplifiers was proposed by Y. Wenger of the Technical University of Braunschweig, Germany, and A. Ghazinour of NXP Semiconductors in 2018 [22]. The results showed that better compensation is achieved in the temperature range of −40 °C to 125 °C. In 2018, Zhiming Chen et al. of the Beijing Institute of Technology proposed a new temperature compensation method for K-band

CMOS amplifiers [23], which achieves better compensation for PA gain in the temperature range of −45 °C to +125 °C. In 2020, Fariborz Lohrabi Pour et al. from Virginia Tech proposed a temperature-compensated power amplifier [24] that can operate reliably over a temperature range of −40 °C to +225 °C.

In summary, various temperature compensation techniques and methods have been successfully applied in the research and design of various single-stage and multi-stage power amplifiers. Still, little research has been reported on the temperature compensation of power amplifiers with stacked structures. However, the stacked structure is widely used to implement various high-output power PAs, because it increases the amplifier's output power [25].

Therefore, this paper presents a temperature compensation circuit for a stacked power amplifier consisting of only two diodes and four resistors. The proposed compensation circuit keeps the gain constant with the temperature by controlling the gate voltage. In addition, the compensation circuit uses the principle that the diode's threshold voltage decreases with the temperature increase. This study first investigated the temperature compensation circuit's operating principle and design method. Then, based on the proposed on-chip temperature compensation circuit and 55 nm CMOS technology, a differential stacked millimeter-wave wideband PA was implemented. As a result, the power amplifier's small-signal gain fluctuated from 2.4 dB to 0.1 dB in the temperature range of −40 °C to +125 °C, and the frequency range was 25−40 GHz.

2. Temperature Characteristics of Single-Stage Amplifier Gain

The gain of a single-stage PA decreases with increasing temperature [26], while the gain of a class AB PA increases with increasing gate voltage [27]. Therefore, the gain of the amplifier can be compensated by controlling the transistor gate voltage. The temperature characteristics of the gain of a single-stage PA are shown in Figure 1. When the gate voltage changes between 0.51 V and 0.61 V, the gain of the single-stage power amplifier remains unchanged in the range of −40 °C to +125 °C.
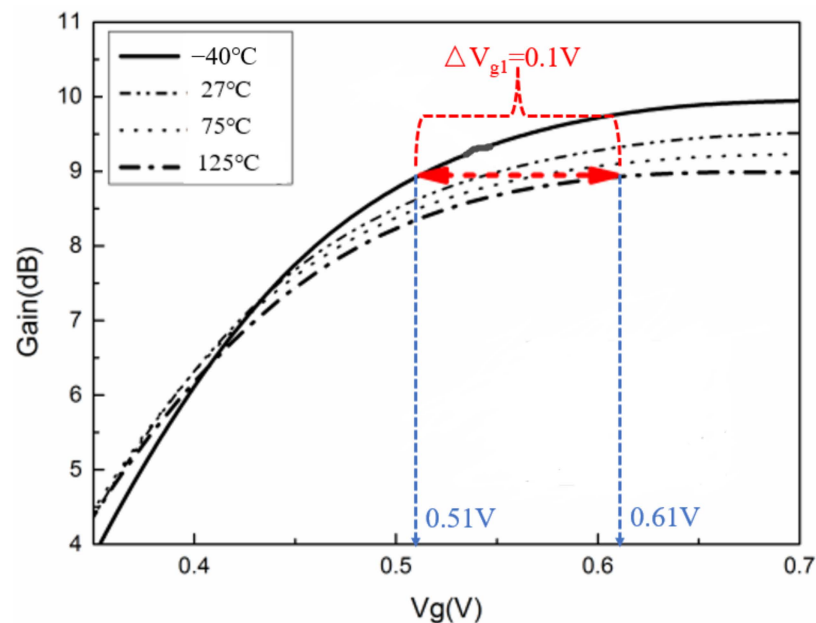

Figure 1. Temperature characteristics of gain of single-stage PA.

The transconductance in the saturated regions [28–30]:

$$g_{ms} = \frac{\partial I_D(sat)}{\partial V_{GS}} = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-3/2}\frac{WC_{ox}}{L}(V_{GS} - V_T),\tag{1}$$

where W is the gate width, μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, L is the gate length, V_{GS} is the gate voltage, V_T is the threshold voltage, V_{DS} is the drain voltage, and $T_0 = 300$ K.

Typically, the saturation voltage (V_{GS}-V_T) is chosen to be relatively large in order to obtain a large transconductance, so that the effect of the threshold voltage can be neglected. Moreover, its influence tends to dominate due to the exponential nature of carrier mobility [30]. Therefore, the transconductance usually decreases with increasing temperature, and the transconductance is usually considered as the gain of the transistor [29]. Consequently, the small-signal gain of the PA decreases with increasing temperature.

3. Principle and Design of Temperature Compensation Circuit

As described in Section 1, increasing the gate voltage can compensate for the change in amplifier gain. This temperature compensation circuit consists of two diodes and four resistors, as shown in Figure 2. The values of gate voltages V_{g1}, V_{g2}, and V_{g3} are determined by the V_r and V_{gc}. In Figure 2, D_1 and D_2 are diodes, R, R_1, R_2, and R_3 are resistors, and V_d and I are the current and voltage through the diodes, respectively. The compensation circuit shown in Figure 2 utilizes the mechanism whereby the threshold voltage of the diode decreases with increasing temperature.
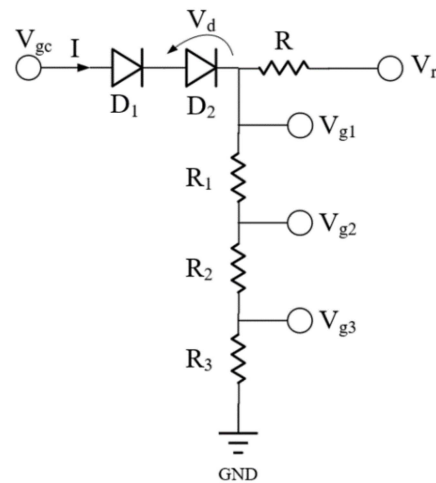

Figure 2. Schematic diagram of the compensation circuit.

To facilitate the presentation of the operating principle of the temperature compensation circuit, it is assumed that $V_{gc} = 0$. The following equation can be derived from Figure 2 [31].

$$-V_r = RI + 2V_d, \tag{2}$$

$$I = I_s \left\{ \exp(\frac{qV_d}{nkT}) - 1 \right\}, \tag{3}$$

where T is the temperature, and n is the ideal coefficient of the diode. I_s can be expressed as

$$I_s = SA^* T^2 \exp(-\frac{q\phi_B}{kT}), \tag{4}$$

where A^* is the temperature-independent Richardson–Dushman constant, φ_B is the material-dependent Schottky barrier voltage, and S is the junction size of the diode. From (2), (3), and (4), it follows that V_{g1} is a function of T:

$$V_{g1} = 2 \left\{ \frac{kT}{q} \ln(\mathrm{SRA}^*) + \frac{2kT}{q} \ln(T) - \phi_B \right\} n, \tag{5}$$

where $V_{g1} = -2V_d$ (as shown in Figure 2).

Assume that $RI_s \ll -(V_r + 2V_d) \ll (1/RI_s)$. Then, from (4), the following equation can be derived.

$$\frac{\partial V_{g1}}{\partial T} = 2\frac{nk}{q}\{\ln(\text{SRA}^*) + 2\ln(T) + 2\}, \tag{6}$$

If T is greater than $-270\ ^\circ\text{C}$, we have $\partial V_{g1}/\partial T > 0$. V_{g1} increases with increasing temperature for T greater than $-270\ ^\circ\text{C}$. The following equation can calculate the variation of V_{g1} (ΔV_{g1}) between two temperatures, T_H and T_L.

$$\begin{aligned} \Delta V_{g1} &= \int_{T_L}^{T_H} \frac{\partial V_{g1}}{\partial T}dT = \int_{T_L}^{T_H} 2\frac{nk}{q}\{\ln(\text{SRA}^*) + 2\ln(T) + 2\}dT \\ &= \frac{2nk}{q}(T_H - T_L)\ln(\text{SRA}^*) + \frac{4nk}{q}(T_H ln(T_H) - T_L ln(T_L)) \end{aligned} \tag{7}$$

Therefore, the expressions for V_{g2} and V_{g3} can be obtained according to Figure 2 and Equation (5).

$$V_{g2} = V_{g1}\frac{R_2 + R_3}{R_1 + R_2 + R_3}, \tag{8}$$

$$V_{g3} = V_{g1}\frac{R_3}{R_1 + R_2 + R_3}, \tag{9}$$

According to (8) and (9), V_{g2} and V_{g3} are proportional to V_{g1}, increasing with temperature. Therefore, V_{g2} and V_{g3} also increase with temperature in order to realize gain compensation. The following explains the compensation circuit's principle to compensate for the PA's small-signal gain.

When the temperature increases, gate voltage V_{g1}, gate voltage V_{g2}, and gate voltage V_{g3} in the temperature compensation circuit all increase as the temperature increases. The increase in gate voltage V_{g1}, gate voltage V_{g2}, and gate voltage V_{g3} is equivalent to the rise in the magnitude of V_{GS} of Equation (1). When V_{g1}, V_{g2}, and V_{g3} increase with temperature, the transconductance of each layer of the stacked PA can be expressed as

$$g_1 = \frac{\partial I_D(\text{sat})}{\partial V_{GS}} = \mu_n(T_0)(\frac{T}{T_0})^{-3/2}\frac{WC_{ox}}{L}(V_{g1} + \Delta V_{g1} - V_T), \tag{10}$$

$$g_2 = \frac{\partial I_D(\text{sat})}{\partial V_{GS}} = \mu_n(T_0)(\frac{T}{T_0})^{-3/2}\frac{WC_{ox}}{L}(V_{g2} + \Delta V_{g2} - V_T), \tag{11}$$

$$g_3 = \frac{\partial I_D(\text{sat})}{\partial V_{GS}} = \mu_n(T_0)(\frac{T}{T_0})^{-3/2}\frac{WC_{ox}}{L}(V_{g3} + \Delta V_{g3} - V_T), \tag{12}$$

According to Equations (10)–(12), the transconductance (i.e., gain) of each layer increases with ΔV_{g1}, ΔV_{g2}, and ΔV_{g3}, i.e., with the increase in temperature. Thus, the compensation for the degradation of the gain of each layer with the increase in temperature is achieved.

It should be noted that the on-chip temperature compensation circuit described in this section does not have any additional requirements or constraints on the design of the PA. In addition, the compensation circuit was designed for a single-stage PA. Specifically, for a multi-stage PA, the parameters of each transistor stage are different. Then, it is necessary to determine the value of ΔV_g, similar to the one shown in Figure 1, based on the parameters of each transistor stage. From Equation (7), it can be seen that the parameters affecting ΔV_{g1} are mainly the junction size (S) and resistance (R) of the diode. Therefore, for a multi-stage PA, the design of the corresponding temperature compensation circuit can be completed by simply adjusting the values of S and R so that the ΔV_{g1} (as shown in Equation (7)) of each stage meets the requirements similar to the ΔV_{g1} in Figure 1.

4. Differential Stacked Millimeter-Wave Broadband PA

To verify the effectiveness of the proposed on-chip temperature compensation circuit, a differential stacked millimeter-wave wideband PA was implemented in this study. Figure 3

shows the schematic of a differential stacked millimeter-wave wideband PA, which is used to compensate for the degradation of small-signal gain. As shown in Figure 1, the required ΔV_{g1} is 0.1 V. Two diodes are connected in series to achieve ΔV_{g1} = 0.1 V.
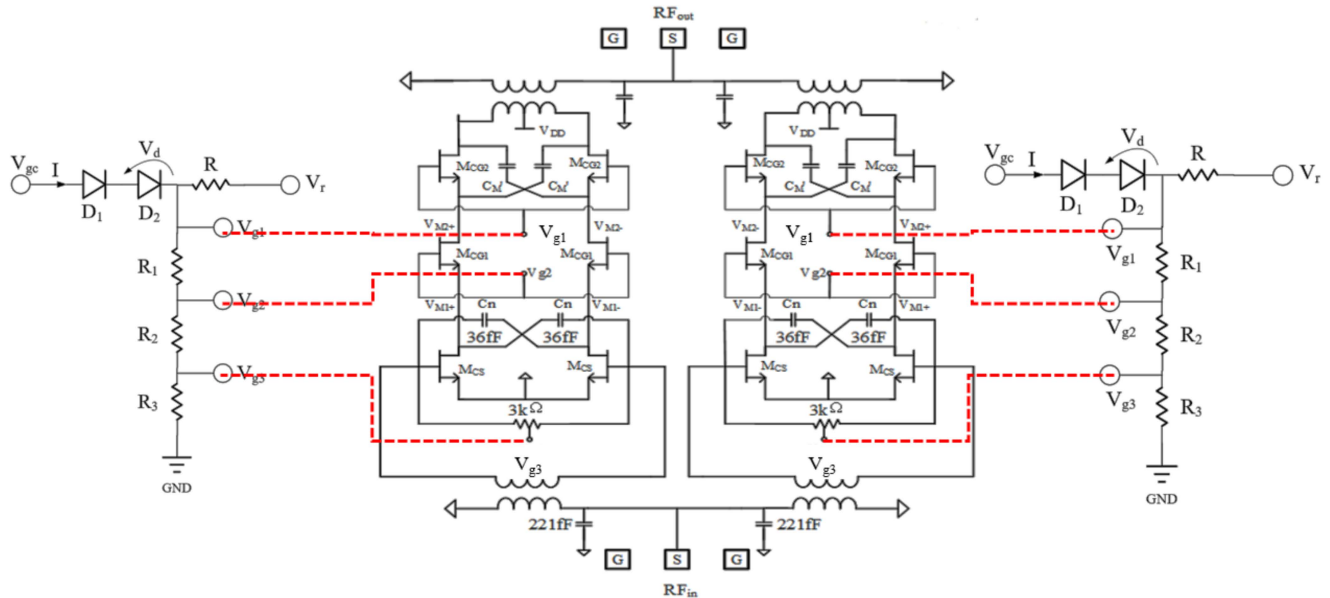

Figure 3. Schematic diagram of differential stacked PA, based on temperature compensation circuit.

Differential common-source structures [32,33] and stacked structures [34,35] are two circuit topologies commonly used in PA design. The differential common-source structure can suppress even harmonics. In contrast, the stacked structure can achieve a large output voltage swing (i.e., the transistors are connected in series to achieve a superposition of bias voltages and increase the output voltage swing of the PA) while ensuring that the transistors do not break down, thus increasing the output power of the PA. We designed and implemented a differential triple-stacked millimeter-wave broadband PA with on-chip temperature compensation based on the differential common-source structure and stacked structure.

The PA uses a two-way differential stacking structure to increase the output power and improve the stability of the PA by introducing a negative feedback network. To increase the bandwidth and reduce losses, on-chip transformers were used for the matching networks at the input/output of the PAs designed in this study. A thick metal layer was used in the design process for the on-chip transformer and interconnecting lines. As shown in Figure 3, the gate width/gate length of transistors M_{CG2}, M_{CG1}, and M_{CS} were 4×60 μm/60 nm, 4×60 μm/60 nm, and 3×60 μm/60 nm, respectively. Meanwhile, to improve power gain, isolation, and gain flatness, the neutralizing capacitor (C_n), shunt capacitor (C_{in}), and shunt resistor (R_g), respectively, were introduced in this study.

Although introducing a neutralization capacitor (C_n) can improve the stability of a PA to some extent, the PA will still be unstable when the parasitic capacitance (C_M) between the source and drain of transistor M_{CG2} is relatively large. This is also one of the main reasons for the instability of the stacked structure amplifier. Therefore, as shown in Figure 4, this study introduced another capacitor (C_M') in the negative feedback network of the top layer in order to improve stability. The capacitor (C_D) is the raw capacitance of the drain of transistor, M_{CG1}. The regulation of C_M' is used to achieve a balance between the three capacitors C_M', C_M, and C_D in order to achieve the stability of the PA.
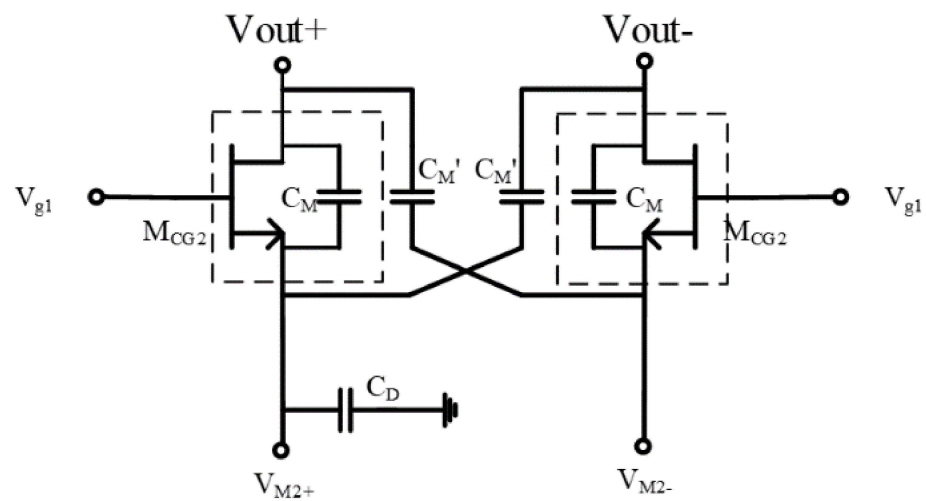
Figure 4. Schematic diagram of the negative feedback network.

The stability of the PA is shown in Figure 5. According to Figure 5, this PA's stability factor (K) in the range of 0–5 GHz was greater than 1 without introducing C_M', and the PA was in a stable state. The StabFact in the other frequency ranges was less than 1, and the PA was in an unstable condition. When C_M' was introduced into the PA, the stability factor of the PA in the whole frequency range was always greater than 1. As a result, the PA remained stable over the entire operating frequency range. This indicates that the introduction of capacitance (C_M') in the negative feedback network of the top layer of this stacked PA can effectively improve the stability of the PA.
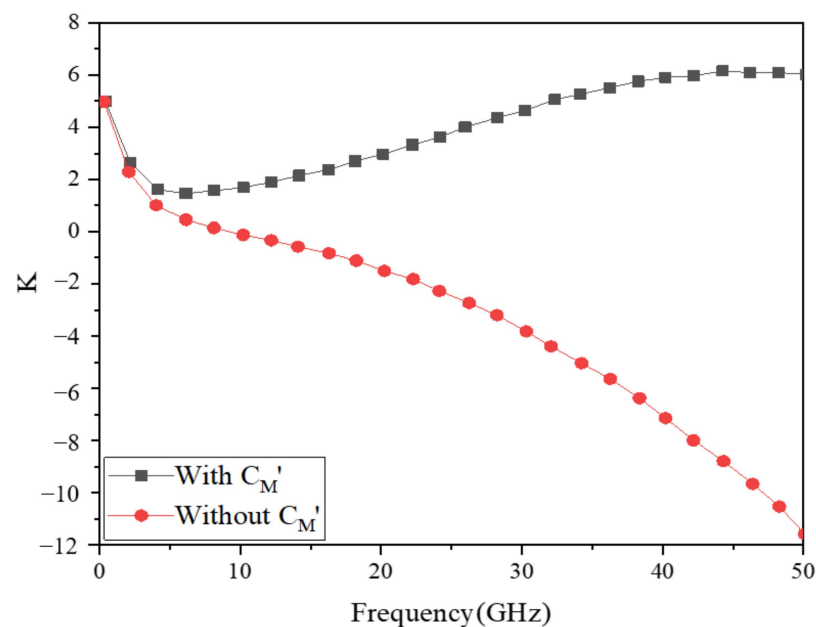

Figure 5. Stability factor of PA.

Figure 6 shows the core layout and overall layout of a differential stacked millimeter-wave wideband PA. The layout of the PA has a significant impact on the performance of the PA. Therefore, to simplify the RF signal path to reduce power consumption, we kept the layout of transistors M_{CG1} and M_{CG2} in the stacked structure, shown Figure 3, perpendicular to the direction of transistor M_{CS} when laying out the PA. The overall area of the PA chip was 0.378 mm^2.
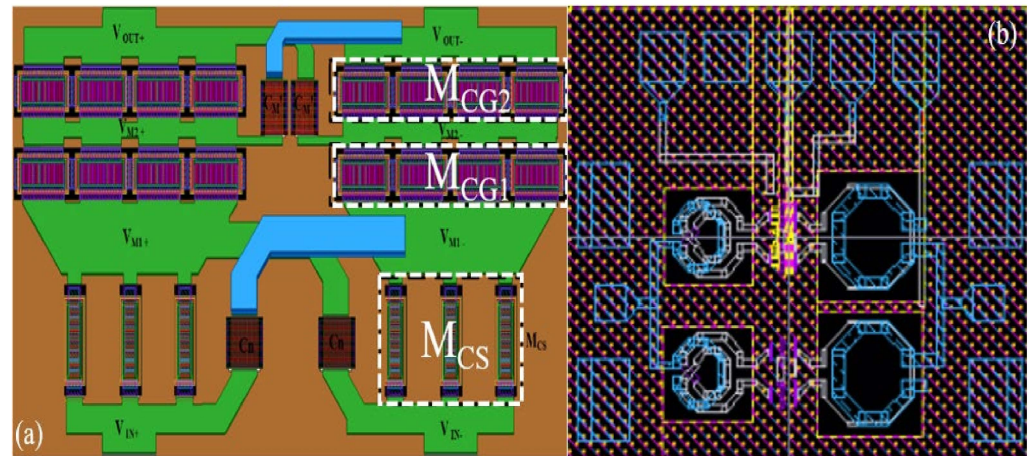
Figure 6. PA's overall layout and core layout: (**a**) core layout; (**b**) overall layout.

5. Results and Discussion

5.1. Small-Signal Gain at Different Temperatures

Figure 7 gives the small-signal gain versus temperature variation for the differential stacked millimeter-wave broadband power amplifier. Figure 7a,b show the results without and with temperature compensation circuits, respectively.
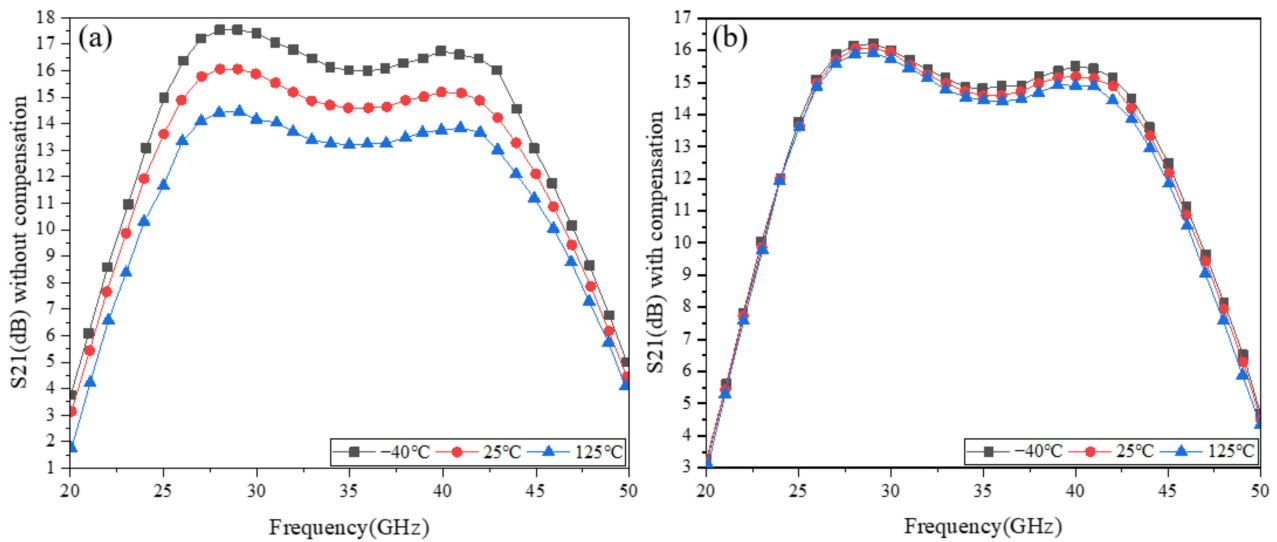

Figure 7. Small-signal gain versus temperature variation: (**a**) without temperature compensation; (**b**) with temperature compensation.

As seen in Figure 7, without the compensation, the small-signal gain varied by 2.4 dB in the frequency range of 25–40 GHz, while with the compensation, the small-signal gain varied by 0.1 dB in the frequency range of 25–40 GHz. The specific reasons are discussed below.

The small-signal gain is the transconductance [29], and the expression for the transconductance is

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{ds}}, \tag{13}$$

and the main factors affecting the transconductance are μ_n and I_{ds}, where the expression for the drain current in the saturation region is [36]

$$I_{ds} = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{gs} - V_{th})^2, \tag{14}$$

where V_{gs} is the gate voltage, and V_{th} is the threshold voltage.

When V_{gs} increases, Ids also increases with the rise of V_{gs}. It is also known from Equation (13) that the small-signal gain increases as I_{ds} increases. When the temperature rises, μ_n decreases with the increase in temperature, resulting in a reduction in small-signal gain. With the compensation, I_{ds} increases as the temperature rises to effectively compensate for the degradation of the small-signal gain due to μ_n. In other words, the gate voltage V_{g1}, gate voltage V_{g2}, and gate voltage V_{g3} increase with the temperature, which increases the I_{ds}, and thus, compensates for the small-signal gain. This indicates that the on-chip temperature compensation circuit has a good compensation effect on the small-signal gain.

5.2. Output Power and PAE at Different Temperatures

The output power (P_{out}) and large-signal gain at the center frequency of the PA versus temperature are shown in Figure 8. As shown in Figure 8a, the P_{out} and large-signal gain with an on-chip temperature compensation circuit varied very little. In contrast, the PA's output power and large-signal gain without a temperature compensation circuit were more significantly affected by temperature variations.

The power-added efficiency (PAE) at the center frequency of the PA versus temperature is shown in Figure 9. It is worth noting that the effect of temperature on the PA's power-added efficiency was relatively large, regardless of whether it was with compensation. This indicates that the compensation circuit has a better compensation effect on the P_{out} and large-signal gain, while the compensation effect on the PAE is insignificant. The specific reasons are discussed below.
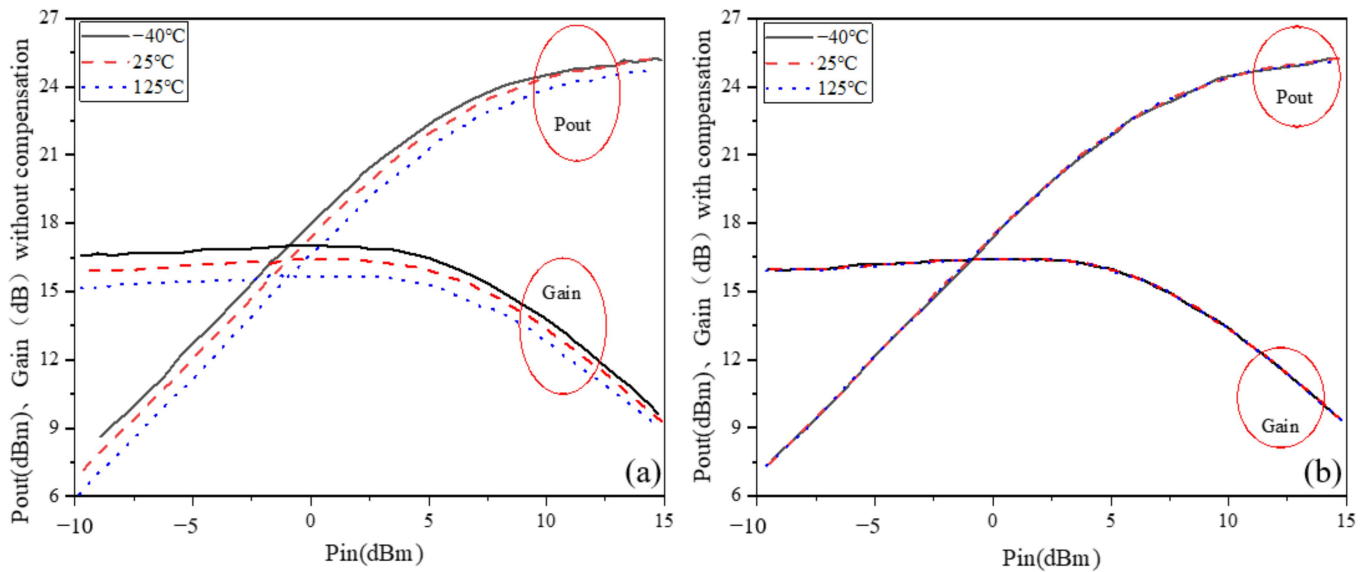

Figure 8. Output power versus temperature variation: (**a**) without temperature compensation; (**b**) with temperature compensation.

Literature studies have shown [37] that the on-state resistance between source and drain increases with temperature, which leads to a drop in the P_{out}. The expression for on-resistance is [37]

$$R_{on} = R_0 + kT^{\alpha} / |V_{gs} - V_{th}|^{\beta}, \tag{15}$$

where the constant k is a process parameter, R_0 is a constant independent of voltage and temperature, $\alpha \approx 1.5$, $\beta \approx 0.2$, V_{gs} is the gate voltage, and V_{th} is the threshold voltage.
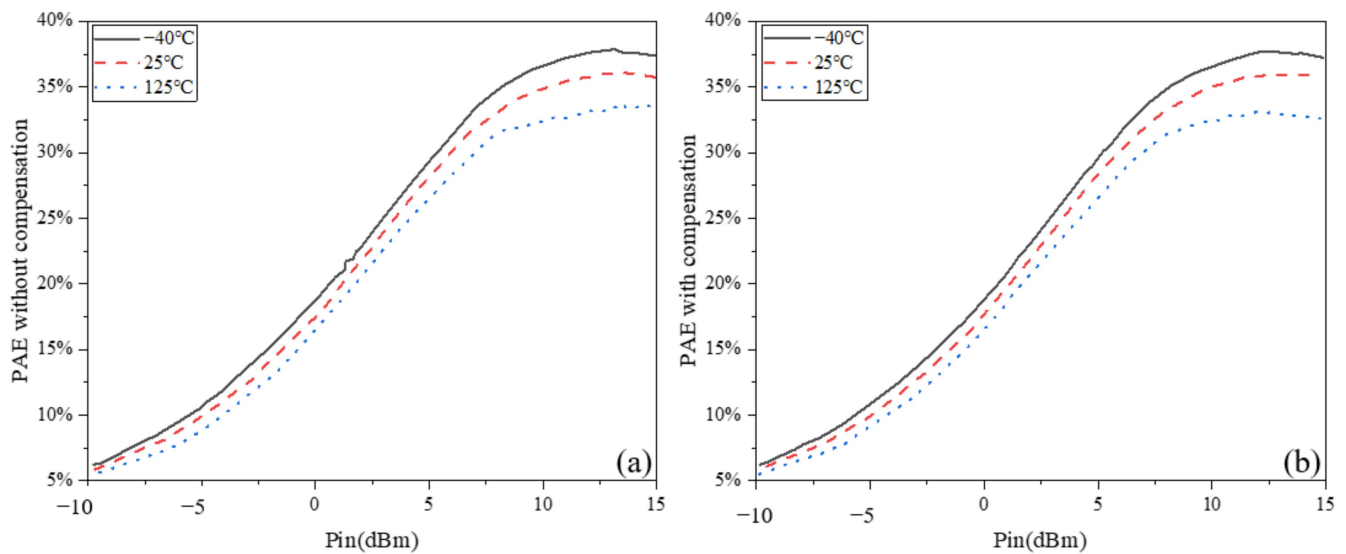
Figure 9. PAE versus temperature variation: (**a**) without temperature compensation; (**b**) with temperature compensation.

According to Equation (15), on-resistance increases with increasing temperature. Therefore, when the PA does not have a temperature compensation circuit, the P_{out} decreases with increasing temperature. On the other hand, when the PA is with compensation, the gate V_{gs} in Equation (15) increases with the temperature, causing the on-resistance to decrease with the gate voltage increase, thus achieving the compensation for the P_{out}. As a result, the compensation for the large-signal gain is also achieved. As for the PAE, the compensation circuit compensates for the P_{out} while increasing the DC power consumption of the PA [24]. Therefore, according to the definition of PAE, the PAE decreases with the increase in DC power consumption. Thus, with or without compensation, the effect of temperature change on PAE of PA is relatively significant [24].

Table 1 compares the amplifier's performance with on-chip temperature compensation circuits. Compared with the compensation circuit structures and methods in the literature [23,24,38–40], the temperature compensation circuit proposed in this paper has a simple structure, a smaller overall chip area, and a better compensation effect for small-signal gain and output power. Still, the compensation effect for PAE was poor. In addition, these post-layout simulation results can be regarded as a supplement to the measured results in Refs. [23,38–40]. This idea is consistent with Ref. [24], and these results are effective in the relative amount of change in small-signal gain, output power, and PAE before and after compensation.

Table 1. Performance comparison with previous works.

Reference	Ref. [23]	Ref. [38]	Ref. [39]	Ref. [40]	Ref. [24]	This Work [2]
Circuit	PA	LNA	LNA	PA	PA	PA
Technology	90 nm	130 nm SOI	130 nm	40 nm	GaN HEMT	55 nm
Topology	2-stage	1-stage	1-stage	3-stage	1-stage	1-stage
Frequency (GHz)	26.5	2.4	15.2	79	4.5–5.5	25–40
Small-signal gain variation (dB)	1.2 (−45~125 °C)	0.9 (25~200 °C)	3.1 (−20~120 °C)	0.6 (10~100 °C)	0.4 (−40~225 °C)	0.1 (−40~125 °C)
Pout variation (dBm) (center frequency)	N/A	N/A	N/A	N/A	24.0 (−40~225 °C)	0.6 (−40~125 °C)

Table 1. *Cont.*

Reference	Ref. [23]	Ref. [38]	Ref. [39]	Ref. [40]	Ref. [24]	This Work [2]
PAE variation (center frequency)	N/A	N/A	N/A	N/A	12% (−40~225 °C)	7.3% (−40~125 °C)
Area (mm^2)	0.5 [1]	0.6 [1]	0.6 [1]	0.11 [1]	6.6	0.378

Note: [1] DC pads are not included. [2] Post-layout simulation results.

Furthermore, in terms of the magnitude of small-signal gain variation with temperature, the compensation circuit can effectively compensate for the small-signal gain. This shows that the proposed compensation circuit for differential stacked millimeter-wave wideband PAs effectively compensates for the degradation of the small-signal gain of PAs due to temperature variations over a wide range.

6. Conclusions

This paper proposes a compensation circuit consisting of two diodes and four resistors for a PA with a stacked structure. To verify the effectiveness of the compensation circuit, we designed and implemented a differential triple-layer stacked structure millimeter-wave wideband PA.

With the temperature-compensation circuit, the small-signal gain variation improved from 2.4 to 0.1 dB in the temperature range between −40 °C and 125 °C. It was demonstrated that the proposed on-chip temperature compensation circuit effectively corrects the small-signal gain, large-signal gain, and P_{out} variations of a millimeter-wave PA with a multi-layer stacked structure over a wide temperature range. In addition, the proposed on-chip temperature compensation circuit also applies to multi-stage cascaded microwave/mm-wave power amplifiers.

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