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N-Type Nanosheet FETs without Ground Plane Region for Process Simplification

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Abstract: This paper proposes a simplified fabrication processing for nanosheet Field-Effect Transistors (FETs) part of beyond-3-nm node technology. Formation of the ground plane (GP) region can be replaced by an epitaxial grown doped ultra-thin (DUT) layer on the starting wafer prior to $Si_x/SiGe_{1-x}$ stack formation. The proposed process flow can be performed in-situ, and does not require changing chambers or a high temperature annealing process. In short, conventional processes such as ion implantation and subsequent thermal annealing, which have been utilized for the GP region, can be replaced without degrading device performance.

Keywords: band-to-band tunneling; epitaxial growth; ground plane region; gate-all-around field-effect-transistors (GAA FETs); nanosheet FETs (NS FETs); parasitic channel leakage; punch-through

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1. Introduction

To suppress short-channel effects (SCEs), which are an important concern with aggressive device scaling, semiconductor devices have evolved from 2-dimensional (2-D) structures to 3-dimensional (3-D) architectures. This has further benefits. For example, due to their superior gate controllability, FinFETs have lower subthreshold swing (*SS*) and off-state leakage (I_{OFF}) than planar devices [1–3]. However, as device scaling approaches extreme levels, it is becoming difficult to control SCEs using FinFETs. As a solution, nanosheet FETs (NS FETs), which have multiple channels with a gate-all-around (GAA) backbone structure, have been introduced as beyond-FinFETs [4–6]. However, even though NS FETs have shown better suppression of SCEs than FinFETs, as well as better output performance, there are still many difficulties related to mass production. Producers such as Samsung Electronics Inc. and TSMC Inc. are planning the mass production of NS FETs in 2022 and 2023, respectively. However, it is unknown whether the yield will be sufficient. The reason for this lies in difficulties in the fabrication processing of the NS FETs. For example, surface roughness scattering stemming from germanium diffusion among the nanosheets, striction stemming from adhesion between nanosheets [6], residue formation (e.g., TiN or Si_3N_4) due to uncontrollable wet etching, unwanted void formation during metal gate filling [7], etc., are very challenging problems in current fabrication processing.

In addition, with respect to source/drain (S/D) modules, the contact depth as well as inner spacer thickness needs to be optimized [8,9]. It should be noted in particular that, unlike bulk FinFETs, which have already been mass produced, NS FETs have a parasitic channel underneath the first floor nanosheet [10–13]. Hence, even though NS FETs have multiple channels that are completely surrounded by metal gates (i.e., GAA), increased I_{OFF} stemming from the parasitic channel is inevitable. V. Jegadheesan et al., have suggested that applying a ground plane (GP) region can effectively minimize the I_{OFF} in the parasitic channel [14]. However, as we have mentioned above, the fabrication process flow of NS FETs is very sensitive. For example, ion implantation and rapid thermal annealing (RTA) for GP region formation are associated with an unwanted non-uniform doping profile [15,16].

In this context, it would be better, in terms of device variability and yield, if the conventional processes could be replaced with an alternative process. However, recently, research papers covering the fabrication process of NS FETs have been modest in number.

In this letter, we propose a fabrication process flow for NS FETs. The proposed process flow does not require ion implantation or additional thermal treatment, which are conventionally performed to form the GP region. Alternatively, a doped ultra-thin (DUT) layer is epitaxially grown on the starting wafer in-situ before $Si_x/SiGe_{1-x}$ stack formation. This achieves process simplification, improved variability, and improved yield during the fabrication of NS FETs.

2. Materials and Method

The proposed fabrication process flow is summarized in Figure 1. In the conventional NS FETs fabrication process, ion implantation and thermal annealing are performed in dashed step two for GP region formation. However, the process can be replaced by Si epitaxial growth for DUT layer formation, as described in the bolded step two. The DUT layer is doped with a p–type dopant (i.e., boron) to minimize the parasitic channel and punch-through underneath the first floor nanosheet. The thickness of the DUT is similar to the thickness of silicon and Si_xGe_{1-x} layers, which are epitaxially grown as nanosheets and sacrificial layers, respectively. Hence, the formation of the DUT layer is not problematic under current processing technology. Above all, it should be noted that the processing from steps one to three in Figure 1 can be performed in-situ without changing chambers.

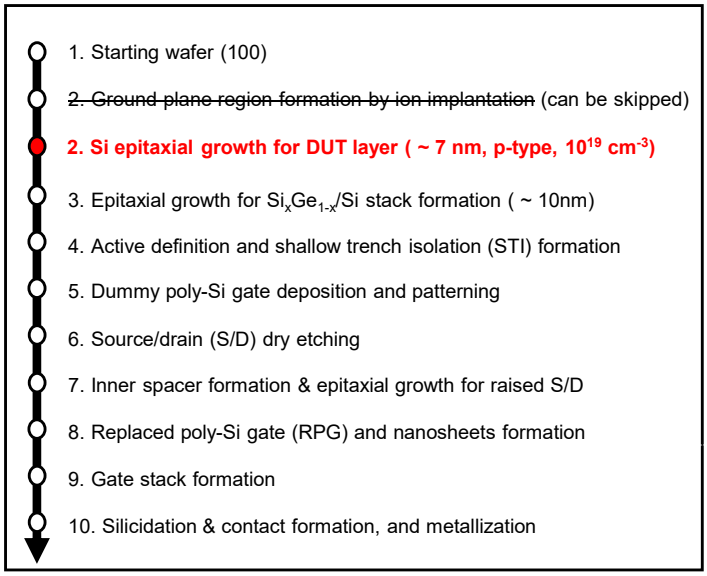


Figure 1. Fabrication process flow of proposed NS FETs including epitaxially grown DUT layer prior to formation of the Si_xGe_{1-x}/Si stack. The bolded step two can be alternatively added instead of the under-lined ion implantation and annealing process.

A 3-D simulator (Synopsys Sentaurus, Mountain View, CA, USA) was utilized to simulate fabrication processing and device characteristics. The drift-diffusion carrier transport equation was combined with the Poisson equation, and the density-gradient model was considered to reflect the quantum confinement effect of the nanosheet channels [17–20]. The Slotboom model was included for doping-dependent bandgap narrowing in the overall region [21]. Thin layer models such as inversion and accumulation layer mobility model (IALMob) were included to reflect impurity and phonon scattering [22]. In addition, the Shockley-Read-Hall (SRH) and non-local band-to-band tunneling (BTBT) recombination models were included to reflect gate-induced drain leakage (GIDL) during the simulations [22].

Figure 2 shows the backbone structure of the NS FETs used in the process simulation. Channel thickness (T_{CH}) and width (W_{NS}) were 5 nm and 45 nm, respectively. To elaborate, the dielectric constant of the HfO_2 gate dielectric and effective-oxide-thickness (EOT) were assumed to be 25 and 0.7 nm, respectively. In terms of doping concentration, epitaxially grown S/D regions were doped with arsenic at 3×10^{20} cm^{-3} [14,23]. The three nanosheet channels and silicon substrate (N_{Sub}) were lightly doped with boron at 1×10^{17} cm^{-3} and 1×10^{16} cm^{-3}, respectively. The doping concentration of the DUT layer was 1×10^{19} cm^{-3} of boron. The work-function of the titanium nitride for the metal gate was 4.5 eV. Detailed device parameters used for the simulations are summarized in Table 1.

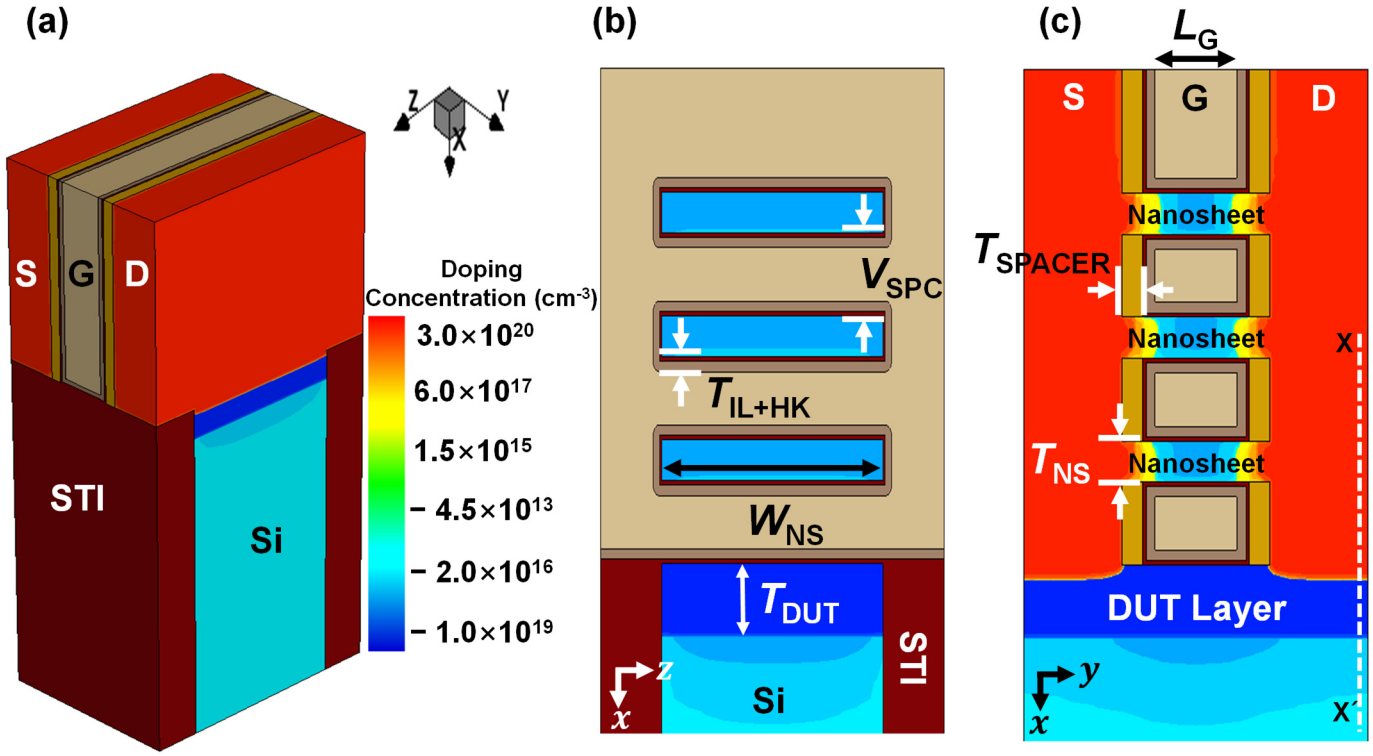


Figure 2. (**a**) Simulated NS FET device structure including the epitaxially–grown DUT layer on the starting wafer. Cross–sectional view of the proposed NS FET with a cut along the (**b**) gate and (**c**) channel directions, respectively.

Table 1. Dimensions and parameters used for the TCAD simulations.

Parameter	Value
Gate Length, L_G	12 nm
Nanosheet Width, W_{NS}	45 nm
Inner Spacer Thickness, T_{SPACER}	3 nm
Nanosheet-to-Nanosheet Vertical Space, V_{SPC}	10 nm
Nanosheet Thickness, T_{NS}	5 nm
Doped Ultra-Thin (DUT) Layer Thickness, T_{DUT}	5–100 nm
Doping Concentration of DUT Layer (N_{DUT})	10^{19} cm^{-3}
Inter Layer SiO_2 Thickness, T_{IL}	0.5 nm
High-*k* Gate Dielectric Thickness, T_{HK}	1.28 nm
Contacted Poly-Si Pitch (CPP)	44 nm

Then, the simulated I_D-V_G was carefully calibrated based on fabricated devices (i.e., such as doping concentration, structure, and gate work function) reported in [6], as shown in Figure 3a. Threshold voltage (V_{TH}) was extracted using a constant current method at I_D of 100 nA. Multiple V_{TH} characteristic can be visible when series resistance of NS FET is high due to defect existence or low doping concentration of S/D regions, as well as excessively long V_{SPC}. However, there was no observable multiple value of V_{TH} observed in the subthreshold region. Hence such concerns were not problematic, as shown in Figure 3b.

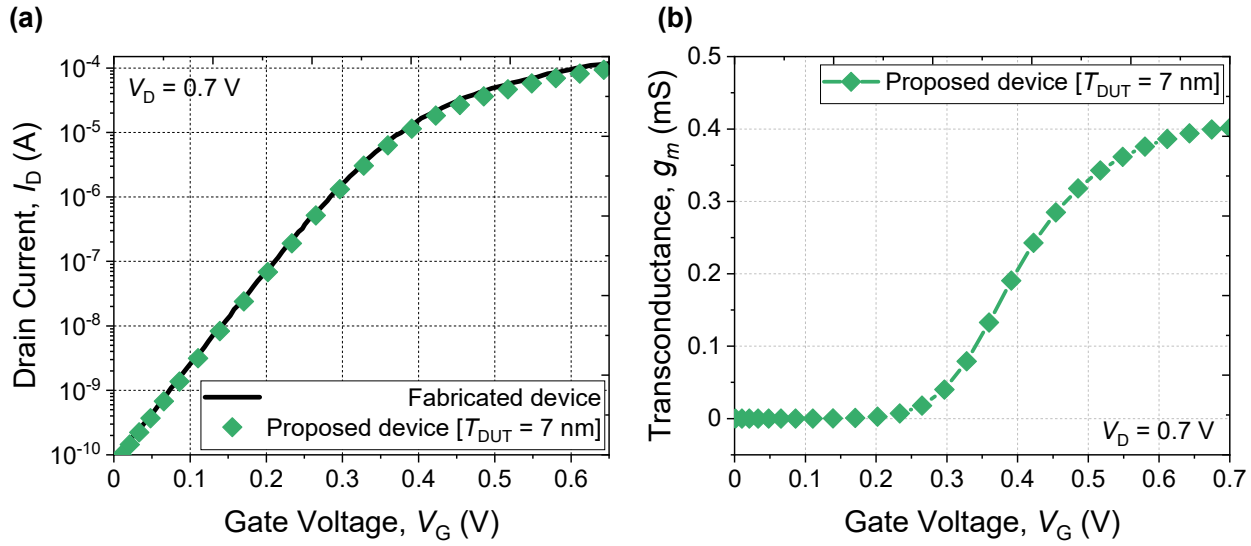


Figure 3. (**a**) Calibration of I_D-V_G curve with the fabricated device in Reference [6]. (**b**) Transconductance of (**a**).

3. Results and Discussion

Figure 4a shows the simulated doping profile during the off-state when the GP region as well as the DUT layer were not included. An unwanted parasitic channel and punch-through were formed underneath the first floor nanosheet. These concerns led to increased I_{OFF} during the off-state (Figure 4b).

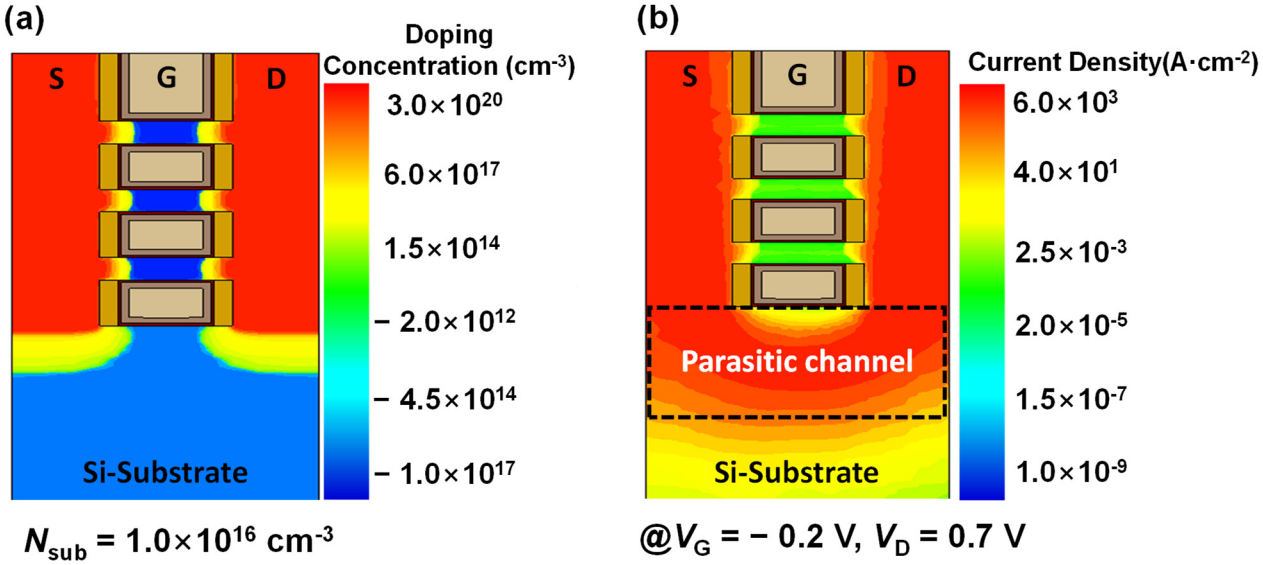


Figure 4. Simulated (**a**) doping profile distribution and (**b**) current density of a NS FET without a DUT layer during off–state.

Figure 5a shows the simulated transfer characteristics of the NS FETs with various thicknesses of DUT layers (T_{DUT}) from 0 nm to 7 nm. As the thickness of the DUT layer increases, I_{OFF}, as well as *SS*, improve. The I_{OFF} extracted at V_G = −0.2 V was 21.8 nA with a 0 nm DUT layer but improved to 0.98 pA with a 7 nm DUT layer. Figure 5b shows the current density profile of the NS FETs in Figure 5a extracted at the off-state with V_D = 0.7 V, V_G = −0.2 V. As the T_{DUT} increases, I_{OFF} flowing through the parasitic channel (Y–Y′ direction) can be suppressed, aided by the increased energy barrier height (Φ_{bi} of the parasitic channel), as shown in Figure 5c. In addition, punch-through can be suppressed by applying a DUT layer.

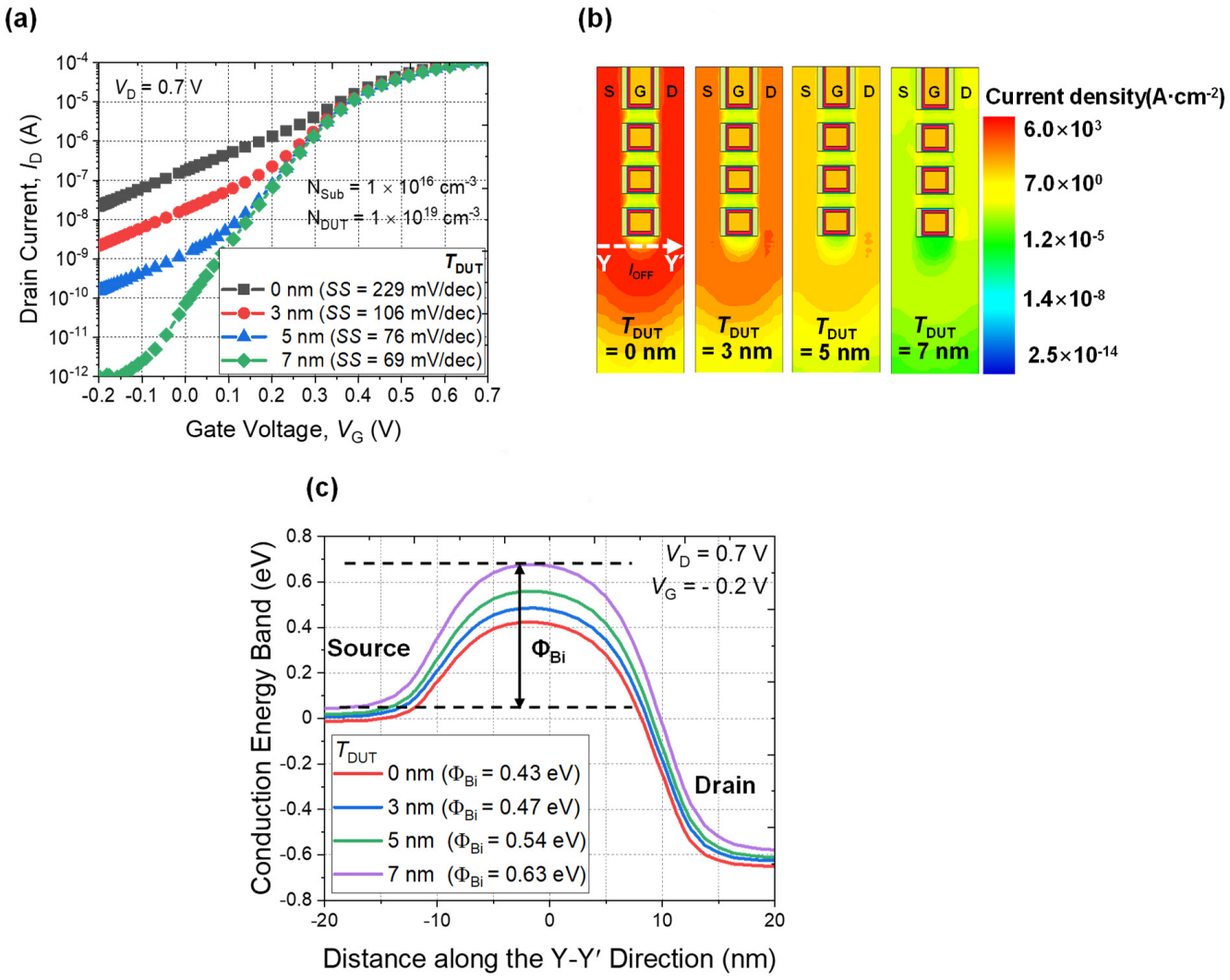


Figure 5. (**a**) Simulated I_D-V_G characteristic of NS FETs with various thicknesses of DUT layers without GP implantation and subsequent annealing. (**b**) Simulated parasitic current distribution profiles with various thicknesses of DUT layers. (**c**) Energy band diagram of parasitic channel along the Y–Y′ direction in (**b**). Conduction energy band height increases as T_{DUT} increases.

However, when T_{DUT} is thicker than 7 nm, the I_{OFF} increases (Figure 6a). Considering the I_{OFF} value in the range of V_G of –0.2 V to 0 V are identical to the drain–to–substrate leakage current, the source of the I_{OFF} increase is not the parasitic channel, but rather the BTBT between the drain and the DUT layer. In other words, when T_{DUT} is thicker than 7 nm, the DUT forms a p-n diode between the drain and the DUT layer, as shown in Figure 6b. During the off-state, the reverse biased p-n diode triggers BTBT of electrons, and increases the I_{OFF}. Figure 6c shows the simulated rate of electron generation between the

drain and the substrate by the BTBT. As the T_{DUT} increases, there is a noticeable increase in electron generation by the BTBT. As a result, it can be concluded that a 7 nm thickness DUT layer is optimal to avoid unwanted increasing I_{OFF}.

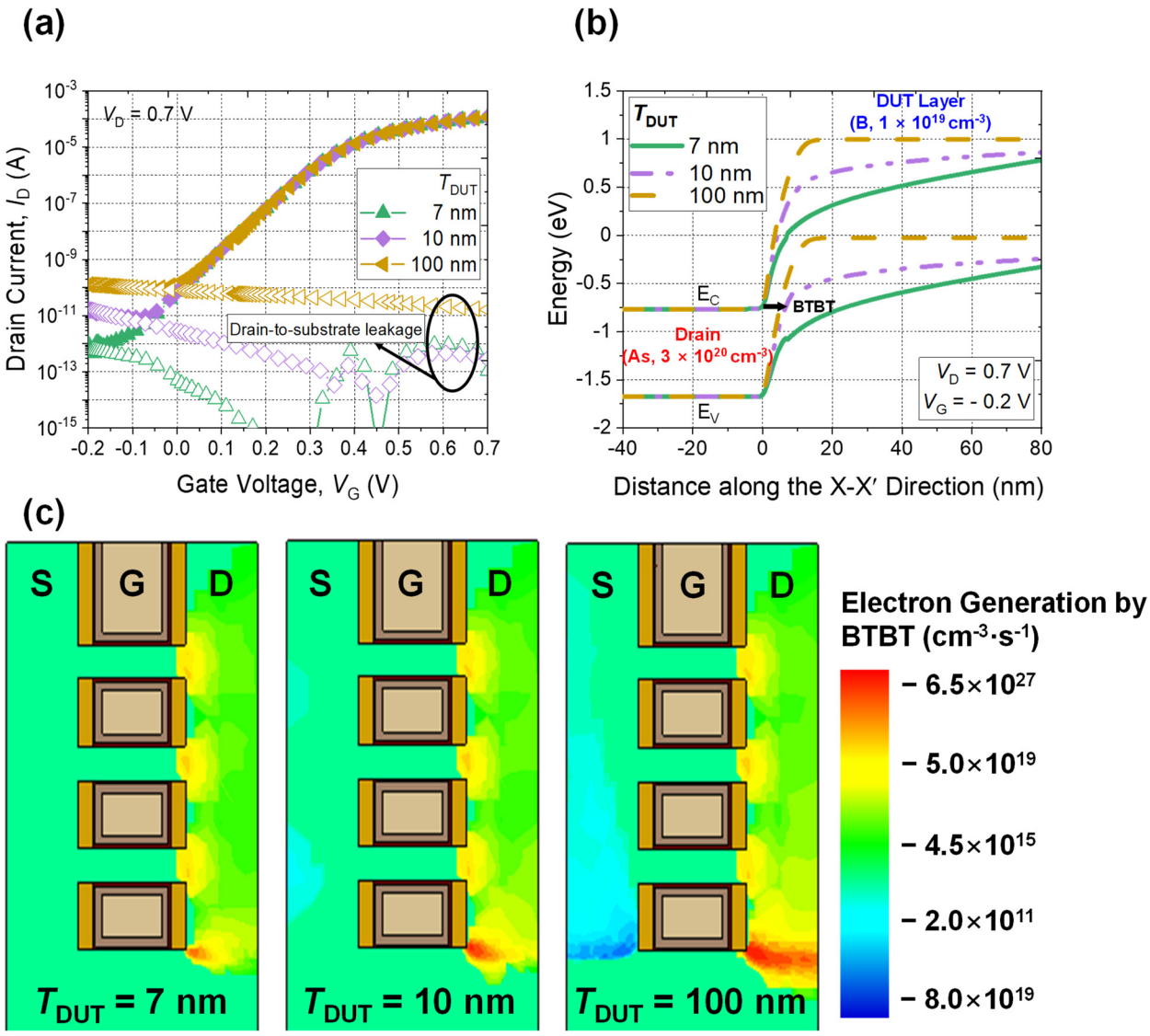


Figure 6. (**a**) Simulated I_D-V_G characteristic and (**b**) extracted energy band diagram of NS FETs (X–X′ direction in Figure 2c) with various thicknesses of DUT layers greater than 7 nm. (**c**) Electron generation rates with various T_{DUT}.

Figure 7a shows a simulated I_D-V_G curve for various doping concentrations (N_{DUT}) of the DUT layer. When the N_{DUT} is a low doping concentration of 1×10^{18} cm^{-3}, the I_{OFF} cannot be controlled due to increased *SS*. However, as the N_{DUT} increases, leakage current through the parasitic channel can be suppressed by the increased built-in potential (Φ_{bi}) from 0.39 eV to 0.59 eV, as shown in Figure 7b. In addition, suppression of punch-through is possible with increased substrate doping concentration.

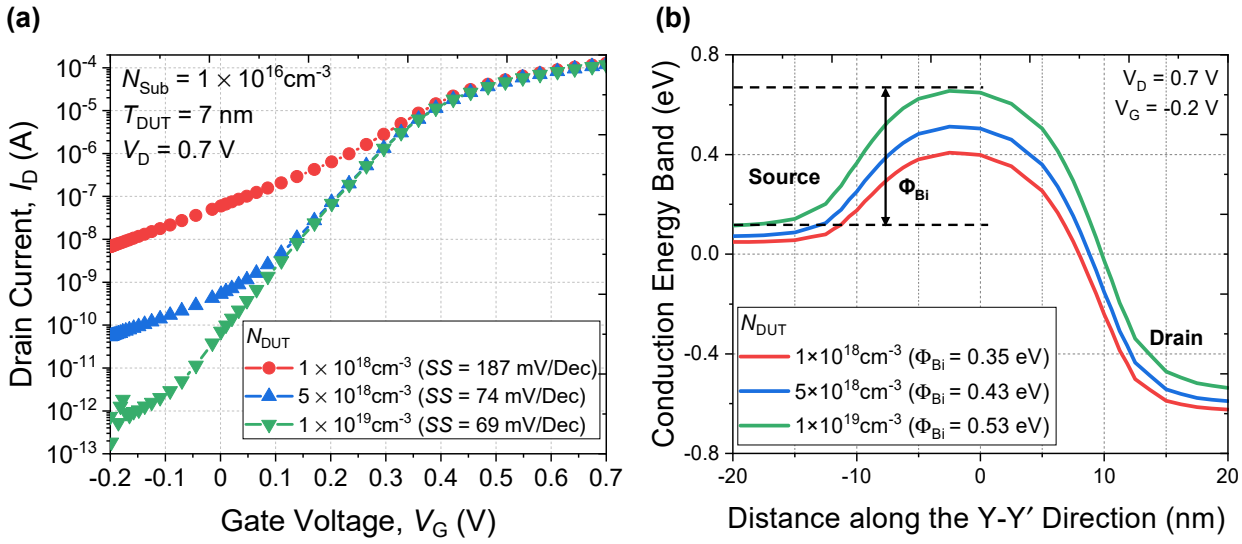


Figure 7. (**a**) I_D-V_G characteristic with different N_{DUT} layer. (**b**) Energy band diagram of the parasitic channel.

Figure 8 shows extracted I_D-V_G curve at V_D = 50 mV and 0.7 V, as well as I_D-V_D curve. The drain-induced barrier lowering (DIBL) of the proposed NS FET is 35 mV, which a low value compared with the value of 33 nm of the planar FET [19] or 15 nm of FinFET [24], as summarized in Table 2. In other words, the superior gate controllability of the NS FET does not degrade even when a DUT layer is applied.

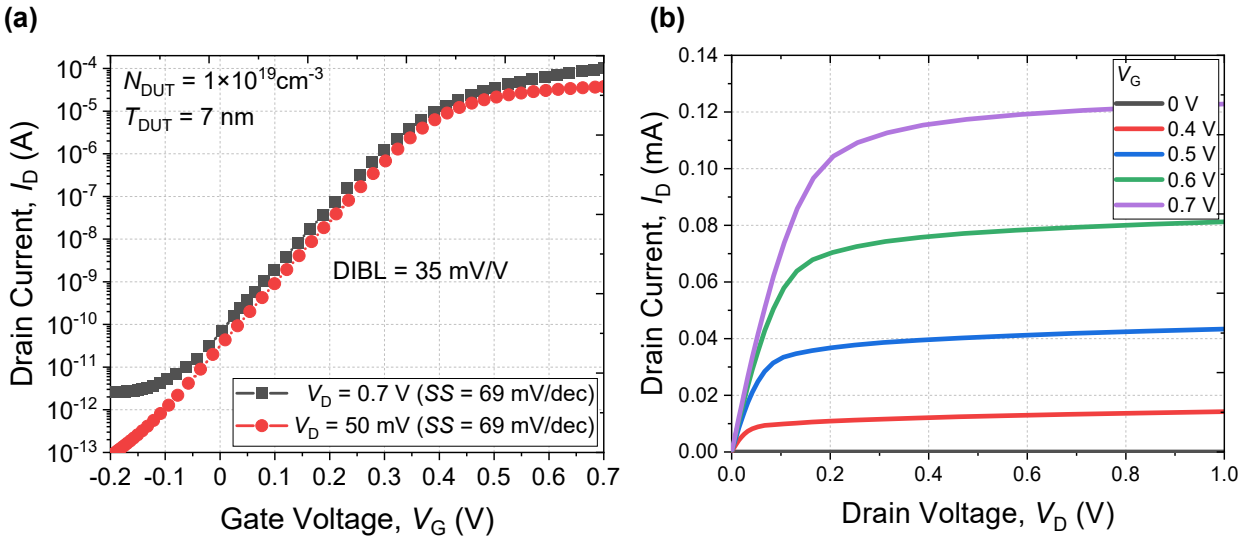


Figure 8. (**a**) Extracted I_D-V_G and (**b**) I_D–V_D characteristics of NS FET with DUT layer.

Table 2. Comparison of DIBL and *SS* characteristics with various devices.

	Planar FET [19]	**FinFET [24]**	**NS FET [This Work]**
DIBL (mV/V) (V_D = 50 mV and 0.7 V)	208	89	35
SS (mV/dec)	-	72	69

Figure 9 introduces various approaches to suppress the leakage current from the parasitic channel without the formation of a GP region [14,25]. A full bottom dielectric

(FBD) can eliminate the parasitic channel perfectly (Figure 9a). However, fabrication of the FBD inevitably requires a starting wafer composed of silicon-on-insulator (SOI) which is vulnerable to self-heating as well as expensive wafer cost. In this context, a steep-retrograde (SSR) region which contains a deep and heavily doped layer is preferred. However, forming an abrupt doping profile for the SSR is impossible using ion implantation and spike annealing. Even though epitaxial growth can be utilized, at least one more epitaxial growth step is required compared to the DUT case. Figure 9d shows the simulated electrical characteristics of the FBD, SSR, and DUT structures, respectively. Even though the DUT layer has a simpler fabrication process than the others, device characteristics in terms of V_{TH}, *SS*, and I_{ON} are not remarkable. Exact device parameters are summarized in Table 3.

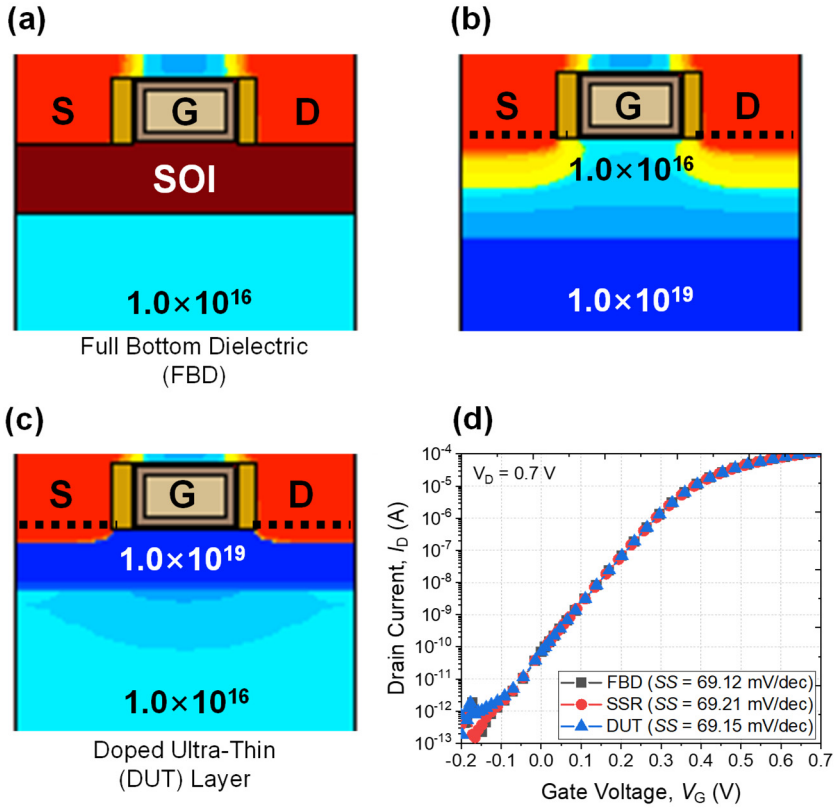


Figure 9. Various device structures without a GP region. NS FET with (**a**) full bottom dielectric (FBD) [25], (**b**) super steep-retrograde (SSR) region [14], and (**c**) the proposed DUT layer. (**d**) Simulated I_D-V_G characteristics of the respective device structures.

Table 3. Comparison of NS FETs based on FBD, SSR, and DUT structures.

	FBD	SSR	DUT
V_{TH} (0.7 V/50 mV) (mV)	212/229	212/233	216/239
SS (mV/dec)	69	69	69
I_{ON} (mA) at V_G = 0.7 V, V_D = 0.7 V	0.117	0.117	0.102
I_{OFF} (pA) at V_G = 0 V, V_D = 0.7 V	71.5	71.0	65.3
DIBL (mV/V) (V_D = 50 mV and 0.7 V)	32	32	35

4. Conclusions

For better process simplification, the fabrication process for nanosheet FETs was newly suggested based on 3-D simulation. The doped ultra-thin (DUT) layer can be epitaxially grown in-situ on the starting wafer. Conventional ground plane (GP) doping implantation as well as annealing process can be excluded while forming the DUT layer. The thickness of the DUT layer has been optimized to suppress parasitic channel leakage, punch-through, and band-to-band tunneling (BTBT). The NS FET with the DUT layer showed comparable performance, but has a simpler fabrication process compared with other NS FETs, including full bottom dielectric (FBD) or steep-retrograde region (SSR).

Author Contributions: For J.-Y.P. conceived this project and designed all of the experiments. K.-S.L. conducted all of the simulations and wrote this paper. All authors have read and agreed to the published version of the manuscript.

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