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Buffer Traps Effect on GaN-on-Si High-Electron-Mobility Transistor at Different Substrate Voltages

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Abstract: Substrate voltage (V_{SUB}) effects on GaN-on-Si high electron mobility transistors (HEMTs) power application performance with superlattice transition layer structure was investigated. The 2DEG conductivity and buffer stack charge redistribution can be affected by neutral/ionized donor and acceptor traps. As the donor/acceptor traps are excessively ionized or de-ionized by applying V_{SUB}, the depletion region between the unintentionally doped (UID)/Carbon-doped (C-doped) GaN layer may exhibit a behavior similar to the p–n junction. An applied negative V_{SUB} increases the concentration of both the ionized donor and acceptor traps, which increases the breakdown voltage (BV) by alleviating the non-uniform distribution of the vertical electric field. On the other hand, an applied positive V_{SUB} causes the energy band bending flattener to refill the ionized traps and slightly improves the dynamic R_{on} degradation. Moreover, the amount of electrons injected into the buffer stack layer from the front side (2DEG channel/Ohmic contact) and the back side (AlN nucleation layer/superlattice transition layer) are asymmetric. Therefore, different V_{SUB} can affect the conductivity of 2DEG through the field effect, buffer trapping effect, and charge redistribution, which can change the electrical performance of the device.

Keywords: GaN; HEMT; substrate voltage; breakdown voltage; dynamic on-resistance; donor trap; charge redistribution

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1. Introduction

In recent years, GaN-on-Si power HEMTs have gained tremendous interest due to their superior electrical characteristics, such as high breakdown voltage (BV), low on-resistance (R_{on}), and fast switching speed [1–3]. Compared to GaN-on-SiC and GaN-on-sapphire, GaN-on-Si is most suitable for commercialization owing to the low cost and the scalability to large wafer sizes [3]. The epitaxial structure of a lateral GaN-on-Si buffer stack from bottom to top is usually composed of an AlN nucleation layer, called a superlattice, or graded AlGaN transition layer, a carbon-doped (C-doped) GaN layer, and an unintentionally doped (UID) GaN channel layer [4]. However, GaN buffer stacks usually have plenty of dislocations, lattice defects, and bulk traps due to the lattice and thermal expansion coefficient mismatch between GaN and silicon [5]. The dynamic R_{on} of GaN-on-Si HEMT is related to the surface- and buffer-induced trapping. When the devices are switched from the off- to on-state, the hot electrons generated in the two-dimensional electron gas (2DEG) channel are injected into the surface and buffer layers. When the surface and buffer traps

cannot immediately release the trapping electrons, the 2DEG channel is partially depleted to increase the dynamic R_{on} [6].

The surface-induced trapping can be suppressed by the passivation and field plate. In contrast, the buffer-induced trapping caused by the compensated doping and crystalline defects is more challenging to address. During the epitaxial growth, the AlN nucleation layer is usually defective. It contains many donor-type impurities (e.g., Si, O), resulting in a lower effective energy barrier at the AlN/Si junction [7,8] for the enhanced charge injection to occur. Moreover, due to the energy barrier at the AlN–Si substrate interface, the electrons induced from the Si substrate may also be injected into the buffer with positive $V_{top\text{-}to\text{-}sub}$ (or negative V_{SUB}) by trap-assisted tunneling, thermionic emission, and Poole–Frenkel emission [7–9].

For the GaN-on-Si HEMT, carbon doped (C-doped) is a common technique to reduce buffer conductivity, reduce current collapse, and increase BV during the epitaxial growth process [10]. The carbon atoms can substitute Ga or N sites, occupy interstitial positions in the nitride, and form chemical complexes with intrinsic defects [11–13]. A dominant deep-acceptor trap at E_V +0.9 eV (generally considered to correspond to the C_N state) and a shallow donor trap at E_C −0.11 eV (more likely related to the C_{Ga} state) of the two main energy states are related to the carbon doping in the GaN buffer [10]. An appropriate ratio of acceptor trap and donor trap concentration may exist to achieve the optimum BV and buffer leakage current due to the vertical electric field modulation [14].

C-doped GaN layers could behave as p-type materials due to sufficient compensation doping and the Fermi level (E_F) in the lower half of the bandgap [15]. UID GaN layers are observed to show light n-type conductivity owing to the existence of nitrogen vacancies [4]. The neutral, ionized donor, and acceptor traps can affect the 2DEG conductivity and buffer-stacks charge redistribution. The applied V_{SUB} or V_D at the UID/C-doped GaN interface may result in a behavior similar to the p–n junction [4]. The applied positive/negative V_{SUB} causes different charging/discharging behaviors, which could be related to the non-uniform spatial distribution of dopant traps and the charge redistribution in the buffer stacks. The intrinsic trap time constants and the charge transport in the buffer stacks are both related to the response of donor/acceptor traps in the UID/C-doped GaN layers [15].

Recently, several studies discussed the impacts of V_{SUB} on buffer-related performances, such as dynamic R_{on} [4,16] BV [17,18] vertical leakage current [19,20], gate charge change [21], and output capacitance [22]. However, most works were limited to the individual properties mentioned above. There are few reports [17,18] to investigate the overall device characteristics such as BV, on-state drain current, and dynamic R_{on} respective to V_{SUB} for a GaN HEMT structure, thus, they are lacking unified models and discussions. Compared to these reports [17,18], which applied a V_{SUB} of about ±60 V, we can apply a higher V_{SUB} because the superlattice transition layer with a higher energy barrier can prevent electrons from injecting into the buffer stack layer at a high V_{SUB}. In this study, we investigate the effects of a positive/negative V_{SUB} on the above-mentioned device characteristics of the AlGaN/GaN HEMT having a superlattice transition layer. The impact of 2DEG conductivity and the charge trapping/de-trapping procedure are also investigated under the different V_{SUB} and off-state V_D.

2. Materials and Methods

The AlGaN/GaN heterostructures were grown on a 6-inch silicon substrate by metal-organic chemical vapor deposition (MOCVD), as shown schematically in Figure 1. The AlGaN/GaN HEMT structure consists of an AlN nucleation layer, a superlattice transition layer, a C-doped GaN layer, a GaN channel layer, and 22 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The mesa isolation was performed by BCl_3 + Cl_2 mixed gas plasma etching. To perform the Ohmic contact formation at source and drain, Ti/Al/Ni/Au was deposited by e-beam evaporation and was annealed by rapid temperature annealing (RTA) at 840 °C for 30 s in N_2 ambient. The Ni/Au (50/300 nm) Schottky gate contact was deposited by the electron beam evaporation. Finally, 20 nm SiN was deposited as a passivation layer. The source-

drain length, gate length, and gate width were maintained at 20, 3, and 25 µm, respectively. The buffer stacks can be considered insulated capacitors when the leakage current of each layer is smaller than the "displacement current"; i.e., $I_{DISS} = C_{TOT}dV_{SUB}/dt$, C_{TOT} is the series combination of the capacitances of UID GaN, C-doped GaN, and superlattice transition layer, respectively [15].

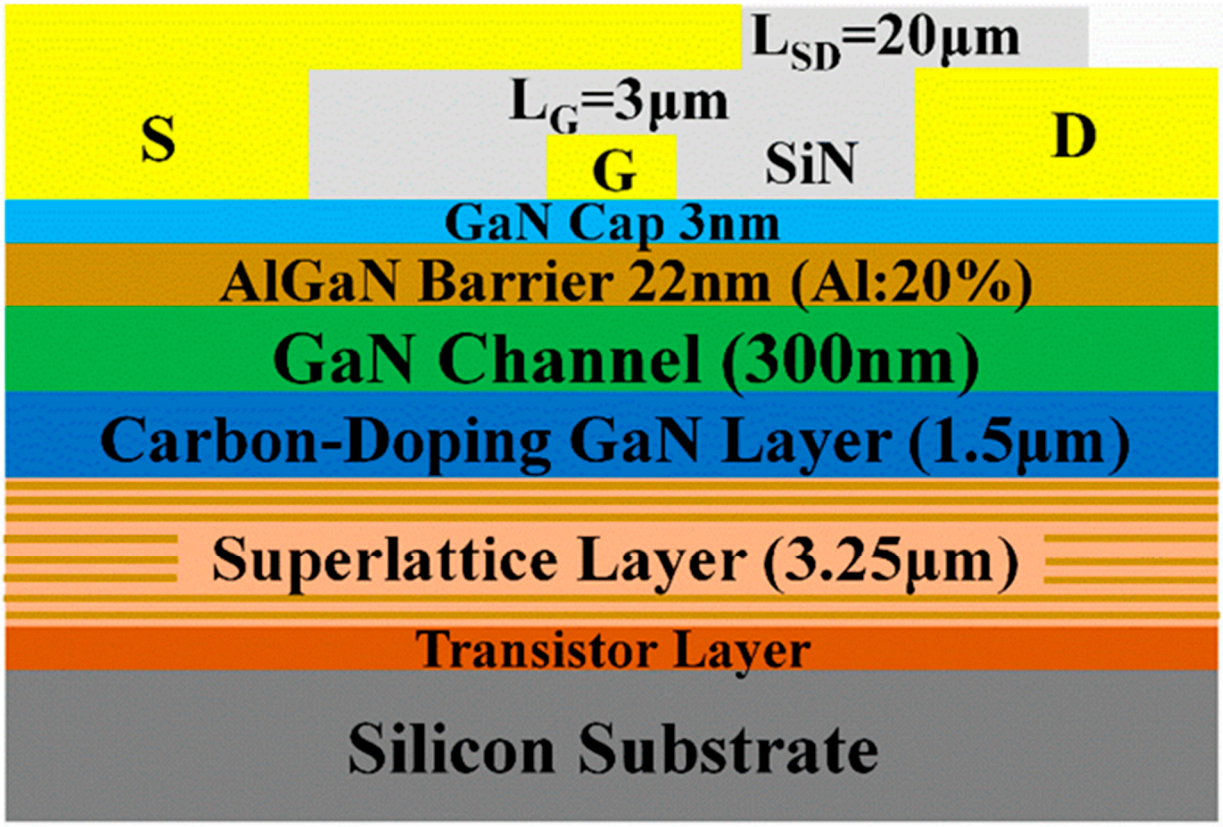

Figure 1. Schematic cross section of the GaN-on-Si device with superlattice buffer.

3. Results and Discussion

As shown in Figure 2, the buffer trap charging/discharging mechanism of HEMT devices with a superlattice transition layer is demonstrated schematically. The substrate of GaN-on-Si power HEMT can be used as an independent contact terminal for applying V_{SUB} [23]. The V_{SUB} can modulate the 2DEG concentration through the back-gate effect. Figure 2a shows that the buffer acceptor and donor traps are partly ionized and neutralized at the initial state. The un-ionized neutral donor/acceptor traps may exist in the UID/C-doped GaN layer. The opposite doping polarities may lead to the formation of the p–n junction at the UID/C-doped GaN interface [4,9,15].

Figure 2b shows that the electrons are injected from the Ohmic contact or 2DEG channel into the buffer layer when applying a positive V_{SUB} [24,25]. The Ohmic contact provides the reservoir of free electrons that can be injected into the buffer layer when applying a positive V_{SUB}. Without applying V_{SUB}, the acceptor trap pulls down the E_F in the buffer/transition layer so that the E_F is below the acceptor trap level (E_{TA}). Many acceptor traps are not ionized (charge-neutral) because the acceptor traps are deep. When the positive V_{SUB} increases, the high vertical electric field induces electron trapping (ionization at the acceptor trap level) in the buffer layer of the acceptor trap [24,25]. Because a positive V_{SUB} of 200 V is smaller than the traps-filled-limit voltage of donor traps (V_{TFL2}), both with the positive V_{SUB} and without the V_{SUB} do not affect the concentration of the ionized donor trap.

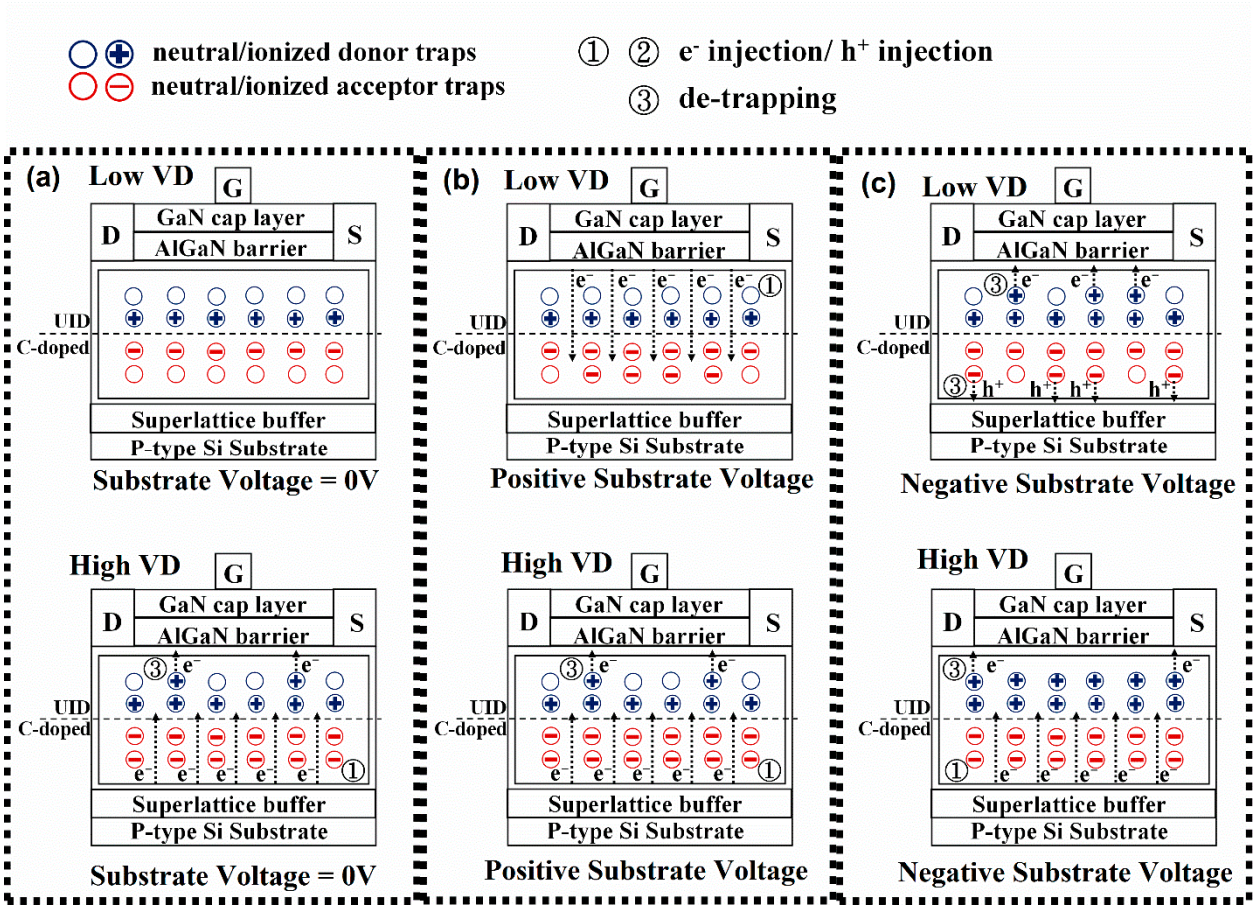

Figure 2. (**a**) Without V_{SUB}: the traps charging/discharging in the buffer while applying the low or high drain voltage (V_D). (**b**) With positive V_{SUB}: the traps charging/discharging in the buffer while applying the low or high V_D. (**c**) With negative V_{SUB}: the traps charging/discharging in the buffer while applying the low or high V_D.

Figure 2c shows that the concentration of both ionized acceptor and donor traps increases with the negative V_{SUB}. In addition to the inherent barrier of the AlN/Si junction, the superlattice transition layer makes the electrons more difficult to be injected into the buffer layer in the off-state under the high V_D. The top and bottom asymmetric vertical leakage and the fundamental difference between the carrier injection/transport mechanisms induced a different buffer layer trapping. The acceptor traps in the carbon-doped GaN are mostly ionized at a V_{SUB} of −100 V, resulting in a net negative charge [4]. This net negative charge lifts the buffer energy band, increasing the energy barrier of the transition layer to a higher value, and injecting fewer electrons to the buffer layer [16]. The transition layer with a superlattice buffer structure can block the electron injections from the AlN/Si junction to the buffer layer. At off-state and high V_D, the electrons from the Si substrate begin to overcome the energy barrier of the superlattice layer and inject into the buffer layer. When part of the buffer layer starts to conduct, the negative charge accumulates in the buffer layer, resulting in an increase in the buffer leakage current [15].

Figure 3 shows the energy band diagram when a different V_{SUB} and low/high V_D are applied. Figure 3a shows that without V_{SUB}, the energy band has more bending as the V_D increases. Figure 3b shows that at low V_D, the applied positive V_{SUB} causes the Si substrate to bend downward. The 2DEG channel tends to inject more electrons into the buffer stack, resulting in an entirely negative charge redistribution in the buffer layer and an increase in the concentration of the ionized acceptor trap. The positive V_{SUB} can alleviate the energy band bending caused by applied high V_D, and the electrons in the inversion layer formed at the Si substrate/AlN interface are less able to overcome the energy barrier of AlN and

superlattice and inject into the buffer layer, avoiding the accumulation of negative charge in the buffer layer. Figure 3c shows that the negative V_{SUB} can raise the energy band of the Si substrate even more and accumulate electrons in the inversion layer at the Si substrate/AlN interface at lower V_D. After the electrons overcome the AlN energy barrier, the electrons are blocked by the superlattice layer and are not injected into the buffer layer. When the V_D becomes larger, the bending of the energy band becomes more significant, which is equal to the applied drain voltage of $|V_D + V_{SUB}|$ to the device. This causes the electrons accumulated in the Si substrate/AlN inversion layer to have higher energy to overcome the energy barrier of AlN and superlattice to inject into the buffer layer. This results in a significant amount of electrons injected into and accumulated in the C-doped GaN layer.

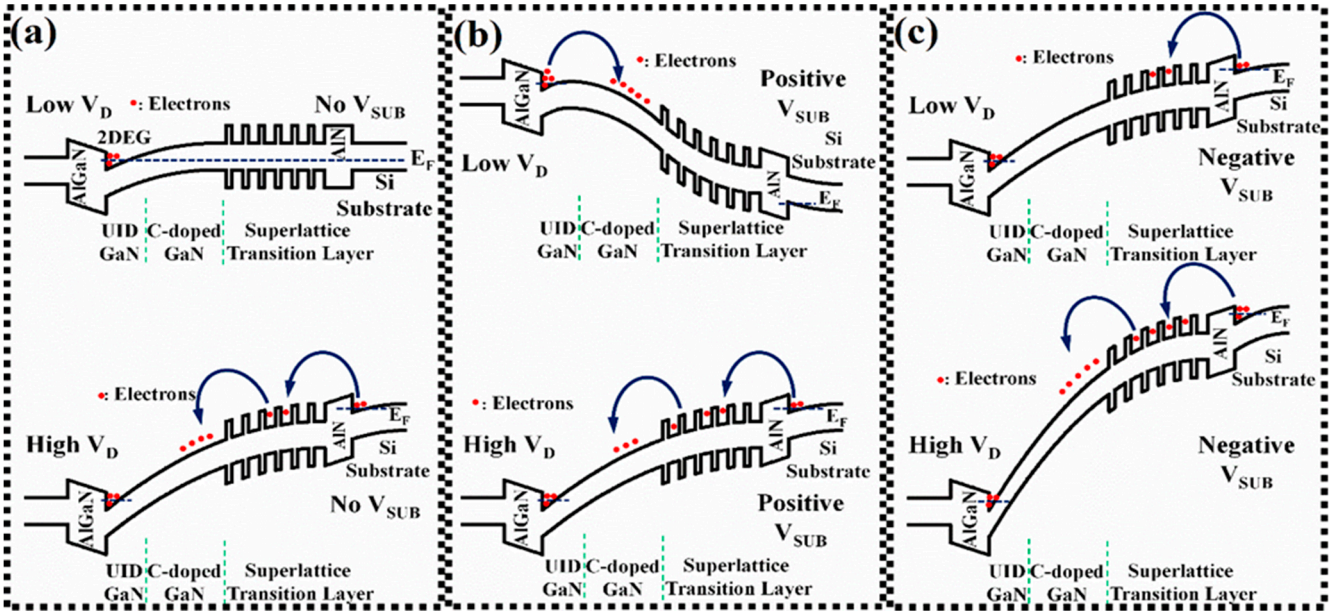

Figure 3. Band diagram with different V_{SUB} and low/high V_D condition. (**a**) Without V_{SUB}, (**b**) with positive V_{SUB}, (**c**) with negative V_{SUB}.

Table 1 and Figure 4 compare the overview of DC characteristics under the positive/negative V_{SUB}. Applying the positive V_{SUB} tends to induce more electrons in the 2DEG channel. However, the maximum drain current (I_D) is almost constant because the ionized acceptor traps caused by injection electrons from the 2DEG channel or ohmic contact could clamp the increasing 2DEG concentration [4]. Under the positive V_{SUB}, the DC characteristics are similar to the device without V_{SUB}. A slightly reduced off-state I_D is observed with a positive V_{SUB} due to the leakage current flow from the drain to the buffer layer. Part of the electrons are also captured by the acceptor trap of the GaN carbon-doped layer, resulting in a slightly reduced total leakage current. Figure 2b shows that due to the applied positive V_{SUB}, the electrons from the Ohmic contact at the interface of source and drain with GaN or 2DEG are injected into the buffer layer, where the acceptor trap of the GaN carbon-doped layer is ionized for the lower V_D (12 V) case. An applied negative V_{SUB} ideally reduces the maximum I_D due to the simple electric field effect or capacitive coupling [15]. The ionization of acceptor traps in the buffer layers depletes the 2DEG channel; both can degrade the 2DEG conductivity. The V_{th} increases because the required gate voltage (V_G) for turning on the depleted channel is increased. As Figure 2c shows, off-state applied negative V_{SUB} causes the ionized donor trap concentration in the UID GaN layer to increase. An increase in ionized donor trap concentration indicates that positive charges have accumulated in the buffer layer. Hence, the positive charges neutralize part of the leakage current flowing into the buffer layer. Therefore, the total off-state I_D decreases, and the on/off current ratio increases. The subthreshold swing (S.S) of this HEMT device is related to the I_D magnitude when V_G is smaller than the threshold voltage (V_{th}). As the

off-state leakage current reduces due to the negative V_{SUB}, a reduction in S.S is observed. The transconductance (g_m) hike of this superlattice HEMT device with a negative V_{SUB} applied is also observed. Firstly, the applied negative V_{SUB} reduced the off current and increased the change in current per unit voltage, making the g_m maximum larger. Secondly, when the negative V_{SUB} is between −50 and −200 V, charge redistribution occurs in the GaN carbon doping layer. The higher maximum g_m is related to the buffer stack charge redistribution due to the capacitance change of UID GaN, C-doped GaN, and superlattice transition layer [26].

Table 1. DC characteristics of the GaN-on-Si HEMT with different substrate voltages.

Substrate Voltage (V)	On/Off I_D Ratio	S.S (mV/dec)	V_{th} (V)	R_{on} (Ω•mm)	g_m (mS/mm)	$I_{D,max}$ (mA/mm)	Off-State I_D (mA/mm)
−200	1.16×10^6	155	−9.59	9.45	87.5	608	5.24×10^{-4}
−100	4.79×10^5	180	−10.59	9.39	82	644	1.34×10^{-3}
0	2.16×10^5	202	−11.76	9.28	80.4	696	3.22×10^{-3}
100	2.91×10^5	203	−11.8	9.21	81.5	702	2.41×10^{-3}
200	3.05×10^5	201	−11.78	9.16	81.7	701	2.3×10^{-3}

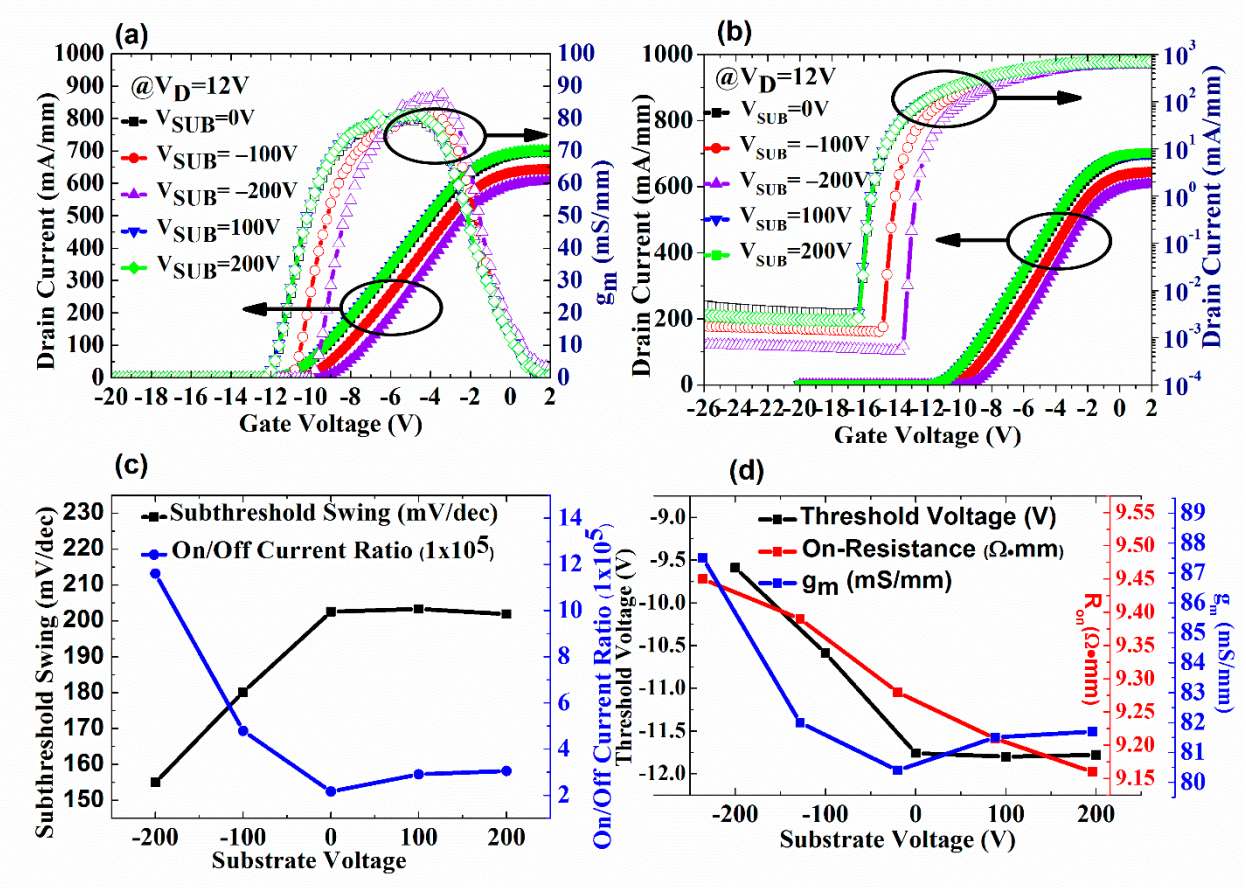

Figure 4. (**a**,**b**) I_D-V_G characteristics of the superlattice-based HEMT for different V_{SUB}. (**c**) Comparisons of drain current (I_D), on/off ratio, and subthreshold swing versus (S.S) different V_{SUB}. (**d**) Comparison of V_{th}, R_{on}, and g_m versus different V_{SUB}.

Figure 5 shows the BV characteristics measured using off-state leakage current with the positive/negative V_{SUB}. Figure 5a,b show that the negative V_{SUB} can increase the BV due to the increased ionized donor trap concentration. The BV was measured starting from V_D = 0 V and gradually increased in voltage by 2 V/s. The electrons forming in the inversion layer between the Si substrate and AlN layer slowly accumulate energy to

overcome the energy barriers to inject into the buffer stack. The electrons injected into the buffer layer have a sufficient reaction time to neutralize the ionized donor trap in the UID GaN with a positive charge. The ionized donor trap is more critical to BV than the ionized acceptor trap due to the alleviation of the non-uniform distribution of the high electric field caused by high V_D [14]. Applying the negative V_{SUB} (or positive $V_{top\text{-}to\text{-}sub}$) causes the donor/acceptor traps to ionize at the UID/carbon-doped GaN interface [27]. An increase in ionized donor trap concentration with a moderate acceptor trap can increase the BV and reduces the off-state leakage current [14]. Therefore, the concentration of ionized donor trap and BV increase when a negative V_{SUB} is applied. On the other hand, Figure 2a,b show that the electrons from the 2DEG channel or the Ohmic contact are primarily injected into the buffer layer to increase the ionized acceptor traps without decreasing the concentration of the ionized donor traps [15]. The BV at the applied positive V_{SUB} and V_{SUB} = 0 are very similar due to the same concentration of ionized donor traps.

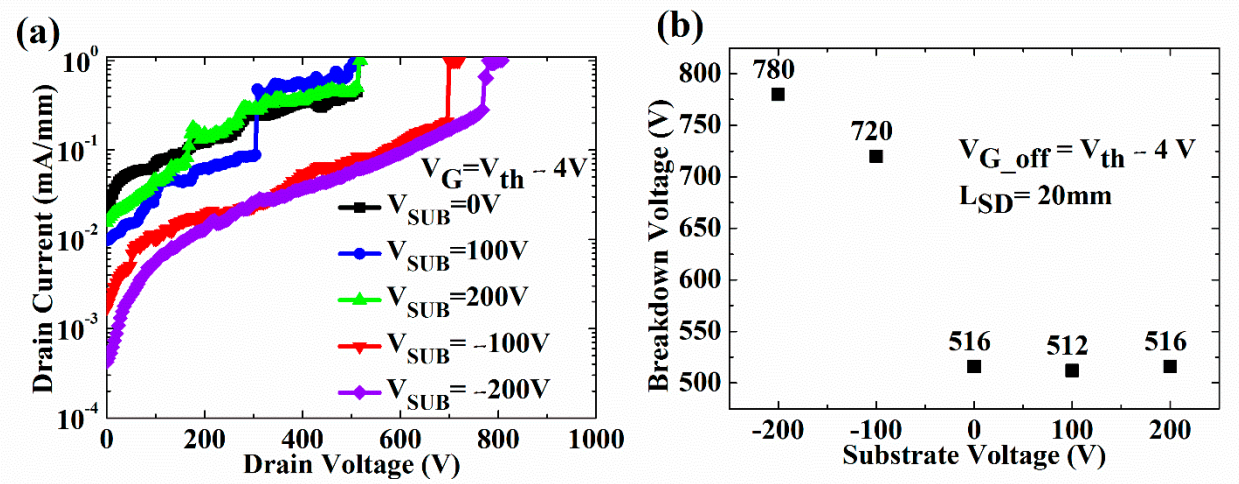

Figure 5. (**a**) Off-state drain leakage current of the GaN-on-Si HEMT as a function of substrate voltage in the log scale. (**b**) BV at different $V_{D,\,off}$ as a function of various V_{SUB}.

The dynamic R_{on} characteristics for the HEMT devices with different V_{sub} were also measured. After each dynamic R_{on} measurement, the device's initial state is fully recovered by shining microscopic light for 30 s, so that all trapped electrons were de-trapped [28]. Figure 6a shows that the device is switched to the on-state with a total switching time of 200 µs after 10 ms of high V_D stress at off-state. As shown in Figure 6b, the positive V_{SUB} slightly reduces the dynamic R_{on}, while the negative V_{SUB} significantly increases the dynamic R_{on}. The dynamic R_{on} ratio for applying the positive V_{SUB} is slightly lower than without V_{SUB} (the off-state V_D is from 100 to 300 V). As shown in Figure 3b, the positive V_{SUB} can relax the energy band bending of the Si substrate/AlN junction caused by high V_D, reducing the electrons that can overcome the energy barrier injected into the buffer layer.

Although an ionized acceptor trap in a C-doped layer may screen the electric field of a positive V_{SUB}, applying a positive V_{SUB} slightly increases the 2DEG conductivity by the field effect. Due to the electron injections into the buffer layer from the 2DEG channel and Ohmic contact, the ionization of the acceptor trap concentration in the C-doped GaN layer increases by applying a positive V_{SUB}. The donor trap concentration is almost similar when applying a positive V_{SUB} and without V_{SUB}. The literature has reported that the ionization donor trap in UID GaN can alleviate the dynamic R_{on} degradation [9,14]. The ionization donor trap leads to a redistribution of the positive charge in the buffer stack. However, as shown in Figure 3c, the negative V_{SUB} aggravates the Si substrate energy band bending, allowing the electrons to have higher energy to overcome the energy barriers between the AlN nucleation layer and superlattice transition layer injection into the buffer layer. The electrons injected into the buffer layer are not neutralized by the ionization donor

trap (positive charge) in a short time. The 2DEG channel may be depleted, resulting in dynamic R_{on} degradation. Therefore, under the negative V_{SUB}, the dynamic R_{on} degraded more seriously.

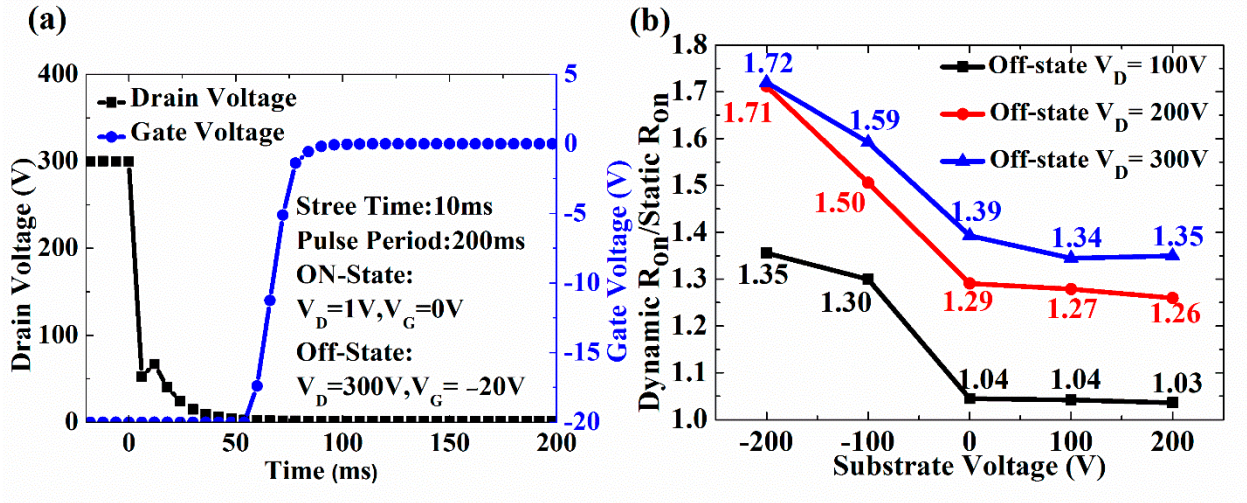

Figure 6. (**a**) Dynamic R_{on} transients of Drain/Gate voltage (V_G) vs. time (μs) (**b**) Dynamic R_{on}/static R_{on} ratio at different off-state V_D as a function of various V_{SUB}.

4. Conclusions

The effect of V_{SUB} on the power application characteristics of GaN-on-Si high electron mobility transistors (HEMTs) with a superlattice transition layer, including breakdown voltage (BV) and dynamic on-resistance (R_{on}), was investigated. The negative V_{SUB} increases the BV due to the increasing ionized donor-trap concentration. However, the positive V_{SUB} and without V_{SUB} do not affect the ionization donor-trap concentration, so both BVs are similar. The applied positive V_{SUB} can relax the energy band bending of the Si substrate/AlN junction caused by the high vertical electric field. Therefore, the reducing electrons inject the buffer stack layer. The dynamic R_{on} ratio can be slightly reduced by applying a positive V_{SUB} of 200 V at high off-state V_D. Although the applied negative V_{SUB} increases the ionized donor trap concentration, it also raises the Si substrate energy band. More electrons overcome the energy barrier and are injected into the buffer layer, causing the buffer trap to capture more electrons, and depleting the two-dimensional electron gas (2DEG) channel, making the dynamic R_{on} degradation more serious. When applying the negative $V_{SUB,}$ S.S decreases, the on/off current ratio increases, and threshold voltage (V_{th}) shifts to positive due to the reduction in source-drain leakage current. When applying the positive V_{SUB}, the DC performances of the devices, such as on/off current ratio, S.S, and V_{th}, remain almost the same as without an applied V_{SUB} because both 2DEG conductivities remain nearly the same.

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References

1. Amano, H.; Baines, Y.; Beam, E.; Borga, M.; Bouchet, T.; Chalker, R.P.; Charles, M.; Chen, K.J.; Chowdhury, N.; Chu, R.; et al. The 2018 GaN power electronics roadmap. *J. Phys. D* **2018**, *51*, 163001. [CrossRef]
2. Chen, J.K.; Häberlen, O.; Lidow, A.; Tsai, C.L.; Ueda, T.; Uemoto, Y.; Wu, Y. GaN-on-Si Power Technology: Devices and Applications. *IEEE Trans. Electron Devices* **2017**, *64*, 779–795. [CrossRef]
3. Zhou, C.D.; Li, W.; Shen, J.; Chen, L.; Zhao, T.; Lin, K.; Zhang, M.; Chen, L.; Chiu, H.C.; Zhang, J.; et al. Reliability of 200 mm E-mode GaN-on-Si Power HEMTs. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 28 April–30 May 2020.
4. Yang, S.; Han, S.; Wei, J.; Sheng, K.; Chen, K.J. Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices. *IEEE Trans. Electron Devices* **2017**, *64*, 5048–5056. [CrossRef]
5. Marchand, H.; Zhao, L.; Zhang, N.; Moran, B.; Coffie, R.; Mishra, U.K.; Speck, J.S.; DenBaars, S.P. Metal organic chemical vapor deposition of GaN on Si(111): Stress control and application to field-effect transistors. *J. Appl. Phys.* **2001**, *89*, 7846. [CrossRef]
6. Yang, S.; Han, S.; Sheng, K.; Chen, K.J. Dynamic on-resistance in GaN power devices: Mechanisms, characterizations, and modeling. *IEEE J. Emerg. Sel. Top. Power Electron* **2019**, *7*, 1425–1439. [CrossRef]
7. Yang, S.; Jiang, Q.; Li, B.; Tang, Z.; Chen, K.J. GaN-to-Si vertical conduction mechanisms in AlGaN/GaN-on-Si lateral heterojunction FET structures. *Phys. Status Solidi C* **2014**, *11*, 949–952. [CrossRef]
8. Moens, P.; Banerjee, A.; Uren, M.J.; Meneghini, M.; Karboyan, S.; Chatterjee, I.; Vanmeerbeek, P.; Cäsar, M.; Liu, C.; Salih, A.; et al. Impact of buffer leakage on intrinsic reliability of 650v AlGaN/GaN HEMTs. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015.
9. Miller, E.J.; Yu, E.T.; Waltereit, P.; Speck, J.S. Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular beam epitaxy. *Appl. Phys. Lett.* **2004**, *84*, 535–537. [CrossRef]
10. Zagni, N.; Chini, A.; Puglisi, F.M.; Pavan, P.; Verzellesi, G. On the modeling of the donor/acceptor compensation ratio in carbon-doped GaN to univocally reproduce breakdown voltage and current collapse in lateral GaN power HEMTs. *Micromachines* **2021**, *12*, 709. [CrossRef]
11. Matsubara, M.; Bellotti, E. A first-principles study of carbon-related energy levels in GaN. I. Complexes formed by substitutional interstitial carbons and gallium nitrogen vacancies. *J. Appl. Phys.* **2017**, *121*, 195701. [CrossRef]
12. Lyons, J.L.; Wickramaratne, D.; Walle, C.G.V.D. A first-principles understanding of point defects and impurities in GaN. *J. Appl. Phys.* **2021**, *129*, 111101. [CrossRef]
13. Remesh, N.; Mohan, N.; Raghavan, S.; Muralidharan, R.; Nath, D.N. Optimum carbon concentration in GaN-on-Silicon for breakdown enhancement in AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2020**, *67*, 2311–2317. [CrossRef]
14. Joshi, V.; Tiwari, S.P.; Shrivastava, M. Part I: Physical insight into carbon-doping-induced delayed avalanche action in GaN buffer in AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2019**, *66*, 561–569.
15. Uren, J.M.; Karboyan, S.; Chatterjee, I.; Pooth, A.; Moens, P.; Banerjee, A.; Kuball, M. "Leaky Dielectric" Model for the Suppression of Dynamic RON in Carbon-Doped AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2017**, *64*, 2826–2834.
16. Yang, W.; Yuan, J.S.; Krishnan, B.; Shea, P. Low-side GaN power device dynamic Ron characteristics under different substrate biases. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 31 March–4 April 2021.
17. Chiu, H.-C.; Peng, L.Y.; Yang, C.W.; Wang, H.C.; Hsin, Y.M.; Chyi, J.I. Analysis of the back-gate effect in normally off p-GaN gate high-electron mobility transistor. *IEEE Trans. Electron Devices* **2015**, *62*, 507–511. [CrossRef]
18. Mahaboob, I.; Yakimov, M.; Hogan, K.; Rocco, E.; Tozier, S.; Shahedipour-Sandvik, F. Dynamic control of AlGaN/GaN HEMT 18 characteristics by implementation of a p-GaN body-diode-based back-gate. *IEEE J. Electron Devices Soc.* **2019**, *7*, 581–588. [CrossRef]
19. Moench, S.; Müller, S.; Reiner, R.; Waltereit, P.; Czap, H.; Basler, M.; Hückelheim, J.; Kirste, L.; Kallfass, I.; Quay, R.; et al. Monolithic integrated AlGaN/GaN power converter topologies on high-voltage AlN/GaN superlattice buffer. *Phys. Status Solidi* **2020**, *218*, 2000404. [CrossRef]
20. He, X.; Feng, Y.; Yang, X.; Wu, S.; Cai, Z.; Wei, J.; Shen, J.; Huang, H.; Liu, D.; Chen, Z.; et al. Step-graded AlGaN vs superlattice: Role of strain relief layer in dynamic on-resistance degradation. *Appl. Phys. Express* **2020**, *15*, 011001. [CrossRef]
21. Yang, W.; Yuan, J.S. Experimental investigation of buffer traps physical mechanisms on the gate charge of GaN-on-Si devices under various substrate biases. *Appl. Phys. Lett.* **2020**, *116*, 083501. [CrossRef]
22. Zhuang, J.; Zulauf, G.; Rivas-Davila, J. Substrate bias effect on e-mode GaN-on-Si HEMT coss losses. In Proceedings of the IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October–2 November 2018.
23. Tang, G.; Wei, J.; Zhang, Z.; Tang, X.; Hua, M.; Wang, H.; Chen, K.J. Dynamic Ron of GaN-on-Si lateral power devices with a floating substrate termination. *IEEE Electron Device Lett.* **2017**, *38*, 937–940. [CrossRef]
24. Zhou, C.; Jiang, Q.; Huang, S.; Chen, J.K. Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices. *IEEE Electron Device Lett.* **2012**, *33*, 1132–1134. [CrossRef]
25. Zhou, C.; Jiang, Q.; Huang, S.; Chen, K.J. Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Structures. In Proceedings of the 24th International Symposium on Power Semiconductor Devices and ICs (24th ISPSD), Bruges, Belgium, 3–7 June 2012.
26. Chatterjee, I.; Uren, J.M.; Karboyan, S.; Pooth, A.; Moens, P.; Banerjee, A.; Kuball, M. Lateral charge transport in the carbon-doped buffer in AlGaN/GaN-on-Si HEMTs. *IEEE Trans. Electron Devices* **2017**, *64*, 977–983. [CrossRef]

27. Zhang, H.; Kang, X.; Jin, Z.; Zheng, Y.; Wu, H.; Wei, K.; Liu, X.; Ye, T. Investigation on Dynamic Characteristics of AlGaN/GaN Lateral Schottky Barrier Diode. *Micromachines* **2021**, *12*, 1296. [CrossRef] [PubMed]
28. Joh, J.; Alamo, J.A.D. A Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors. *IEEE Trans. Electron Devices* **2011**, *58*, 132–140. [CrossRef]