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Dynamic Enhancement for Dual Active Bridge Converter with a Deadbeat Current Controller

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Abstract: This paper investigates the deadbeat current controllers for isolated bidirectional dual-active-bridge dc-dc converter (IBDC), including the peak current mode (PCM) and middle current mode (MCM). The controller uses an enhanced single phase shift (ESPS) modulation method by exploiting pulse width as an extra control variable in addition to phase shift ratio. The control variables for PCM controllers are derived in detail and the two different current controllers are compared. A double-closed-loop control method is then employed, which could directly control the high-frequency inductor current and eliminate the transient DC current bias of the transformer. Furthermore, load feedforward was introduced to further enhance the dynamic of the converter. With the proposed control method, the settling time could be reduced within several PWM cycles during load disturbance without transient DC current bias. A 5 kW IBDC converter prototype was built and the settling time of 6 PWM cycles during load change with voltage regulation mode was achieved, which verifies the superior dynamic performance of the control method.

Keywords: dual active bridge; deadbeat controller; load feedforward

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1. Introduction

The isolated bi-directional dual-active-bridge dc-dc converter (IBDC) has been a hot topic in recent years due to its simple structure, high efficiency and ultrafast response [1]. The transient DC current offset of the transformer and the inductor, which might saturate the transformer and increase the system's current stress during the abrupt load change, has attracted people's attention. Different dynamic modulation methods have been proposed to solve the problem [2–5]. Additionally, to increase the dynamics of IBDCs, the current mode controller could be a competitive alternative. It also has other inherent benefits including over-current protection, elimination of transient DC current offset and easy implementation of current sharing between multiple IBDCs [6].

Digital predictive current controllers based on conventional single phase shift (CSPS) modulation was proposed in [7,8], where the phase shift ratio was used to control the transformer current. In [7], the average current calculated by an analog integrator of the DC bus current was used as the feedback signal, which can achieve fast dynamic performance. However, transient DC current offset occurs during the sudden change in phase shift ratio for CSPS modulation.

The predictive duty cycle mode (PDCM) controller, shown in Figure 1b, was proposed in [6] to eliminate the transient DC current offset, which was applied in [8]. The drive signals of the primary side are fixed. The transformer current needs to be oversampled, and duty cycles d1 for S2,3 and d2 for S1,4 are calculated in turn in every half cycle. Another limitation of this method is that the controller only works in the ZVS range (IP1 > 0) shown in Figure 1b and may lose effectiveness when IP1 < 0.

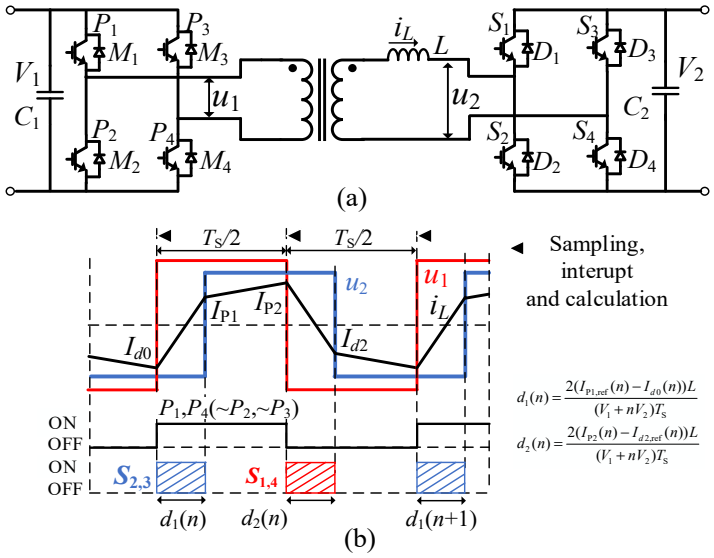

Figure 1. Principle of the PDCM controller. (**a**) IBDC, (**b**) waveforms.

A deadbeat current controller based on the middle current and enhanced PWM modulation was proposed in [9]. However, regulation of the output voltage and current was not introduced, which is more important in real application. To overcome the drawbacks, this paper investigated the deadbeat current controllers, including the peak current mode (PCM) and middle current mode (MCM). Based on the controllers, a double-closed-loop control method with load feedforward was introduced. Furthermore, a 5 kW IBDC converter prototype was built, and the settling time of 6 PWM cycles during load change could be achieved, which validates its superior dynamic performance.

2. Deadbeat Peak Current Mode Controller

2.1. Basic Model of IBDC for SPS Modulation

The basic model of SPS modulation-based IBDC is presented prior to introducing the proposed current controller. Figure 2 illustrates the theoretical waveforms of the IBDC using the SPS modulation method when converter voltage gain $k \geq 1$, where $k = V_1/(nV_2)$ and n is the turn ratio of the transformer. The waveforms are symmetrical for the same transmission power of two opposite directions.

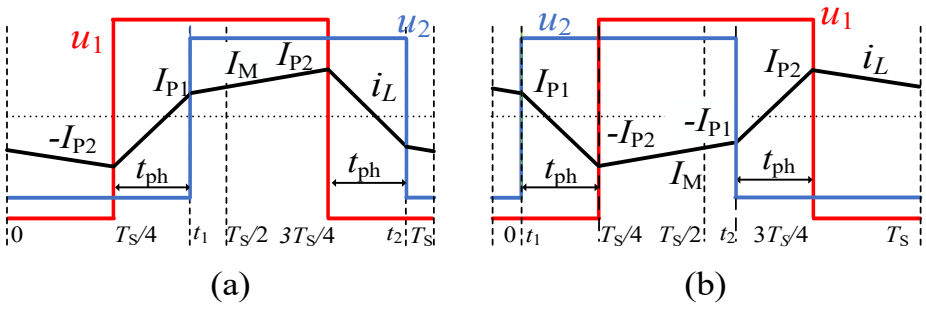

Figure 2. Waveforms of IBDC at steady state for CSPS modulation: (**a**) forward power transmission ($P > 0$), (**b**) reverse power transmission ($P < 0$).

The symbols in Figure 2 are defined as follows: TS is the switching cycle, f is the switching frequency, D is the phase shift ratio and tph is the shifted time. $D \geq 0$ ($t_{ph} \geq 0$) stands for $P \geq 0$ and $D < 0$ ($t_{ph} < 0$) for $P < 0$. I_{P1} and I_{P2} are the two "switching currents" and I_{P2} is the peak current when $k > 1$. The middle current IM, defined as the instantaneous

current at $T_S/2$, is taken into consideration instead of the average current, which equals zero in one cycle. The basic equations for the IBDC are derived as follows:

$$\begin{cases} P = \frac{V_1^2}{2fLk} D(1-|D|)\,,\, t_{ph} = \frac{DT_S}{2} \\ I_{P1} = \frac{V_1(2k|D|-k+1)}{4fLk},\, I_{P2} = \frac{V_1(2|D|+k-1)}{4fLk},\, I_M = \frac{V_1 D}{2fLk} \end{cases} \tag{1}$$

The relationships among the variables P, I_{P1}, I_{P2}, I_M, D and t_{ph} at steady state can then be derived. Therefore, for a given value of one variable, other variables can be calculated.

2.2. Peak Current Mode Controller

Peak current mode (PCM) controllers are introduced in this section. Figure 3a,b show the transient waveforms of a PCM current controller in one cycle for forward and reverse power transmission, respectively. P_1, P_2, P_3 and P_4 are the drive signals for the primary side and S_1, S_2, S_3 and S_4 are the drive signals for the secondary side. The variable $t_{ph,ref}$ is shifted-time at the steady state for the given $I_{P2,ref}$ which can be derived from (1). A sawtooth carrier with the same frequency of the converter was utilized to generate the reference signals. The "switching on" moment t_1 and "switching off" moment t_2 should meet the constrains as: $0 < t_1 < T_S/2$ and $3T_S/4 < t_2 < T_S$. The variables t_D and t_W are defined as "delay time" and "width time", respectively. P_{ref} is the power reference, and $I_{P2,ref}$ and $I_{P1,ref}$ are the references for the corresponding "switching currents", respectively.

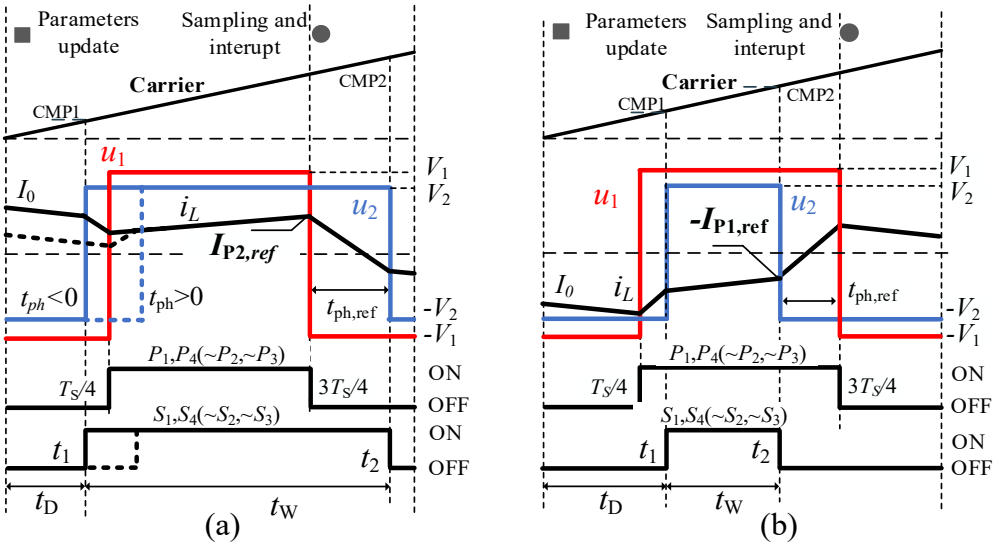

Figure 3. Transient waveforms of PCM controller: (**a**) forward power transmission ($P_{ref} > 0$), (**b**) reverse power transmission ($P_{ref} < 0$).

As shown in Figure 3a, there are two cases according to the initial current I_0 and reference current $I_{p2,ref}$: u_2 leads u_1 ($t_{ph} < 0$) for the solid line waveforms and u_2 lags u_1 ($t_{ph} > 0$) for dotted line waveforms. For the sake of brevity, the superposition principle was used to derivate the inductor current when calculating t_D and t_W.

For forward power transmission, the requirement was imposed that $I_{P2} = I_{P2,ref}$ and $t_{ph,ref} > 0$. According to the superposition principle, the inductor current ripple ΔI_L during 0 and $3T_S/4$ can be calculated by adding up the two ripple currents as follows:

$$\begin{cases} \Delta I_L = \Delta I_{L,u_1} + \Delta I_{L,u_2} \\ \Delta I_{L,u_1} = \frac{-V_1}{L} \cdot \frac{T_S}{4} + \frac{-V_1}{L} \cdot \frac{T_S}{2}\,,\, \Delta I_{L,u_2} = \frac{V_2}{L} \cdot t_D + \frac{-V_2}{L} \cdot (\frac{3T_S}{4} - t_D) \\ I_{P2} = I_0 + \Delta I_L = I_{P2,ref} \end{cases} \tag{2}$$

where $\Delta I_{L,u_1}$ and $\Delta I_{L,u_2}$ are current ripples generated by the two dependent voltage source u_1 and u_2, respectively. t_D is then derived as:

$$t_D = \frac{(I_{P2,ref} - I_0)Lk}{2V_1} + \frac{3-k}{8f} \tag{3}$$

Furthermore, t_W is derived as:

$$t_W = \frac{3T_S}{4} - t_D + t_{ph,ref} \tag{4}$$

With regard to reverse power transmission, the switching current at t_2 is set to be—$I_{P1,ref}$ and $t_{ph,ref} < 0$ as shown in Figure 4. Similar to forward power transmission, t_D and t_W can be obtained. Thus, the equations for the PCM controller are written as:

$$\begin{cases} t_D = \frac{kL(I_{P2,ref}-I_0)}{2V_1} + \frac{3-k}{8f};\ t_W = \frac{kL(I_{P2,ref}+I_0)}{2V_1} - \frac{k-5}{8f},\ P_{ref} \geq 0 \\ t_D = -\frac{kL(I_{P2,ref}+I_0)}{2V_1} + \frac{k+1}{8f};\ t_W = -\frac{kL(I_{P2,ref}-I_0)}{2V_1} + \frac{k+3}{8f},\ P_{ref} < 0 \end{cases} \tag{5}$$

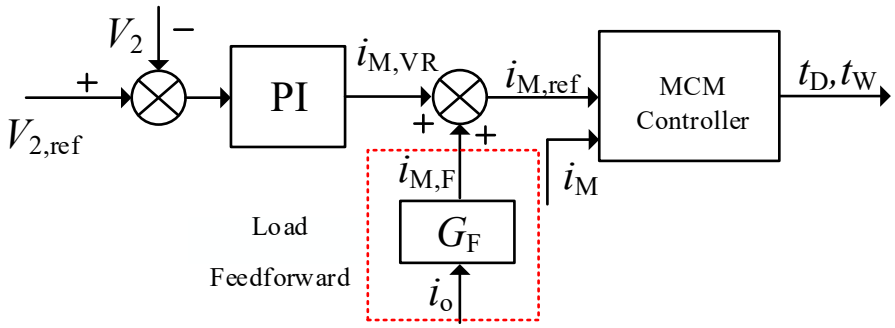

Figure 4. Voltage control scheme based on the MCM-ESPS controller.

As in the aforementioned Equations (6) and (7), initial current I_0 is sampled to calculate the t_D and t_W. However, a one-cycle delay exists between the sampling instant and control update due to the algorithm implementation of the digital processor. I_{P2} for the PCM controller is sampled at $3T_S/4$, and DSP interrupt occurs to calculate the new parameters shown in Figure 3. t_D and t_W update at the beginning of the next cycle. Assuming DC bus voltage V_1 and V_2 are constant in two adjacent periods, the relationships between the $I_{P2}(n-1)$, $I_M(n-1)$ in the $(n-1)$th cycle and the initial current in the nth switching cycle $I_0(n)$ could be derived as:

$$I_0(n) = \begin{cases} I_{P2}(n-1) - \frac{2V_1(k-1)}{Lk}(t_D(n-1) + t_W(n-1)) + \frac{V_1(7-k)}{4fLk},\ P_{ref}(n-1) \geq 0 \\ I_{P2}(n-1) - \frac{V_1(k-1)}{4fLk},\ P_{ref}(n-1) < 0 \end{cases} \tag{6}$$

According to the power transmission directions in two adjacent cycles, four situations are considered for the PCM controller: case 1 when $P_{ref}(n-1) \geq 0$ and $P_{ref}(n) \geq 0$; case 2 when $P_{ref}(n-1) < 0$ and $P_{ref}(n) \geq 0$; case 3 when $P_{ref}(n-1) \geq 0$ and $P_{ref}(n) < 0$; and case 4 when $P_{ref}(n-1) < 0$ and $P_{ref}(n) < 0$. Combining (6)–(9), the control variables t_D and t_W with delay compensation can be derived as shown in Table 1. With the control variables in Table 1, the inductor peak current could be tracked to the reference in two cycles, which is consistent with the idea of the deadbeat control in ref [10].

Table 1. Control variable calculation with one-cycle delay compensation.

Mode		$t_D(n)$	$t_W(n)$
CSPS ($P_{ref} \geq 0$)		$\frac{kL(I_{M,ref}(n)-I_M(n-1))}{2V_1} + t_D(n-1)$	$\frac{1}{2f}$
ESPS-PCM	Case 1	$\frac{kL(I_{M,ref}(n)-I_M(n-1))}{2V_1} + t_D(n-1) + t_W(n-1) - \frac{1}{2f}$	$\frac{kL(I_{P2,ref}(n)+I_{P2}(n-1))}{2V_1} - (k-1)(t_D(n-1)+t_W(n-1)) + \frac{6-k}{4f}$
	Case 2	$\frac{kL(I_{P2,ref}(n)-I_{P2}(n-1))}{2V_1} + \frac{1}{4f}$	$\frac{kL(I_{P2,ref}(n)+I_{P2}(n-1))}{2V_1} - \frac{k-3}{4f}$
	Case 3	$-\frac{kL(I_{P2,ref}(n)+I_{P2}(n-1))}{2V_1} + (k-1)(t_D(n-1) + t_W(n-1)) + \frac{k-3}{4f}$	$-\frac{kL(I_{P2,ref}(n)-I_{P2}(n-1))}{2V_1} - (k-1)(t_D(n-1) + t_W(n-1)) + \frac{5}{4f}$
	Case 4	$-\frac{kL(I_{P2,ref}(n)+I_{P2}(n-1))}{2V_1} + \frac{k}{4f}$	$-\frac{kL(I_{P2,ref}(n)-I_{P2}(n-1))}{2V_1} + \frac{1}{4f}$
ESPS-MCM		$\frac{kL(I_{M,ref}(n)-I_M(n-1))}{2V_1} + t_D(n-1) + t_W(n-1) - \frac{1}{2f}$	$\frac{kL(I_{M,ref}(n)+I_M(n-1))}{2V_1} - t_D(n-1) - t_W(n-1) + \frac{5}{4f}$

3. Double-Closed-Loop Control with Load Feedforward

In practice, instead of the high-frequency inductor current, the DC voltage, current or power should always be regulated. In this section, the voltage mode control strategy based on the MCM-ESPS controller is introduced.

Figure 4 shows the output voltage control scheme based on the deadbeat current controller, where two control loops are involved. The load feedforward control could substantially increase the system dynamic [11,12]. In order to improve the stability of output voltage under load disturbance, load feedforward under double-closed-loop control is presented. As shown in Figure 4, the feedforward current $i_{M,F}$ corresponding to the load was superimposed on the current reference $i_{M,VR}$, which is the output of the outer voltage loop, to form the final current reference value $i_{M,ref}$.

The relationships of the middle current were derived as:

$$I_M = \begin{cases} \frac{V_1}{2fLk}\left(\frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2fLkP}{{V_1}^2}}\right), P \geq 0 \\ -\frac{V_1}{2fLk}\left(\frac{1}{2} - \sqrt{\frac{1}{4} + \frac{2fLkP}{{V_1}^2}}\right), P < 0 \end{cases} \quad (7)$$

Without considering the power loss of the converter, we could obtain:

$$P = V_2 i_o \quad (8)$$

Thus, the relationship between the middle current I_M and the load current i_o could be expressed as (9) and (10):

$$I_M = \begin{cases} \frac{V_1}{2fLk}\left(\frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2fLi_o}{V_1}}\right), i_o \geq 0 \\ -\frac{V_1}{2fLk}\left(\frac{1}{2} - \sqrt{\frac{1}{4} + \frac{2fLi_o}{V_1}}\right), i_o < 0 \end{cases} \quad (9)$$

$$i_o = NI_M\left(1 - \frac{2fLkI_M}{V_1}\right) \quad (10)$$

The small signal model of the system, as shown in Figure 5, can be obtained from the control block diagram in Figure 4, where i_S is the average output current of an H bridge in a single period and $G_o(s)$ is the transfer function of capacitance voltage and capacitance current, denoted as:

$$G_o(s) = 1/(C_2 s) \quad (11)$$

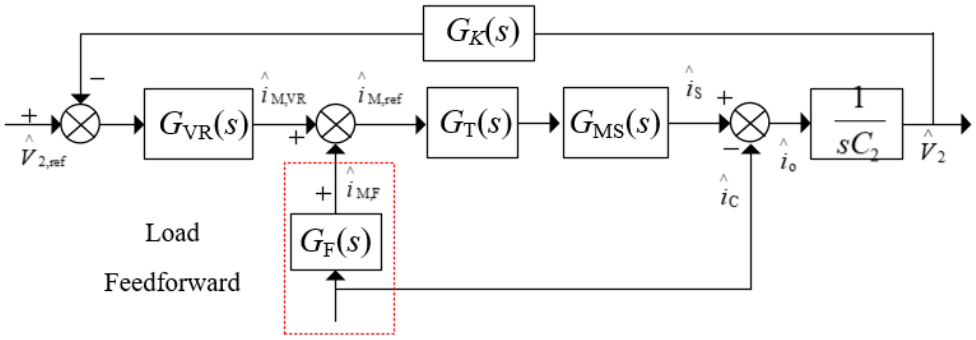

Figure 5. Small signal model of an IBDC with the double-closed-loop control strategy.

$G_{VR}(s)$ is the volatge regulation transfer function, where the conventional PI controller is always used. K_P and K_I are the proportional and integral coefficients of the PI regulator, respectively. Thus, we could obtain:

$$G_{VR}(s) = K_P + K_I s \tag{12}$$

$G_F(s)$ represents the transfer function of the load feedforward and $G_{MS}(s)$ is the relationship between i_M and i_s. $G_C(s)$ is the transfer function of the deadbeat current controller. Considering a one-cylce delay, it could be written as:

$$G_C(s) = \frac{1 - e^{-sT_s}}{s} \tag{13}$$

The feedforward transfer function $G_F(s)$ can be calculated using small-signal analysis based on Equation (10). To substitute $i_o = \bar{i}_o + \hat{i}_o$ and $I_M = \bar{I}_M + \hat{I}_M$ into (10), ignoring the higher-order terms, $G_F(s)$ be derived as:

$$G_F(s) = \hat{I}_{M,F}(s)/\hat{i}_o(s) = 1/(N(1 - 4fLkI_M/V_1)) \tag{14}$$

The average output current of H bridge in the secondary side is derived as:

$$i_s = \frac{V_1 N}{2fL} D(1 - D) \tag{15}$$

Combing (1) with (16), the $G_{MS}(s)$ could be derived as:

$$G_{MS}(s) = \hat{i}_S(s)/\hat{I}_M(s) = N(1 - 4fLkI_M/V_1) \tag{16}$$

According to the small signal model in Figure 5, the output impedance $R_{o1}(s)$ without and with feedforward could be calculated as (17) and (18), respectively.

$$R_{o1}(s) = \frac{\hat{V}_2(s)}{\hat{i}_o(s)} = -\frac{G_o(s)}{1 + G_{VR}(s)G_C(s)G_{MS}(s)G_o(s)} \tag{17}$$

$$R_{o2}(s) = \frac{\hat{V}_2(s)}{\hat{i}_o(s)} = \frac{(G_F(s)G_C(s)G_{MS}(s) - 1)G_o(s)}{1 + G_{VR}(s)G_C(s)G_{MS}(s)G_o(s)} \tag{18}$$

By substituting the circuit parameters and control parameters into Equations (17) and (18), baud diagrams of output impedance with different loads under the double-closed-loop control strategy can be drawn as shown in Figure 6. In this case, the inductance L = μH, the voltage V_1 = 300V and V_2 = 280V.The coefficients of the PI regulator are K_P = 2 and K_I = 4000.

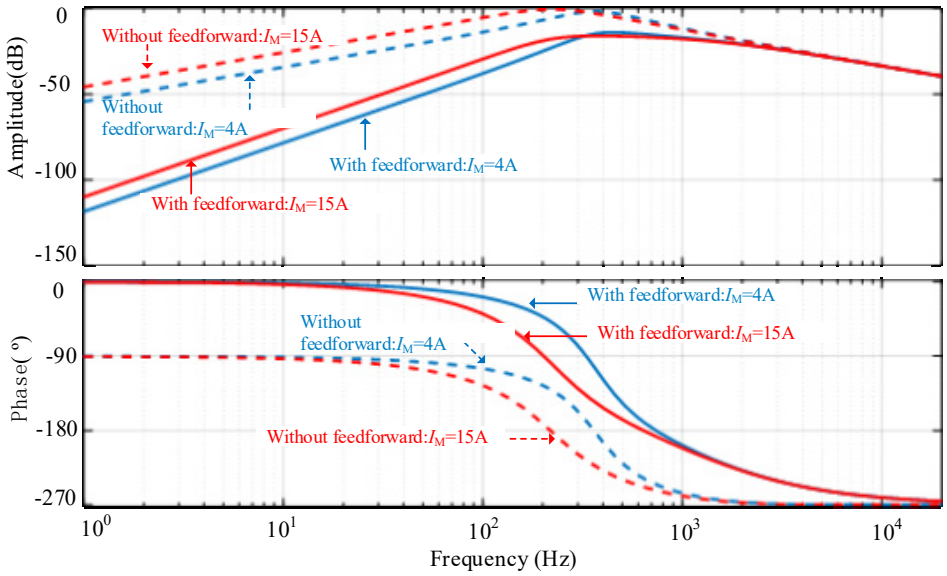

Figure 6. Output impedance of the converter with different loads.

As shown in Figure 6, the closed-loop output impedance at low frequency decreases significantly after the feedforward is added. When I_M = 4 A, the output impedance at a frequency of 100 Hz decreases from −15 dB to −35 dB, whereas when I_M = 15 A, the output impedance decreases from −8 dB to −30 dB at 100 Hz. If the frequency is further reduced, the amplitude attenuation of the closed-loop output impedance brought by the feedforward control become more obvious, which indicates a more robust output voltage under the load disturbance.

4. Experimental Verification

4.1. Experimental Platform

The laboratory IBDC experimental platform shown in Figure 7 was used to verify the proposed control method. The main circuit parameters are listed in Table 2. The current sensor LA55-P had a 200 kHz bandwidth from LEM. PE-Expert4 from Myway was utilized as the digital controller including DSP and FPGA cores. FPGA XC6SLX45 was used to generate PWM signals. The control variables were calculated in each cycle in DSP, and the corresponding PWM compare values CMP1 and CMP2 were updated at the beginning of the next cycle.

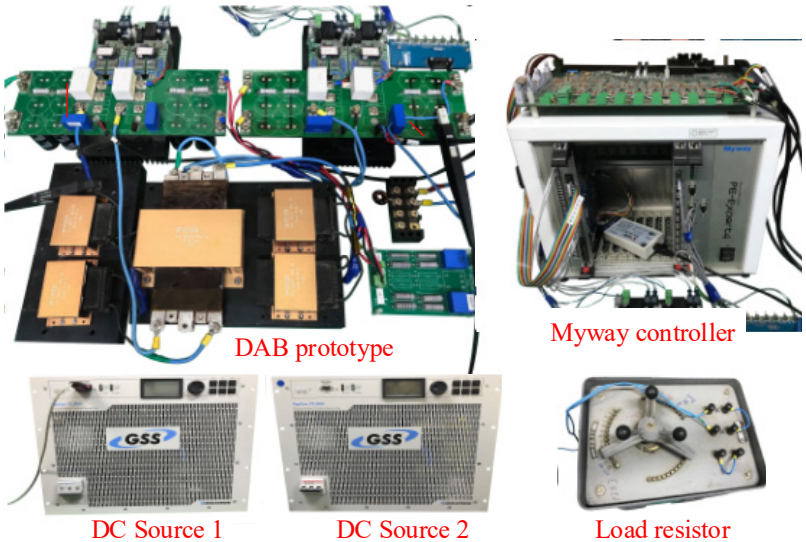

Figure 7. Experimental platform.

Table 2. System Parameters.

Input voltage V_1	300 V	Output voltage V_1	280 V
Turns ratio n	1:1	Switching frequency f	10 kHz
Primary capacitor C_1	2460 μF	Secondary capacitor C_2	2460 μF
Inductor L	652 μH	Equivalent resistor Rs	80 mΩ

4.2. Comparisons of Different Current Controllers for Forward Power Transmission

The performance of the CSPS modulation-based current controller in [5] and the proposed ESPS-PCM were compared for the forward power transmission mode.

Figure 8 shows the experimental waveforms of current i_L when the references have step changes. The references could be tracked for all the controllers when the current reference steps up from 3 A to 8 A and steps down from 8 A to 3 A. The settling time t_{set} in Figure 8a is obvious, while the settling time in Figure 8b is negligible. Additionally, the ESPS-PCM controller eliminates the transient DC current offset that exists in CSPS modulation-based controller, as shown in the dashed circle of Figure 8a.

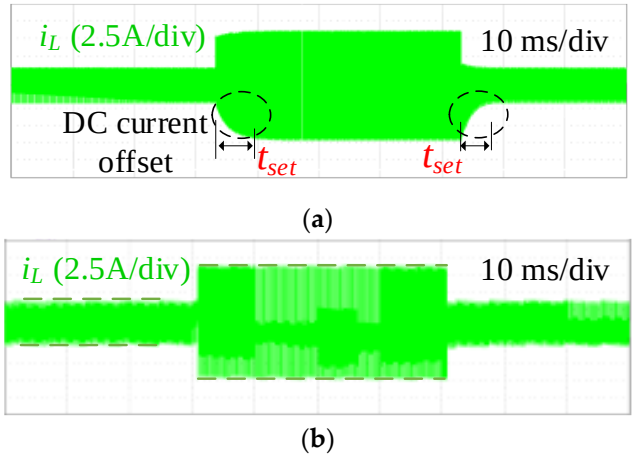

Figure 8. Zoomed-out waveforms during the step change of the current reference for forward power transmission. (**a**) CSPS modulation-based current controller. (**b**) ESPS-PCM controller.

To verify the performance of the current controllers during bidirectional power transmission, a sequence of current references was set to investigate the response. Figure 9 shows the waveforms of the ESPS-PCM controller. The transmission power P stepped up from 600 W to 1450 W at t_1, changed direction to −1450 W at t_3, reversed direction to 1450 W at t_5 and then stepped down to 600 W at t_7. The current references were smoothly reached with a one-cycle delay during the whole transient process, including the transition between two opposite power transmissions.

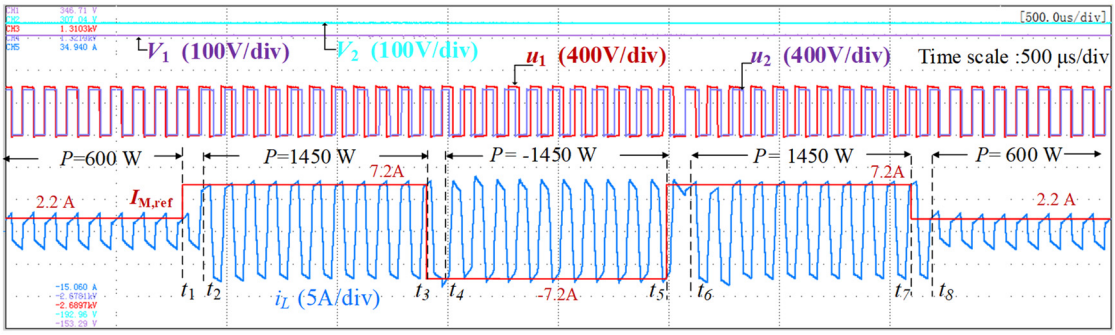

Figure 9. Transient waveforms of bidirectional power transmission.

4.3. Dynamic Performance Comparison between Different Control Methods

The experimetal results with traditional single-voltage loop control, double-closed-loop control and double-closed-loop control with feedforward under load disturbance are shown in Figures 10–12. The output voltage V_2 was 280 V, and the load increased abruptly at t_1 with load resistance decreases from 75 Ω to 25 Ω and decreased sharply at t_2 with load resistance increases from 25 Ω to 75 Ω. When the load increases, the DC voltage will fall, and the control loop will increase the phase shift angle to transfer more power to maintain the DC load. Simillarly, when the DC load decreases, the DC voltage will rise and the control loop will decrease the phase shift angle to reduce the transmitted power.

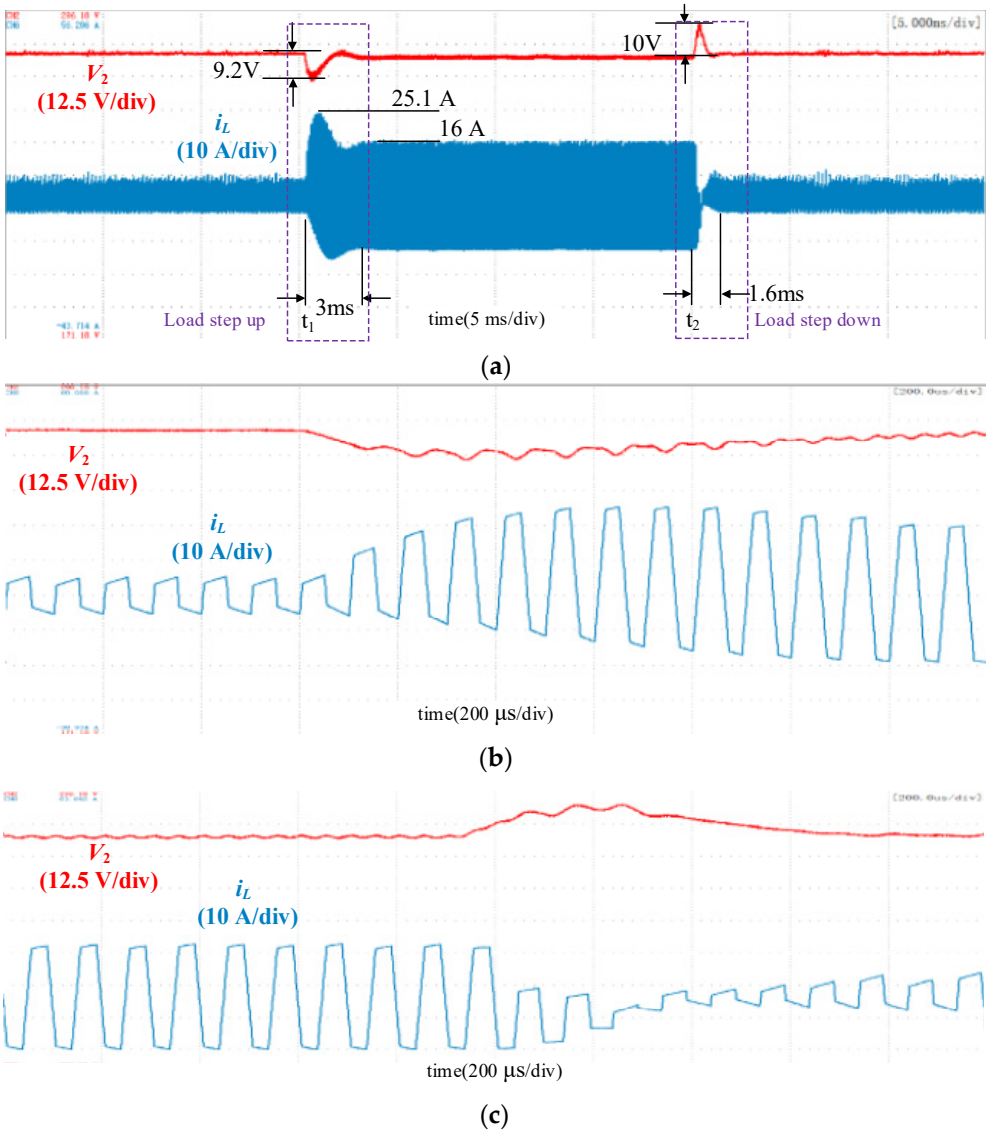

Figure 10. Waveforms using the conventional single-loop control. (**a**) Overall waveforms; (**b**) Zoomed-in waveforms during the load increase; (**c**) Zoomed-in waveforms during the load decrease.

Figure 10 shows the waveform using the conventional single-loop control. The inductor current shows obvious transient DC bias during abrupt load change. When the load increased, the peak current reached 25.1 A, and the current overshoot was 9.1 A. In the experiment, both the static and dynamic performances under load increase and decrease were considered when tuning the PI parameters. The waveform showed that the voltage sag was 9.2 V, and the settling time was 3 ms when the load increased. The voltage overshoot was 10 V, and the settling time was 1.6 ms when the load decreased. Figure 11 shows the waveform using the double-closed-loop control. The inductor current

was symmetrical, and the transient DC bias was eliminated. When the load increased, the voltage sag was 8.2 V, and the settling time was 1.9 ms. The voltage overshoot was 9 V, and the settling time was 1.3 ms when the load decreased.

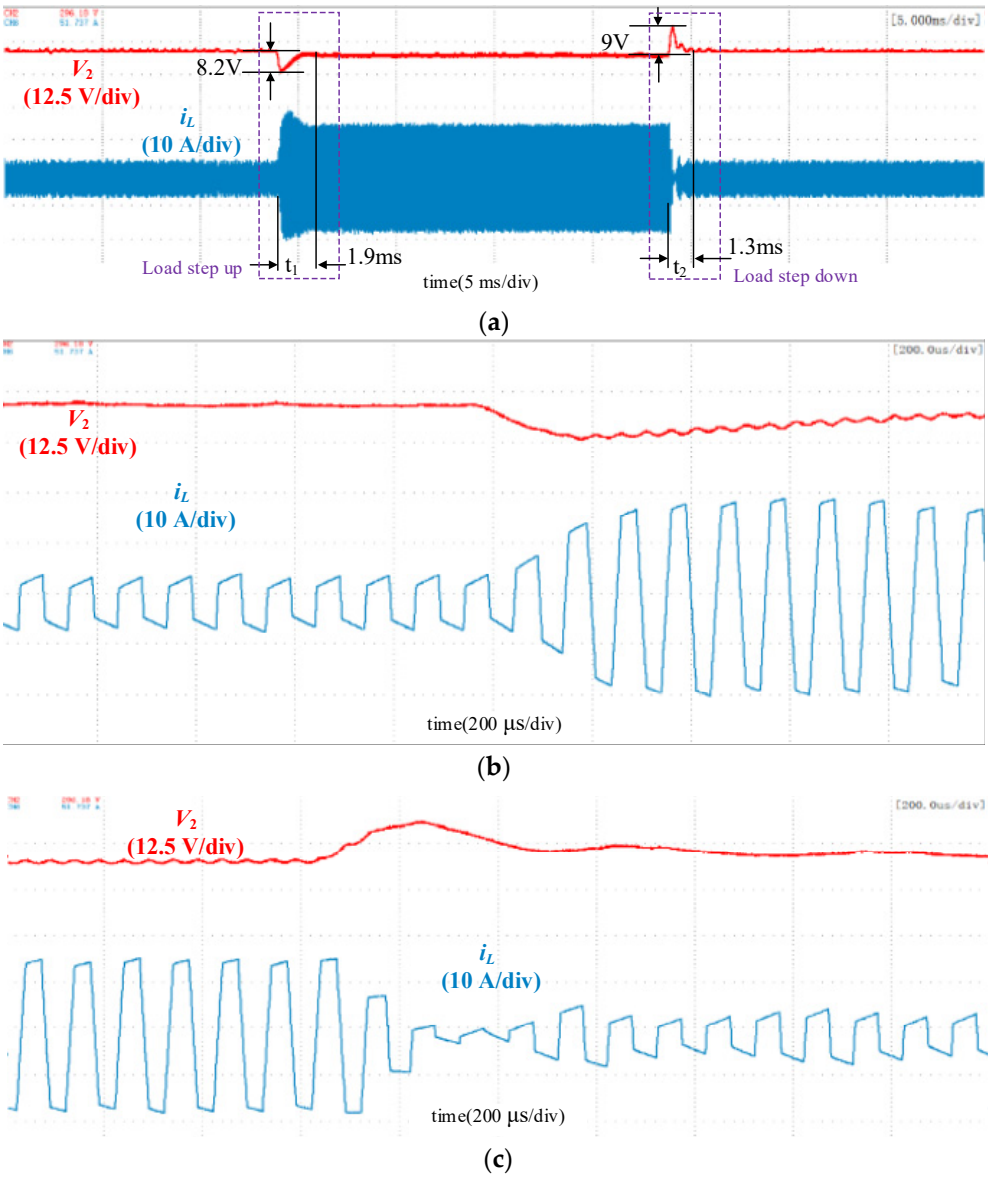

Figure 11. Waveforms using the double-closed-loop control. (**a**) Overall waveforms; (**b**) Zoomed-in waveforms during the load increase; (**c**) Zoomed-in waveforms during the load decrease.

Figure 12 shows the waveforms using the double-closed-loop control with load feedforward. The transient DC bias was eliminated. During the transient process, the DC voltage variation was significantly reduced, and the settling time was obviously shortened compared with the double-closed-loop control without load feedforward. The voltage sag was 3 V when the load increased, and the voltage overshoot was 4.4 V when the load decreased. In the process of load surge, the recovery time for DC voltage was 0.5 ms, which is five switching cycles. The recovery time was 0.6 ms, which is six switching cycles, in the process of load decreases.

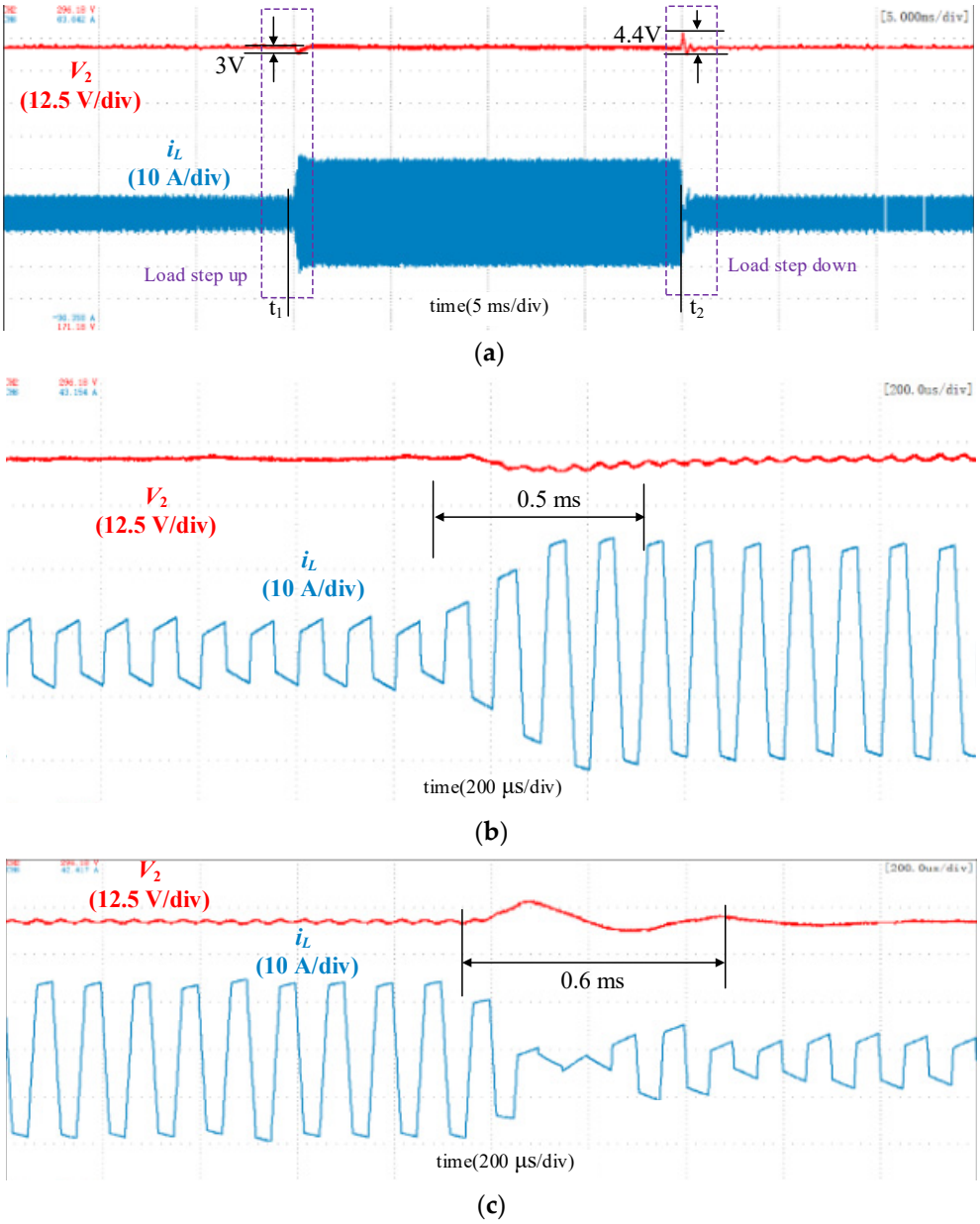

Figure 12. Waveforms using the double-closed-loop control with load feedforward. (**a**) Overall waveforms; (**b**) Zoomed-in waveforms during the load increase; (**c**) Zoomed-in waveforms during the load decrease.

Compared with the traditional single-voltage loop control, the double-closed-loop control utilizes the deadbeat current controller as the inner loop, which directly regulates the high-frequency AC current of the transformer. Thus, the transient DC current bias could be eliminated. Meanwhile, the dynamic performance the of the IBDC with voltage mode mainly depends on the bandwidth of the feedback signal [12]. With the feedforward control samples, the load changes directly, which could significantly increase the robustness of the DC voltage under the load disturblances. The dynamic performance enhancement of the proposed control can be seen by comparison of Figures 11 and 12.

5. Conclusions

A double-closed-loop control strategy based on the deadbeat current controller was proposed in this paper, which directly regulates the high-frequency inductor current to the reference and eliminates the transient DC current bias during the transient process.

Furthermore, load feedforward was introduced to enhance the dynamic of the converter. The proposed control method shows potential in the application of IBDC under voltage mode. With the proposed method, the settling time could be reduced to within several PWM cycles during load disturbance. A 5 kW IBDC converter prototype was built, and the superior dynamic performance of the proposed control strategy was verified by the experimental results.

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