



## Article

# A High-Gain and High-Efficiency Photovoltaic Grid-Connected Inverter with Magnetic Coupling

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**Abstract:** Conventional photovoltaic (PV) grid-connected systems consist of a boost converter cascaded with an inverter, resulting in poor efficiency due to performing energy processing twice. Many pseudo DC-link inverters with single energy processing have been proposed to improve system efficiency and simplify circuits. However, their output voltage gain is limited by the non-ideal characteristics of the power diode, making them difficult to apply in high-output voltage applications. This paper proposes combining a boost converter with magnetic coupling and a full-bridge unfolding circuit to develop an inverter featuring high voltage-gain and high efficiency. According to the desired instantaneous output voltage, the high-gain boost converter and the full-bridge unfolding circuit are sequentially and respectively controlled by SPWM. A sinusoidal output voltage can be generated by performing energy processing only once, effectively improving the conversion efficiency. Magnetic coupling is adopted to increase the voltage gain of step-up, and the step-down function is realized by the full-bridge unfolding circuit to reduce conduction loss. Finally, a 500 W prototype was fabricated for the proposed high-gain inverter. The experimental results were used to verify the correctness of the theoretical analysis and the feasibility of the circuit structure.



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**Keywords:** high gain; high efficiency; inverter; magnetic coupling

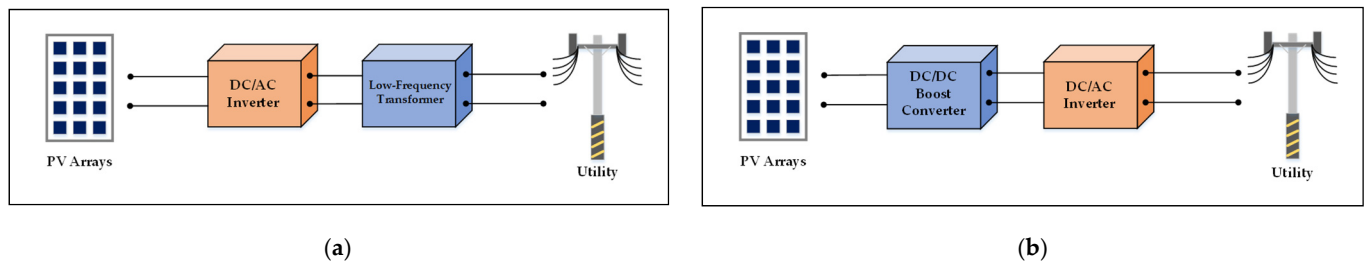
## 1. Introduction

Recently, air pollution has become increasingly serious due to the high consumption of fossil fuels. To reduce carbon dioxide emissions to mitigate global warming and climate change, many researchers are committed to developing renewable energy sources such as photovoltaic (PV), wind, hydro, geothermal and biogas [1–3]. Among them, PV energy is attracting increasing attention, and is widely used around the world. There are three types of PV power systems: grid-connected, stand-alone, and hybrid [4–6], in which grid-connected systems are the most popular. The PV grid-connected system converts the direct current (DC) of solar energy into alternating current (AC) and feeds it into the grid [7,8].

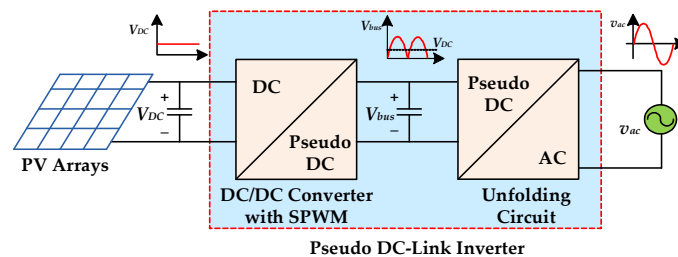
Due to the low voltage of the PV panels, a low-frequency transformer needs to be added after the inverter in order to be connected with utility, as shown in Figure 1a. However, the low-frequency transformer significantly increases the size and cost of this PV power system. The transformer-less PV grid-connected system is the alternative structure, as shown in Figure 1b. It uses a boost converter to step-up the PV voltage and then converts it to AC power for connection with the utility [9,10]. The transformer-less structure has the advantages of small size and low cost, but its efficiency is reduced because of multiple energy processing stages.

Several single-stage inverters derived from boost or buck converters have been proposed to improve the efficiency [11–13], but their application is limited by the need for multiple input sources and the inability to cover a wide range of input voltage variations. Therefore, many pseudo DC-Link inverters have been proposed to overcome these drawbacks [14–18]. Figure 2 shows the block diagram of the pseudo DC-Link inverter, in which a DC/DC converter with both step-up and step-down capabilities is used to generate a

rectified sine wave with unipolarity, and an unfolding circuit is cascaded to switch the polarity and to obtain a sinusoidal output voltage. Since the unfolding circuit switches only with the frequency of utility line, a pseudo DC-link inverter that requires only one energy processing can effectively improve conversion efficiency. However, the step-down function is achieved by connecting an additional power switch in series, resulting in higher conduction loss. In addition, the output voltage gain is limited because of the non-ideal characteristics of the power diode, making it unusable for low input voltage or high output voltage applications.



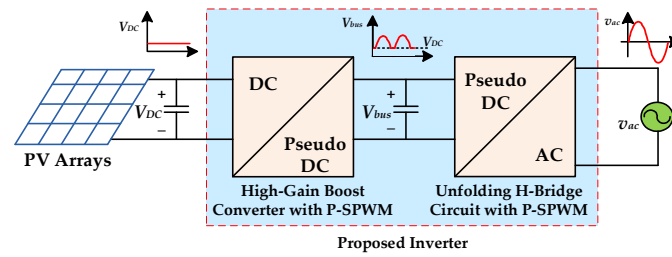
**Figure 1.** The structures of PV grid-connected power systems with (a) a low-frequency transformer; (b) a boost converter.



**Figure 2.** The grid-connected PV power system with a pseudo DC-link inverter.

Based on the above considerations, this paper proposes a high-gain and high-efficiency inverter with magnetic coupling, the block diagram of which is shown in Figure 3. The proposed inverter combines a high-gain boost converter with coupling inductor and a full-bridge unfolding circuit. When the instantaneous output voltage is higher than the input voltage, the high-gain boost converter is controlled by sinusoidal pulse-width modulation (SPWM), and the full-bridge unfolding circuit is only used for switching the polarity of the output voltage. When the instantaneous output voltage is lower than the input voltage, the power switch of the high-gain boost converter remains in off state, and the full-bridge unfolding circuit is controlled by SPWM to step down the input voltage to the desired output voltage. This control method is called partial SPWM (P-SPWM), because the high-gain boost converter and the full-bridge unfolding circuit are sequentially and respectively controlled by high-frequency SPWM as the instantaneous output voltage varies. Generally, the following features of the proposed inverter are:

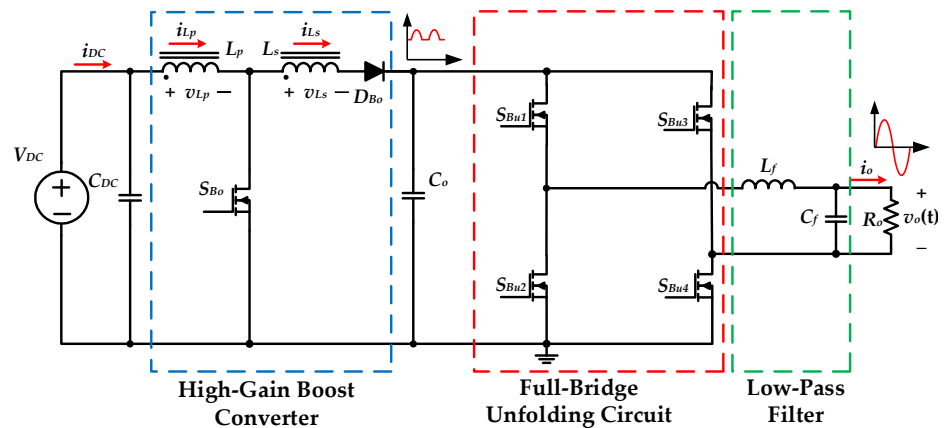
1. Because the high-gain boost converter and the full-bridge unfolding circuit perform high-frequency switching at different times, only one energy processing stage is required to generate the sinusoidal output voltage, which can effectively improve the conversion efficiency.
2. Magnetic coupling is adopted to increase the voltage gain of step-up so that the proposed inverter can be operated with utility of high voltage [19,20].
3. The full-bridge unfolding circuit is used to realize the step-down function so that additional series power switch is not required, which can reduce conduction losses.
4. The proposed inverter has both step-up and step-down capabilities, making it suitable for applications with a wide range of input voltage variations.



**Figure 3.** The grid-connected PV power system with the proposed high-efficiency inverter.

## 2. Circuit Configuration

Figure 4 shows the circuit configuration of the proposed high-gain inverter with magnetic coupling, in which  $V_{DC}$  is the input voltage, and  $v_o(t)$  is the output voltage. In this circuit, the first stage is a high-gain DC-DC boost converter that is controlled by P-SPWM to generate a rectified sine wave with unipolarity. It is formed mainly by the power switch  $S_{Bo}$ , the diode  $D_{Bo}$ , and the coupled inductor. The second stage is a full-bridge unfolding circuit that is controlled by P-SPWM to accomplish step-down function and switches the polarity of the rectified sine wave during step-up mode. The unfolding circuit is mainly composed of the switches  $S_{Bu1}$ ,  $S_{Bu2}$ ,  $S_{Bu3}$ , and  $S_{Bu4}$ , and a low-pass filter formed by the inductor  $L_f$  and the capacitor  $C_f$ .



**Figure 4.** The circuit configuration of the proposed high-gain inverter with magnetic coupling.

The proposed inverter can be operated in either step-up or step-down mode, depending on the levels of the input and output voltages. In step-down mode, the switch  $S_{Bo}$  remains in off state, and the diode  $D_{Bo}$  remains in the on state. The switches  $S_{Bu1}$  and  $S_{Bu2}$  are controlled by high-frequency SPWM and switch complementarily. The switches  $S_{Bu3}$  and  $S_{Bu4}$  switch complementarily with line frequency. Additionally, the low-pass filter is used to filter out the high-frequency components of the output voltage.

When the desired output voltage is higher than the input voltage, the proposed inverter enters step-up mode. In this mode, the switch  $S_{Bo}$  switches with the high-frequency SPWM control. The switches  $S_{Bu1}$ ,  $S_{Bu4}$  maintain conductance to transfer energy to the output side during the positive half-cycle, and the switches  $S_{Bu2}$ ,  $S_{Bu3}$  maintain cut-off. In the negative half-cycle, the roles of the switches  $S_{Bu1}$ ,  $S_{Bu4}$  and the switches  $S_{Bu2}$ ,  $S_{Bu3}$  are swapped so that the output voltage polarity can be switched.

The high-gain DC-DC boost converter and the full-bridge unfolding circuit do not perform high-frequency switching at the same time, which means that only one energy processing stage is required to convert a low DC voltage into the required AC voltage. Therefore, the conversion efficiency of the proposed inverter can be effectively improved.

### 3. Operation Principles

In this section, the detailed operating principles of the proposed inverter are addressed; the following assumptions are made to simplify the circuit analysis:

1. All circuit elements are ideal.
2. The circuit operates in steady state.
3. Inductor currents are continuous.
4. The dead time of power switches is extremely short and can be ignored.

Figure 5 presents the timing diagram of the proposed high-gain inverter within one cycle of output voltage  $v_o(t)$ , where  $V_M$  is the amplitude of  $v_o(t)$ ,  $T_o$  is the period of  $v_o(t)$ , and  $d_{Bo}(t)$ ,  $d_{Bu1}(t)$ , and  $d_{Bu3}(t)$  are the duty ratios of switches  $S_{Bo}$ ,  $S_{Bu1}$ , and  $S_{Bu3}$ . Additionally,  $V_{GS,Bo}(t)$ ,  $V_{GS,Bu1}(t)$ ,  $V_{GS,Bu2}(t)$ ,  $V_{GS,Bu3}(t)$ , and  $V_{GS,Bu4}(t)$  are the conceptual gate-driving signals of all power switches.

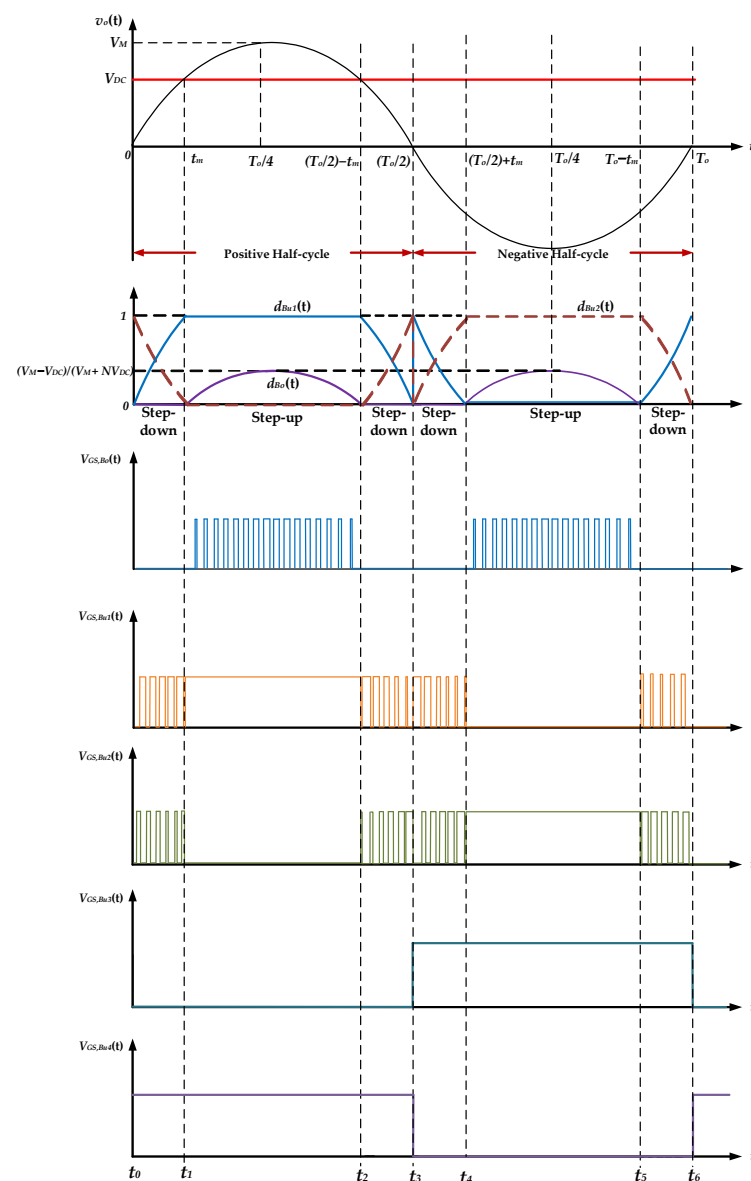


Figure 5. The timing diagram of the proposed high-gain inverter.

The output voltage  $v_o(t)$  is sinusoidal and can be divided into positive and negative half-cycles. When the input voltage  $V_{DC}$  is higher than the absolute value of the instantaneous output voltage  $v_o(t)$ , the inverter operates in step-down mode; otherwise, the inverter

operates in step-up mode. The operation principles of the negative half-cycle are the same as those of the positive half-cycle, except that the driving signals of switches  $S_{Bu1}$  and  $S_{Bu2}$  are swapped and the driving signals of switches  $S_{Bu3}$  and  $S_{Bu4}$  are swapped. In the following, the operation principles of the proposed inverter are illustrated with respect to the positive half-cycle.

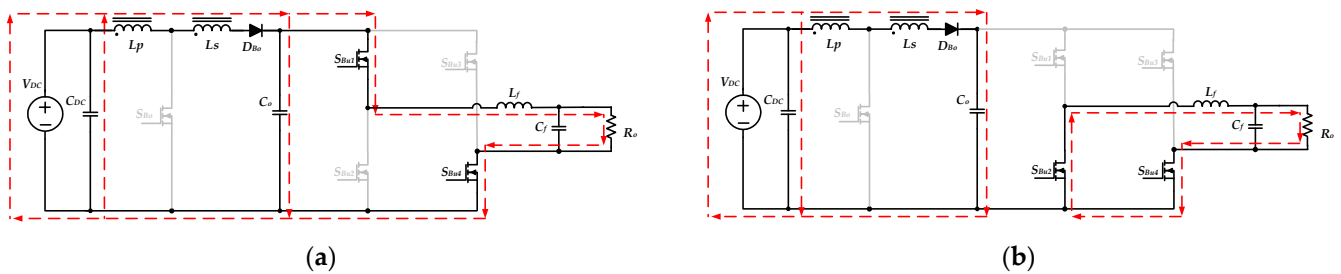
### 3.1. Step-Down Mode

During the positive half-cycle ( $0 < t < T_o/2$ ), the switch  $S_{Bu4}$  keeps turning on, and the switch  $S_{Bu3}$  keeps turning off. When the input voltage  $V_{DC}$  is higher than the output voltage  $v_o(t)$ , the inverter operates in step-down mode. In this mode, the switch  $S_{Bo}$  keeps turning off, and its duty ratio  $d_{Bo}(t)$  is zero. The coupled inductors  $L_p$  and  $L_s$  are connected in series as an input filter. The full-bridge unfolding circuit is controlled by unipolar SPWM. The gate driving signals of the switches  $S_{Bu1}$ ,  $S_{Bu2}$  are complementary, and their duty ratios can be expressed as follows:

$$d_{Bu1}(t) = \frac{V_M \cdot \sin \omega t}{V_{DC}}, \quad (1)$$

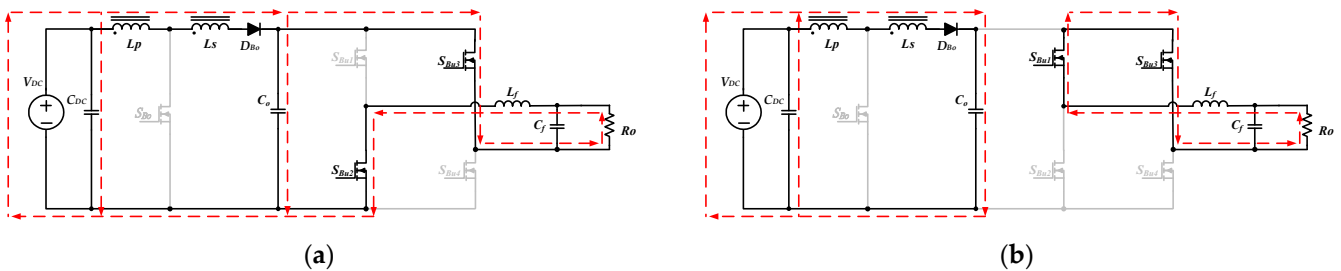
$$d_{Bu2}(t) = 1 - \frac{V_M \cdot \sin \omega t}{V_{DC}}, \quad (2)$$

within one switching period, when  $S_{Bu1}$  is turned on, and  $S_{Bu2}$  is turned off, the input voltage  $V_{DC}$  simultaneously charges the inductor  $L_f$  and provides the energy required for the output load through the diode  $D_{Bo}$ . The equivalent circuit is shown in Figure 6a. When  $S_{Bu1}$  is turned off, and  $S_{Bu2}$  is turned on, the inductor  $L_f$  releases energy to the output load. The equivalent circuit is shown in Figure 6b.



**Figure 6.** The equivalent circuits of the inverter operating in step-down mode during the positive half-cycle: (a)  $S_{Bu1}$  on, and  $S_{Bu2}$  off; (b)  $S_{Bu1}$  off, and  $S_{Bu2}$  on.

Moreover, during the negative half-cycle ( $T_o/2 < t < T_o$ ), the switches  $S_{Bu3}$  and  $S_{Bu4}$  exchange their operation states, and the switch  $S_{Bo}$  keeps turning off. The input voltage  $V_{DC}$  charges the inductor  $L_f$  and provides energy to the output load when the switch  $S_{Bu2}$  turns on, and the equivalent circuit is shown in Figure 7a. When the switch  $S_{Bu2}$  is turned off and the switch  $S_{Bu1}$  is turned on, the inductor  $L_f$  releases energy to the output load. Figure 7b shows the equivalent circuit.



**Figure 7.** The equivalent circuits of the inverter operating in step-down mode during the negative half-cycle: (a)  $S_{Bu1}$  off and  $S_{Bu2}$  on; (b)  $S_{Bu1}$  on and  $S_{Bu2}$  off.

### 3.2. Step-Up Mode

When the instantaneous output voltage  $v_o(t)$  is higher than the input voltage  $V_{DC}$ , the proposed inverter enters step-up mode. During the positive half-cycle ( $0 < t < T_o/2$ ), the switches  $S_{Bu1}$  and  $S_{Bu4}$  keep turning on, and the switches  $S_{Bu2}$  and  $S_{Bu3}$  keep turning off. The switch  $S_{Bo}$  operates with high-frequency SPWM control. Figure 8 shows the current waveforms of the coupled inductor operating in continuous current mode (CCM), in which  $T$  is the switching period. At the initial time  $t = 0$ , the switch  $S_{Bo}$  turns on to force the diode  $D_{Bo}$  to be off, and the capacitor  $C_o$  provides energy for the output load. Figure 9a shows the equivalent circuit of the switch  $S_{Bo}$  turning on.

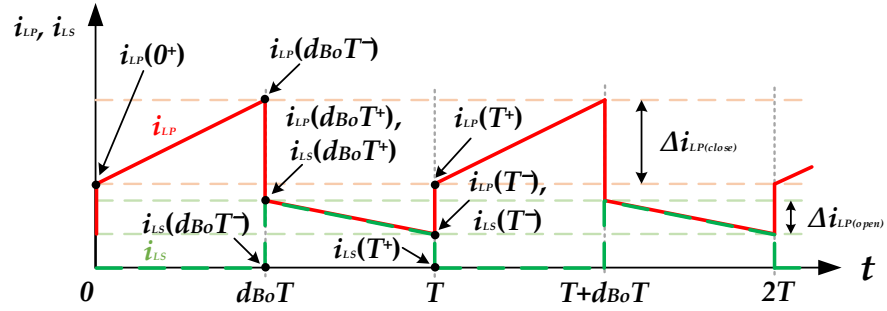


Figure 8. The current waveforms of the coupled inductor operating in CCM.

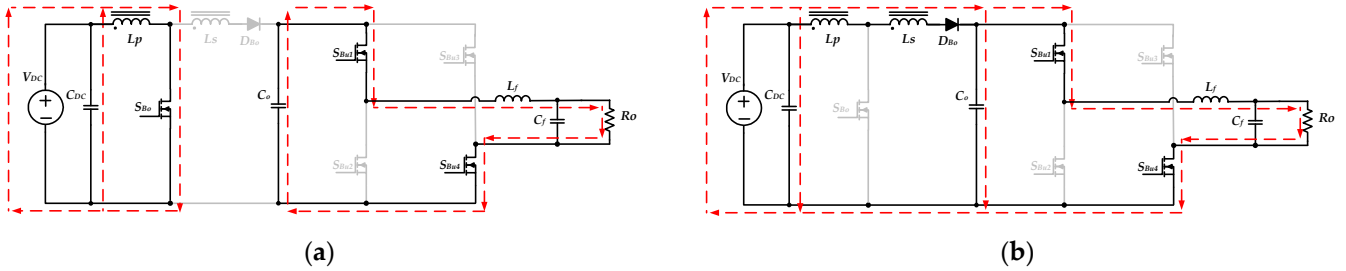


Figure 9. The equivalent circuits of the inverter operating in step-up mode during the positive half-cycle: (a)  $S_{Bo}$  on; (b)  $S_{Bo}$  off.

The voltage across the primary winding of the coupled inductor,  $v_{LP}$ , is equal to the input voltage  $V_{DC}$ , and can be expressed as follows:

$$v_{LP} = V_{DC} = L_P \frac{di_{LP}}{dt} \quad (3)$$

According to Equation (3), the amount of current change in the primary inductor  $L_P$  during the on state of the switch  $S_{Bo}$  can be expressed as

$$\Delta i_{LP(close)} = \frac{V_{DC} \cdot d_{Bo} T}{L_P}, \quad (4)$$

where  $d_{Bo}$  is the duty ratio of  $S_{Bo}$ . In Figure 8,  $i_{LP}(0^+)$  is the initial value of the primary inductor current, so the end value  $i_{LP}(d_{Bo} T^-)$  of the on state of the switch  $S_{Bo}$  can be expressed as

$$i_{LP}(d_{Bo} T^-) = i_{LP}(0^+) + \frac{V_{DC} \cdot d_{Bo} T}{L_P}, \quad (5)$$

Assuming that the coupled inductor is an ideal element (coupling coefficient  $k = 1$ ), the mutual inductance  $M$  can be expressed as follows:

$$M = \sqrt{L_P L_S}, \quad (6)$$

In addition, if the turn ratio between primary and secondary windings is defined as  $1/N$ , the relationship between primary inductor  $L_P$  and secondary inductor  $L_S$  can be expressed as follows:

$$L_S = N^2 L_P, \quad (7)$$

Substituting Equation (7) into Equation (6) yields the following equation:

$$M = N L_P, \quad (8)$$

At the time  $t = d_{B0} T^-$ , the switch  $S_{B0}$  turns off, and the diode  $D_{B0}$  is forced into the on state. The primary inductor  $L_P$  is connected in series with the secondary inductor  $L_S$  to release energy. The coupled inductor and the input voltage  $V_{DC}$  simultaneously transfer energy to the output and charge the capacitor  $C_o$ , as shown in Figure 9b. Since the primary and the secondary inductor currents are equal, the primary inductor current  $i_{LP}(d_{B0} T^+)$  after switch  $S_{B0}$  turns off can be determined by the law of energy conservation as follows:

$$i_{LP}(d_{B0} T^+) = i_{LS}(d_{B0} T^+) = \frac{1}{(1+N)} \times i_{LP}(d_{B0} T^-), \quad (9)$$

When the switch  $S_{B0}$  is in the off state, the voltage across the coupled inductor can be expressed as

$$v_{LP} + v_{LS} = (V_{DC} - v_o(t)) = (L_P + L_S + 2M) \times \frac{di_{LP}}{dt}, \quad (10)$$

Substituting Equations (7) and (8) into Equation (10), it can be simplified as follows:

$$(V_{DC} - v_o(t)) = (1+N)^2 L_P \times \frac{di_{LP}}{dt}, \quad (11)$$

During the time between  $d_{B0} T$  and  $T$ , the inductor current decreases linearly due to the negative voltage across the coupled inductor in Equation (11). The amount of inductor current change during this time interval can be expressed as follows:

$$\Delta i_{LP(open)} = \Delta i_{LS(open)} = \frac{(V_{DC} - v_o(t)) \cdot (1 - d_{B0}) \times T}{(1+N)^2 \times L_P}, \quad (12)$$

From Equations (9) and (12), the minimum current on the primary winding of the coupled inductor  $i_{LP}(T^-)$  can be expressed as follows:

$$i_{LP}(T^-) = i_{LP}(d_{B0} T^+) + \Delta i_{LP(open)} = \frac{i_{LP}(d_{B0} T^-)}{(1+N)} + \frac{(V_{DC} - v_o(t)) \cdot (1 - d_{B0}) \times T}{(1+N)^2 L_P}, \quad (13)$$

Substituting Equation (5) into Equation (13), the following equation is obtained:

$$i_{LP}(T^-) = \frac{1}{(1+N)} \left[ i_{LP}(0^+) + \frac{V_{DC} \cdot d_{B0} T}{L_P} \right] + \frac{(V_{DC} - v_o(t))(1 - d_{B0}) T}{(1+N)^2 L_P}, \quad (14)$$

At the time  $t = T$ , the switch  $S_{B01}$  turns on, and the primary inductor current can be obtained by the law of energy conservation as follows:

$$i_{LP}(T^+) = (1+N) \times i_{LP}(T^-), \quad (15)$$

In steady-state operation, since the current  $i_{LP}(T^+)$  is equal to  $i_{LP}(0^+)$ , the output voltage gain can be obtained by substituting Equation (15) into Equation (14) as follows:

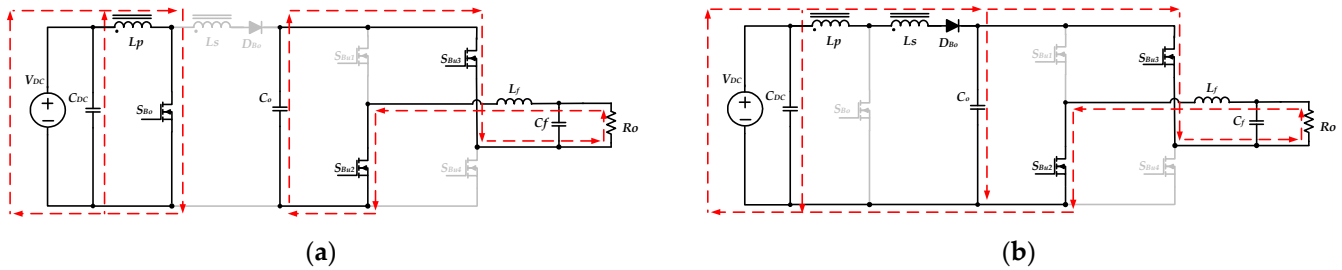
$$\frac{v_o(t)}{V_{DC}} = \frac{1 + N d_{B0}(t)}{1 - d_{B0}(t)}, \quad (16)$$



By expressing the output voltage  $v_o(t)$  as  $V_M \cdot \sin \omega t$ , the duty ratio of the switch  $S_{Bo}$  in step-up mode can be obtained as follows:

$$d_{Bo}(t) = \frac{V_M \cdot \sin \omega t - V_{DC}}{V_M \cdot \sin \omega t + NV_{DC}}, \quad (17)$$

Moreover, when the proposed inverter operates in step-up mode during the negative half-cycle ( $T_0/2 < t < T_0$ ), the switches  $S_{Bu1}$ ,  $S_{Bu4}$  are in the off state, and the switches  $S_{Bu2}$ ,  $S_{Bu3}$  are in the on state. The switch  $S_{Bo}$  keeps switching with high frequency, and the operation principles are the same as those for the positive half-cycle. The equivalent circuits for when switch  $S_{Bo}$  is turning on and off are shown in Figure 10a,b, respectively.



**Figure 10.** The equivalent circuits of the inverter operating in step-up mode during the negative half cycle: (a)  $S_{Bo}$  on; (b)  $S_{Bo}$  off.

According to the analysis above, the status of all switching elements is listed in Table 1. It can be clearly understood that the proposed inverter has only two power elements switching with high frequency in both step-down and step-up modes; therefore, switching losses can be reduced to improve the efficiency.

**Table 1.** Status of switching elements of the proposed high-gain inverter.

Element	Positive Half-Cycle ( $0 < t < T_0/2$ )		Negative Half-Cycle ( $T_0/2 < t < T_0$ )	
	Step-Down Mode	Step-Up Mode	Step-Down Mode	Step-Up Mode
$S_{Bu1}$	Switching with $d_{Bu1}(t)$	Always on	Switching with $(1 - d_{Bu1}(t))$	Always off
$S_{Bu2}$	Switching with $(1 - d_{Bu1}(t))$	Always off	Switching with $d_{Bu1}(t)$	Always on
$S_{Bu3}$	Always off	Always off	Always on	Always on
$S_{Bu4}$	Always on	Always on	Always off	Always off
$S_{Bo}$	Always off	Switching with $d_{Bo}(t)$	Always off	Switching with $d_{Bo}(t)$
$D_{Bo}$	Always on	Switching with $(1 - d_{Bo}(t))$	Always on	Switching with $(1 - d_{Bo}(t))$

#### 4. Design Considerations

To explain how to determine the component parameters, the design considerations of the coupled inductor, the semiconductor components, and the output filter are addressed in this section.

##### 4.1. Boundary Condition of the Coupled Inductor

If the coupled inductor operates in boundary conduction mode (BCM), the minimum current on the primary side  $i_{LP}(T^-)$ , as shown in Figure 8, will reach zero just before the switch  $S_{Bo}$  enters the next switching cycle. In BCM, the average inductor current  $I_{LB}$  within one high-frequency cycle can be calculated as follows:

$$I_{LB} = \frac{1}{2} \Delta i_{LP(\text{close})} \times d_{Bo} + \frac{1}{2} \Delta i_{LP(\text{open})} \times (1 - d_{Bo}) \quad (18)$$



The amount of current increase and decrease on the primary winding in BCM have the following relationship:

$$\Delta i_{LP(\text{open})} = \frac{\Delta i_{LP(\text{close})}}{(1 + N)} \quad (19)$$

Substituting Equation (19) into Equation (18) gives

$$I_{LB} = \frac{\Delta i_{LP(\text{close})} \times (1 + Nd_{Bo})}{2(1 + N)} \quad (20)$$

Substituting Equation (4) into Equation (20) yields

$$I_{LB} = \frac{V_{DC} \times d_{Bo} T \times (1 + Nd_{Bo})}{2L_P(1 + N)} \quad (21)$$

Since the average current  $I_{LB}$  is equal to the instantaneous input current, the boundary condition  $I_{o(B)}$  of the instantaneous output current can be obtained from Equations (16) and (21), and the relationship of power balance as follows:

$$I_{o(B)} = \frac{V_{DC} \times d_{Bo} T \times (1 - d_{Bo})}{2L_P(1 + N)} \quad (22)$$

When the instantaneous output current  $i_o(t)$  is equal to  $I_{o(B)}$ , the proposed inverter operates in BCM, and the boundary inductance of the primary winding  $L_{P(B)}$  can be obtained as follows:

$$L_{P(B)} = \frac{V_{DC} \times d_{Bo} T \times (1 - d_{Bo})}{2 \times i_o(t) \times (1 + N)} \quad (23)$$

#### 4.2. Voltage Stresses of the Power Components

When the switch  $S_{Bo}$  turns off in step-up mode, as shown in Figure 9b, the maximum voltage stress on  $S_{Bo}$  occurs at the peak output voltage, and can be expressed as follows:

$$V_{ds, Bo(\text{Max})} = V_{DC} + \frac{V_M - V_{DC}}{1 + N} \quad (24)$$

When the switch  $S_{Bo}$  turns on, the diode  $D_{Bo}$  is forced to turn off, as shown in Figure 9a. The maximum voltage stress on  $D_{Bo}$  also occurs at the peak output voltage, and can be expressed as follows:

$$V_{D-Bo(\text{Max})} = NV_{DC} + V_M, \quad (25)$$

The maximum voltage stress on both the capacitor  $C_o$  and the capacitor  $C_f$  is the peak output voltage  $V_M$ , and can be expressed as follows:

$$V_{Co(\text{Max})} = V_{Cf(\text{Max})} = V_M, \quad (26)$$

According to Figures 9 and 10, the voltage stresses on the switches  $S_{Bu1}$ ,  $S_{Bu2}$ ,  $S_{Bu3}$  and  $S_{Bu4}$  are equal to the voltage across the capacitor  $C_o$ . Therefore, the maximum voltage stresses on these four switches of the unfolding circuit can be expressed as follows:

$$V_{ds, Bu1(\text{Max})} = V_{ds, Bu2(\text{Max})} = V_{ds, Bu3(\text{Max})} = V_{ds, Bu4(\text{Max})} = V_M. \quad (27)$$

#### 4.3. Current Stresses of the Power Components

When the inverter operates in step-up mode and the switch  $S_{Bo}$  turns on, the current in the primary winding of the coupled inductor rises. When the output voltage  $v_o$  reaches the peak  $V_M$ , the current stress on the primary winding reaches its maximum, as indicated below:

$$I_{LP(\text{Max})} = \frac{V_M (1 + Nd_{Bo})}{R(1 - d_{Bo})} + \frac{V_{DC} d_{Bo} T}{L_P} \quad (28)$$

When the switch  $S_{Bo}$  turns off, the diode  $D_{Bo}$  is forward biased. The primary and secondary windings are connected in series to the discharge, so the maximum current stress of the secondary winding can be known from Equations (9) and (28), as follows:

$$I_{LS(\text{Max})} = I_{LP(\text{Max})} \times \frac{1}{(1+N)} = \left[ \frac{V_M (1 + Nd_{Bo})}{R(1 - d_{Bo})} + \frac{V_{DC} d_{Bo} T}{L_P} \right] \times \frac{1}{(1+N)} \quad (29)$$

In step-up mode, the maximum current stress on the switch  $S_{Bo1}$  is the same as that of the primary winding, expressed as follows:

$$I_{ds, Bo(\text{Max})} = I_{LP(\text{Max})} = \frac{V_M (1 + Nd_{Bo})}{R(1 - d_{Bo})} + \frac{V_{DC} d_{Bo} T}{L_P} \quad (30)$$

Additionally, when the diode  $D_{Bo}$  is conducting, its maximum current stress is the same as that of the secondary winding, expressed as follows:

$$I_{DBo(\text{Max})} = I_{LS(\text{Max})} = \left[ \frac{V_M (1 + Nd_{Bo})}{R(1 - d_{Bo})} + \frac{V_{DC} d_{Bo} T}{L_P} \right] \times \frac{1}{(1+N)} \quad (31)$$

Assuming that the output high-frequency current ripple can be completely filtered out and ignored, the current stresses of the switches  $S_{Bu1}$ ,  $S_{Bu2}$ ,  $S_{Bu3}$ ,  $S_{Bu4}$ , and the inductor  $L_S$  are the same as the output current, and their maximum values can be expressed as follows:

$$I_{ds, Bu1(\text{Max})} = I_{ds, Bu2(\text{Max})} = I_{ds, Bu3(\text{Max})} = I_{ds, Bu4(\text{Max})} = I_{Lf(\text{Max})} = \frac{V_M}{R} \quad (32)$$

#### 4.4. Selection of the Output Filter

When the converter operates in step-down mode, the full-bridge unfolding circuit is controlled by SPWM, and the inductor  $L_f$  is used for energy storage. The boundary inductance of  $L_f$  can be expressed as follows:

$$L_{f(B)} = \frac{R \times (1 - d_{Bu1}) T}{2} \quad (33)$$

The inverter can operate in the CCM of step-down mode by selecting the inductance of  $L_f$  to be greater than the boundary inductance  $L_{f(B)}$ .

In addition, the inductor  $L_f$  and the capacitor  $C_f$  are used as a low-pass filter in step-up mode, and its cut-off frequency  $f_c$  can be expressed as:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \quad (34)$$

Once the inductance of  $L_f$  is determined, the capacitance of  $C_f$  can be designed on the basis of Equation (34) according to the desired cut-off frequency.

## 5. Experimental Results

To verify the feasibility of the proposed high-gain inverter, an experimental prototype was built according to the electrical specifications listed in Table 2. The prototype was tested using input voltages between 100 V and 200 V, in order to verify that the proposed inverter is suitable for PV panels with wide-range voltage variations. Additionally, the output voltage was selected as 220 V<sub>rms</sub> in order to prove the high boosting capacity of the proposed inverter.

**Table 2.** Electrical specifications of the proposed high-gain inverter.

Electrical Specifications	
Input voltage, $V_{DC}$	100–200 (V)
Output voltage, $v_o$	220 (V <sub>rms</sub> )
Line frequency, $f_o$	60 (Hz)
Output power, $P_o$	500 (W)
Switching frequency, $f$	20 (kHz)
Switching period, $T$	50 ( $\mu$ s)

On the basis of the output voltage of 220 V<sub>rms</sub> and the output power of 500 W, the equivalent load resistance ( $R$ ) can be calculated as being 96.8  $\Omega$ . By selecting the BCM of step-down mode at an instantaneous output current  $i_o(t)$  of 0.6 A and an input voltage  $V_{DC}$  of 100 V, the boundary inductance of  $L_f$  can be calculated as being about 1 mH using Equation (33). By selecting a cut-off frequency  $f_c$  of 5 kHz, the capacitance of  $C_f$  can be obtained using Equation (34) as 1  $\mu$ F.

To ensure that the maximum duty ratio is below 0.5, the turn ratio  $N$  is chosen as 1.5. At the input voltage of 100 V and the peak output voltage of 312 V, the maximum duty ratio can be calculated using Equation (17) as being around 0.46. Additionally, the condition of peak output current and 40% load is selected to operate in BCM, thus avoiding excessive values of primary inductance and the saturation of the magnetic core. From Equation (23), the boundary inductance of the primary winding  $L_{P(B)}$  can be obtained as being about 193  $\mu$ H. In the actual design, 200  $\mu$ H is used as the primary inductance, and the secondary inductance of 450  $\mu$ H can be obtained from Equation (7). Based on the previous design and calculations, the selected component parameters of the experimental prototype are summarized in Table 3.

**Table 3.** Component parameters of the proposed high-gain inverter.

Component Parameters	
MOSEET, $S_{B0}$	SPW47N60C3 (650 V/47 A)
MOSEETs, $S_{B11}$ , $S_{B12}$ , $S_{B13}$ and $S_{B14}$	IRFP460 (500 V/20 A)
Diode, $D_{B0}$	C4D10120A (1200 V/14 A)
Turn Ratio, $N$	1.5
Primary Inductance, $L_P$	200 $\mu$ H
Secondary Inductance, $L_S$	450 $\mu$ H
Capacitor, $C_o$	1 $\mu$ F
Inductor, $L_f$	1 mH
Capacitor, $C_f$	1 $\mu$ F

Figure 11 shows the measured waveforms of the output voltage  $v_o(t)$  and the output current  $i_o(t)$  under the condition of 100 V input voltage and 500 W output power. It can be seen that the output voltage and current are both near-ideal sinusoidal waves with low distortion, verifying that the proposed circuit is indeed capable of converting DC input to AC output.

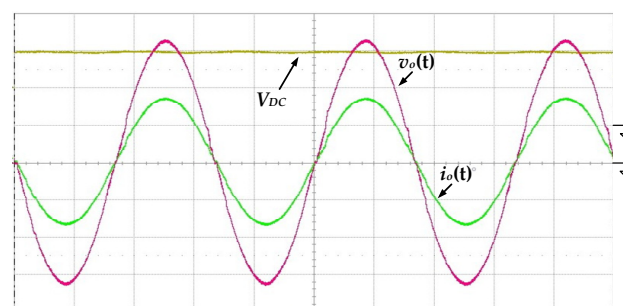
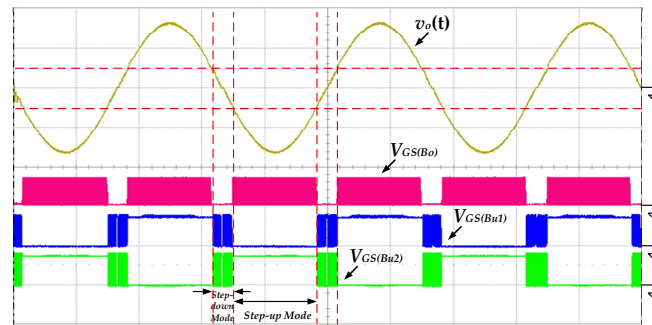
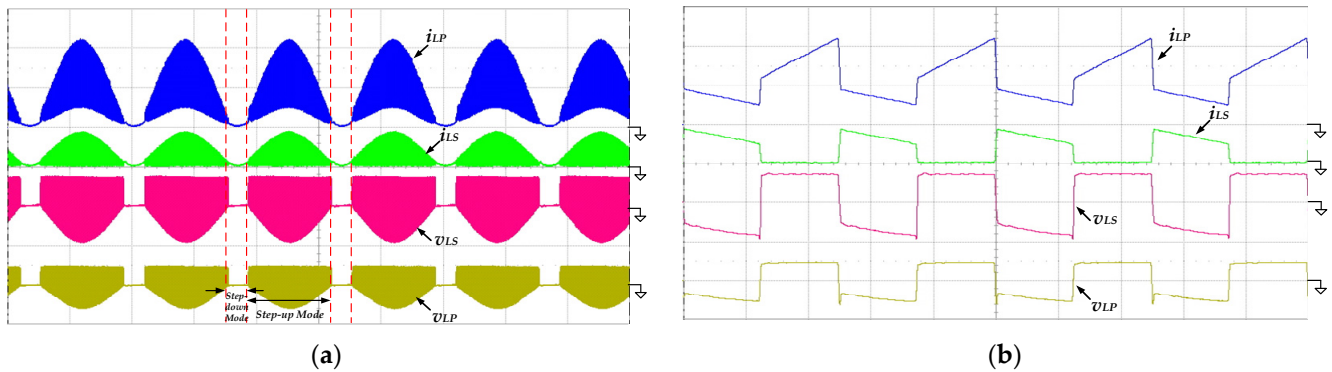
**Figure 11.** The measured waveforms of the output voltage  $v_o(t)$  and output current  $i_o(t)$  at 100 V input voltage and 500 W output load ( $v_o(t)$ : 100 V/div;  $i_o(t)$ : 2 A/div;  $V_{DC}$ : 100 V/div; time: 5 ms/div).

Figure 12 shows the measured waveforms of the gate-driving signals of the switches  $S_{B0}$ ,  $S_{Bu1}$  and  $S_{Bu2}$  under the condition of 100 V input voltage and 500 W output power. When the absolute output voltage  $|v_o(t)|$  is lower than 100 V, the proposed inverter operates in step-down mode. The switches  $S_{Bu1}$  and  $S_{Bu2}$  switch with high frequency, and the switch  $S_{B0}$  remains in the off state. Conversely, the proposed inverter operates in step-up mode. The switch  $S_{B0}$  is switching with high frequency, and the switches  $S_{Bu1}$  and  $S_{Bu2}$  perform low-frequency switching only to switch the polarity of output voltage.



**Figure 12.** The measured waveforms of the gate-driving signals at 100 V input voltage and 500 W output load ( $v_o(t)$ : 200 V/div;  $V_{GS(B0)}$ ,  $V_{GS(Bu1)}$ ,  $V_{GS(Bu2)}$ : 20 V/div; time: 5 ms/div).

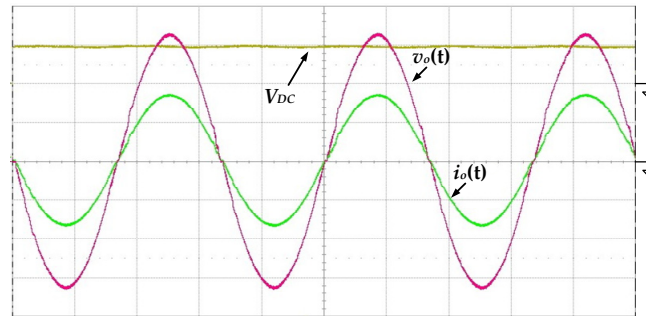
Figure 13 shows the measured waveforms of the currents and the voltages of the coupled inductor. From Figure 13a, the coupled inductor functions as a filter in step-down mode, so that the voltages  $v_{LP}$  and  $v_{LS}$  are almost zero. When the inverter operates in step-up mode, the voltages  $v_{LP}$  and  $v_{LS}$  vary with high-frequency switching of the switch  $S_{B0}$ . Figure 13b shows the zoomed-in waveforms at the peak of the output voltage  $v_o(t)$ . The inductor current  $i_{LP}$  is operated in CCM, verifying previous theoretical calculations and parametric design. Additionally, the inductor currents  $i_{LP}$  and  $i_{LS}$  are equal during the switch  $S_{B0}$  turning off, because the primary and secondary inductors discharge in series.



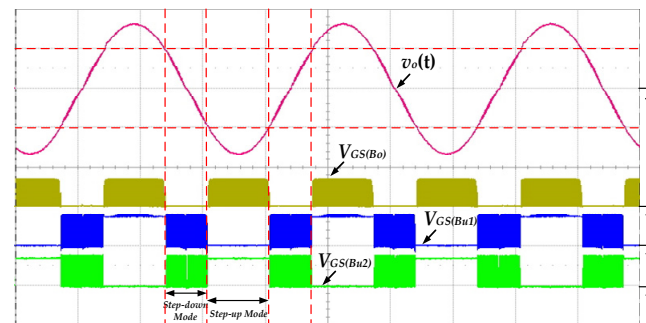
**Figure 13.** The measured waveforms of the inductor currents  $i_{LP}$ ,  $i_{LS}$  and the inductor voltages  $v_{LP}$  and  $v_{LS}$  at 100 V input voltage, 500 W output load and (a) low-frequency line cycle ( $v_{LP}$ ,  $v_{LS}$ : 200 V/div;  $i_{LP}$ ,  $i_{LS}$ : 10 A/div; time: 5 ms/div); (b) high-frequency switching cycle ( $v_{LP}$ ,  $v_{LS}$ : 200 V/div;  $i_{LP}$ ,  $i_{LS}$ : 10 A/div; time: 20  $\mu$ s/div).

To verify that the proposed inverter is suitable for a wide range of input voltages, the input voltage is increased to 200 V for testing. Figure 14 shows the measured waveforms of the output voltage  $v_o(t)$  and the output current  $i_o(t)$  under the condition of 200 V input voltage and 500 W output power. Both the output voltage and current can be maintained in low-distortion sine waves, which proves that the proposed inverter is suitable for a wide range of input voltages. The gate-driving signals at 200 V input voltage are shown in Figure 15. The control strategy is similar to that at 100 V input. Due to the higher input

voltage, the time interval becomes longer for the step-down mode and shorter for the step-up mode.

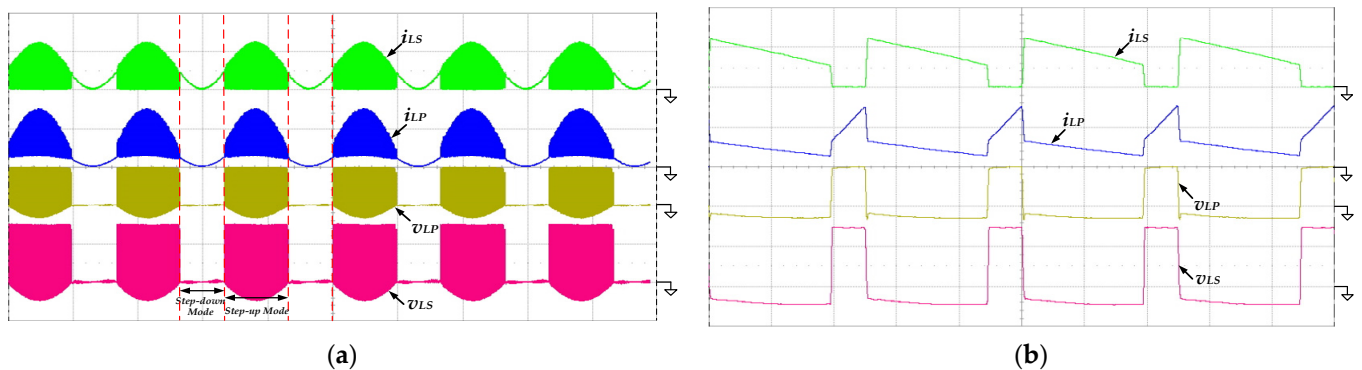


**Figure 14.** The measured waveforms of the output voltage  $v_o(t)$  and output current  $i_o(t)$  at 200 V input voltage and 500 W output load ( $v_o(t)$ : 100 V/div;  $i_o(t)$ : 2 A/div;  $V_{DC}$ : 200 V/div; time: 5 ms/div).



**Figure 15.** The measured waveforms of the gate-driving signals at 200 V input voltage and 500 W output load ( $v_o(t)$ : 200 V/div;  $V_{GS(B0)}$ ,  $V_{GS(Bu1)}$ ,  $V_{GS(Bu2)}$ : 20 V/div; time: 5 ms/div).

Figure 16 presents the measured waveforms of the currents and the voltages of the coupled inductor. As shown in Figure 16a, the coupled inductor is still used as a filter in step-down mode, and the inductor voltages are almost zero. The waveforms are zoomed-in at the peak of the output voltage  $v_o(t)$  and shown in Figure 13b. Due to the higher input voltage, the duty ratio of the switch  $S_{B0}$  is reduced, and the charging time of the primary inductor is shorter. During the switch  $S_{B0}$  turning off, the inductor currents  $i_{LP}$  and  $i_{LS}$  are still the same, proving that the primary and secondary inductors are discharging in series to increase voltage gain.

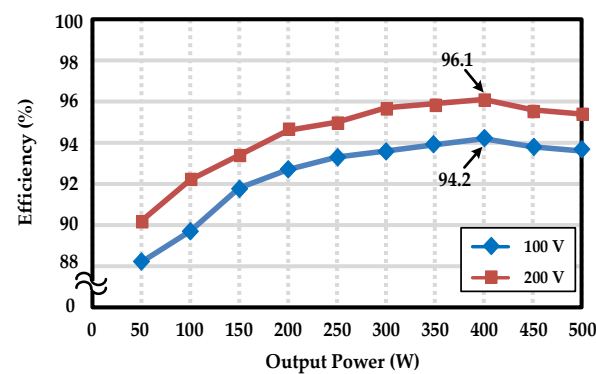


**Figure 16.** The measured waveforms of the inductor currents  $i_{LP}$ ,  $i_{LS}$  and the inductor voltages  $v_{LP}$  and  $v_{LS}$  at 200 V input voltage, 500 W output load and (a) low-frequency line cycle ( $v_{LP}$ ,  $v_{LS}$ : 200 V/div;  $i_{LP}$ : 10 A/div;  $i_{LS}$ : 5 A/div; time: 5 ms/div); (b) high-frequency switching cycle ( $v_{LP}$ ,  $v_{LS}$ : 200 V/div;  $i_{LP}$ : 10 A/div;  $i_{LS}$ : 5 A/div; time: 20  $\mu$ s/div).

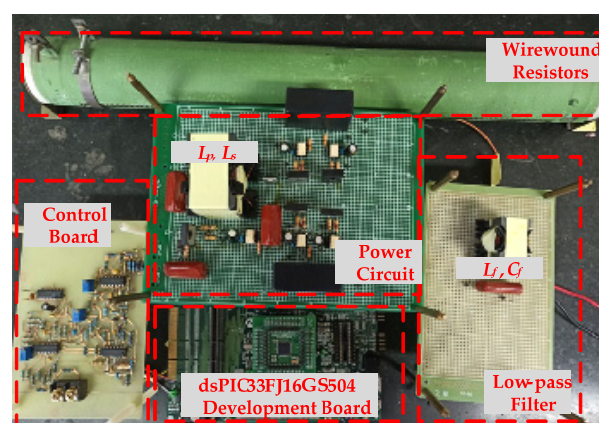
The total harmonic distortion (T.H.D.) and odd-order harmonics of the output voltage at full load are measured and listed in Table 4. All measured harmonics comply with the standard of EN6100-3-2 Class C. The efficiency curves of the proposed inverter are illustrated in Figure 17. As can be seen, the conversion efficiencies reach up to 96.1% at 200V input voltage and up to 94.2% at 100V input voltage, verifying that the proposed inverter can indeed achieve high efficiency. Additionally, Figure 18 shows a photograph of the prototype hardware used for the experimental measurements, in which the dsPIC33FJ16GS504 development board is used to generate the P-SPWM driving signals, and a wire-wound resistor is used as a testing load.

**Table 4.** The total harmonic distortion and odd-order harmonics of the output voltages.

Harmonic	100 V	200 V
T.H.D.	1.73%	1.13%
3rd Harmonic	1.57%	0.87%
5th Harmonic	0.36%	0.29%
7th Harmonic	0.24%	0.33%
9th Harmonic	0.11%	0.17%
11th Harmonic	0.07%	0.12%



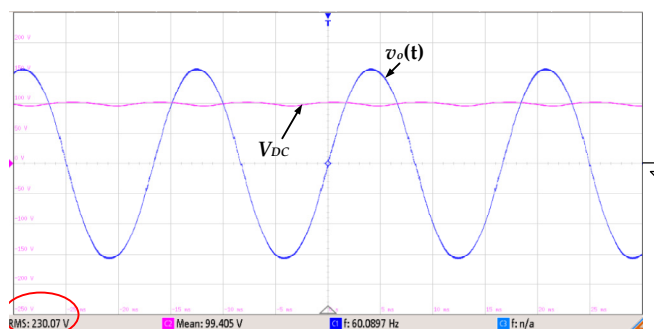
**Figure 17.** Measured efficiency curves of the proposed inverter.



**Figure 18.** Photograph of the experimental prototype.

To further verify that the proposed inverter has the ability to adjust with utility line voltage fluctuations, Figure 19 shows the experimental waveforms at 230 V<sub>rms</sub> output and 100 V input. It can be seen that the output voltage is still a near-ideal sinusoidal wave with low distortions. Its measured T.H.D. is 1.75%, which is slightly higher than that of 220 V<sub>rms</sub> output.





**Figure 19.** The experimental waveforms of the output voltage  $v_o(t)$  and input voltage  $V_{DC}$  at 230 V<sub>rms</sub> output and 100 V input ( $v_o(t)$ : 100 V/div;  $V_{DC}$ : 50 V/div; time: 5 ms/div).

## 6. Conclusions

A high-gain and high-efficiency inverter with magnetic coupling was successfully developed and implemented. The digital signal processor dsPIC33FJ16GS504 was used to generate the gate-driving signals of the proposed inverter, which can simplify the complexity of the control circuit and improve the reliability. As the instantaneous output voltage changes, the proposed circuit sequentially operates in step-down and step-up modes. In each operation mode, only one energy processing is required to obtain the desired output voltage. In addition, to significantly reduce switching losses, conversion efficiency can be effectively improved because part of the energy is delivered directly to the output load. Additionally, by adding a coupled inductor to the boost circuit, the voltage gain of the proposed inverter can be increased, so that it is suitable for applications with low input voltage.

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