

Article

A 20–44 GHz Wideband LNA Design Using the SiGe Technology for 5G Millimeter-Wave Applications

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Abstract: This paper presents the design and implementation of a low-noise amplifier (LNA) for millimeter-wave (mm-Wave) 5G wireless applications. The LNA was based on a common-emitter configuration with cascode amplifier topology using an IHP's 0.13 μm Silicon Germanium (SiGe) heterojunction bipolar transistor (HBT) whose f_T/f_{MAX} /gate-delay is 360/450 GHz/2.0 ps, utilizing transmission lines for simultaneous noise and input matching. A noise figure of 3.02–3.4 dB was obtained for the entire wide bandwidth from 20 to 44 GHz. The designed LNA exhibited a gain (S_{21}) greater than 20 dB across the 20–44 GHz frequency range and dissipated 9.6 mW power from a 1.2 V supply. The input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) were below -10 dB, and reverse isolation (S_{12}) was below -55 dB for the 20–44 GHz frequency band. The input 1 dB (P1dB) compression point of -18 dBm at 34.5 GHz was obtained. The proposed LNA occupies only a 0.715 mm^2 area, with input and output RF (Radio Frequency) bond pads. To the authors' knowledge, this work evidences the lowest noise figure, lowest power consumption with reasonable highest gain, and highest bandwidth attained so far at this frequency band in any silicon-based technology.

Keywords: mm-wave; LNA; SiGe HBT; 5G sub-system



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1. Introduction

Recent technological advancement has made 5G deployment a reality, promoting the growth of mobile data with a wide range of RF (radio frequency) connectivity solutions. The lower lag time in 5G networks compared to that of previous ones has brought in a paradigm transformation in consumer needs, thus enabling new applications. In addition, 5G systems will be tremendously fast—as much as 10 to 20 times faster than the fastest systems of today. The ever-increasing utilization of video in any setting, from social media posts and on-demand movies to video communications and security monitoring cameras, augments the need for speed in mobile systems. Furthermore, most microwave and millimeter-wave (mm-Wave) receivers have a low-noise amplifier (LNA) as the first component at the front ends. The LNA determines the performance of mm-Wave and RF receivers. Primarily, the LNA is responsible for amplifying a signal while injecting as little noise into the signal as possible. The silicon germanium (SiGe) heterojunction bipolar transistor (HBT) has the characteristics of producing very low noise and high gain over a wide bandwidth. Due to these characteristics, SiGe HBTs have seamlessly improved and

presently compete with GaN and GaAs HEMTs for low-noise amplification. Hence, SiGe HBTs allow LNA integration on a single chip for mm-wave 5G sub-systems.

Earlier work focused on bandwidth extension techniques using shunt and series peaking inductors at the base. A bandwidth of 24–48 GHz and a noise figure of 3.1 dB with an overall power consumption of 17.6 mA were demonstrated [1]. In [2], an LNA was designed to operate from 26 to 42 GHz in 90 nm SOI (Silicon on Insulator) CMOS technology, providing a gain of 11.9 dB with 17 mA power consumption with a noise figure of 3.6 dB. A 20–44 GHz LNA was introduced [3] in 22 nm FDSOI (Fully Depleted Silicon on Insulator) process, which demonstrated a gain of 17 dB, the minimum noise figure of 3.1 dB, and overall power consumption of 20.5 mW. In [4], a 24–44 GHz LNA was designed in a 45 nm CMOS process, which provided a gain of 20 dB and a minimum noise figure of 4.2 dB, with a power consumption of 58 mW. A 20–44 GHz LNA was designed [5] in a 22 nm GF FDSOI process with a gain of 23 dB, a noise figure of 3.3 dB, and overall power consumption of 20.5 mW. Unfortunately, for a similar frequency band, all the above LNAs have either high power consumption or high noise figure (NF) or are still not competitive for wideband applications.

In the presented LNA design, an approach consisting in reducing the base resistance (R_B) and choosing the appropriate transistor size and current density is demonstrated to achieve low power consumption and low noise figure with high gain capabilities. The transistor size is the parameter that decides the overall power consumption as well as its noise performance. The methodology to reduce the base resistance and select the optimum transistor size is discussed in the following section. The presented LNA can be used to support applications falling under Ka-band, millimeter-wave receivers, and 5G communication systems [6–10]. The proposed LNA reports the lowest noise figure, lowest power consumption with reasonable highest gain, and highest bandwidth realized so far at this frequency band in any silicon-based technology.

2. Technology and Transistor Sizing

The presented LNA was designed in IHP's 130 nm BiCMOS process. The technology traits high-speed HBTs with $f_T/f_{MAX}/gate - delay$ of 360 GHz/450 GHz/2.0 ps. The technology sets out seven aluminum metallization layers, with two thick top metal layers of 2 μm and 3 μm thickness for designing high-quality passives. As reported in Figure 1, a 1.8 $\mu\text{m} \times 0.07 \mu\text{m}$ NPN transistor achieves f_T of 360 GHz. These features of the active device assist transistor sizing in the LNA design.

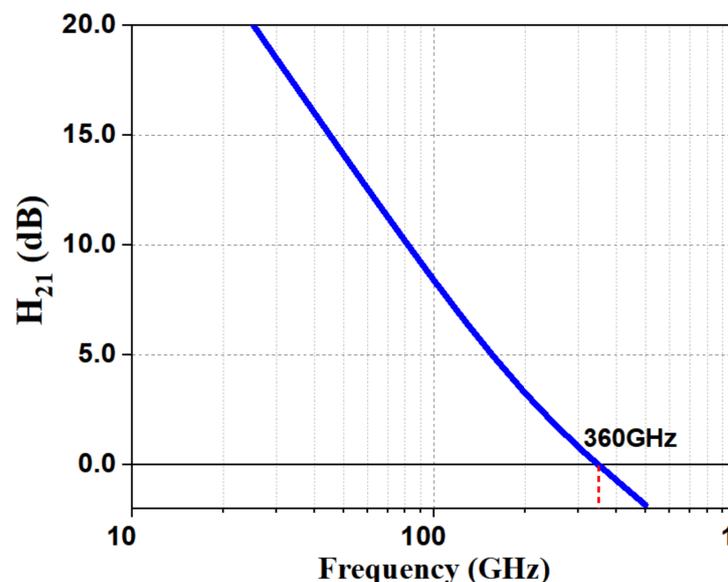


Figure 1. f_T of an NPN transistor.

As there is a trade-off between noise figure and gain, the appropriate transistor size needs to be selected to get the optimum values of noise figure and gain. The minimum noise figure (NF_{min}) for a SiGe HBT is given by Equation (1) [11].

$$NF_{min} \cong 1 + \frac{n}{\beta} + \sqrt{\frac{2I_C}{V_T}(R_B + R_E) \left(\frac{f^2}{f_T^2} + \frac{1}{\beta} \right) + \frac{n^2}{\beta}} \quad (1)$$

where $V_T = kT/q$, R_B is the base resistance, R_E is the emitter resistance, n is the I_C ideality factor.

For recent SiGe HBTs, Equation (1) can be simplified so that n is very close to 1, β is greater than 100, and R_B is much larger than R_E . Equation (1) can be rewritten as [11] (2).

$$NF_{min} \cong 1 + \sqrt{\frac{2I_C}{V_T}(R_B) \left(\frac{f^2}{f_T^2} + \frac{1}{\beta} \right)} \quad (2)$$

The transistor size was scaled to obtain noise matching by selecting the optimum source admittance.

For that, initially, we determined the optimum collector current density to achieve the minimum noise figure and meet the requirements for the application in hand. From Equation (2), it can be seen that reducing R_B improves the noise performance.

For low-noise operations, the optimum source resistance is given by Equation (3) [12].

$$R_{s,opt} \cong \frac{f_T}{f} \frac{1}{\sqrt{L_E}} \sqrt{\frac{2R_B}{J_C W_E} \frac{kT}{q}} \quad (3)$$

From Equation (3), it is evident that $R_{s,opt}$ depends on the length of the emitter (L_E) and on the base resistance (R_B). Most of the previously published reports focused on optimizing the current density and the length of the emitter to bring the optimum source resistance to 50 Ω , which resulted in high noise figures and high power consumption. In this paper, an effort was made to optimize the base resistance along with I_C and L_E . By defining additional metal layers (i.e., Metal 1 to Metal 3) on the top of the base of the transistor, we could further reduce the base resistance and hence bring the source resistance close to 50 Ω .

Figure 2 shows the 3D structure of the HBT transistor. From Figure 1, Base and Collector of the HBT were defined in Metal 1, whereas Emitter was defined in Metal 2 in the pcell structure. Each of these terminals were connected to the respective matching impedances outside the pcell. In the design, transmission lines were used for matching the impedance to 50 Ω . The transmission lines were defined in top Metal 2 layers, whereas the pcell terminals were defined in base Metal layers. Hence, it was necessary to transit from the base metal layers to the top metal layers. The transition from base metal layers to top metal layer alters the impedance matching and hence affects the overall performance of the LNA. The transition from lower metal levels to higher metal levels is unavoidable as the input RF signal always traverses from top to bottom metal levels. In order to have good impedance matching along with good performance, an effort was made to bring the real part of the input impedance close to 50 Ω before performing actual matching at the input. This was achieved by defining additional metal layers on top of the base before we physically connected the base to the transmission line. This is depicted in Figure 3. Base was defined in Metal 1, and above Metal 1, we introduced the additional Metal 2 and Metal 3 without violating any of the design rules imposed by the foundry. When these three metal layers were parallel, their effective resistance was reduced, and this in turn helped to reduce the effective base resistance. (Note: Respective via connections between the metal layers has been defined for interconnection). Now, from the HBT transistor pcell, the Base connection exited in Metal 3 instead of Metal 1. Outside the pcell, a Metal 3 to

Top Metal 2 arrangement was used to connect the base to the transmission line. An EM simulation was performed in order to evaluate the effectiveness of the introduction of additional metal layers on the base. From the EM simulation, it was found that, by defining additional metal layers (i.e., Metal 2 to Metal 3) on the top of the base of the transistor, we could further reduce the base resistance and hence bring the source resistance close to 50 Ω .

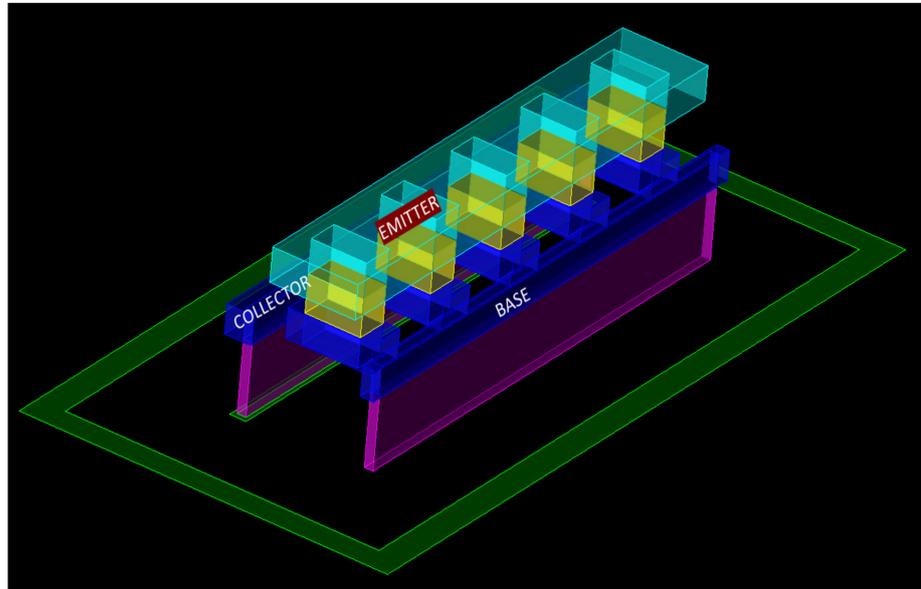


Figure 2. The 3D structure of the heterojunction bipolar transistor (HBT) transistor.

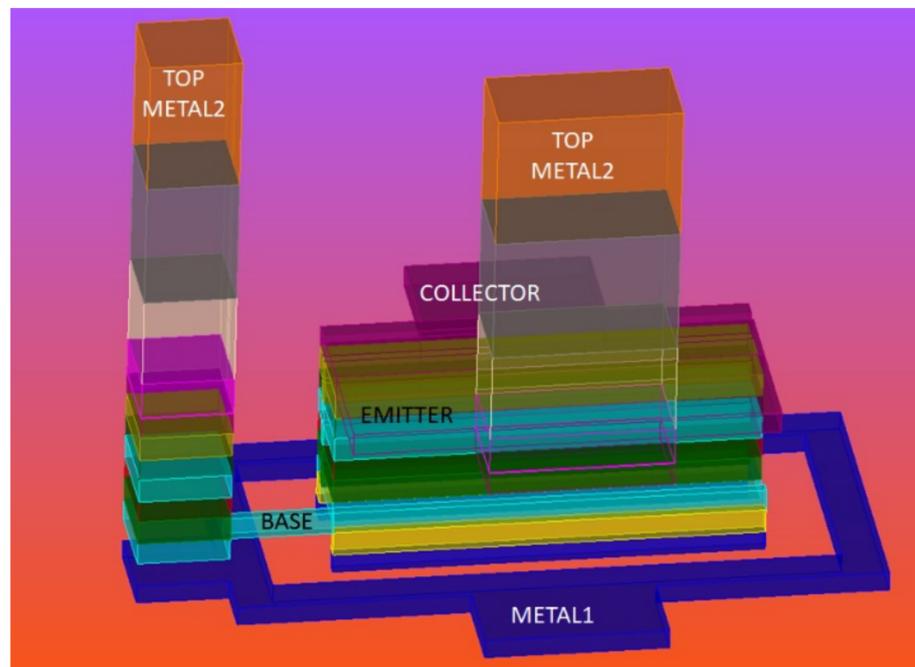


Figure 3. The 3D EM structure of HBT with metal stacked up on Base, Collector, and Emitter.

An electromagnetic (EM) simulation was performed, and its performance was evaluated. Figure 4 shows the effectiveness of introducing additional metal layers on the base region in terms of reflection coefficient, which eventually resulted in bringing the source impedance to 50 Ohms. Γ_{in} denotes the source impedance before adding any metal layers

to the base region, and Γ'_{in} represents the source impedance after adding Metal 2 to Metal 3 layers to the base region.

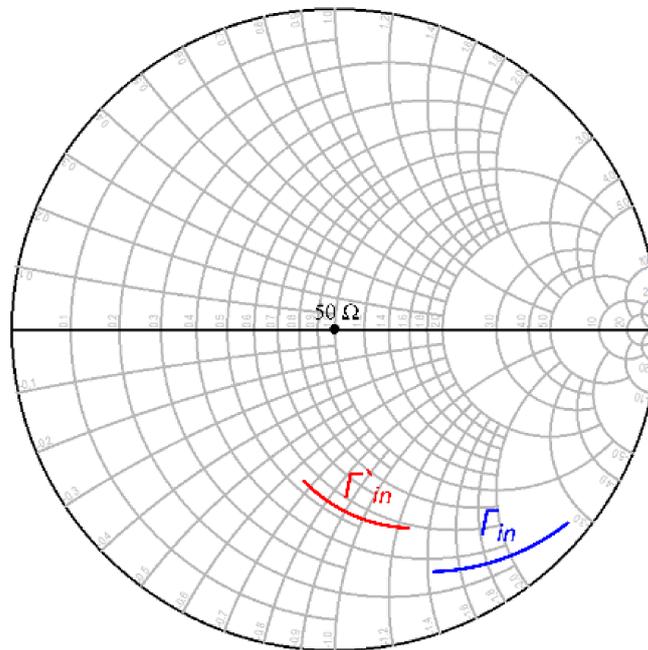


Figure 4. Γ_{in} and Γ'_{in} for a common-emitter (CE) common base emitter base collector (CBEB) HBT.

Figure 5 illustrates the EM simulation results. Point B ($R_B = 17.6 - j103.14 \Omega @ 32 \text{ GHz}$) is the input impedance measured without additional metal layers on the base region, and Point A ($R_A = 41.4 - j55.86 \Omega @ 32 \text{ GHz}$) is the input impedance measured with additional metal layers on the base region. From this analysis, it is very clear that the introduction of additional metal layers helped to bring the input impedance close to 50Ω . In fact, some additional capacitance due to the introduction of metals, helped to bring the input impedance close to 50Ω .

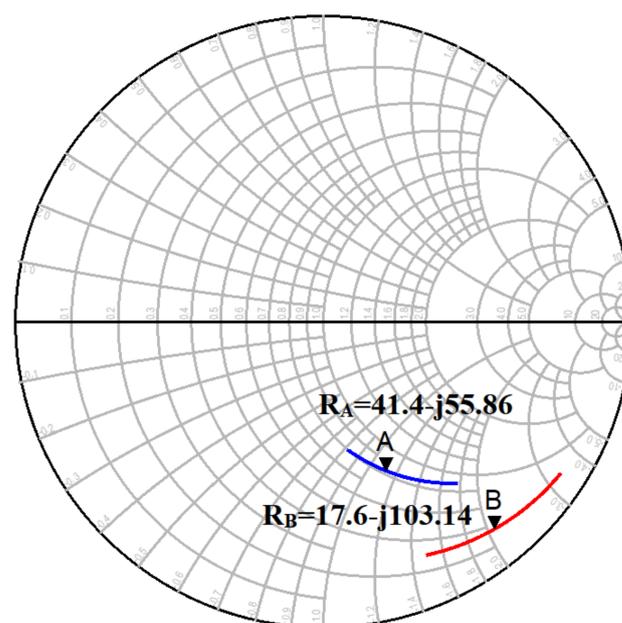


Figure 5. Input impedance with (A) and without (B) additional metal layers on the base region.

Figure 6 shows the primary setup used for characterization, required to ascertain the current density. NPN HBT parameterized cells (pcells) are present in IHP’s 130 nm BiCMOS SiGe technology with tunable emitter length (L_E). By sweeping the collector current for a fixed emitter area, one can find the optimum current density. As shown in Figure 5, a collector current of 4 mA appeared to be an optimized value for a transistor with an emitter length (L_E) of 5 μm .

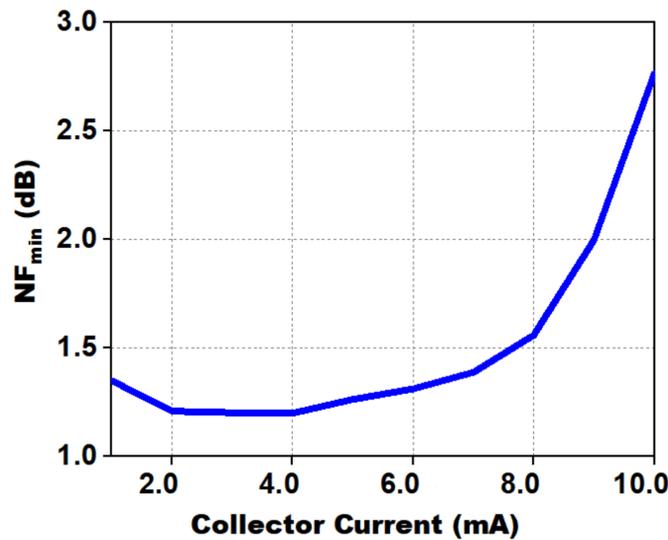


Figure 6. Simulated NF_{min} vs. Collector Current (mA).

The optimum transistor size and current bias were first assessed for minimum noise, maximum gain, and simplicity of matching over a wider bandwidth. In the design of the LNA, initially a parametric analysis was performed by sweeping collector current and emitter length with respect to frequency. From this analysis, we needed to find the optimum transistor size and bias current to get the minimum noise and maximum gain along, with simultaneous matching between input and output terminals.

A typical bias current of 0.8 mA/ μm at a collector–emitter voltage of 1.2 V was initially chosen as a trade-off between maximum available gain (G_{max}) and minimum noise figure (NF_{min}). The NF_{min} and G_{max} for inductively emitter degenerated HBT’s over frequency versus emitter length (L_E) is shown in Figure 7.

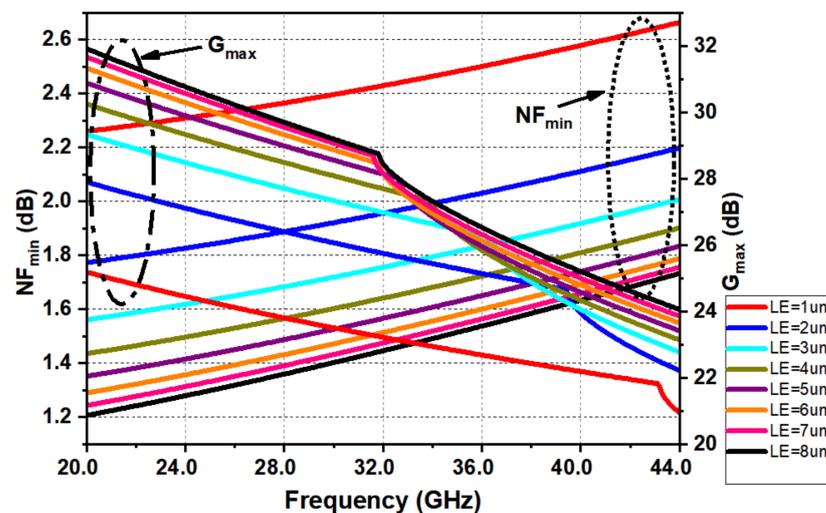


Figure 7. NF_{min} and G_{max} for a CE CBEBC HBT with emitter inductive degeneration.

Clearly, NF_{min} was not affected as much as G_{max} with respect to the device size; hence, the focus was instead placed on sizing for ease of device matching while maintaining high G_{max} . Once the collector current density was decided, scaling of the emitter length had to be carried out to shift the real part of the impedance to 50Ω for noise matching.

To achieve this, the transistor current density was kept constant, and the emitter length (L_E) of the transistor was varied to ascertain a point for which the real part of the impedance was 50Ω for optimum noise performance. Figure 8 shows the optimal noise impedance in terms of optimal reflection coefficient for the chosen emitter length of $5 \mu\text{m}$, which corresponded to a collector current of 4 mA .

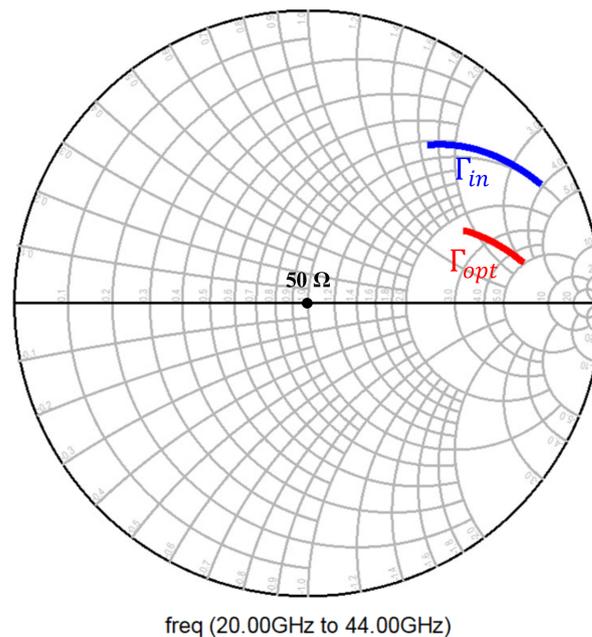


Figure 8. Γ_{in} and Γ_{opt} for a common-emitter CBEBC HBT with inductive emitter degeneration.

3. LNA Circuit Design

Low power continues to be one of the primary objectives in LNA design. The ease of cascode configuration enables low-power LNAs to be employed. The presented LNA accomplishes an inductively degenerated cascode common-emitter (CE) circuit arrangement, as shown in Figure 9a. The biasing circuit used is shown in Figure 9b. Two amplification stages were incorporated in the designed LNA to realize the dynamic range with a high gain and low noise. Cascoding transistors Q1/Q2 (and Q3/Q4) were employed to impact the isolation between input and output and to minimize the effect of the parasitic base-collector capacitance of Q1/Q2 (and Q3/Q4).

The presented LNA utilizes a design procedure where the first stage is matched for minimum noise, and the second stage is matched for maximum gain. The two stages were designed such that the gain of the LNA was greater than 20 dB throughout the bandwidth of the LNA.

Input matching was primarily addressed by the series and shunt transmission lines used for biasing the base, given that the transistor size and the inductive emitter degeneration were chosen to bring Γ_{in} and Γ_{opt} close to 50Ω , as shown in Figure 8.

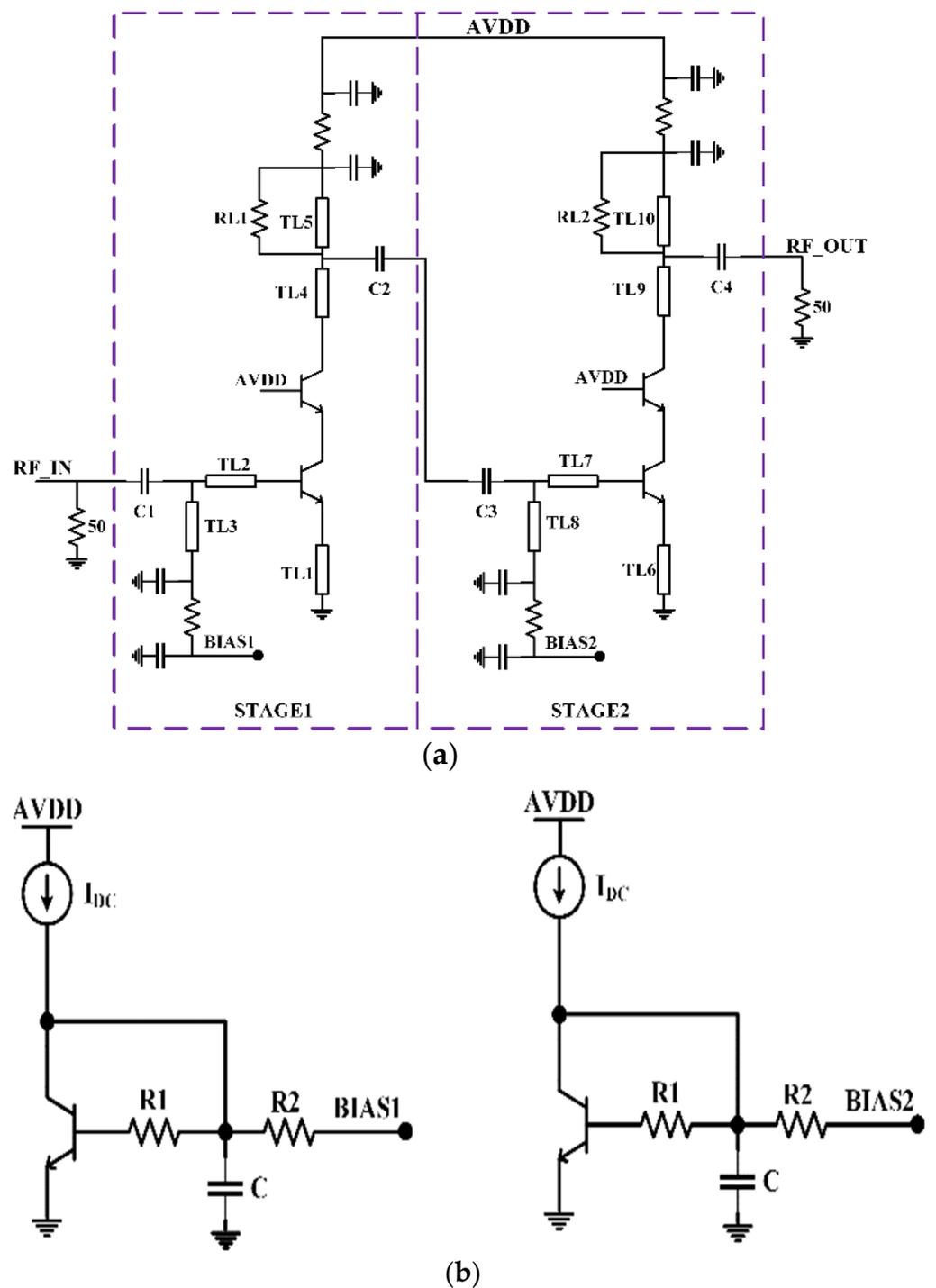
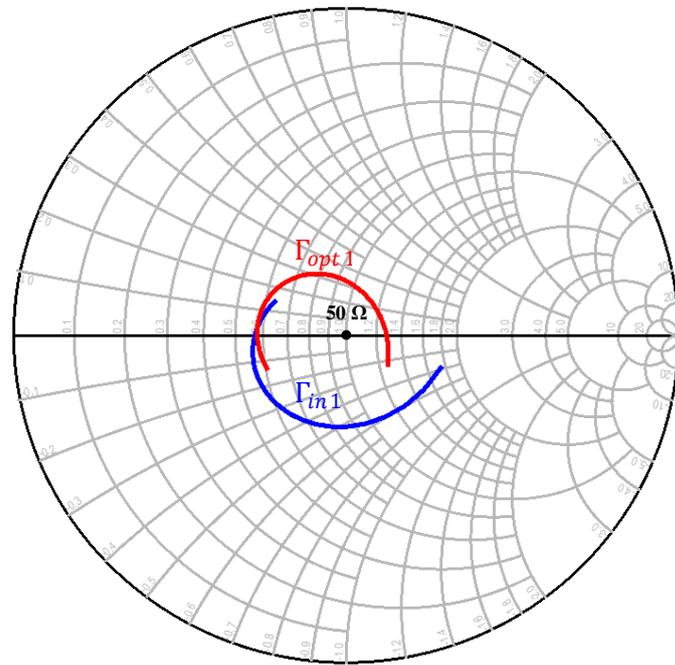


Figure 9. (a) Proposed schematic of LNA; (b) bias circuit.

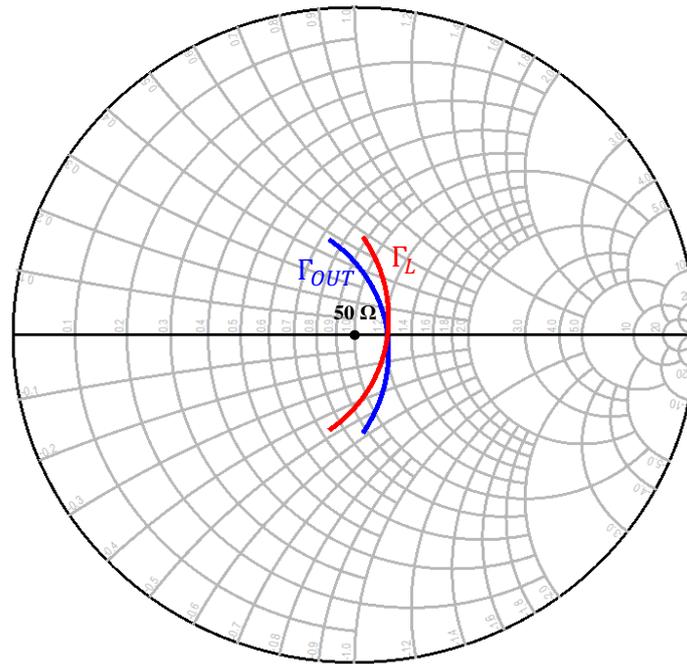
As mentioned earlier, input matching was essentially addressed by the series-resonant DC block MIM capacitor, the series transmission line, and the shunt 96 Ω transmission line used for biasing the base, as the transistor sizing and inductive emitter degeneration were already selected to move the input matching close to 50 Ω. The smith chart of the input matching network is shown in Figure 10a. The input impedance of the circuit is given by Equation (4) [13,14].

$$Z_{in} = -\frac{j}{\omega C_{\pi}} + j\omega L_e + \frac{g_m L_e}{C_{\pi}} + j\omega L_b \quad (4)$$



freq (20.00GHz to 44.00GHz)

(a)



freq (20.00GHz to 44.00GHz)

(b)

Figure 10. Smith chart of (a) input-matching network and (b) output-matching network over a frequency of 20–44 GHz.

To match the input impedance to $50 \Omega (R_s)$, the imaginary part Equation (4) should be equal to zero, and the real part should be 50Ω . We can obtain the emitter and base inductor values from the Equations (5) and (6), respectively.

$$L_e = \frac{R_s C_\pi}{g_m} \tag{5}$$

$$L_b = \frac{1}{C_\pi \omega^2} - \frac{R_s C_\pi}{g_m} \quad (6)$$

Equations (4)–(6), provide elements to design the input-matching circuit, which is again improved by simulation of the S_{11} parameter. The first stage output and second stage input were matched by incorporating interstage matching. Initially, the output impedance (Z_{out1}) of the first stage and input impedance (Z_{in2}) of the second stage were determined. Complex conjugate matching ($Z_{out1}^* = Z_{in2}$) was incorporated between first-stage output and second-stage input [15,16]. This kind of interstage matching helped to reduce losses between the interstage and thus preserved the signal properties.

Output matching of the stage was accomplished with a series 96Ω transmission line and a shunt 96Ω transmission line used for biasing the collector. The smith chart of the output-matching network is shown in Figure 10b. The biasing short stubs utilized for biasing the collector and base nodes were built by dual 2 pF shunt Metal Insulator Metal (MIM) capacitors, a 20Ω series TaN resistor, and 500 fF of shunt MIM capacitors.

4. Results and Discussion

In the first stage, input-matching elements were formed by the transmission lines TL1, TL2, and TL3 and a series MIM capacitor, whereas output-matching elements were formed by the transmission line TL4 and TL5 and a series DC blocking capacitor.

Similarly, the second-stage input-matching elements were formed by the transmission lines TL6, TL7 and TL8 and a series MIM capacitor, whereas the output-matching elements were formed by the transmission line TL9 and TL10 and a series DC blocking capacitor. All transmission lines were realized as microstrip lines, with the top metal layer (Top Metal 2) being the signal line, and the bottom metal layer (Metal 1) being the RF ground.

These transmission lines were synthesized and EM (electromagnetically) simulated using the Momentum tool (version 6). The EM simulation was carried out on an overall two-stage LNA layout excluding the transistors, resistors, and MIM capacitors, and an EM model was generated [7]. The EM layout model is shown in Figure 11. A test bench was created with the synthesized model of layout and plugged in with resistors, transistors, and MIM caps. The parasitic effect of RF pads was also considered while designing the respective matching sections.

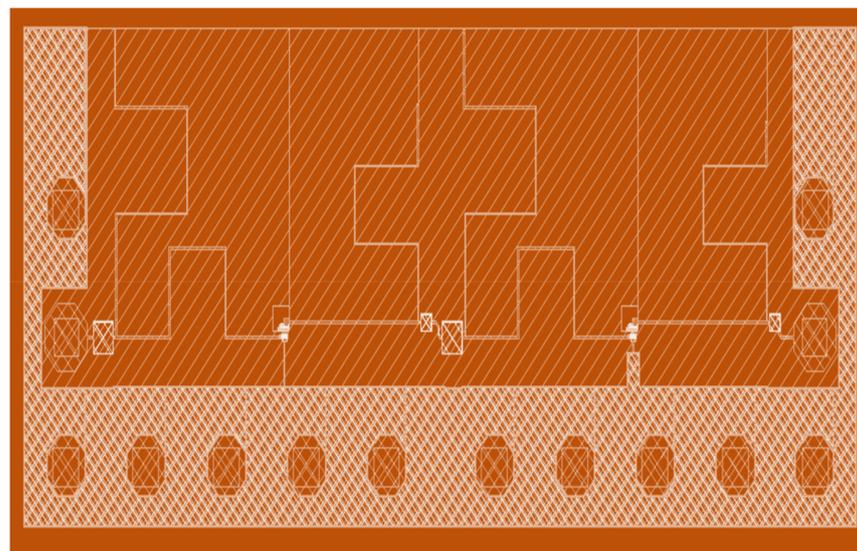


Figure 11. EM Layout of the two-stage LNA.

The complete two-stage LNA layout is depicted in Figure 12. A considerably small form factor was achieved by the use of bent transmission line structures. The presented

LNA occupies a total area of $1300 \mu\text{m} \times 550 \mu\text{m}$ with RF pads and consumes only 8 mA of total current from a 1.2 V power supply.

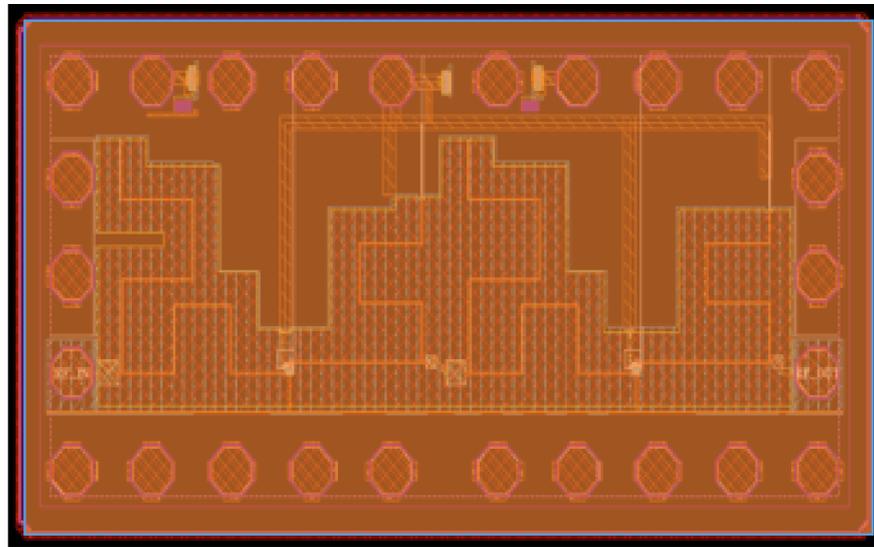


Figure 12. Layout of the two-stage LNA.

The characteristics of the LNA were validated by simulating two-port S-parameters from a frequency of 20–44 GHz. The simulated input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) are shown in Figure 13. S_{11} and S_{22} of < -10 dB were achieved from a frequency of 20–44 GHz with a 50Ω source and load impedance. The simulated NF (Noise Figure) is as shown in Figure 13, and IP1dB (input 1 dB gain compression point) [17,18] is shown in Figure 14; they were 3.42 dB and -18 dBm, respectively. In Figure 13, the simulated gain appears greater than 20 dB from 20–44 GHz. The reverse isolation (S_{12}) of the presented LNA was < -65 dB, as shown in Figure 13.

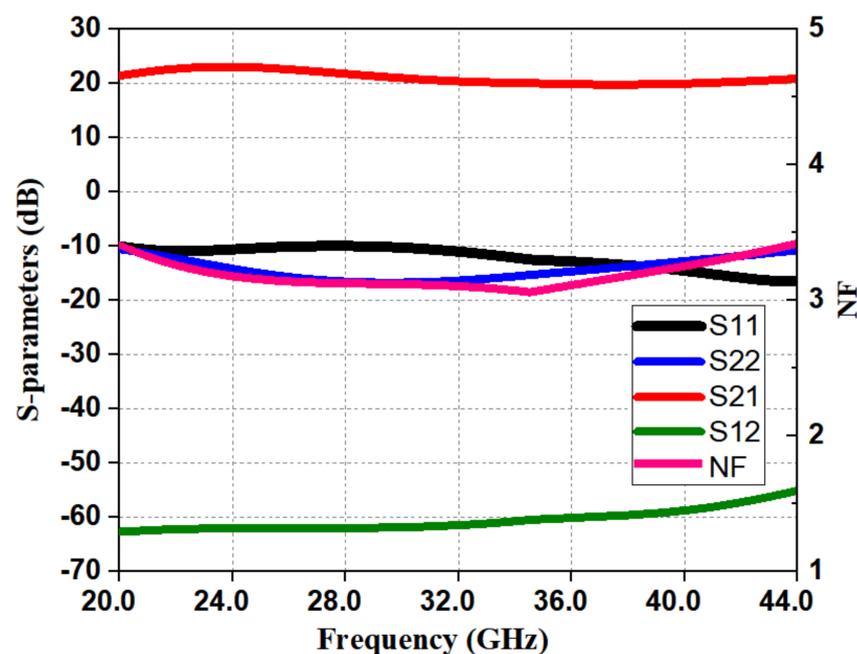


Figure 13. Simulated S parameters of the LNA.

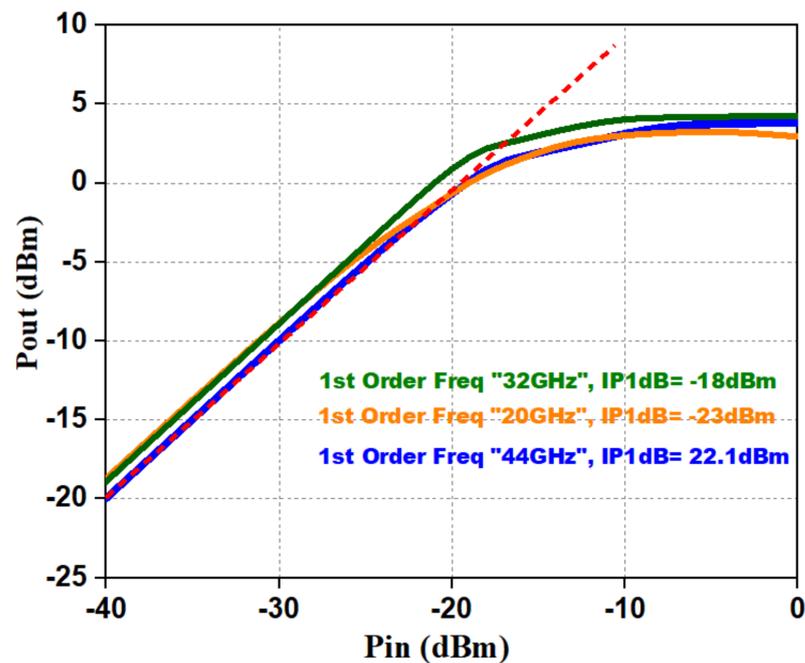


Figure 14. Pout vs. pin and 1 dB compression point of the LNA.

In order to validate the stability of the LNA, a stability analysis was performed across a frequency range of 10–60 GHz. For unconditional stability, the stability factor (K_f) should be greater than 1 [19,20]. The proposed LNA was unconditionally stable in the frequency range of 10–60 GHz, which is way beyond the operating frequency range of LNAs, and its stability factor (K_f) was as shown in Figure 15.

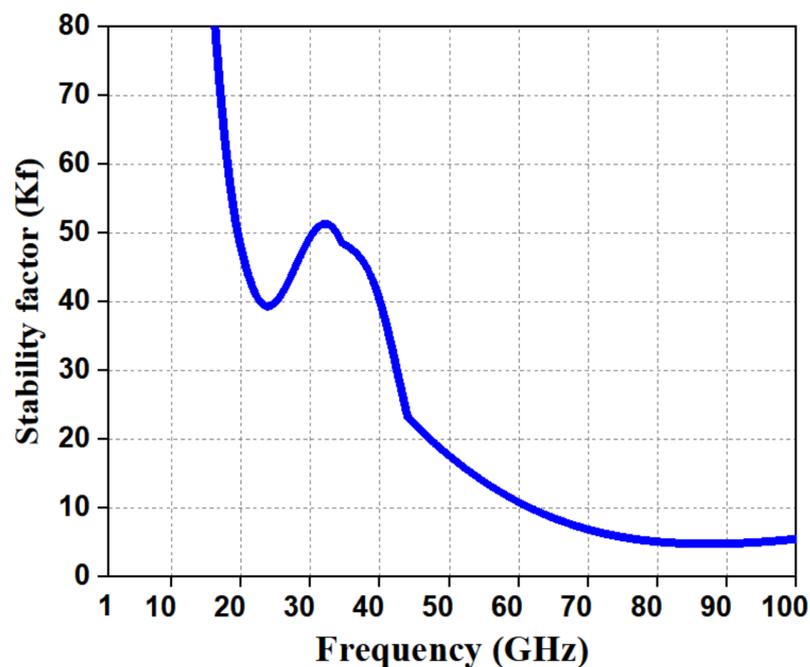


Figure 15. Stability factor (K_f) of the LNA.

A comparison of the LNA performance determined in this work with that from simulation tests carried out in previous publications is summarized in Table 1. The presented LNA exhibited the lowest noise figure and lowest power consumption in comparison to all previ-

ously published values. Two Figures of Merit (FoM) were defined in [6–8], to evaluate the performances among the wideband LNAs and are calculated using Equations (7) and (8).

$$FoM_I = 20 \log_{10} \frac{Gain[lin] \times BW[GHz]}{Power[mW] \times (NF[lin] - 1)} \quad (7)$$

$$FoM_{II} = 20 \log_{10} \frac{IIP_3[mW] \times Gain[lin] \times BW[GHz]}{Power[mW] \times (NF[lin] - 1)} \quad (8)$$

Table 1. Performance comparison with respect to simulated results.

Ref.	Technology	Frequency (GHz)	Gain (dB)	NF (min) (dB)	IP1 dB (dBm)
[1]	90 nm LP	24–48	Not given		—
[2]	90 nm SOI	26–42	10.5	25	—
[3]	22 nm FDSOI	24–43	19	3.5	—
[4]	45 nm CMOS SOI	24–44	18	4.2	—
[5]	22 nm FDSOI	20–44	22	4.2	−23
[21]	130 nm SiGe	55–64	24	2.5	−30
[22]	130 nm SiGe	8–12	14.5	1.4	—
[23]	130 nm SiGe	108–143	18	7.5	—
Prop.	130 nm SiGe	20–44	20	3.02	−18

The input third-order intercept (IIP_3) of the presented LNA resulted to be -4.2 dBm. The FoM_I and FoM_{II} for the proposed LNA were 26.52 and 18.11, respectively.

5. Conclusions

This paper details the design and simulation results of a state-of-the-art 20–44 GHz LNA circuit, implemented in a 130 nm SiGe BiCMOS technology for mm-Wave and 5G applications. A simple layout technique was adopted to minimize the base resistance of the HBT, which helped to bring the real impedance closer to 50Ω . This design strategy was proven to be efficient to minimize the noise figure, improve the bandwidth, and lower the power consumption. The presented LNA demonstrated a gain greater than 20 dB, with a noise figure <3.4 dB in the whole 20–44 GHz bandwidth. The simulated input P1dB of -18 dBm was obtained. This work demonstrates the excellent applicability of the designed LNA for millimeter-wave applications.

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References

1. Cao, J.; Li, Z.; Tian, J.; Liu, H.; Li, Q. A 24–48-GHz low power low noise amplifier using gain peaking techniques. In Proceedings of the 2016 IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT), Beijing, China, 5–8 June 2016; Volume 1, pp. 126–128.

2. Ellinger, F. 26–42 GHz SOI CMOS low noise amplifier. *IEEE J. Solid-State Circuits* **2004**, *39*, 522–528. [[CrossRef](#)]
3. Gao, L.; Rebeiz, G.M. A 24–43 GHz LNA with 3.1–3.7 dB noise figure and embedded 3-pole elliptic high-pass response for 5G applications in 22 nm FDSOI. In Proceedings of the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2–4 June 2019; pp. 239–242.
4. Chauhan, V.; Floyd, B. A 24–44 GHz UWB LNA for 5G cellular frequency bands. In Proceedings of the 2018 11th Global Symposium on Millimeter Waves (GSMM), Boulder, CO, USA, 22–24 May 2018; pp. 1–3.
5. Gao, L.; Ma, Q.; Rebeiz, G.M. A 20–44 GHz Image-Rejection Receiver With >75-dB Image-Rejection Ratio in 22-nm CMOS FD-SOI for 5G Applications. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 2823–2832. [[CrossRef](#)]
6. Pan, Z.; Qin, C.; Ye, Z.; Wang, Y. A low power inductor less wideband LNA with G m enhancement and noise cancellation. *IEEE Microw. Wirel. Compon. Lett.* **2016**, *27*, 58–60. [[CrossRef](#)]
7. Garg, D.K.; Kumar, V.; Kumar, M.M.; Verma, Y.; Chaturvedi, S. Low Noise Amplifier at Ka Band. In Proceedings of the 2017 IEEE MTT-S International Microwave and RF Conference (IMaRC), Ahmedabad, India, 11–13 December 2017; pp. 1–4.
8. Abdeen HA, Y.; Yuan, S.; Schumacher, H.; Ziegler, V.; Meusling, A.; Feldle, P. 10 to 40 GHz super heterodyne receiver frontend in 0.13 μm SiGe BiCMOS technology. *Frequenz* **2017**, *71*, 151–160.
9. Chen, Z.; Gao, H.; Leenaerts, D.M.W.; Milosevic, D.; Baltus, P.G.M. A 29–37 GHz BiCMOS low-noise amplifier with 28. In 5 dB peak gain and 3.1–4.1 dB NF. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, 10–12 June 2018; pp. 288–291.
10. Wu, X.; Kalantari, M.; Shin, D.H.; Yue, C.P. A 24–32GHz gm-boosted LNA with Triple Coupling Input Transformer for 5G Applications. In Proceedings of the 2019 IEEE MTT-S International Wireless Symposium (IWS), Guangzhou, China, 19–22 May 2019; pp. 1–3.
11. Rieh, J.S.; Greenberg, D.; Stricker, A.; Freeman, G. Scaling of SiGe heterojunction bipolar transistors. *Proc. IEEE* **2005**, *93*, 1522–1538. [[CrossRef](#)]
12. Shen, P.; Zhang, W.; Xie, H.; Jin, D. Geometry optimization of SiGe HBTs for noise performance of the monolithic low noise amplifier. In Proceedings of the 2009 IEEE 8th International Conference on ASIC, Changsha, China, 20–23 October 2009; pp. 785–788.
13. Feng, C.; Yu, X.P.; Lim, W.M.; Yeo, K.S. A Compact 21–39 GHz Self-Biased Low-Noise Amplifier in 65 nm CMOS Technology. *IEEE Microw. Wirel. Compon. Lett.* **2013**, *23*, 662–664. [[CrossRef](#)]
14. Mazzanti, A.; Sosio, M.; Repossi, M.; Svelto, F. A 24 GHz Subharmonic Direct Conversion Receiver in 65 nm CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2011**, *58*, 88–97. [[CrossRef](#)]
15. Qin, P.; Xue, Q. Design of Wideband LNA Employing Cascaded Complimentary Common Gate and Common Source Stages. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *27*, 587–589. [[CrossRef](#)]
16. Li, Z.; Cao, J.; Li, Q.; Wang, Z. A wideband Ka-band receiver front-end in 90-nm CMOS technology. In Proceedings of the 2013 European Microwave Integrated Circuit Conference, Nuremberg, Germany, 6–8 October 2013; pp. 5–8.
17. Niu, G.; Liang, Q.; Cressler, J.D.; Webster, C.S.; Hareme, D.L. RF linearity characteristics of SiGe HBTs. *IEEE Trans. Microw. Theory Tech.* **2001**, *49*, 1558–1565.
18. Antonopoulos, A.; Papathanasiou, K.; Bucher, M.; Papathanasiou, K. CMOS LNA design at 30 GHz—A case study. In Proceedings of the 2012 8th International Caribbean Conference on Devices, Circuits and Systems (ICDCS), Playa del Carmen, Mexico, 14–17 March 2012; pp. 1–4.
19. Cuadrado-Calle, D.; George, D.; Fuller, G. A GaAs Ka-band (26–36 GHz) LNA for radio astronomy. In Proceedings of the 2014 IEEE International Microwave and RF Conference (IMaRC), Bangalore, India, 15–17 December 2014; pp. 301–303.
20. Liang, Q.; Niu, G.; Cressler, J.D.; Taylor, S.; Hareme, D. Geometry and bias current optimization for SiGe HBT cascode low-noise amplifiers. In Proceedings of the 2002 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. Digest of Papers (Cat. No.02CH37280), Seattle, WA, USA, 3–4 June 2002; pp. 407–410.
21. Völkel, M.; Dietz, M.; Hagelauer, A.; Weigel, R.; Kissinger, D. A 60-GHz low-noise variable-gain amplifier in a 130-nm BiCMOS technology for sixport applications. In Proceedings of the 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 28–31 May 2017; pp. 1–4.
22. Davulcu, M.; Çalışkan, C.; Ozeren, E.; Gurbuz, Y.; Kaynak, M. X-band high dynamic range flat gain SiGe BiCMOS low noise amplifier. In Proceedings of the 2015 10th European Microwave Integrated Circuits Conference (EuMIC), Paris, France, 7–8 September 2015; pp. 242–245.
23. Ulusoy, A.Ç.; Song, P.; Khan, W.T.; Kaynak, M.; Tillack, B.; Papapolymerou, J.; Cressler, J.D. A SiGe D-band low-noise amplifier utilizing gain-boosting technique. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *25*, 61–63. [[CrossRef](#)]