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Melt Blown Fiber-Assisted Solvent-Free Device Fabrication at Low-Temperature

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Abstract: In this paper, we propose a solvent-free device fabrication method using a melt-blown (MB) fiber to minimize potential chemical and thermal damages to transition-metal-dichalcogenides (TMDCs)-based semiconductor channel. The fabrication process is composed of three steps; (1) MB fibers alignment as a shadow mask, (2) metal deposition, and (3) lifting-up MB fibers. The resulting WSe_2-based p-type metal-oxide-semiconductor (PMOS) device shows an ON/OFF current ratio of $\sim 2 \times 10^5$ (ON current of ~ -40 μA) and a remarkable linear hole mobility of ~ 205 cm^2/V·s at a drain voltage of -0.1 V. These results can be a strong evidence supporting that this MB fiber-assisted device fabrication can effectively suppress materials damage by minimizing chemical and thermal exposures. Followed by an MoS_2-based n-type MOS (NMOS) device demonstration, a complementary MOS (CMOS) inverter circuit application was successfully implemented, consisted of an MoS_2 NMOS and a WSe_2 PMOS as a load and a driver transistor, respectively. This MB fiber-based device fabrication can be a promising method for future electronics based on chemically reactive or thermally vulnerable materials.

Keywords: solvent-free lithography; transition metal dichalcogenides; melt blown fiber; micro-scaled shadow mask; complementary metal-oxide-semiconductor

1. Introduction

Microfabrication techniques have been persistently developed as industrial standards increase for high-performance next-generation electronic device applications. Photolithography has been a commonly used method for the spatially precise patterning process in the integrated circuit (IC) technology. Although this conventional photolithography can provide high-resolution patterns, process complexity and high-cost equipment should be involved. Furthermore, several steps incorporated with solvent and thermal exposure, such as photoresist (PR) coating, curing, and developing, can cause detrimental effects to fully exploit intrinsic properties of semiconductors. In order to overcome the limitations, soft lithography has been considered, as promising alternatives have many advantages, such as low-cost, low-temperature processable, and chemical-free methods [1,2]. Although the PR-based patterning steps are not involved during the soft-lithography process, which can avoid chemical and thermal exposure, poor electrical contacts between metal-semiconductor junctions are still remaining as a challenge. Beyond the electronic device fabrications, chemical and thermal exposure-free approaches are desired in the field of display. To handle chemically sensitive organic materials for organic-light-emitting diode fabrication, a chemical-free fabrication process is highly demanded to minimize potential chemical reaction of organic materials. In an effort to find solutions to overcome such limitations,

several approaches have been introduced, including inkjet printing [3], fine-metal-shadow masking [4,5], and microcontact-printing [6].

In a decade, two-dimensional (2D) van der Waals semiconductors such as transition-metal-dichalcogenides (TMDCs) have been intensively studied to fully exploit their superlative electronic properties [7–10]. For example, MoS_2 and WSe_2 as semiconducting members of TMDCs have been extensively studied with great possibilities for future electronics within high-speed [11], flexible [12], and immune short channel effects in the device, which scale down [13]. Similar to the other semiconductors, however, the photolithography process also causes electrical property degradations of such semiconductors, due to solvent-induced chemical reactions and/or thermal degradation [14,15]. Furthermore, securing a clean interface between the source/drain (S/D) electrodes and a TMDCs channel layer is another significant issue towards high-performance device demonstrations [16–19]. Here, we report a melt blown (MB) fiber-assisted solvent-free lithography method for fabrication of field-effect transistors (FETs). The resulting electrical behaviors of TMDCs-based FETs are thoroughly compared with those of devices fabricated using a conventional photolithography process.

2. Materials and Methods

TMDCs-based FETs were fabricated on a thermally oxidized 285 nm-thick SiO_2/p^+ silicon substrate. Silicon substrate was ultrasonically cleaned by sequentially immersing in acetone, methyl alcohol, and isopropyl alcohol each for 15 min. Polydimethylsiloxane (PDMS) stamps were used to exfoliate and transfer 2D semiconductor active channels to a designated place. To fabricate PDMS stamps, base resin and cross-linker (Sylgard 184, Dow Corning) solutions were mixed with a 10:1 volume ratio, and trapped-air bubbles were removed by degassing in a vacuum for 20 min. The solution was then poured onto a cleaned silicon wafer mold and thermally cured on a hot plate in ambient condition at 423 K for 1 h.

Figure 1 shows a non-lithographic micro-scaled device fabrication process using an MB fiber-based shadow mask. First of all, 2D TMDC semiconductors were mechanically exfoliated and transferred on a silicon substrate by a PDMS-based direct imprinting method, as shown in Figure 1a. In Figure 1b, an MB fiber-based shadow mask was aligned and subsequently transferred onto a targeted TMDC nanoflake under an optical microscope (OM) to define micropatterned S/D electrodes. The MB fiber-based shadow mask consisted of a punched PDMS frame and a selected MB fiber with an average diameter of ~1.5 μm. The suspending MB fiber was attached on the bottom side of the punched PDMS stamp (see Figure S1 with further details of MB fiber-based shadow mask technique in the Supplementary Materials (SM) section). The MB fiber could be efficiently attached at the 2D TMDC semiconductors on a silicon substrate due to its strong electrostatic force. Figure 1c,d shows a metal S/D electrodes patterning using a DC magnetron sputtering system, and we named this process as the "lift-up" method. By lifting-up the MB fiber-based shadow mask, a narrow gap between S/D electrodes (channel length) was formed with a distance corresponding to the diameter of a used MB fiber. This method is a straightforward way to form micro-scaled S/D electrodes without PR-casting and thermal curing process, and it can effectively reduce the whole process steps and the cost compared to the conventional photolithography. Based on this approach, WSe_2 and the MoS_2-based PMOS and NMOS devices were fabricated with Pt (50 nm) and Ti/Au (25 nm/25 nm) as S/D electrodes, respectively.
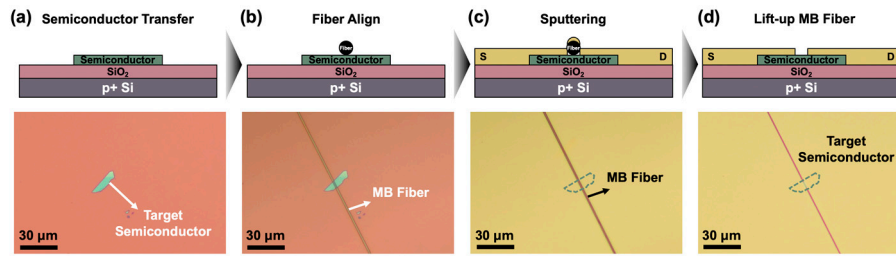
Figure 1. The non-lithographic micro-scaled device fabrication flow steps; (**a**) 2D transition-metal-dichalcogenides (TMDC) transferring on the silicon substrate; (**b**) melt-blown (MB) fiber alignment on the target TMDC nanoflake; (**c**) metal sputtering; (**d**) lifting-up MB fiber for S/D electrodes formation.

3. Results and Discussion

Figure 2 shows drain current-gate voltage (I_D-V_G) transfer characteristic curves of a WSe$_2$-based PMOS transistor. As shown in Figure 2a, the as-fabricated WSe$_2$ PMOS shows an ambipolar behavior, and both drain ON current (I_{ON}) levels in p-type and n-type regions ($I_{ON,p}$ and $I_{ON,n}$) were ~0.3 μA at a drain voltage (V_D) of −1 V (black line). After a post-annealing process (423 K for 1 h in ambient air), the WSe$_2$ PMOS shows a strong p-type property, while the n-type characteristic is suppressed (blue line). The thermally annealed WSe$_2$ PMOS shows excellent $I_{ON,p}$ of ~−0.4 mA at V_D of −1 V, which is ~10^3 times higher $I_{ON,p}$ than the as-fabricated device at the same bias conditions. It implies that the post-annealing process in an ambient condition forms an atomically thin tungsten oxides (WO_x) layer, having a p-type electrical characteristic on the surface of WSe$_2$ nanoflake, and it can be understood as a p-doping process at the WSe$_2$ channel surface [20–23]. Figure 2b shows I_D-V_G transfer characteristic curves and linear mobility (μ_{lin}) plot (inset) at V_D of −1 mV, −10 mV, and −100 mV. The μ_{lin} was calculated by using the following equation:

$$\mu_{lin} = \left(\frac{dI_D}{dV_G}\right)\left(\frac{L}{WC_{OX}|V_D|}\right)$$

where, C_{OX} is the capacitance of SiO$_2$ gate insulator, W and L are the width and the length of the FET channel, respectively. From this equation, the maximum linear mobility ($\mu_{lin,max}$) of our WSe$_2$ PMOS was calculated as ~205 cm^2/V·s at V_D of −100 mV. Moreover, another WSe$_2$ PMOS also showed excellent $\mu_{lin,max}$ of ~244 cm^2/V·s, as shown in Figure S2 in Supplementary Materials. As shown in Figure 2b, the I_D of our WSe$_2$ PMOS is proportionally increased by the V_D variation. This result can be a strong evidence that our non-lithographic fabrication method provides a high-quality Ohmic contact between the WSe$_2$ and Pt S/D electrodes. As a result, we can successfully achieve the high-performance WSe$_2$ PMOS device with excellent $\mu_{lin,max}$.
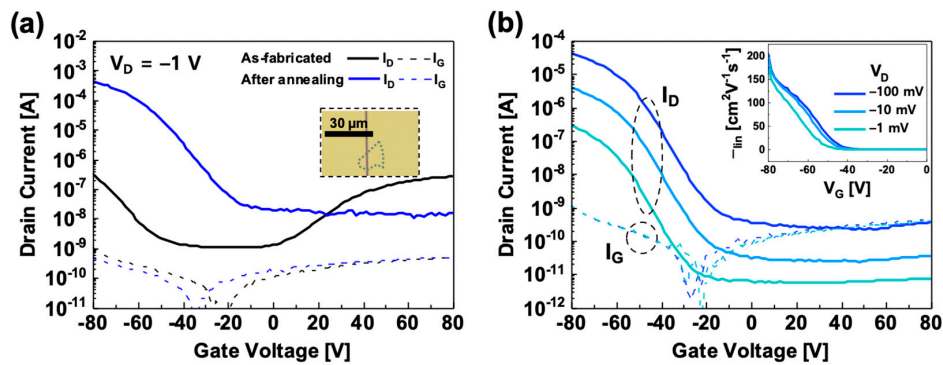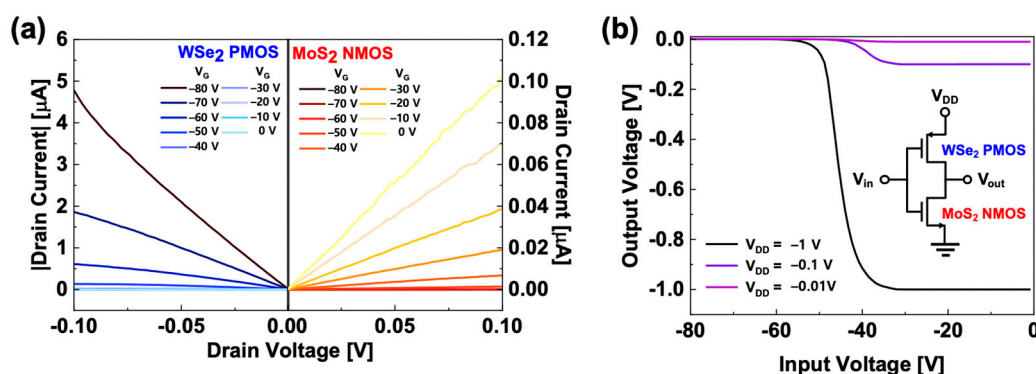

Figure 2. (**a**) Transfer characteristic curves of the WSe$_2$ p-type metal-oxide-semiconductor (PMOS) before (as-fabricated) and after the post-annealing process at V_D of −1 V (W/L = 10); (**b**) Transfer characteristic curves and linear mobility plot (inset) of the post-annealed WSe$_2$ PMOS at V_D of −1 mV, −10 mV, and −100 mV.

In addition to the WSe$_2$-based PMOS device, an n-type MoS$_2$ nanoflake-based NMOS device was investigated in a similar manner. Figure 3a,b shows schematics of device structures and OM images of an MoS$_2$ NMOS and an annealed WSe$_2$ PMOS on 285 nm-thick SiO$_2$/p$^+$ silicon substrate, respectively. Figure 3c,d show I_D-V_G transfer characteristics of each device. The scattered symbol and solid line display the semi-logarithmic and linear I_D, respectively. The MoS$_2$ NMOS shows I_{ON}/I_{OFF} ratio of ~2 × 10^4, a threshold voltage (V_{th}) of ~−32.6 V, and I_{ON} of ~0.3 μA at V_D = 0.1 V, while the WSe$_2$ PMOS shows higher I_{ON}/I_{OFF} ratio of ~10^6, V_{th} of ~−42.1 V and higher I_{ON} of ~−6.5 μA at V_D = −0.1 V. Figure 3e,f show the I_D-V_D output characteristic curves of the MoS$_2$ NMOS and WSe$_2$ PMOS for a V_G range of −80 V to 0 V with +10 V step increment. Both output curves clearly show excellent ohmic contact behaviors of the MoS$_2$/Ti-Au contact and the WSe$_2$/Pt contact within the linear operation region.
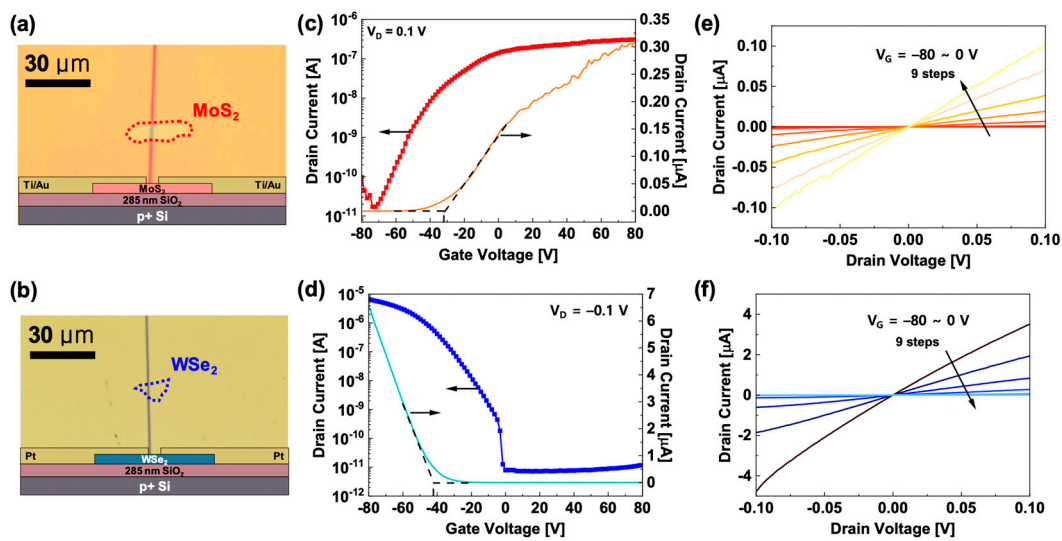
Figure 3. (**a**,**b**) Device schematic structures and OM images of the MoS$_2$ n-type metal-oxide-semiconductor (NMOS) and the WSe$_2$ PMOS; (**c**,**d**) Transfer characteristic curves of the MoS$_2$ NMOS and the WSe$_2$ PMOS; (**e**,**f**) Output characteristic curves of the MoS$_2$ NMOS and the WSe$_2$ PMOS, respectively.

Based on the PMOS and NMOS devices, a CMOS inverter circuit application was implemented, and I_D-V_D output characteristics curves of PMOS and NMOS FETs are displayed in Figure 4a (see Figure S3 with further details of load-line analysis in the Supplementary Materials section). The MoS$_2$ NMOS and WSe$_2$ PMOS were used as a load and a driver transistor, respectively, because the MoS$_2$ NMOS and WSe$_2$ PMOS showed negative V_{th}. Moreover, the WSe$_2$ PMOS had better electrical performances, such as higher I_D and linear hole mobility, than those of the MoS$_2$ NMOS device. Figure 4b shows the voltage transfer characteristic (VTC) curves of our CMOS inverter circuit device, and the transition voltage is ~−42 V, which is well-matched with V_{th} of WSe$_2$ PMOS driver transistor. The inset of Figure 4b shows our CMOS inverter circuit diagram by connecting with the MoS$_2$ NMOS and WSe$_2$ PMOS through an Au wire-bonding technique. To the best of our knowledge, this is the first demonstration of a 2D nanomaterial-based CMOS inverter circuit application through fully dried fabrication processes.

Figure 4. (**a**) Output characteristics curves of the WSe$_2$ field-effect transistors (FET) (driver) and MoS$_2$ FET (load) for complementary metal-oxide-semiconductor (CMOS) inverter circuit application; (**b**) VTC curves of our CMOS inverter circuit device at V_{DD} of −0.01 V, −0.1 V, and −1 V. The inset is the circuit diagram.

4. Conclusions

We demonstrated a solvent-free device fabrication method using an MB fiber-based shadow mask to minimize high-temperature and/or solvent-induced chemical degradation of semiconducting materials. This process effectively reduces the entire process protocols and the cost compared to the conventional photolithography. Moreover, the pattern size is easily tunable based on the diameter of the MB fiber (~1.5 μm). As a result, our WSe$_2$ PMOS shows excellent electrical performances, such as $\mu_{lin,max}$ of 205 cm^2/V·s, I_{ON} of ~−40 μA, and I_{ON}/I_{OFF} ratio of ~2×10^5 at $V_D = -0.1$ V, because this approach provides a high-quality interface between the semiconductor active channel and the metal S/D electrode. Lastly, we successfully achieved the CMOS inverter circuit demonstrations consisted of a WSe$_2$ PMOS as a driver and an MoS$_2$ NMOS as a load transistor. This micro-scaled shadow masking process exhibits a promising key technique to unlock the unlimited potential of materials for future advanced electronics.

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