Figures and Tables

Circuit Simulation Considering Electrical Coupling 3 in Monolithic 3D Logics with Junctionless FETs

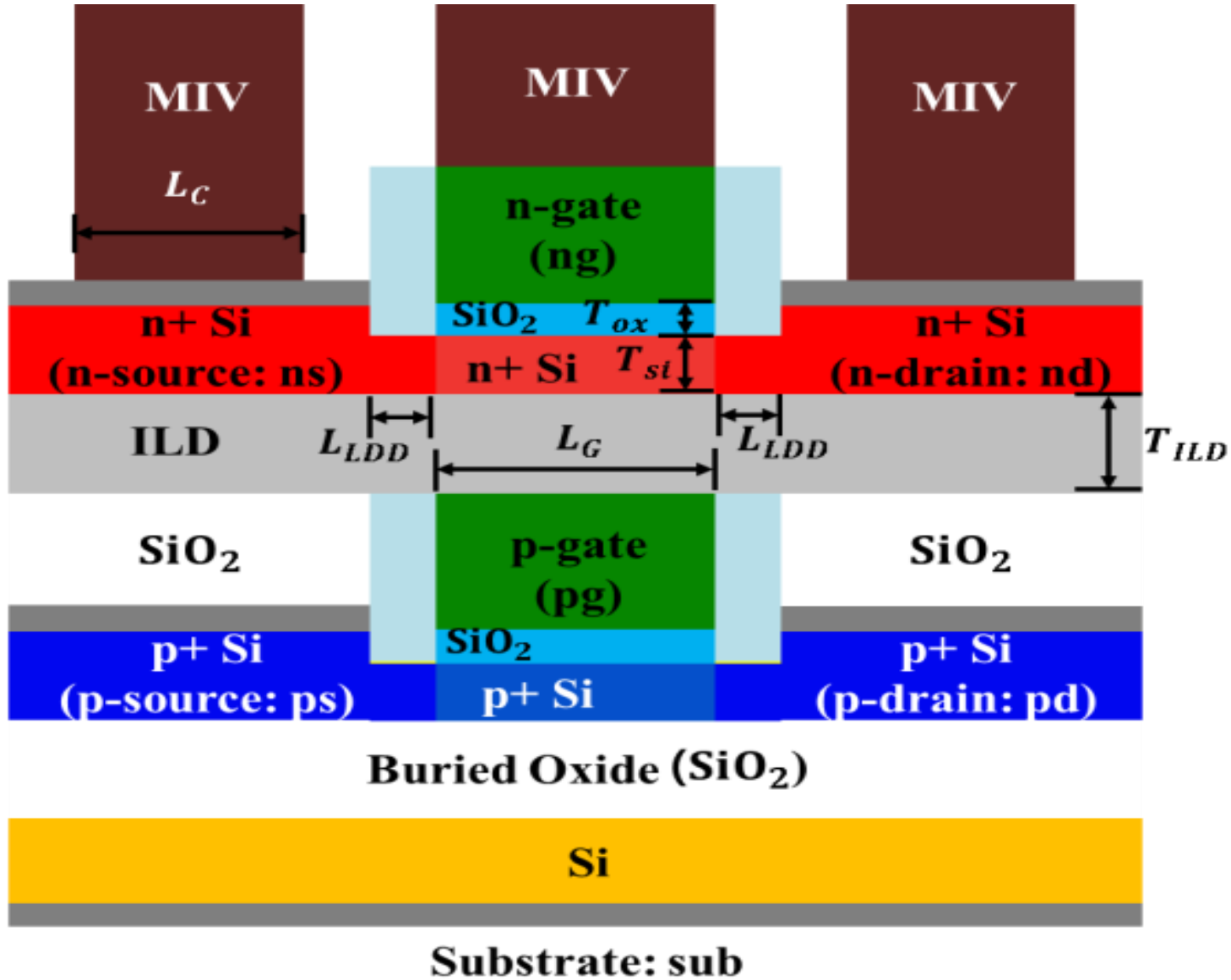
MIV
MIV
MIV
L_C
n-gate
(ng)
SiO_2
T_{ox}
T_{si}
n+ Si
(n-source: ns)
n+ Si
n+ Si
(n-drain: nd)
ILD
L_{LDD}
L_G
L_{LDD}
T_{ILD}
SiO_2
p-gate
(pg)
SiO_2
p+ Si
(p-source: ps)
p+ Si
p+ Si
(p-drain: pd)
Buried Oxide (SiO_2)
Si
Substrate: sub

Fig. 1(a)

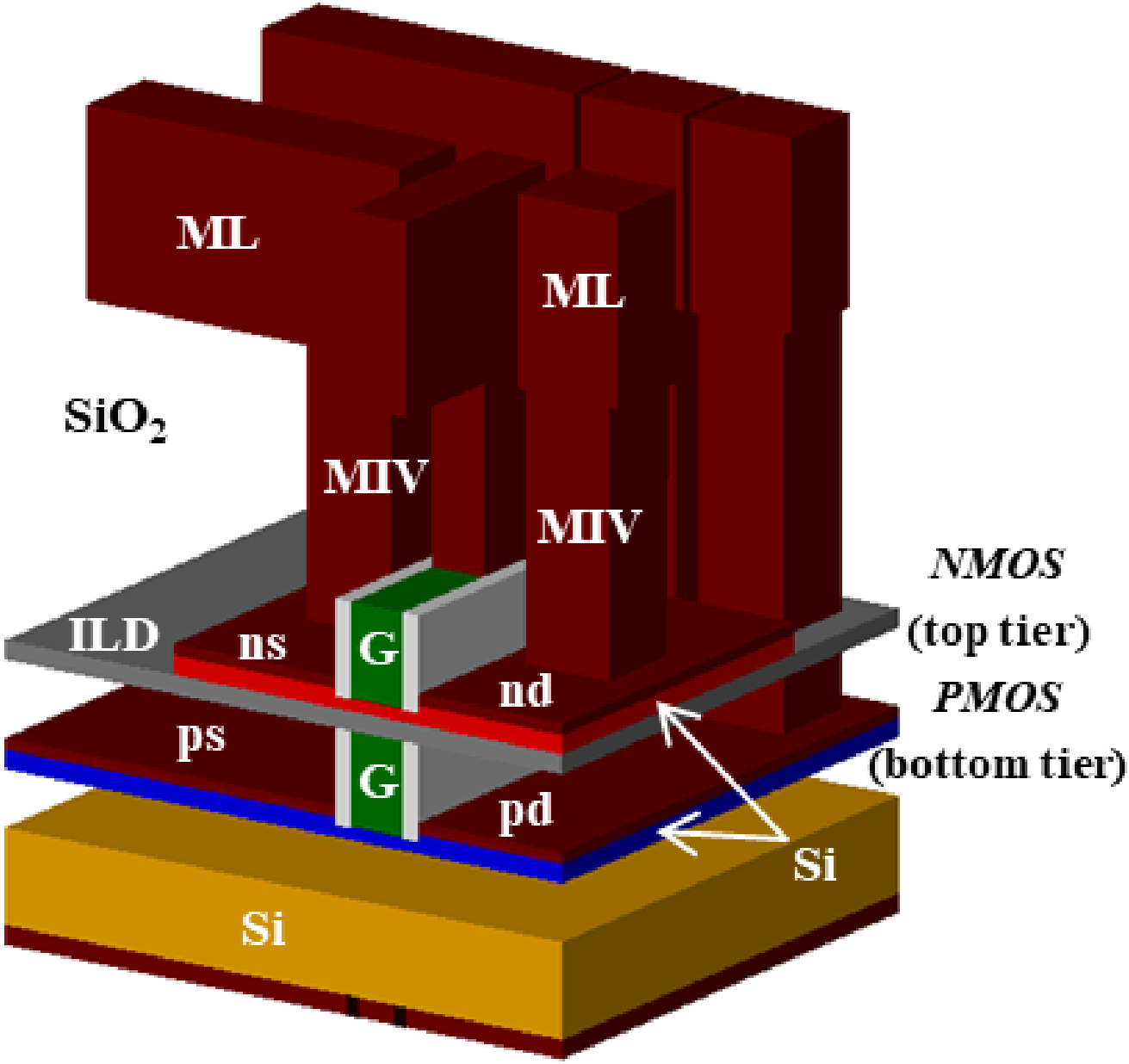
ML
ML
SiO_2
MIV
MIV
ILD
ns
G
nd
ps
G
pd
Si
Si
NMOS
(top tier)
PMOS
(bottom tier)

Fig. 1(b)

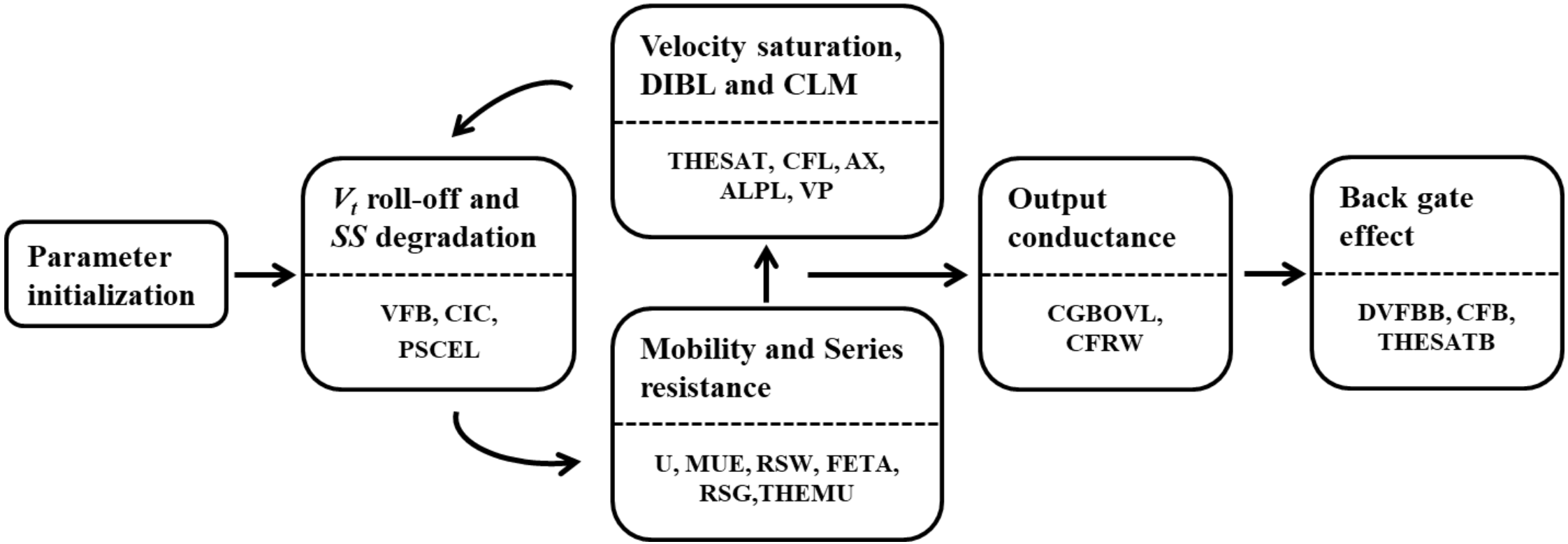
Parameter initialization
V_t roll-off and SS degradation
VFB, CIC, PSCEL
Velocity saturation, DIBL and CLM
THESAT, CFL, AX, ALPL, VP
Mobility and Series resistance
U, MUE, RSW, FETA, RSG,THEMU
Output conductance
CGBOVL, CFRW
Back gate effect
DVFBB, CFB, THESATB

Fig. 2

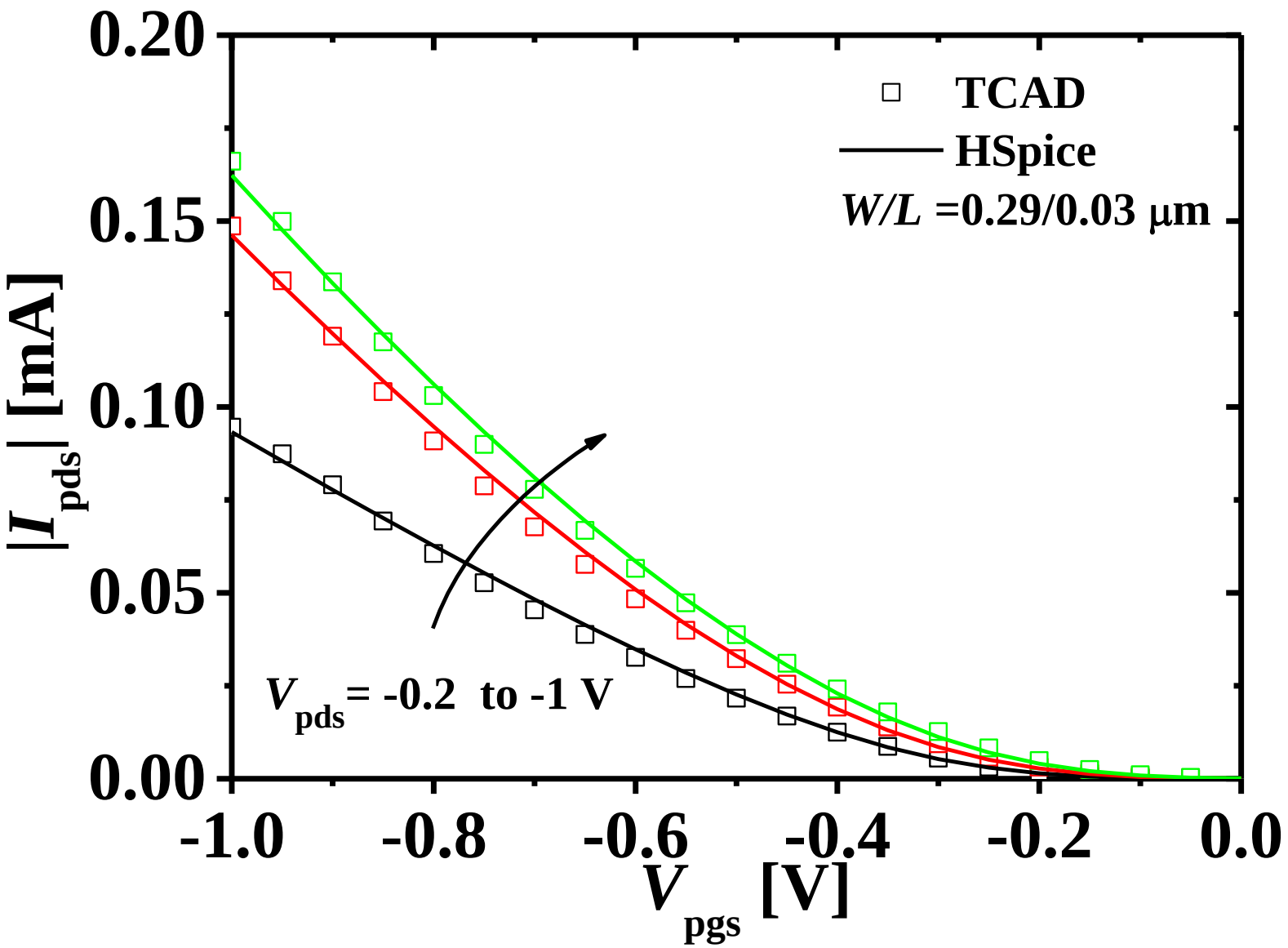
Bottom Transistor Ids-Vgs
TCAD
HSpice
W/L =0.29/0.03 μm
V pds = -0.2 to -1 V
|I pds| [mA]
V pgs [V]
0.20
0.15
0.10
0.05
0.00
-1.0
-0.8
-0.6
-0.4
-0.2
0.0

Fig. 3(a)

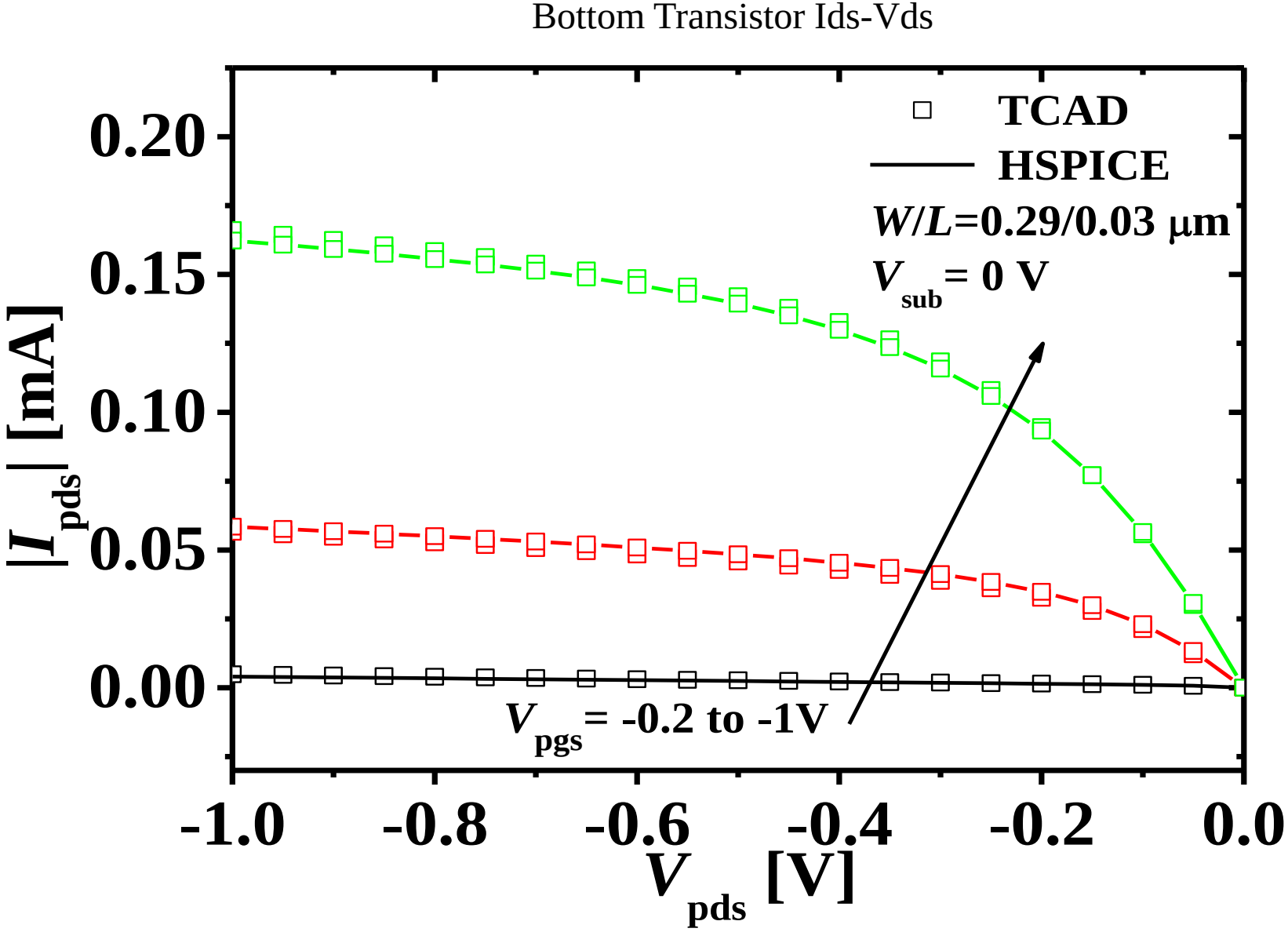
Bottom Transistor Ids-Vds
TCAD
HSPICE
W/L=0.29/0.03 μm
V sub = 0 V
V pgs = -0.2 to -1V
|I pds| [mA]
V pds [V]
0.20
0.15
0.10
0.05
0.00
-1.0
-0.8
-0.6
-0.4
-0.2
0.0

Fig. 3(b)

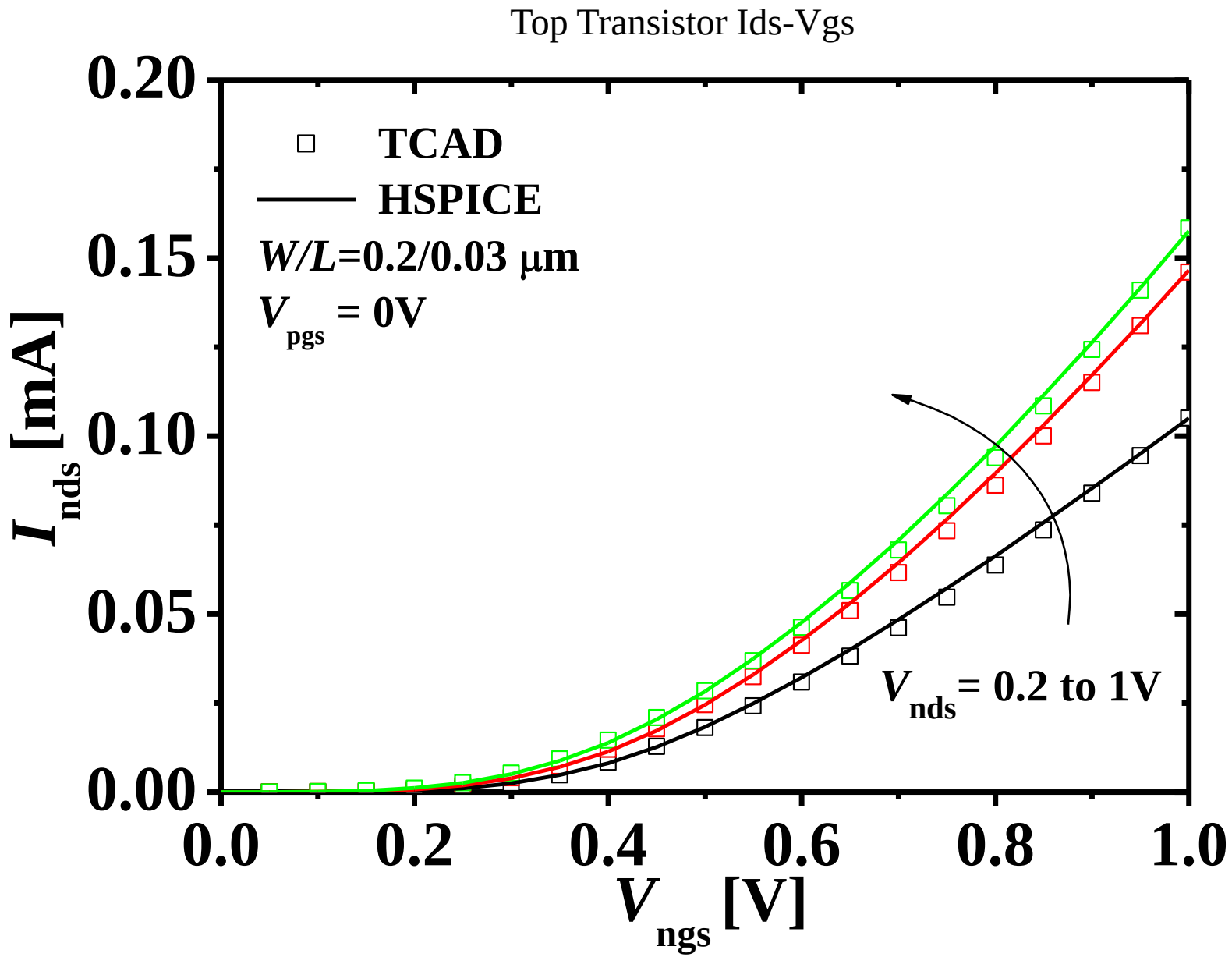
Top Transistor Ids-Vgs
0.20
0.15
0.10
0.05
0.00
0.0
0.2
0.4
0.6
0.8
1.0
TCAD
HSPICE
W/L=0.2/0.03 μm
V pgs = 0V
V nds = 0.2 to 1V
I nds [mA]
V ngs [V]

Fig. 4(a)

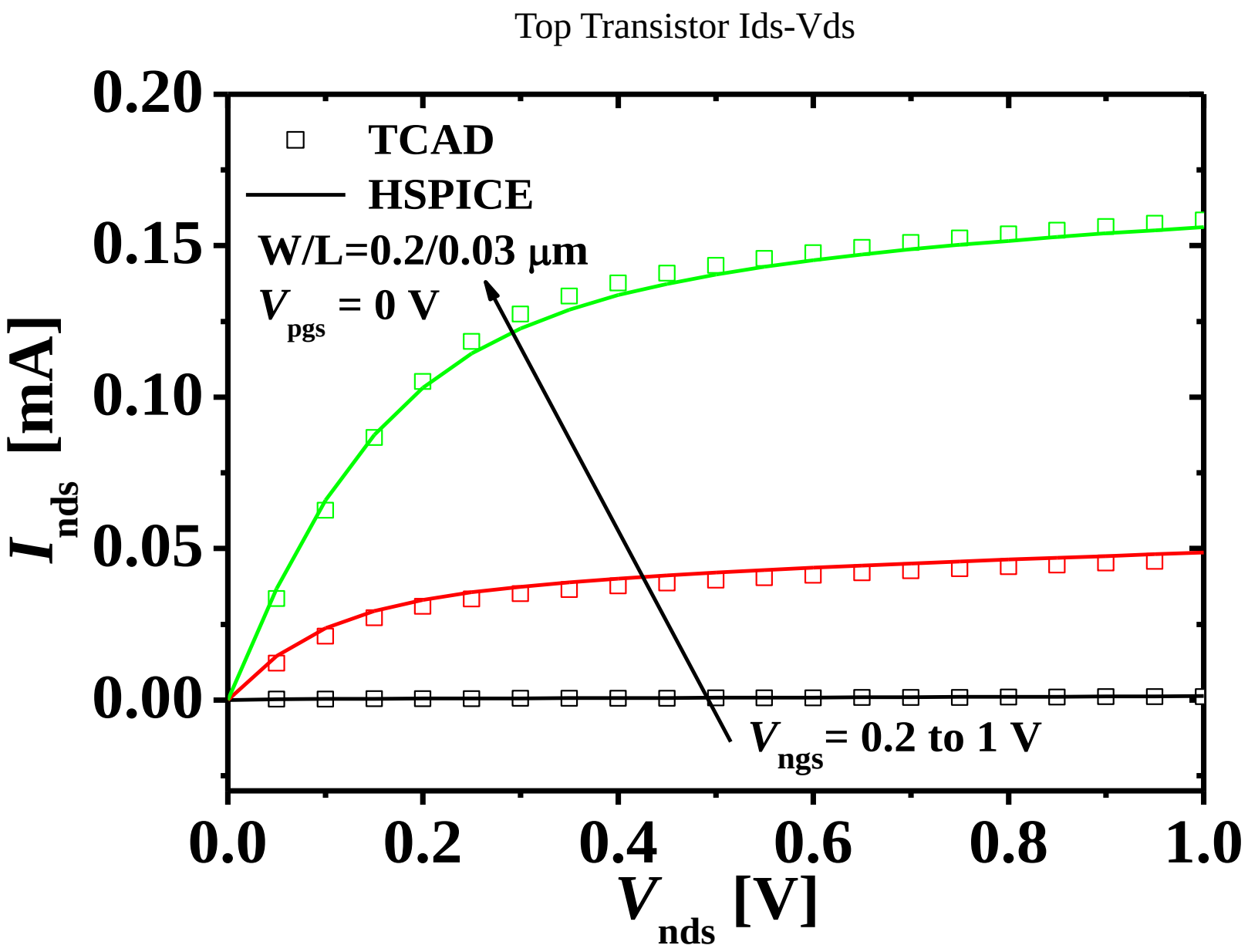
Top Transistor Ids-Vds
TCAD
HSPICE
W/L=0.2/0.03 μm
V_{pgs} = 0 V
V_{ngs} = 0.2 to 1 V
I_{nds} [mA]
V_{nds} [V]
0.20
0.15
0.10
0.05
0.00
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4(b)

Top Transistor Ids-Vds (at Vds=1V and Vbg=0V, 0.5V, 1V)

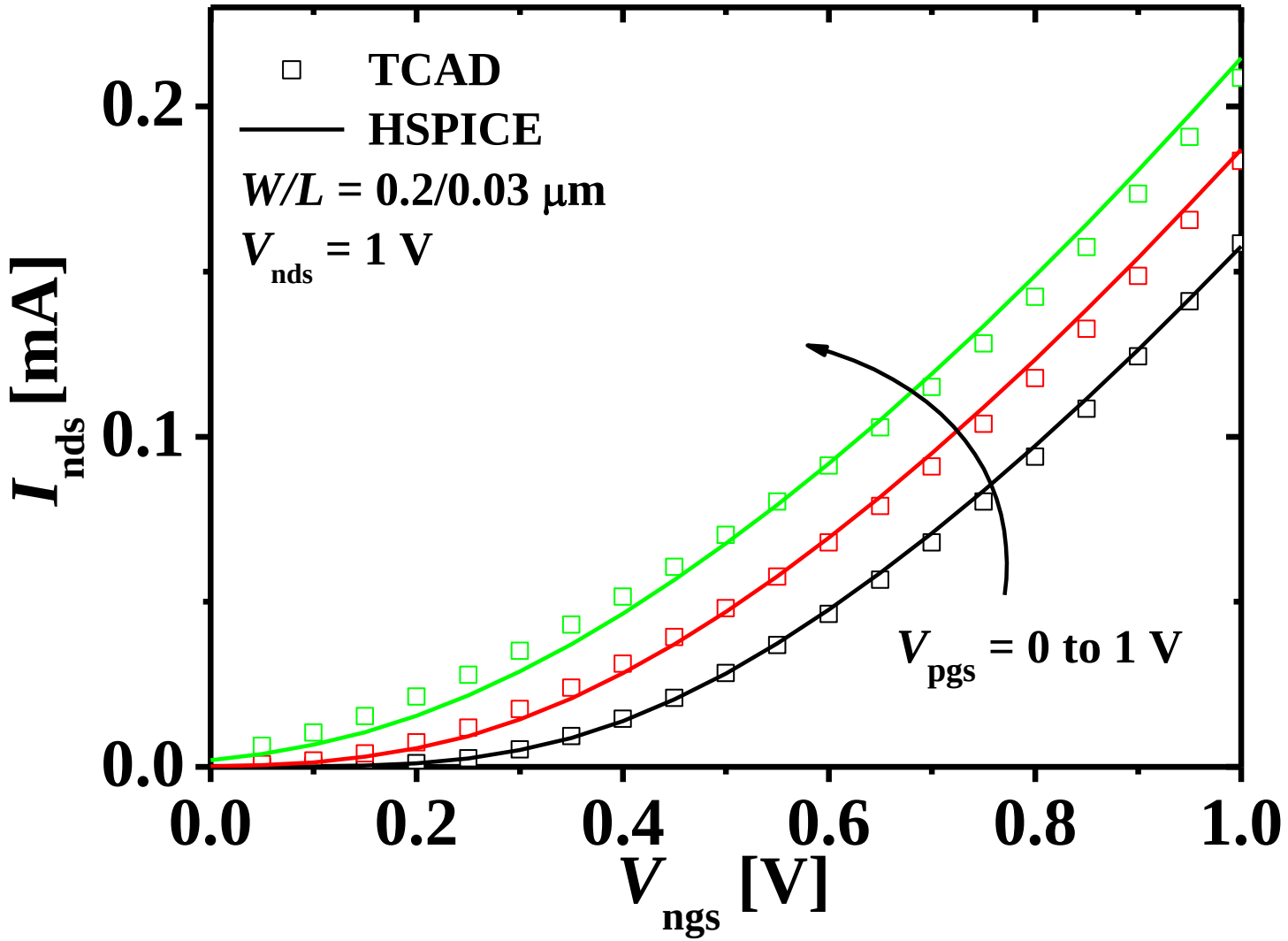

Fig. 5(a)

Top Transistor Ids-Vds

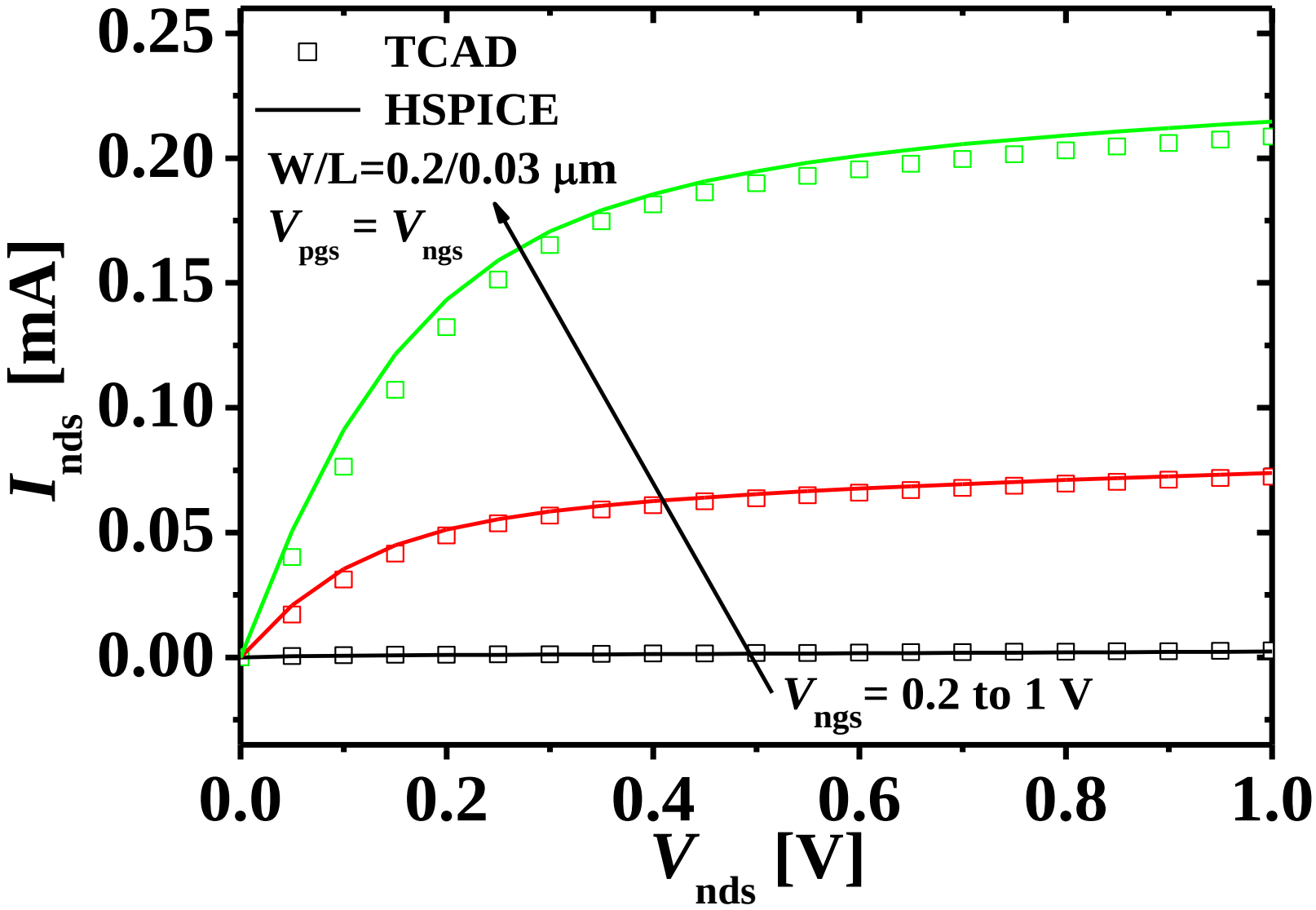

Fig. 5(b)

Bottom Origin Gm

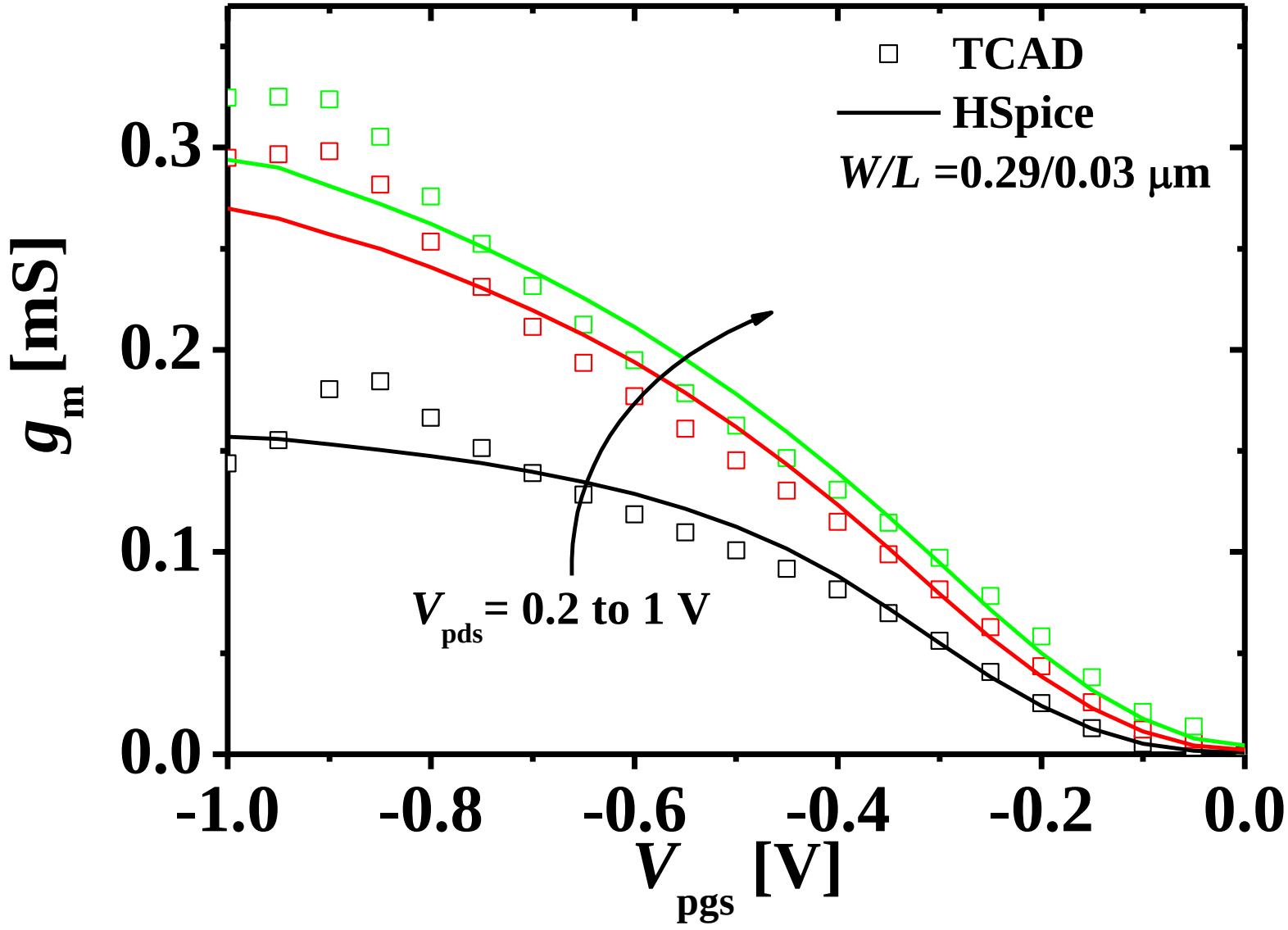

Fig. 6(a)

Bottom Origin Gm

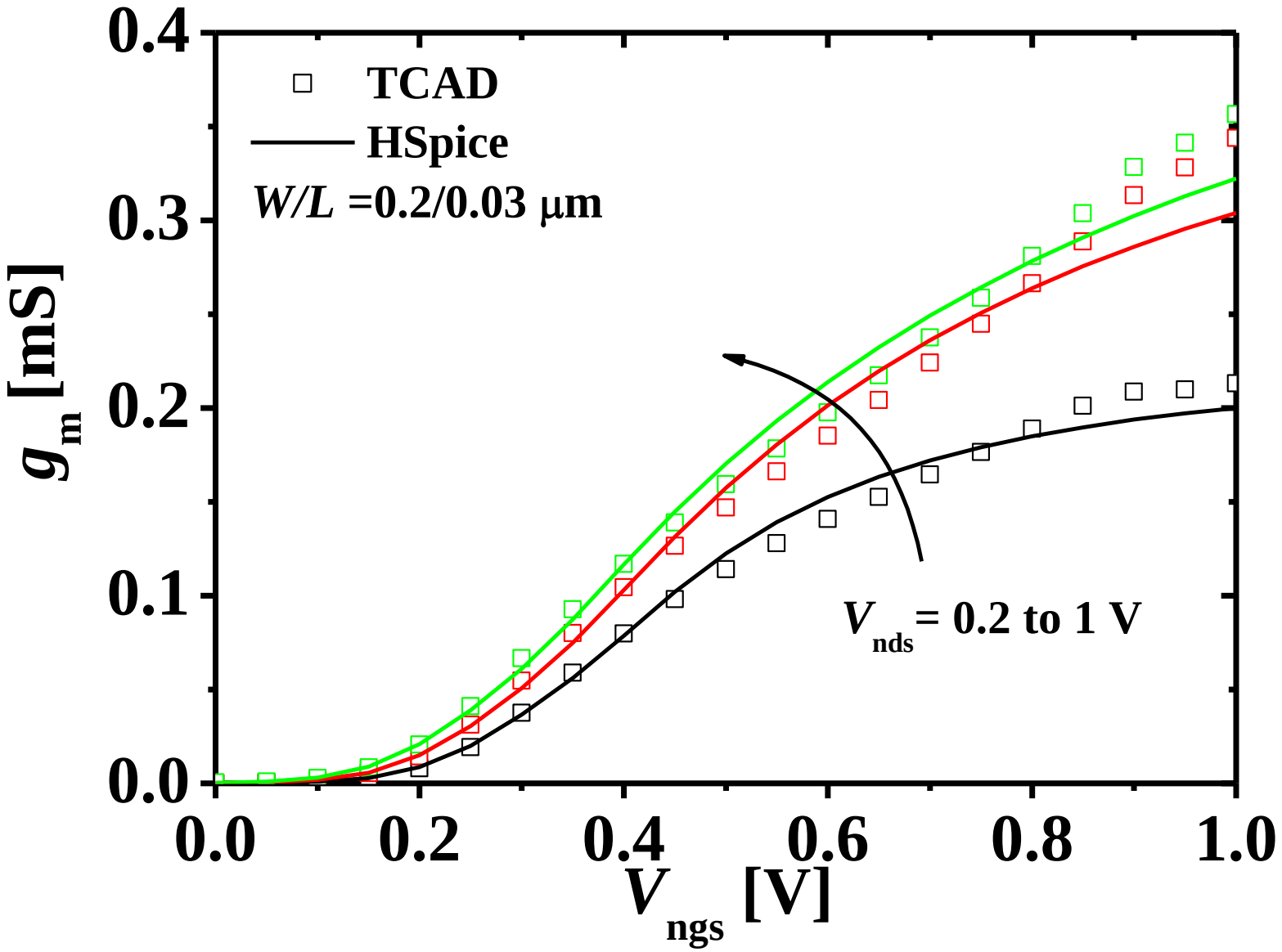

Fig. 6(b)

Bottom Origin Gm

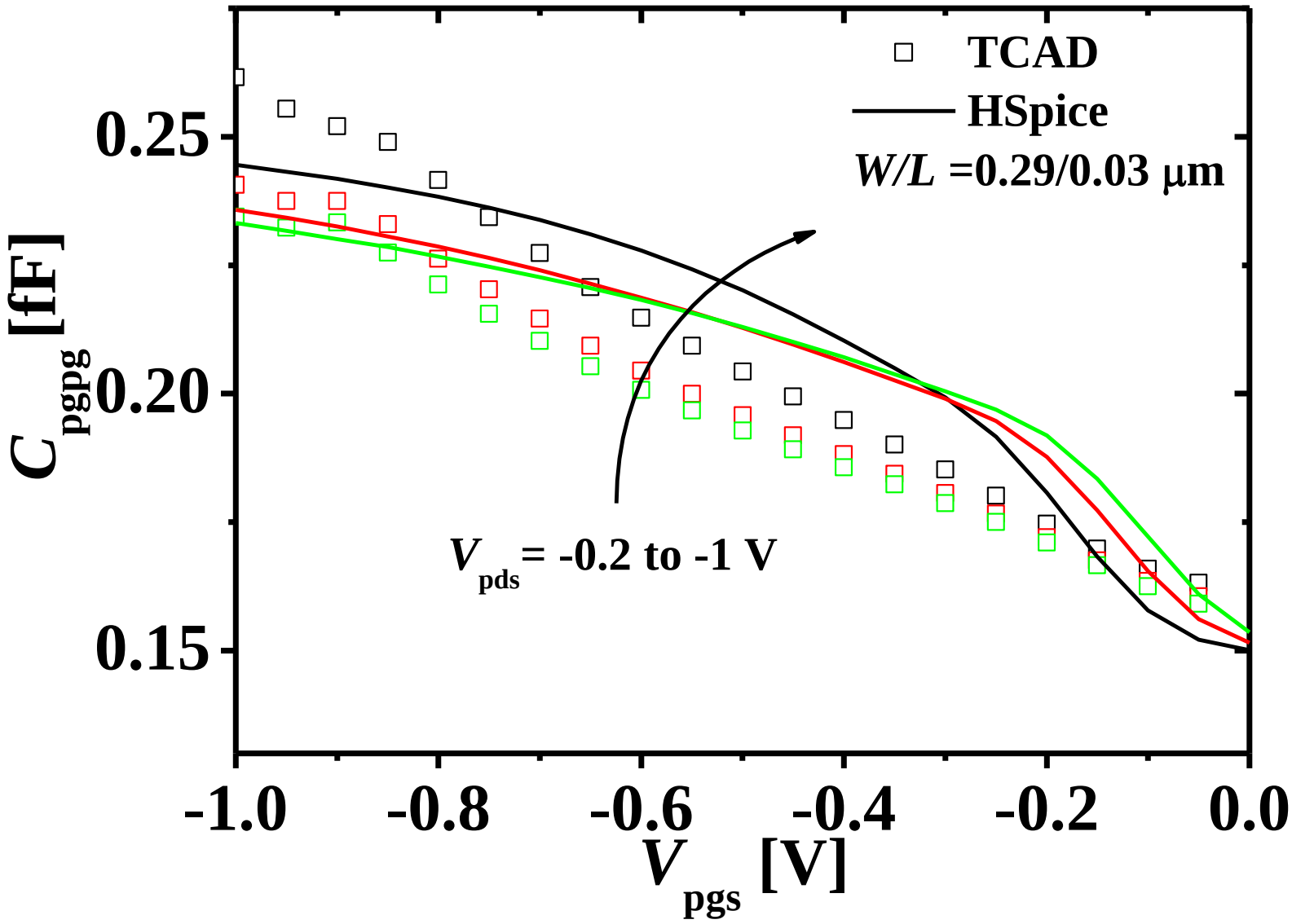

Fig. 7(a)

Bottom Origin Gm

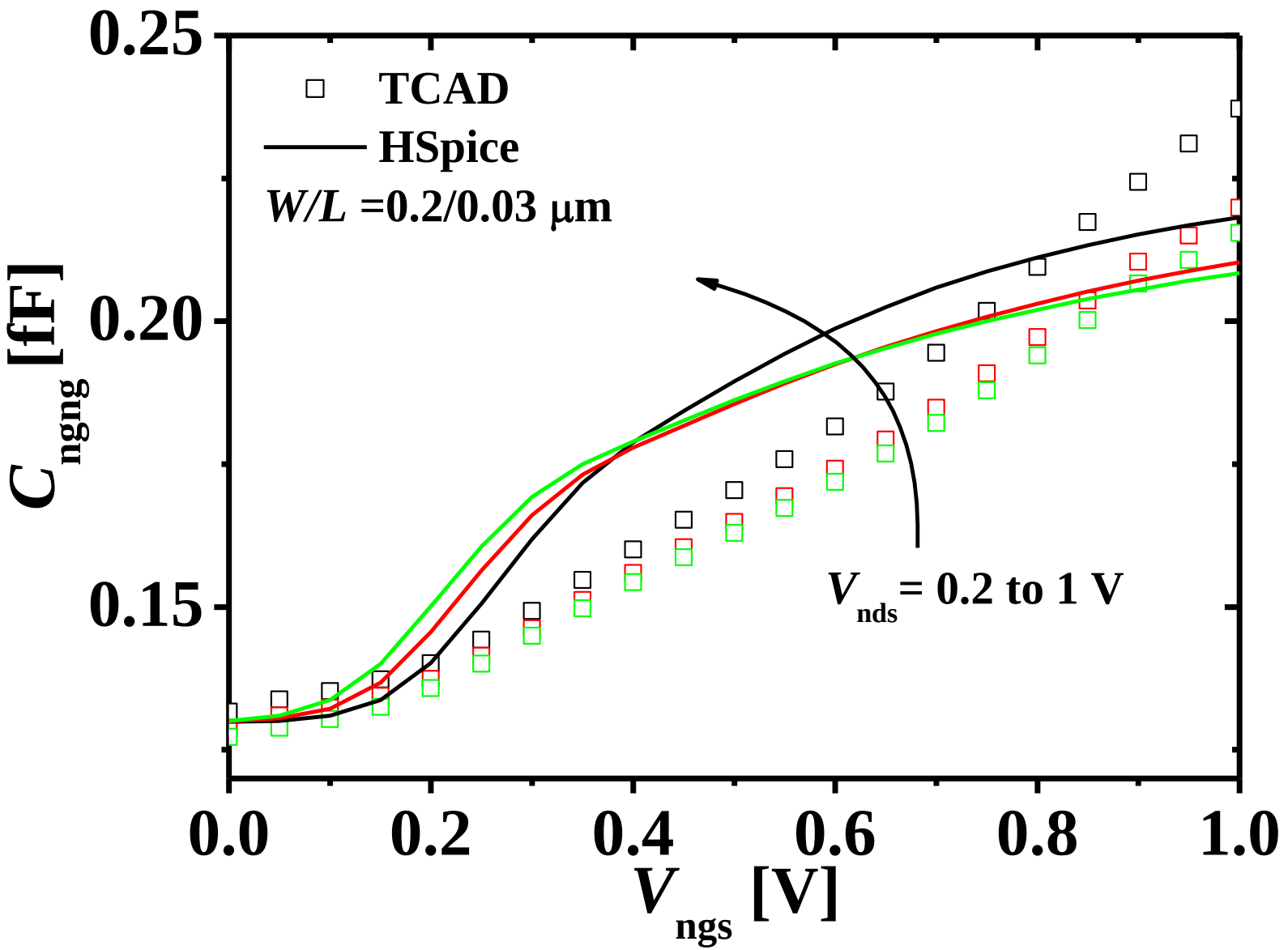

Fig. 7(b)

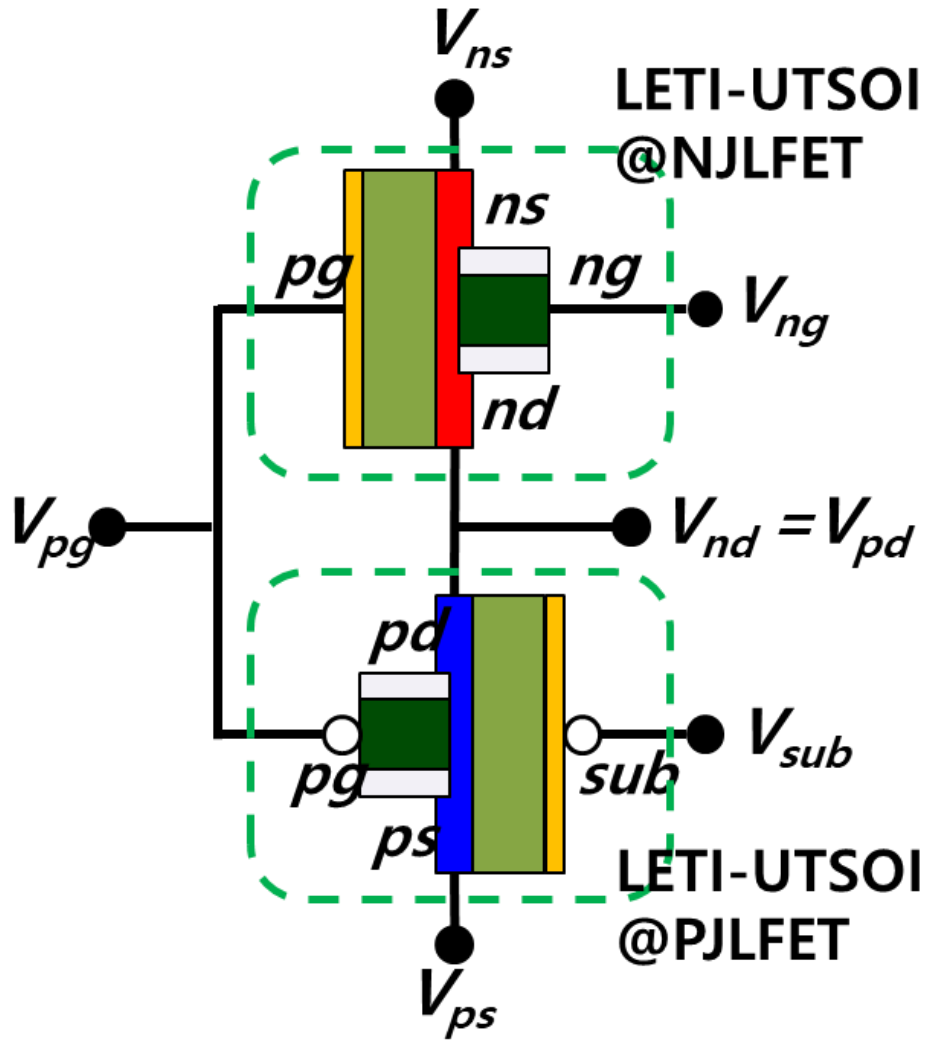
V_{ns}
LETI-UTSOI
@NJLFET
ns
pg
ng
V_{ng}
nd
V_{pg}
$V_{nd} = V_{pd}$
pd
pg
sub
V_{sub}
ps
LETI-UTSOI
@PJLFET
V_{ps}

Fig. 8(a)

3DIC Inverter VTC

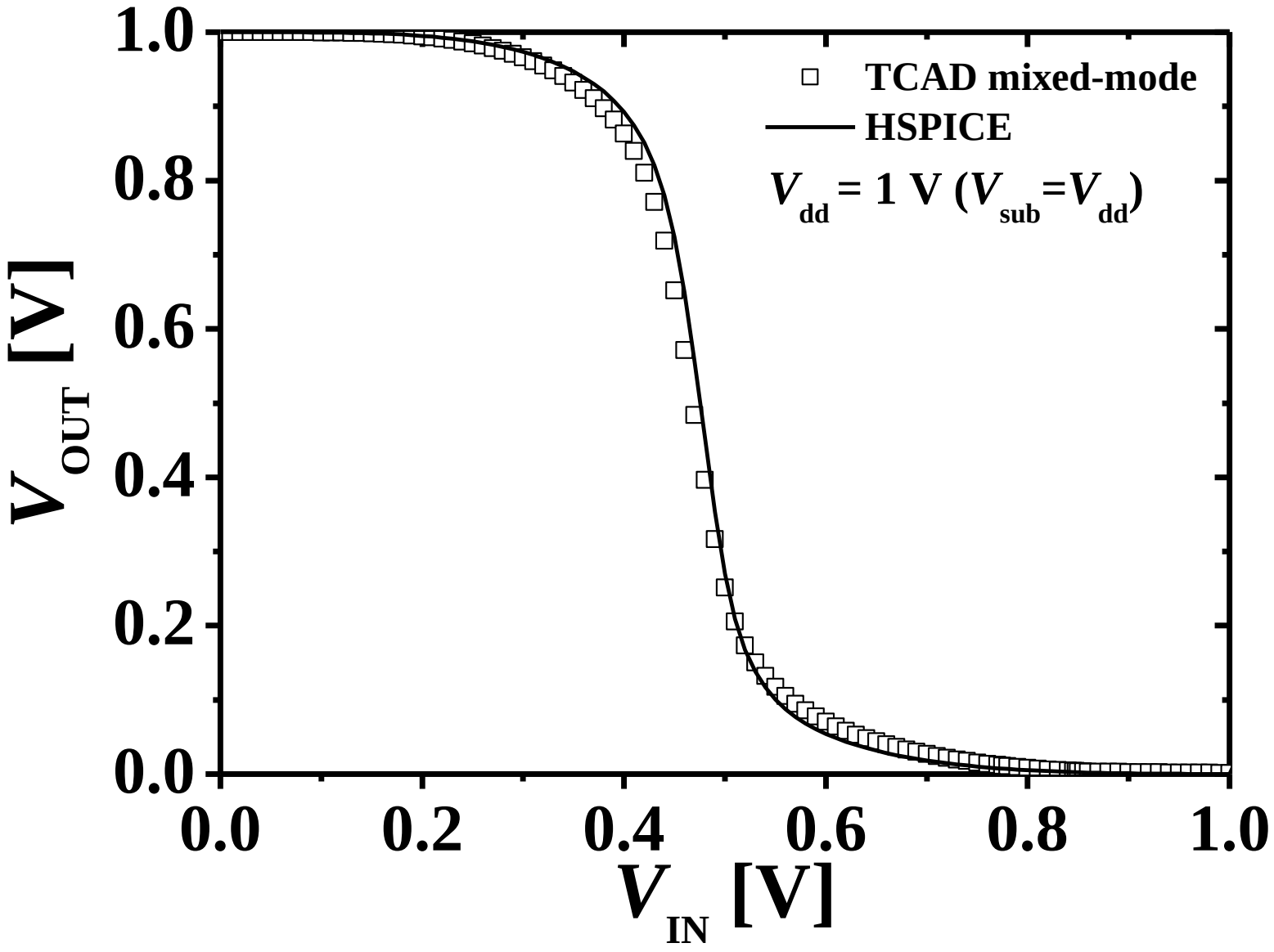

Fig. 8(b)

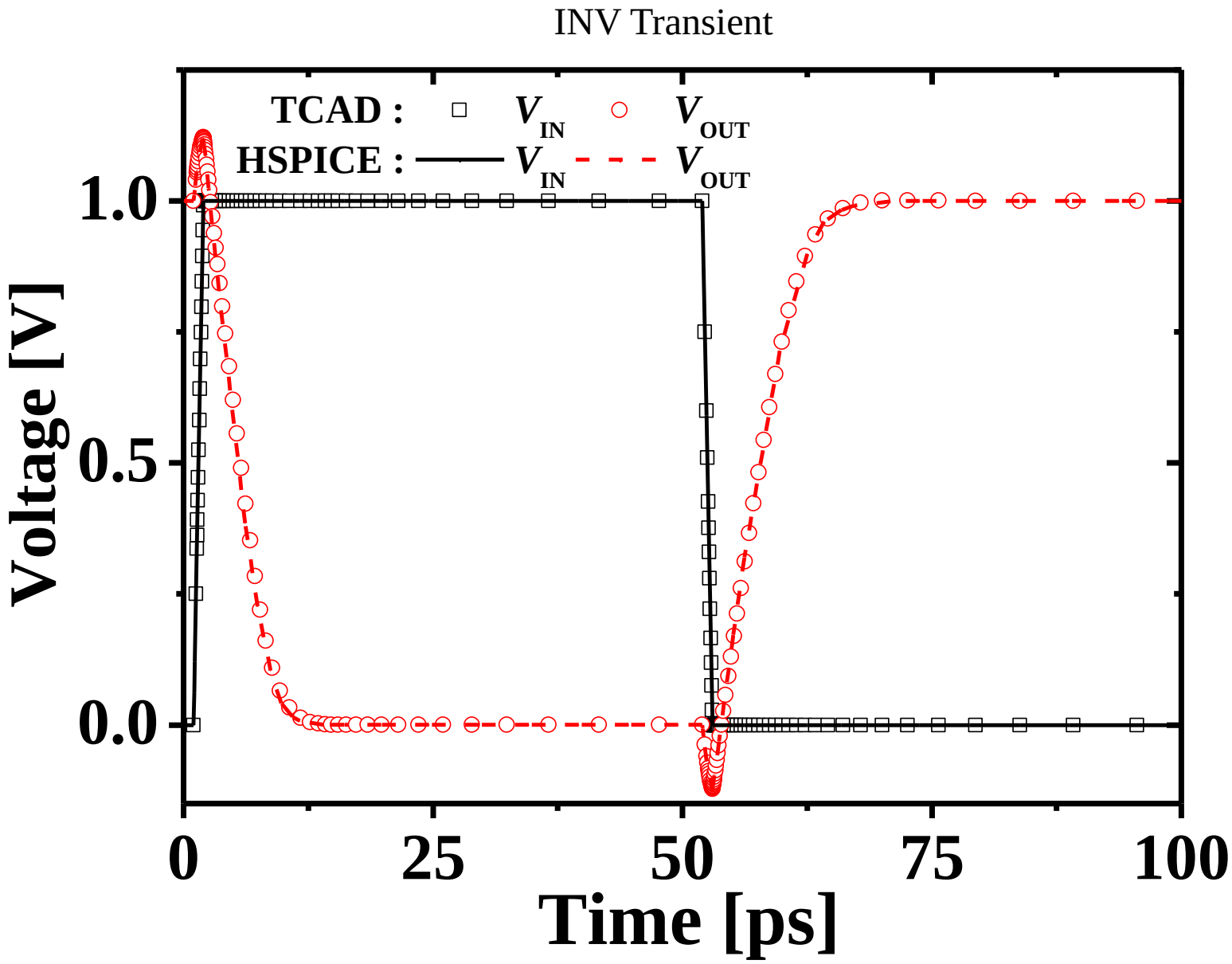
INV Transient
TCAD : V_{IN} V_{OUT}
HSPICE : V_{IN} V_{OUT}
1.0
0.5
0.0
Voltage [V]
0
25
50
75
100
Time [ps]

Fig. 9

Table 1. Description and dimensions of models/parameters used in TCAD simulation

Models/Parameters	Description	Value/Unit
CVT	Lombardi model and complete mobility model including doping density N, temperature T, and transverse electric field E//.	–
SRH	Shockley–Read–Hall recombination model	–
BGN	Band gap narrowing model	–
AUGER	Auger recombination model	–
FERMI	Fermi–Dirac carrier statistics	–
NEWTON	Newton method which solves a linearized version of the entire nonlinear algebraic system	–
GUMMEL	GUMMEL method, which solves a sequence of relatively small linear subproblems	–
ΦN	Gate work function of N-type JLFET	5.06 eV
ΦP	Gate work function of P-type JLFET	4.41 eV

Table 2. Summary of the extracted parameters of the LETI-UTSOI model for the bottom P-type and top N-type JLFET.

Parameter	Unit	Description	Value	
			P-type	N-type
DLQ	m	Effective channel length offset for CV	$2e^{-8}$	$1e^{-8}$
VBFO	V	Geometry-independent flat-band voltage	0.29	-0.28
CICO	–	Geometry-independent part of substrate bias dependence factor of in terface coupling	0.65	3
PSCEL	–	Length dependence of short channel effect above threshold	0.5	0.1
CFL	V^{-1}	Length dependence of DIBL parameter	2.7	2
UO	$m^2/V/s$	Zero-field mobility	$6.5e^{-3}$	$1.75e^{-2}$
MUEO	m/V	Mobility reduction coefficient	1	1
THEMUO	–	Mobility reduction exponent	1.22	1.8
RSGO	–	Gate-bias dependence of RS	2	1
THESATO	V^{-1}	Geometry-independent Velocity saturation parameter	1.8	2.7
THESATBO	V^{-1}	Substrate bias dependence of velocity saturation	0.1	0.28
FETAO	–	Effective field parameter	0	-3
AXO	–	Geometry-independent of linear/ saturation transition factor	1.6	1.6
ALPL1	–	Length dependence of CLM pre-factor ALP	0.0005	0.00001
VPO	V	CLM logarithm dependence factor	0.04	0.04
CFRW	F	Outer fringe capacitance	$2e^{-16}$	$2e^{-16}$

Table 3. FO3 ring oscillator performance Using M3DINV models (MOSFET and JLFET).

Stages	Power [*mW*]		Frequency [GHz]		Delay per stage [ps]	
	MOSFET	**JLFET**	**MOSFET**	**JLFET**	**MOSFET**	**JLFET**
3	281	275 (-2.13%)	18.7	18.18 (-2.78%)	9.04	9.165 (1.38%)
19	279	277 (-0.71%)	2.88	2.86 (-0.69%)	9.16	9.18 (0.2%)
101	281	283 (0.71%)	0.52	0.52 (0%)	9.28	9.35 (0.7%)

Table 4. Performance comparison of MOSFET and JLFET M3D logics

Performances	MOSFET					JLFET				
	INV	**NAND**	**NOR**	**MUX**	**D-FF**	**INV**	**NAND**	**NOR**	**MUX**	**D-FF**
Static power [nW]	4.89	1.63	2.41	4.21	17.4	10.6 (116.7%)	1.67 (2.45%)	3.12 (29.4%)	7.5 (78.1%)	27.9 (60.3%)
Dynamic power [μW]	9.85	13.9	13.8	22.6	41.9	16.5 (67.5%)	14.2 (2.15%)	14.3 (3.62%)	26.5 (17.2%)	47.8 (14%)
Average delay [ps]	4.17	5.45	5.22	2.3	10.25	4.65 (11.5%)	6.62 (21.4%)	5.29 (1.34%)	2.74 (19.1%)	11.9 (16%)
Static power [nW]	4.89	1.63	2.41	4.21	17.4	10.6 (116.7%)	1.67 (2.45%)	3.12 (29.4%)	7.5 (78.1%)	27.9 (60.3%)