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Matrix Mapping on Crossbar Memory Arrays with Resistive Interconnects and Its Use in In-Memory Compression of Biosignals

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Abstract: Recent advances in nanoscale resistive memory devices offer promising opportunities for in-memory computing with their capability of simultaneous information storage and processing. The relationship between current and memory conductance can be utilized to perform matrix-vector multiplication for data-intensive tasks, such as training and inference in machine learning and analysis of continuous data stream. This work implements a mapping algorithm of memory conductance for matrix-vector multiplication using a realistic crossbar model with finite cell-to-cell resistance. An iterative simulation calculates the matrix-specific local junction voltages at each crosspoint, and systematically compensates the voltage drop by multiplying the memory conductance with the ratio between the applied and real junction potential. The calibration factors depend both on the location of the crosspoints and the matrix structure. This modification enabled the compression of Electrocardiographic signals, which was not possible with uncalibrated conductance. The results suggest potential utilities of the calibration scheme in the processing of data generated from mobile sensing or communication devices that requires energy/areal efficiencies.

Keywords: resistive memory; crossbar; in-memory computing; analogue computing; matrix-vector multiplication; ECG

1. Introduction

Emerging classes of mobile electronic devices offer attractive capabilities for real-time analytics of the physical world through the connection to central computing systems. One of the critical challenges in this emerging Internet of Things (IoT) is the instantaneous extraction of relevant information from the abundant data with the limited power and communication bandwidth for data transmission. This challenge demands smart components on the edge of the mobile devices that can filter, compress, or classify the data outputs onsite [1–4]. This pre-processing needs to be extremely power efficient and quick to handle the large volume of data continuously generated from the surrounding world.

A subset of the processing operations can be categorized as a linear transformation which can be expressed as a matrix-vector multiplication (MVM). The MVM can be performed in an analogue domain using a resistive memory crossbar array by storing the matrix values as the conductance of the memory cell. The operation can take a constant time complexity ($O(1)$), and be energy efficient owing to the functional integration of the processing and memory units [5–7]. The scalability of the crossbar structure down to $4F^2$ (F : feature size of a technology node) is also beneficial for the device miniaturization. Envisioned applications include linear equation solver and training of or inference on neural networks as demonstrated recently [1,7–11].

Prior studies have shown that the throughputs per area and the energy efficiency can exceed today's von Neumann computing scheme, but computational accuracy remained as a non-trivial challenge for high-precision analogue-based MVM. In device levels, output errors can be originated from the variations of the electrical characteristics between the cells, non-linear current-voltage relationship, and stochasticity in resistance switching process. Separate from the efforts in development of the reliable devices, it is also important to optimize the conductance mapping scheme using realistic crossbar arrays. Finite conductivity of interconnecting wire has been suggested as one of the important factors causing errors in the crossbar-based MVM [9,12]. Empirical calibration methods that are based on the comparison between the desired output and real measurements have shown to improve the accuracy level although the origin of the discrepancy of the measurement values was not clearly identified [1]. To overcome the limitation of such hardware-based methods, model-based theoretical analysis attempted more systematic approach to understand the computational error [9,12]. Hu et al. first introduced a comprehensive crossbar array model for MVM, and applied it to the training of neural network for pattern recognition [9]. This simulation-based optimization of the conductance minimizes the time and power consumption to post-process the outputs and provides explanation for the computational outputs with given circuits.

This work implemented a mapping algorithm of memory conductance for MVM using a crossbar model with finite wire resistance, and analyzed the calibration performance for the compression of electrocardiographic (ECG) signals. An iterative software simulation calculates the matrix-specific local junction voltages at each cross-point, and calculate the ratio between the junction voltages and input voltage applied from the source. The ratio becomes a calibration factor to update the memory conductance to systematically compensates the voltage drop. The results indicate that the calibration factors both depend on the location of the junctions and matrix structure. This correction enabled the in-memory compression of ECG signals whose reconstruction error is comparable to the double precision calculation. The findings suggest a possible route to overcome difficulties in analogue computing in realizing diverse edge computing devices for onsite data processing.

2. Methods

2.1. Calibration Factor for Matrix Mapping on Proposed Crossbar Model

Figure 1a shows a schematic representation of the crossbar model that includes interconnection line resistance to calculate the local potential at each cross-point. The model incorporates both the cell-to-cell resistance and the access resistance from a voltage source to the first column/row metal lines. The analogue-based MVM using a crossbar array assuming an ideal behavior has the current output from the column (or bit) line (BL) as follows.

$$I_j^{ideal} = G_{1,j}V_{1,app} + \dots + G_{m,j}V_{m,app} \quad (1)$$

Here, I_j^{ideal} is the current output from j^{th} BL. $G_{i,j}$ is the conductance of memory cell located at a crosspoint of the i^{th} word and the j^{th} bit lines. The conductance ($G_{i,j}$) represents a linear-transformed matrix element to map the matrix values within the range of the achievable conductance of the device. $V_{i,app}$ is input voltage to the i^{th} word lines (WL). (BLs are assumed to be grounded.) Equation (1) holds true only if the series resistance of the interconnection wires is negligible. Considering the resistivity of conventional metal wires ($\rho = 10^{-8}$ to $10^{-7} \Omega \cdot m$), the resistance between the nearest cells ($R = \rho F / (F \cdot d)$, F : feature size, d : metal thickness) ranges from 10^0 to $10^1 \Omega$ when d is assumed ~ 10 nm. The wire resistance may further increase due to lower density caused by vapor deposition. For a $4F^2$ crossbar structure, the interconnect resistance between two adjacent cells can be estimated to be $\sim 4.53, 2.97$, and 1.55Ω under 16 nm, 22 nm, and 32 nm technology node, respectively, according to the International Technology Roadmap for Semiconductors 2013 [12]. Simple calculation estimates the voltage drop can be a significant source of errors considering the realistic conductivity of the resistive

memories. For example, if we assume ~100 by 100 bits of crossbar arrays and 0.1 to 1 mA total current along the word line, iR drop at the end of the word line can be 0.01 to 0.1V. (e.g., $0.1\text{--}1\text{ mA} \times R(\text{cell-cell}) \times 100 \rightarrow 0.01\text{--}0.1\text{ V}$). In this realistic case, the current output needs to be modified as

$$I_j^{real} = G_{1,j}V_{1,j} + G_{2,j}V_{2,j} + \dots + G_{m,j}V_{m,j} \quad (2)$$

instead of Equation (1) with $V_{i,app}$ terms to conform with the Ohm's law. Here, $V_{i,j}$ is the local junction potentials across the memory cell at (i, j) crosspoint. Since $V_{i,j}$ is not guaranteed to be equal to the applied voltage to the i^{th} WL due to voltage drop, I_j becomes small compared to the ideal case as observed in previous studies [1,9].

One way to compensate the smaller current output can be the increase of the conductance level of the memory according to the local voltage drop. If the voltage drop for arbitrary WL and BL input voltages can be estimated, the conductance of the memory can be set as

$$G'_{i,j} = G_{i,j} \frac{V_{i,app}}{V_{i,j}} \quad (3)$$

instead of $G_{i,j}$. With the calibrated conductance ($G'_{i,j}$), the current outputs become the ideal current as follows.

$$I_j^{real} = G_{1,j} \frac{V_{1,app}}{V_{1,j}} \cdot V_{1,j} + \dots + G_{m,j} \frac{V_{m,app}}{V_{m,j}} \cdot V_{m,j} = I_j^{ideal} \quad (4)$$

Thus, the ratio ($V_{i,app}/V_{i,j}$) can be considered as a calibration factor for the memory conductance for in-memory MVM when the junction potential deviates from the applied voltage. There can be other approaches that use equivalent conductance terms multiplied by the applied voltage to describe the measured current. This approach may be useful if measurement data are available and the calibration algorithm to drive the real current to the ideal one is developed. Yet, the current work is more focused on the calibration based only on theoretical model circuits without requirement for any real measurements.

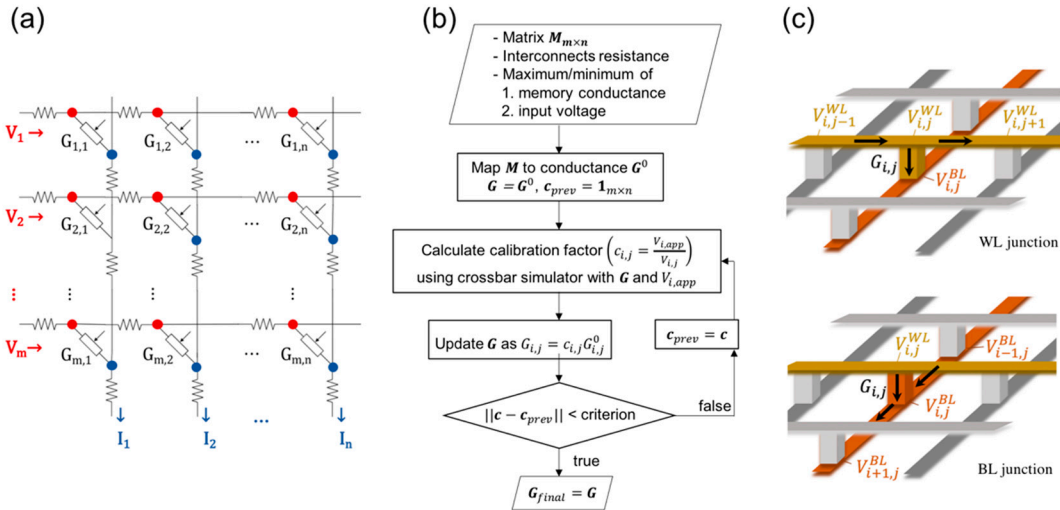


Figure 1. (a) Simulation model for resistive memory crossbar array with finite conductance of interconnects. (b) Conductance calibration algorithm for mapping of an $m \times n$ matrix using a crossbar simulator. (c) Local currents at word lines (WL) and bit line (BL) junctions in accordance with Kirchhoff's law.

2.2. Iterative Calibration Based on Crossbar Simulation

An iterative algorithm was developed to progressively increase conductance values based on the simulated $V_{i,j}$ at individual junctions. Figure 1b summarizes the procedure of the calibration process.

Through the iterations, $V_{i,j}$'s are updated by solving the $2mn$ Kirchhoff's relations (mn WL junctions + mn BL junctions) that need to be simultaneously satisfied with given memory conductance and the voltage inputs [13]. Figure 1c, for example, illustrates the local currents on the WL junction that follow the equation below.

$$G_w(V_{i,j}^{WL} - V_{i,j-1}^{WL}) = G_{i,j}(V_{i,j}^{BL} - V_{i,j}^{WL}) + G_w(V_{i,j+1}^{WL} - V_{i,j}^{WL}) \quad (5)$$

Here, G_w is a cell-to-cell conductance, and $V_{i,j}^{WL}$ and $V_{i,j}^{BL}$ are voltages at (i, j) crosspoint on WL and BL, respectively. $2mn$ Kirchhoff's equations can be arranged in a simple matrix form whose details are described in the Appendix A. Since the calibrated conductance ($G'_{i,j}$) is higher than the previous conductance ($G_{i,j}$), the overall current increases, and the voltage drops need to be recalculated with this new $G'_{i,j}$ by the next iteration of the simulation. The iteration is repeated until the conductance (or $V_{i,app}/V_{i,j}$ ratios) converge, and the final ratios determine the conductance level of the memory to represent the arithmetic matrix elements. The simulation code is implemented in MATLAB and each iteration takes ~ 1 sec with single 3.5 GHz Intel Core i7 for 64×64 crossbar arrays. The calibration factors were converged after 10 to 20 iterations depending on the cell-to-cell resistance and termination criteria. The runtime and error depend on the termination criteria, and assumed to be a similar level to the previous report [9].

3. Results and Discussion

The in-memory MVM can be used for low-power data processing, such as compression or high- or low-pass filtering. Here, as an example, the discrete wavelet transform (DWT) matrix is mapped to the final memory conductance ranging from 0.01 to 70 μ S [14,15]. The cell-to-cell resistance (R) and the access resistance from the voltage source to the crossbar are assumed to be 1 Ω and 100 Ω , respectively. Larger R (10 Ω) is also studied for comparison. Voltages are supplied from the left for WLs and the bottom for BLs. For the calculation of the voltage drops at each junction, the supply voltage of 0.1 V was assumed for all WLs. (The calibration factors were insensitive to the voltage (0.1 to 0.5 V) since $V_{i,j} \sim V_{i,app} - iR$ where iR varies approximately with the same factor as $V_{i,app}$). The operation parameters were set to be consistent with the practical values reported in the previous PRAM-based studies [7].

Figure 2 presents the simulation results of the conductance mapping of 64×64 DWT matrix using biorthogonal filters with 4-level of decomposition. Figure 2a describes the change in the calibration factors through the iteration represented by the 2-norm of the difference matrix. The conductance is quickly converged, and the norm values less than 10^{-4} were achieved after 10 cycles ($R = 1 \Omega$) and 16 cycles (10 Ω). Figure 2b compares the initial conductance ($G_{i,j}^0$) and final conductance for $R = 10 \Omega$ case. Figure 2c plots the final calibration factors to visualize the voltage drop across the crossbar. ($R = 1 \Omega$ (left), 10 Ω (right)) Calibration factors range from 1.1 to 1.4 for 1 Ω case, and 1.1 to 2.2 for 10 Ω case. 10 Ω resistance shows larger dependency of the calibration factor on the distance from the voltage source. The location dependency of the calibration factors implies that the effect of possible fluctuation in the resistance of nanoscale wires can be averaged over the long distance from the voltage source for the junctions with large calibration factors. The colormaps also reveal the large values for the first four columns and small values for every four rows. As depicted in Figure 2d, the calibration factors reflect the matrix structure. The conductance sum ($\sum_i G_{i,j}^0$) is large for the first four columns, which results in a large current gathered along the four BLs. For the same reason, the small conductance sum ($\sum_j G_{i,j}^0$) for every four rows result in small overall current along the WLs: thus, smaller calibration factors. This variation in the overall current along the metal line causes different level of iR drop, resulting in matrix-dependent calibration factors.

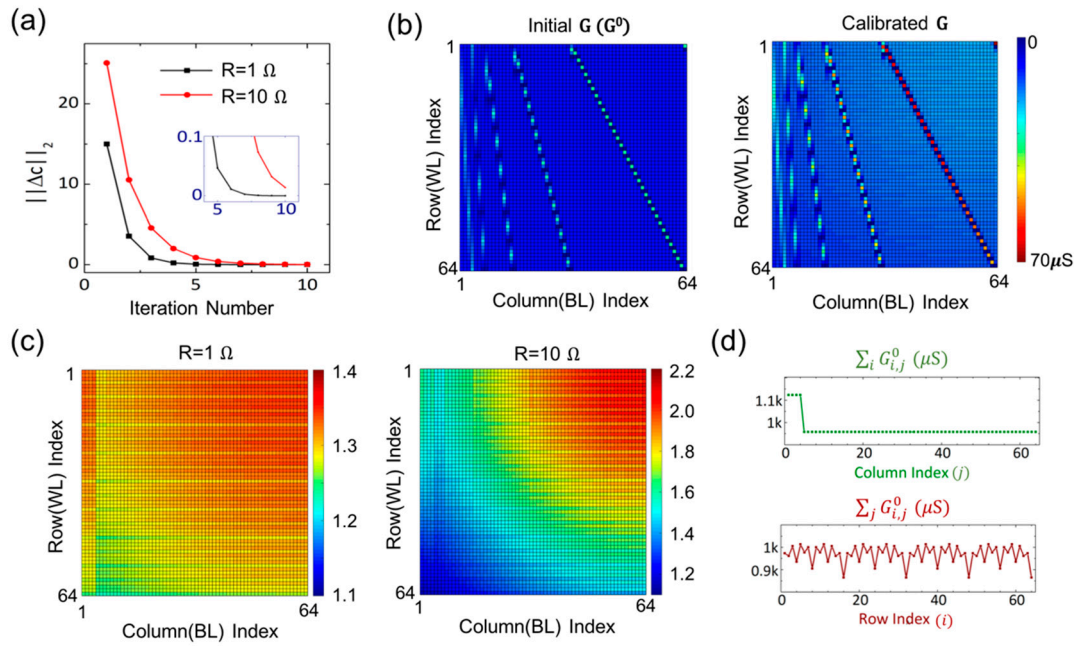


Figure 2. Conductance mapping of 64×64 matrix for discrete wavelet transform (DWT). (a) Convergence of calibration factors through the iterations for $1\ \Omega$ and $10\ \Omega$ cell-cell resistance. (b) Colored map of cell conductance of a crossbar before/after calibration. ($R = 10\ \Omega$). (c) Matrix-specific calibration factors at individual cross-points for $R = 1\ \Omega$ (left) and $R = 10\ \Omega$ (right). (d) Conductance sum of each column (top) or row (bottom) of the initial conductance.

Figure 3 summarizes the effect of the conductance calibration on the data compression and reconstruction performance. Rescaled ECG signals from the MIT-BIH database were applied as the input voltage (0–0.3 V) for DWT [16]. Figure 3a,b show the coefficients of the DWT converted from the simulated currents from the BLs for $R = 1\ \Omega$ and $10\ \Omega$, respectively. The black squares present the exact coefficients calculated in double-precision (64 bits), and the green diamond lines present the simulated coefficients with the initial memory conductance before calibration. The negatively shifted values of the simulated coefficients result from the small currents due to the voltage drop along the resistive metal interconnects. This shift fails the threshold-based compression of data where the small coefficients are cut off based on their absolute quantity (distance from zero). The larger negative slope in Figure 3b compared to Figure 3a reflects a severe reduction in current outputs for the columns located far from the voltage source due to the larger R ($10\ \Omega$). The other lines in the figures show the coefficients calculated with the calibrated memory conductance at different stages of iteration. The red lines in Figure 3a,b show that the fully calibrated coefficients well match to the exact values for both R values. The 2-norms of the difference between the exact and the experimental coefficient vectors were 4.2 ($1\ \Omega$) and 8.6 ($10\ \Omega$), and the maximum difference were 3.5 ($1\ \Omega$) and 7.2 ($10\ \Omega$) at the peak of the coefficient (exact coefficient value: 224.8, index: 29). Figure 3c shows the reconstructed ECG signals using the calibrated coefficients. (ECG signals were vertically shifted for visibility of individual lines.) The magenta line shows the reconstructed signals from the 15 largest exact coefficients out of 64. By filtering of the small coefficients, the noise in the original signal was removed as the case with exact coefficients. Figure 3d plots the error of the reconstructed signal. The reconstructed signal-to-noise ratios, defined as $20\log_{10}(\|x\|_2/\|x - \hat{x}\|_2)$ (x : original ECG, \hat{x} : reconstructed ECG), were 28.2/43.4 ($1\ \Omega$) and 27.8/37.1 ($10\ \Omega$) with/without cut-off, respectively, compared to 28.3 for the reconstruction using 15 largest exact coefficients.

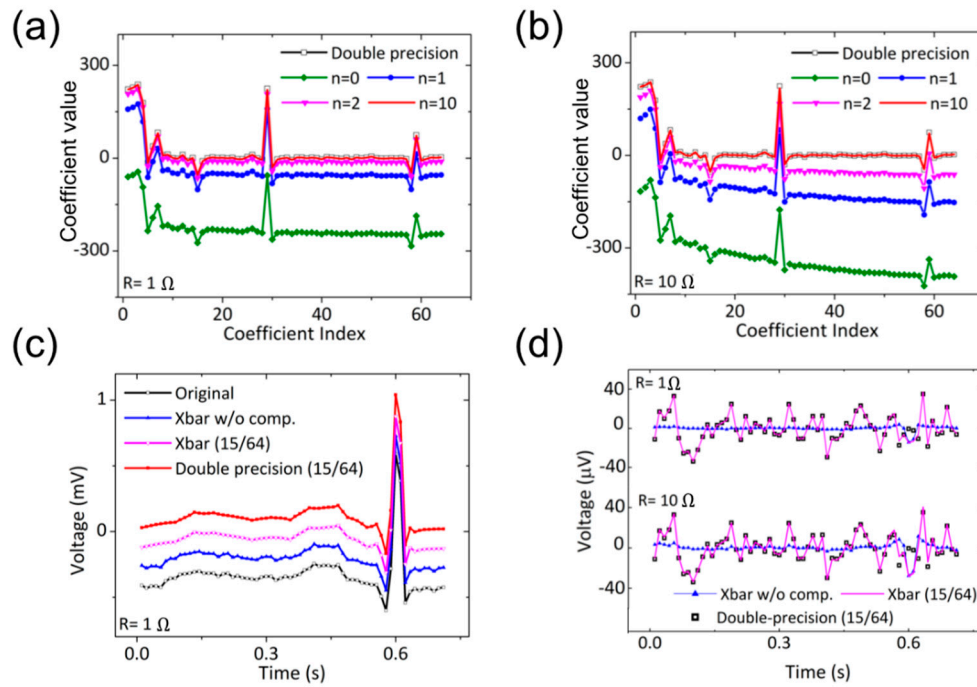


Figure 3. Electrocardiographic (ECG) signal compression using in-memory computing. (a,b) Coefficients of ECG signal after DWT using crossbar (Xbar) conductance determined by simulation. n: iteration number of simulation for conductance calibration. (a) $R = 1 \Omega$. (b) 10Ω . (c) Reconstruction of ECG from the coefficients. Compression ratio = 15/64. (d) Reconstruction error.

4. Conclusions

A conversion algorithm of a matrix to conductance was proposed in a crossbar memory array when the metal interconnects have finite conductance. The iterative simulation systematically compensates for the voltage drop along the interconnects by increasing the memory conductance. The calibration enables in-memory data compression. Considering the power limit in healthcare-related mobile devices, the proposed real-time compression using a memory crossbar can have potential as pre-processing units in such devices for diagnosis/therapeutic purposes.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The crossbar model aims to calculate junction potentials at each cross-point. Since we can build one Kirchhoff's equation for each junction, $2mn$ relations (Figure A1, mn junctions on WL + mn junctions on BL) need to be simultaneously satisfied with given memory resistances and the applied WL and BL applied potentials. Here, G_w and G_{ij} are the wire and memory conductance, and V_{ij}^{WL} and V_{ij}^{BL} are the local voltages at the junctions in a real system with finite conductance of the interconnects.

$$(WL, (i, j)) \quad G_w(V_{ij}^{WL} - V_{i,j-1}^{WL}) - G_{ij}(V_{ij}^{BL} - V_{ij}^{WL}) - G_w(V_{i,j+1}^{WL} - V_{ij}^{WL}) = 0 \quad (A1)$$

$$(WL, j = 1) \quad G_{i,access}^{WL}(V_{i,1}^{WL} - V_{i,applied}^{WL}) - G_{i,1}(V_{i,1}^{BL} - V_{i,1}^{WL}) - G_w(V_{i,2}^{WL} - V_{i,1}^{WL}) = 0 \quad (A2)$$

$$(WL, j = n) \quad G_w(V_{i,n}^{WL} - V_{i,n-1}^{WL}) - G_{i,n}(V_{i,n}^{BL} - V_{i,n}^{WL}) = 0 \quad (A3)$$

$$(BL, (i, j)) \quad G_w(V_{i+1,j}^{BL} - V_{i,j}^{BL}) - G_{i,j}(V_{i,j}^{BL} - V_{i,j}^{WL}) - G_w(V_{i,j}^{BL} - V_{i-1,j}^{BL}) = 0 \quad (A4)$$

$$(BL, i = m) \quad G_{j,access}^{BL}(V_{j,applied}^{BL} - V_{m,j}^{BL}) - G_{m,j}(V_{m,j}^{BL} - V_{m,j}^{WL}) - G_w(V_{m,j}^{BL} - V_{m-1,j}^{BL}) = 0 \quad (A5)$$

$$(BL, i = 1) \quad G_w(V_{2,j}^{BL} - V_{1,j}^{BL}) - G_{i,j}(V_{1,j}^{BL} - V_{1,j}^{WL}) = 0 \quad (A6)$$

When the equations are arranged in the order as described in Figure A1, the equations can be simplified as the following matrix formulation:

$$\mathbf{A}_{mn \times mn} \mathbf{v}_{WL} + \mathbf{B}_{mn \times mn} \mathbf{v}_{BL} = \mathbf{E}_{WL} \quad (\text{for WL junctions}) \quad (A7)$$

$$\mathbf{C}_{mn \times mn} \mathbf{v}_{WL} + \mathbf{D}_{mn \times mn} \mathbf{v}_{BL} = \mathbf{E}_{BL} \quad (\text{for BL junctions}) \quad (A8)$$

$$\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{WL} \\ \mathbf{v}_{BL} \end{bmatrix} = \begin{bmatrix} \mathbf{E}_{WL} \\ \mathbf{E}_{BL} \end{bmatrix} \quad (A9)$$

where

$$\mathbf{v}_{WL, mn \times 1} = [V_{1,1}^{WL}, V_{1,2}^{WL}, \dots, V_{1,n}^{WL}, V_{2,1}^{WL}, \dots, V_{m,n}^{WL}]^T = [\mathbf{v}_{WL,i=1}, \mathbf{v}_{WL,i=2}, \dots, \mathbf{v}_{WL,i=m}]^T \quad (A10)$$

$$\mathbf{v}_{BL, mn \times 1} = [V_{1,1}^{BL}, V_{1,2}^{BL}, \dots, V_{1,n}^{BL}, V_{2,1}^{BL}, \dots, V_{m,n}^{BL}]^T = [\mathbf{v}_{BL,i=1}, \mathbf{v}_{BL,i=2}, \dots, \mathbf{v}_{BL,i=m}]^T. \quad (A11)$$

$$\mathbf{E}_{WL, mn \times 1} = [G_{1,access}^{WL} V_{1,app}^{WL}, 0, \dots, G_{2,access}^{WL} V_{2,app}^{WL}, 0, \dots, G_{m,access}^{WL} V_{m,app}^{WL}, 0, \dots]^T \quad (A12)$$

$$\mathbf{E}_{BL, mn \times 1} = -[G_{1,access}^{BL} V_{1,app}^{BL}, G_{2,access}^{BL} V_{2,app}^{BL}, \dots, G_{n,access}^{BL} V_{n,app}^{BL}, 0, \dots]^T \quad (A13)$$

Here, \mathbf{A} and \mathbf{D} are sparse matrices whose nonzero elements are the ones that are multiplied by the local potentials adjacent to the junction under consideration along the WL (for \mathbf{A}) or BL (for \mathbf{D}). For example, the Kirchhoff's law on the (i, j) WL junction is described by

$$\mathbf{A}_{(i-1) \times j + j^{th} \text{ row}} \mathbf{v}_{WL} + \mathbf{B}_{(i-1) \times j + j^{th} \text{ row}} \mathbf{v}_{BL} = \mathbf{E}_{WL, (i-1) \times j + j^{th} \text{ row}} \quad (A14)$$

The only nonzero elements of $(i-1) \times j + j^{th}$ row of \mathbf{A} are $j-1, j, j+1^{th}$ elements of the row. \mathbf{B} and \mathbf{C} are $mn \times mn$ diagonal matrices related to the conductance of the resistive memory to describe the currents flow through the memory layer. More details are available in [13] although the structure of the matrices $\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{D}, \mathbf{E}_{WL}$ and \mathbf{E}_{BL} depends on the order of the Kirchhoff's equations that correspond to the individual junctions.

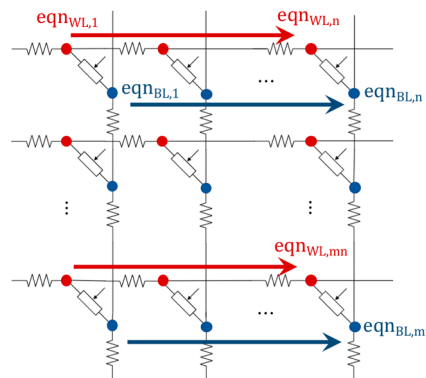


Figure A1. Kirchhoff's law produces $2mn$ equations.

For the simulation where all the applied potentials to the WL and BL are set, local potentials at the crossbar junctions can be obtained in two steps by solving the following two equations:

$$(B - AC^{-1}D)v_{BL} = E_{WL} - AC^{-1}E_{BL} \quad (A15)$$

$$v_{WL} = C^{-1}(E_{BL} - Dv_{BL}) \quad (A16)$$

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