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# A Modulation Method for Three-Phase Dual-Active-Bridge Converters in Battery Charging Applications

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**Abstract:** The Three-phase Dual-Active-Bridge (DAB3) converters are a common choice for quick charging stations for batteries in electric vehicles due to their high power density, versatility, and galvanic isolation capability. However, the DAB3 topology has limited soft-switching range, particularly under light load conditions when the voltage conversion ratio differs significantly from unity, resulting in hard switching, increased loss, and higher electromagnetic interference. To address these issues, various techniques have been proposed, but they often lead to other problems such as higher current ripple or unbalanced thermal distribution. In this paper, a new modulation scheme, called symmetric duty-cycle control (SDM), is proposed for DAB3 converters to overcome these issues. A multiaspect comparison of SDM was conducted against two existing techniques, SPS and ADCC, and its superiority was validated through simulation and experimental results. Our proposed SDM scheme provides a current ripple within 10% to 15% of the average current and enables zero current switching for the whole voltage and power ranges. Additionally, a modified version of SDM can even improve overall efficiency by 7% compared to the conventional SPS technique.

**Keywords:** symmetric duty-cycle control; asymmetric duty-cycle control; single-phase-shift; dual active bridge



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## 1. Introduction

The electric vehicle (EV) quick charging problem has gained increased attention in recent years with the proliferation of EVs. For one, the EVs can be refilled thanks to the charging station; for another, their large-capacity battery can help improve the stability of a weak grid (i.e., vehicle to grid or V2G interface [1,2]). This is done via the charging station that supports V2G according to some protocols (e.g., CHAdeMO, CCS/Combo) [3,4]. In order for a V2G charging station to function, bidirectional converters must be employed. Among various bidirectional converter typologies [5,6], dual active bridge (DAB) appears to be a good option owing to its various advantages [7–10], such as bidirectional power transmission, inherited soft-switching capability, and galvanic isolation [11,12]. A DAB converter is usually constructed in single-phase (DAB1) or three-phase (DAB3) forms. While DAB1 suffers from high output current ripple and is suitable for low-to-mid power range applications, DAB3 can output current ripple with a lower amplitude and a higher frequency [13,14]. Its power density is also higher, making DAB3 a good choice for high-power applications such as battery charging stations [15,16]. In this study, DAB3 was used as the designated topology for these applications.

As mentioned above, DAB3 converters have a soft-switching capability when modulated by the conventional single-phase-shift (SPS) scheme [7] . However, that capability

depends strongly on the working condition. When the voltage conversion ratio is considerably different from the unity, the soft-switching area becomes narrower, and vice versa [11,17]. As a consequence, more unwanted electromagnetic interference (EMI) and power dissipation are generated. In fact, according to [18], the required voltage range at the battery side should be from 150 V to 500 V. Assuming a DC-bus input voltage of 500 V, the voltage gain ratio ranges from 0.3 to 1.0, which is remarkably large. Therefore, improving the DAB3 converters performance under the hard-switching area is a problem that needs to be solved.

From another aspect, AC impedance of a lithium-ion battery increases rapidly as the frequency of the charging current goes beyond its self-resonance frequency [19,20]. When the charging current contains ripple and if the ripple is of high amplitude and high frequency, extra heat may be generated during charging, and battery lifetime may be affected. According to Uddin et al., it is critical that high-frequency current remains small to prolong the battery life [21]. Therefore, to enhance the overall system performance, not only should soft-switching capability be improved, but the modulation strategy should have the ability to reduce the current ripple at the output side of the converters.

Unlike the DAB1 counterpart, advanced control techniques applicable for DAB1 to extend the soft-switching area, such as EPS [22,23], DPS [24], and TPS [25], cannot be straightforwardly be applied to DAB3. Some efforts dedicated for DAB3 to expand the operation range have been reported in the literature. In 2013, Hoek et.al. proposed treating the DAB3 as a DAB1 converter by controlling two phases among three in parallel [26]; however, in this configuration, the advantage of low-current ripple has to be compromised. Moreover, losses and stresses are not evenly distributed among switches and transformers.

A technique called ADCC (asymmetric duty-cycle control) was reported in [27,28] to extend the soft-switching range under a wide voltage range. In this method, duty cycles of the high side and low side switches are made to be complementary. As a result, transformer voltage and current become asymmetric. Although the soft-switching region can be extended, ADCC causes unbalanced loss distribution and unequal stress on switches that may result in difficulties in thermal management. Therefore, the thermal balancing technique needs to be applied, thus increasing the complexity of this modulation. Moreover, the output current ripple is always discontinuous when the converter is modulated with the ADCC method. Hence, when the input power increases, the output current ripple also increases significantly. Not only does this have a negative effect on the battery life, but the size of output capacitors also becomes larger. Combining the ADCC and SPS methods is also a problem because the two obtained power characteristics are not seamlessly transitable.

Another technique,DCC (duty-cycle control) was proposed in [29]. In fact, DCC is an optimized version of ADCC in which three modulation variables are obtained by minimizing the conduction loss of the converter. As reported in the paper, the soft-switching area was extended, and the converter efficiency was improved. However, the control system suffers from high computational burden in solving the nonlinear optimization problem, and although soft switching can be achieved, the output current is discontinuous, or in other words, a high-current ripple forms on the output side.

In this article, a symmetric duty-cycle control (SDM) is proposed, which is easily to implement, extends the soft-switching range, and reduces the output current ripple at the secondary inverter over a whole range of the buck region. In contrast to the multicontrol variables used in the ADCC or DCC techniques, the proposed SDM modulation uses only one variable (duty cycle). However, phase currents under the SDM technique are always made symmetrically. Therefore, the stress on all switches is automatically balanced, and the advanced thermal balancing technique is no longer required. For this reason, the SDM technique can be implemented easily. Furthermore, the phase currents are made discontinuous. Zero-current turn-on can be always achieved, and thus in theory, the soft-switching area can be extended to the whole voltage range. Additionally, as seen later in the paper, the output current ripple is small compared to that obtained with the existing methods.

However, it should be noted that in practical implementation, since the dead-time interval of the SDM method is relatively large in making the current freewheel through the body diode and attenuate completely to zero. In this interval, the power dissipation on the body diode decreases the efficiency of the converter. This is not a problem if the hardware uses the low-forward=voltage drop of the body diode, such as in the Si MOSFET, IGBT, or a type of Schottky diode connected in parallel with the switches [30–32]. Unfortunately, the modern silicon carbine (SiC) switches have the body diode with a high-forward-voltage drop (i.e., the CREE C2M0025120D is about 3 V). Therefore, the SDM modulation significantly decreases the system efficiency.

Beyond the work presented in [33,34], this paper provides a full close form solution for all modes, extended experimental; results, and analysis. In addition, considering the practical implementation, a modified symmetric duty-cycle control (SDMM) technique is presented to overcome the problem of diode conduction loss. The proposed SDMM aims to avoid the diode conduction period by forcing the current to flow through the source-to-drain channel of the MOSFET using the synchronous rectification mechanism. As a result, higher performance can be attained. A laboratory-scaled prototype of the converter was implemented to verify the proposed concept.

This paper is structured as follows: the detailed analysis of the proposed symmetrical SDM method is provided in Section 2; comparison analysis with several existing methods is presented in Section 3, and experimental results are given in Section 4 to demonstrate the proposed modulation strategy.

## 2. Symmetric Duty-Cycle Modulation Method

### *2.1. Three-Phase Dual-Active-Bridge Converters*

Figure 1 shows the circuit diagram of a DAB3 converter. Conventionally, the single-phase shift (SPS) technique is used to modulate the converter. According to [11], the soft-switching area of the converter modulated by the SPS is strongly affected by the voltage conversion ratio. When it is other than the unity, the soft-switching area becomes narrower. The ds symmetric duty-cycle modulation (SDM) method is here proposed to be used where the conventional SPS method suffers from hard switching.

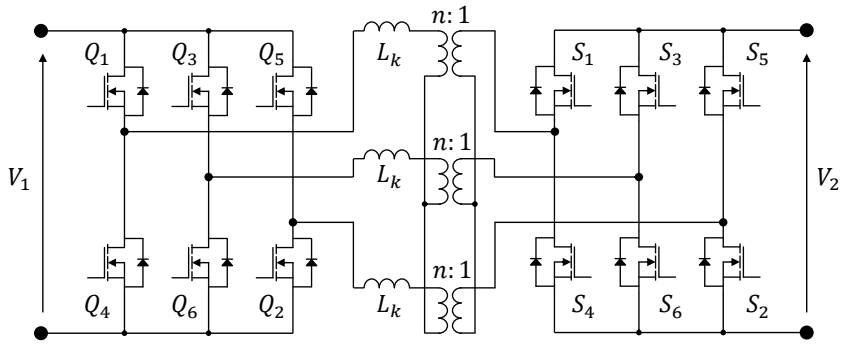



**Figure 1.** Three-phase dual-active=bridge converter topology.

In the SDM method, the phase shift $\varphi$ is always set to zero, with only duty cycle $D$ being manipulated. The duty cycle $D$ is defined by $D = t_{on} f_s$, where $t_{on}$ is the on-time of the active switches, and $f_s$ is the switching frequency. The variation range of $D$ is from $1/6$ to $1/2$. For the range of $D$ from 0 to $1/6$, there is only one phase triggered in a one-sixth period; thus, the phase current has no circuits to conduct. Based on the value of $D$ and the voltage conversion ratio $M$, $M = V_1/nV_2$ with $V_1$ and $V_2$ are the DC terminal voltages, and there are six operation modes in total. Their boundaries in the $(D - M)$ frame are illustrated in Figure 2. Explanation of the boundaries and modes are detailed later in the paper.

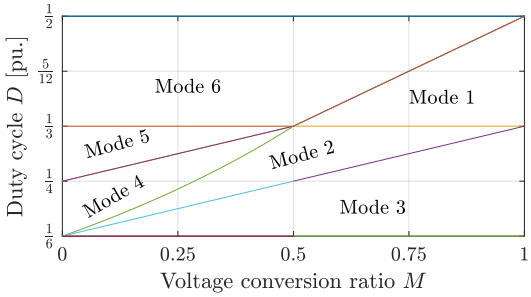



**Figure 2.** Six operation modes dependent on the duty-cycle and voltage conversion ratio.

The theoretical waveform of all modes is presented in Figure 3. Zero-current turn-on can be achieved for all modes from 1 to 4 as shown in Figure 3a–d because the phase current is discontinuous. In Modes 5 and 6, however, the current is continuous, and the secondary inverter suffers from hard switching as can be seen in Figure 3e,f. Therefore, these two modes are excluded from consideration. The details for the analysis of Mode 1 follow below. The same method can be applied to investigate the operation of other modes.

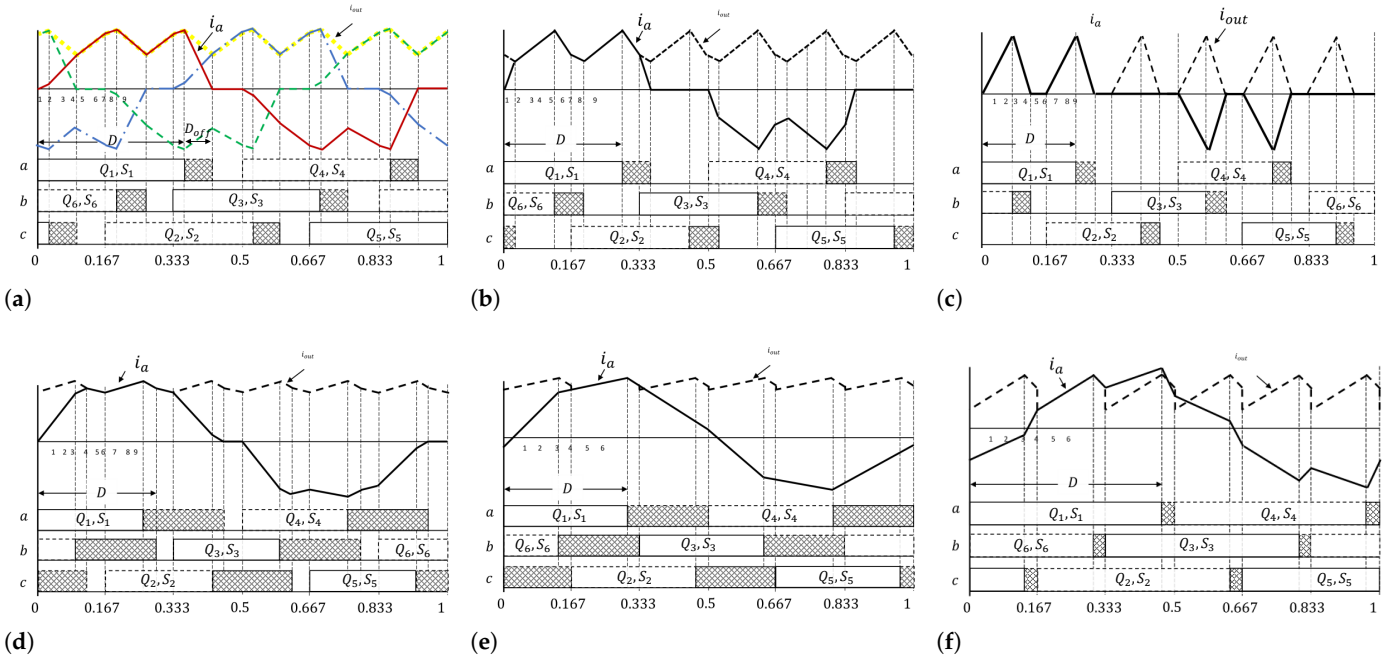



**Figure 3.** Theoretical waveforms: (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3, (**d**), Mode 4, (**e**), Mode 5, (**f**), and Mode 6.

### *2.2. Steady-State Analysis of the Proposed SDM Method*

It is worth making some assumptions to simplify the analysis: (i) switches are that can transit without transients are ideal; (ii) series resistances of transformers can be ignored; and (iii) input and output voltages are constant in a switching cycle. Let us consider Mode 1 for example. Current waveform and gate signals are given in Figure 3a. Phase currents are denoted as continuous, dashed and dot-dashed lines represent phases A, B, and C, respectively; shaded areas denote diode conduction intervals; rectangles with continuous edges represent gate signals of odd group switches; and those with dashed edges represent gate signals of even numbered switches. There are nine states in the first half cycle in Mode 1. The primarily referred diagrams of all states are given in Figure 4. Let $t$ be the present time instant:

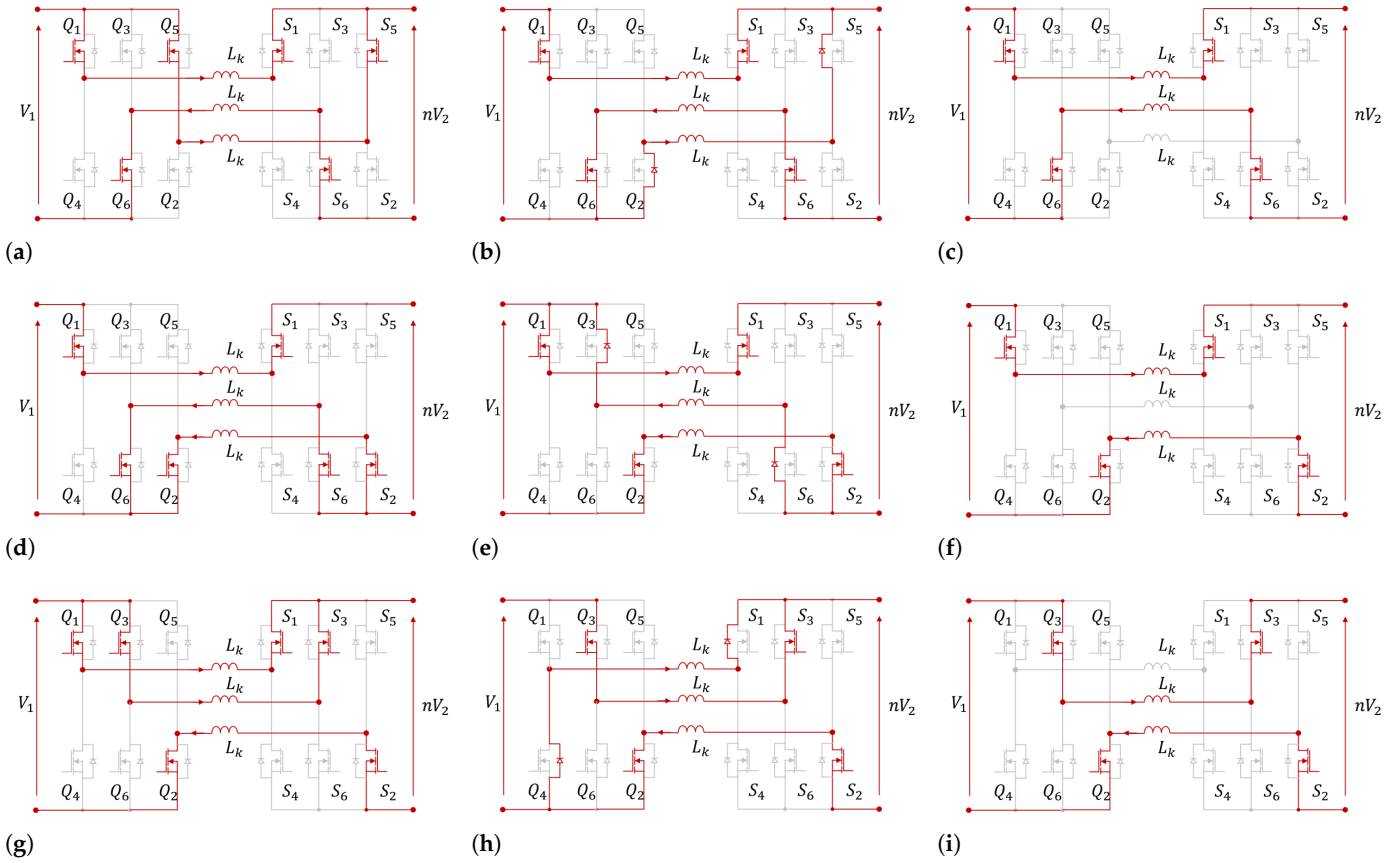



**Figure 4.** Primary referred diagram of all states in Mode 1: (**a**) State 1, (**b**) State 2, (**c**) State 3, (**d**) State 4, (**e**) State 5, (**f**) State 6, (**g**) State 7, (**h**) State 8, (**i**), and State 9.

In this state, $Q_1, Q_6, Q_5$ of the primary inverter and $S_1, S_6, S_5$ of the second inverter conduct. The primary referred equivalent diagram of this state is given in Figure 4a. Phase currents in this state are as follows:

$$\boldsymbol{i}(t) = \boldsymbol{I}_0 + \frac{V_1}{3f_s L_k}\begin{bmatrix} 1-M \\ -2+2M \\ 1-M \end{bmatrix} t \tag{1}$$

where $\boldsymbol{i}(t)$ is the instantaneous phase current vector, and $\boldsymbol{i}(t) = [i_a(t), i_b(t), i_c(t)]^T$; and $\boldsymbol{I}_0$ is the transition current vector at the beginning of the switching period, $\boldsymbol{I}_0 = [i_{a0}, i_{b0}, i_{c0}]^T$.

2.2.1. State 2: $D - 1/3 \leq t \cdot f_s \leq D - 1/3 + D_{off}$

When $t \cdot f_s = D - 1/3$, $Q_5$ and $S_5$ turn off, there are no gate signals to switches of phase $C$ in both sides. Phase $C$ current flows through the body diode of $Q_2$ and $S_5$ to maintain its direction. Since there is no more energy supply to phase $C$, $i_C(t)$ attenuates after some time. Let $(D_{off}/f_s)$ be the required time for the current to attenuate to zero. The equivalent circuit of State 2 is shown in Figure 4a, and phase currents are determined by (2). This state ends when $(t \cdot f_s) = (D - 1/3 + D_{off})$; then, the system proceeds to State 3.

$$\boldsymbol{i}(t) = \boldsymbol{I}_1 + \frac{V_1}{3f_s L_k}\begin{bmatrix} 2-M \\ -1+2M \\ -1-M \end{bmatrix}\left(t - \left(D + \frac{1}{3}\right)\frac{1}{f_s}\right) \tag{2}$$

where $\boldsymbol{I}_1$ is the transition current vector at the end of State 1.

2.2.2. State 3: $(D - 1/3 + D_{off} \leq t \cdot f_s \leq 1/6)$

When $(t \cdot f_s) = (D - 1/3 + D_{off})$, phase *C* current is zero. It then starts to oscillate between the parasitic capacitor of the transistors and the leakage inductance of the transformers causing resonance in the phase *C* voltage and current. This phenomenon is popular for discontinuous current mode converters and, in theory, causes no power loss but may have an EMI issue. By ignoring the resonance, the equivalent circuit can be simplified as depicted in Figure 4c, and the phase currents can be computed in the following fashion:

$$\boldsymbol{i}(t) = \boldsymbol{I}_2 + \frac{V_1}{3f_s L_k}\begin{bmatrix} 1-M \\ -1+M \\ 0 \end{bmatrix}\left(t - \left(D - D_{off} + \frac{1}{3}\right)\frac{1}{f_s}\right) \tag{3}$$

where $\boldsymbol{I}_2$ is the transition current at the end of State 2.

The operations in States 4 to 6 and States 7 to 9 are similar, but the attenuating phase is *B* and *A*, respectively. Figure 4d–i show the theoretical waveform in those modes. If a similar analysis is applied, the conditions and phase currents of States 4 to 9 can be obtained. At the steady state, the current at the end of State 9, $\boldsymbol{I}_9$, must be equal to that at the beginning of State 1, $\boldsymbol{I}_0$ . By solving $\boldsymbol{I}_0 = \boldsymbol{I}_9$, all the transition currents can be obtained. From this, the diode conduction period $D_{off}$ and the transmission power can be calculated as (4) and (5), where $P_m = V_1^2/(12 f_s L_k)$ is as follows:

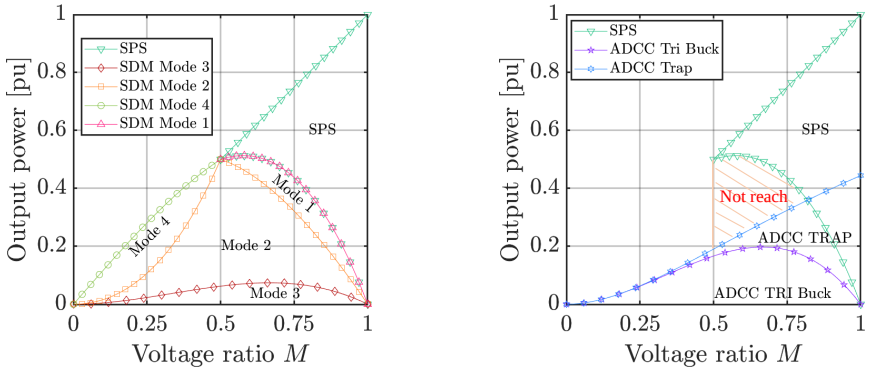
$$D_{off} = \frac{1-M}{1+M}\left(D + \frac{1}{6}\right) \tag{4}$$

$$P_1 = \frac{MP_m}{3} \cdot \frac{1-M}{1+M} \cdot (6D+1)^2 \tag{5}$$

Analogously,the output power and boundary of all modes can be obtained as listed in Table 1. Figure 2 shows the product of plotting the boundaries in the $D - M$ frame. The power characteristics of Modes 1 to 4 are illustrated in Figure 5a. As can be seen, the union of the area limited by the power curves of Modes 1 to 4 perfectly covers the hard-switching zone created by the SPS method. Therefore, by hybridizing SDM Modes 1 to 4 and SPS, the whole voltage and power ranges can be fulfilled and soft switching achieved.

**Table 1.** Mode boundaries and output power.

| | |
|---|---|
| Mode 1: | $\frac{1}{3} \leq D \leq \frac{1}{6} + \frac{M}{3}$<br>$P_1 = \frac{MP_m}{3} \times \frac{1-M}{1+M} \times (6D+1)^2$ |
| Mode 2: | $\left(\frac{1+M}{6} \leq D\right) \cup \left(D \leq \frac{1}{3}\right) \cup \left(D \leq \frac{1+M}{3(2-M)}\right)$<br>$P_2 = MP_m \times \left(18 \times \frac{2-M}{1+M} D^2 - 1\right)$ |
| Mode 3: | $\frac{1}{6} \leq D \leq \frac{1+M}{6}$<br>$P_3 = \frac{P_m}{2} \times (1-M) \times (6D-1)^2$ |
| Mode 4: | $\frac{1+M}{3(2-M)} \leq D \leq \frac{1}{4} + \frac{M}{6}$<br>$P_4 = \frac{MP_m}{6} \times \left(\frac{2-M}{2+M}(12D+1)^2 - 9\right)$ |
| Mode 5: | $\frac{1}{4} + \frac{M}{6} \leq D \leq \frac{1}{3}$<br>$P_5 = \frac{MP_m}{6} \times \left(7 - 9(4D-1)^2\right)$ |
| Mode 6: | $\left(D \leq \frac{1}{2}\right) \cup \left(\frac{1}{3} \leq D\right) \cup \left(\frac{1}{6} + \frac{M}{3} \leq D\right)$<br>$P_6 = \frac{MP_m}{3} \times \left(4 - (6D-1)^2\right)$ |




(**a**) SDM vs. SPS (**b**) ADCC vs. SPS

**Figure 5.** Soft switching boundary.

## 3. Comparison

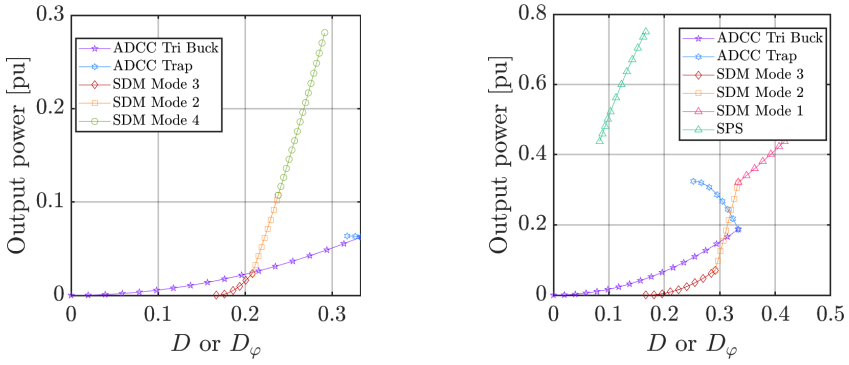
In order to demonstrate the advantage of the proposed modulation technique, a comparison to SPS and ADCC methods was conducted which considered several aspects described below.

### *3.1. Soft-Switching Range*

Figure 5 shows the power characteristics obtained with SPS, SDM, and ADCC. When $M \leq 0.5$, SPS is not applicable and both ADCC and SDM can be applied. Figure 5b shows the soft-switching boundaries of the SPS and ADCC methods. The boundary curves cross each other, limiting a hard-switching area that cannot be covered by either SPS or ADCC as discussed and reported in [26,27]. Meanwhile, the soft-switching boundaries of the proposed SDM scheme divide the hard-switching zone of SPS into subzones that are seamlessly and perfectly fitted to each other, as shown in Figure 5a.

### *3.2. Power Flow with Mode Changing*

Figure 6 shows the power characteristics with respect to the duty cycle $D$ (for SDM, SDMM, and ADCC) or the normalized phase shift $D_\varphi$ (for SPS, $D_\varphi = \varphi/(2\pi)$, where $\varphi$ is the phase shift) at some given voltage conversion ratios. Although the power curves obtained with SDM are divided into subsections due to the presence of submodes, the sections are relatively linear and exhibit monotonic increasing. Moreover, the maximum power reached by SDM is suits the minimum covered with SPS. Combining SPS and SDM allows for the continuous power characterization the converter. The power characteristics of the ADCC method are, however, relatively nonlinear and nonmonotonic. For a given voltage conversion ratio, there is a gap between the power generated with ADCC and SPS, as shown in Figure 6. This may make mode selection and shifting from ADCC to SPS (and vice versa) complicated.

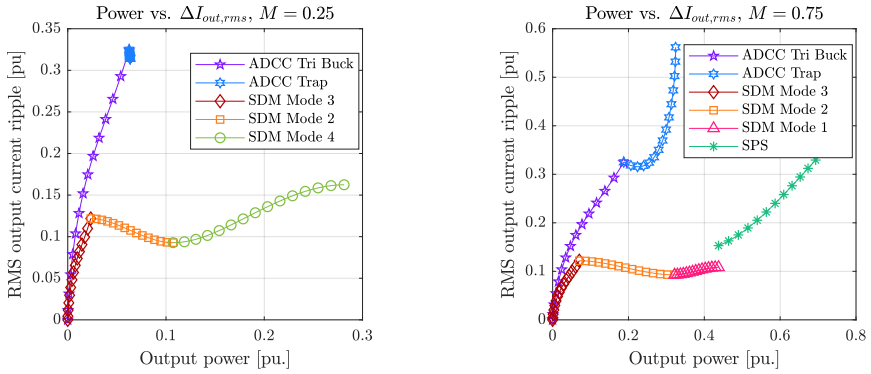



(**a**) $M = 0.25$ (**b**) $M = 0.75$

**Figure 6.** Power range comparison.

### *3.3. Output Current Ripple*

As mentioned above, the current ripple is critical for battery charging applications. Therefore, it is worth considering the output current ripple generated by the modulation techniques. Figure 7 demonstrates the root-mean-square (RMS) output ripple current (or capacitor current) of the aforementioned methods. At any given power transmission, the current ripple generated by ADCC is higher than that caused by the proposed SDM. The current ripple obtained by SDM ranges from 10 to 15% of the $I_m$, where $I_m = V_1/(18 f_s L_k)$. Particularly, when $M = 0.5$, the current ripple is eliminated under SDM at half of $P_m$. When $M > 0.5$, $\Delta I_{out,rms}$ of ADCC is even much greater than that of the conventional SPS method.




(**a**) $M = 0.25$ (**b**) $M = 0.75$

**Figure 7.** Current ripple comparison.

## 4. Diode Loss Elimination Technique

### *4.1. Proposed SDMM Technique*

As analyzed above, in State 8 of Mode 1, the phase $A$ current attenuates to zero through the body diode of $Q_4$ and $S_1$, causing conduction loss. For switching devices with a high-voltage drop on the body diode (such as C2M0025120D from Woldspeed), loss caused by diode conduction might be significant and affect the overall converter performance.

The diode loss can, however, be eliminated by making the current flow through the source-drain channel of the FET. By using (4), the diode conduction interval can be estimated. During $\left(D_{off}/f_s\right)$ interval, the corresponding FET is forced ON for the current to flow. Hence, the loss on the switch is now proportional to its ON resistance instead of the forward voltage on the diode. By using low ON-resistance devices or connecting them in parallel, the conduction loss can be reduced. This technique is named modified SDM or SDMM.

Figure 8 shows the typical gate signal of phase $A$ switches. In the original SDM, after the duty cycle $D$, both $Q_1$ and $S_1$ are OFF, and the current starts its freewheeling. Here, in the SDMM method, $S_1$ remains ON in an extra duty cycle of $D_{off}$. In the meantime, $Q_4$ is forced ON to conduct the freewheeling current. A small dead time is added between the transition of $Q_1$ and $Q_4$ to avoid a shoot-through. Zero-voltage turn-on is thus achieved for $Q_4$. After $(D_{off}/f_s)$ seconds, the phase $A$ current reaches zero, and then both $Q_4$ and $S_1$ are OFF. Hence, zero-current turn-off is obtained for $Q_4$ and $S_1$. Note that SDMM does not introduce new switching states; therefore, all the above analyses remain valid.

This idea is motivated by the synchronous rectification technique which is commonly used in LLC converters. However, in the SDMM method, modulation patterns of both sides are modified, making it relatively complicated to implement because primary switches transit twice in a switching cycle. Additionally, $D_{off}$ determined by (4) is highly nonlinear and system state-dependent ($D_{off}$ depends on $M$).

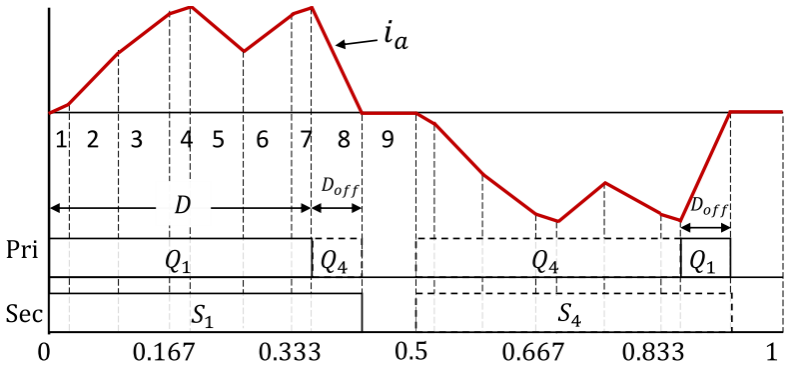



**Figure 8.** SDMM modulation scheme.

The above presents the implementation of SDMM using a software approach; that is, the modulation pattern is created by computing the conduction period manually with mathematics equations obtained from theoretical analysis. To be feasible, this approach requires certain conditions:

i Precise determination of the present voltage gain $M$. The DC terminal voltages are sensed and from this, the voltage gain ratio $M$ is calculated. A mismatch in determining $M$ may lead to early or late turn-off of the corresponding switch that may reduce the effect of the proposed method.

ii A high-resolution pulse-width modulation (PWM) module of the microcontroller. For instance, in this study, an STM32G474RE microcontroller from STMicroelectronics was used to generate the SDMM modulation pattern.

iii Finally, the microcontroller with a floating-point unit (FPU). This is needed because the calculation of the diode conduction interval consists of some division and multiplication operations.

If the above conditions cannot be met, hardware implementation can be considered. For example, a special gate driver design which allows automatic generation of a synchronous rectification signal based on the sensing current can be used. This problem is, however, beyond the scope of this paper. It will be readdressed in future publications.

### *4.2. Loss Breakdown Analysis*

This loss breakdown analysis employs the loss models presented in [35] by the same author, specifically, power dissipation, including the power electronic loss (conduction and switching losses) and transformer loss (core and copper losses). The conduction loss is easy to determine with the RMS phase current. These current equations can be found in [35,36]. The switching loss is calculated by using the rising and falling time in the datasheet, i.e., CREE C2M0025120D SiC MOSFET for both sides of inverter systems. The core loss of transformer is estimated by using the Steinmetz equation [37], and the winding loss is estimated for the Lizt wire, with considerations given to the skin and proximity effects. From this, the loss models of the SDM, SDMM, SPS, and ADCC were determined and compared.

Figure 9 shows the loss distribution under three case studies: (1) $M$ = 0.8 & $P$ = 0.34 p.u; (2), $M$ = 0.7 & $P$ = 0.21 p.u; and (3), $M$ = 0.6 & $P$ = 0.15 p.u. Note that all the power here is expressed per unit with respect to $P_m$, $P_m = V_1^2/(12 f_s L_k)$. In the first case study, power is transferred at a high-voltage conversion ratio. The calculated efficiencies in this case are 96.27%, 94.99%, 93.64%, and 92.93% for SPS, SDMM, SDM, and ADCC, respectively. As shown in Figure 5, the point $M = 0.8$ and $P = 0.34$ p.u. are located in the hard-switching area of SPS, whereas, in the SDM and ADCC regions, the point belongs to SDM-Mode 1 and ADCC-TRAP, respectively. Despite this, SPS appears to be the most efficient modulation scheme, as the generated loss is the lowest compared to that caused by the other techniques. This is because even if hard switching occurs under SPS modulation, the extra turn-on loss is still much lower than the turn-off loss generated by SDM (and SDMM) and ADCC, for

which phase current is discontinuous (i.e., turn off loss is considerably increased). While the transformer loss is comparable for all schemes, switching loss and, in particular, the conduction loss generated by ADCC, is more than that generate by SPS, SDM, and SDMM. However, in term soft diode loss, SDM is the worst, while the others cause no diode loss.

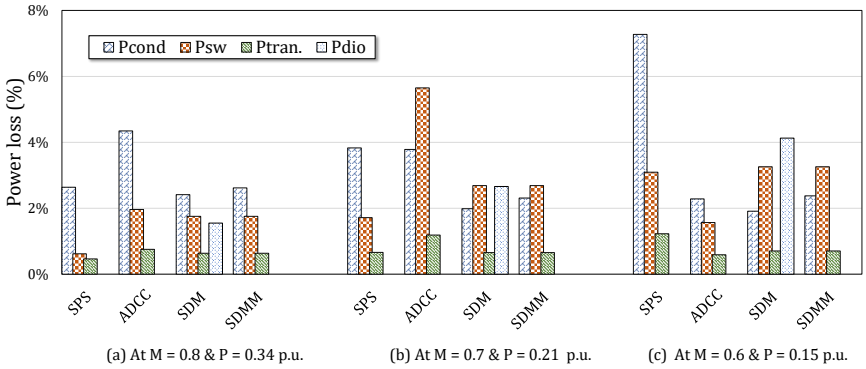



**Figure 9.** Loss breakdown analysis.

In the second case study, the calculated efficiencies are 93.79%, 94.35%, 92.02%, and 89.38% for SPS, SDMM, SDM, and ADCC, respectively. Figure 5 shows that points $M = 0.7$ and $P = 0.21$ p.u. belong to either SPS hard switching , SDM-Mode 2, or DCC-Trap mode. In this condition, SDMM appears to be superior to ADCC. Switching loss obtained with ADCC is remarkably high while that obtained with SDM (and SDMM) is much lower. As SPS goes further into the hard-switching zone, the generated switching loss is now higher even though it is still less than that obtained with SDM and SDMM for the same reason mentioned in the previous case study.

In the last case study, where $M = 0.6$ and $P = 0.15$ p.u., the working regions observed in Figure 5 are SPS hard switching, SDM-Mode 2, and ADCC-TRI-Buck. The computed efficiencies are 88.41%, 93.66%, 89.99%, and 95.56% for SPS, SDMM, SDM, and ADCC, respectively. Under this condition, ADCC, however, is the best choice in terms of converter efficiency. Both the conduction and switching losses caused by ADCC are the lowest. SDMM appears to be second best in terms of efficiency. Although it generates a comparable conduction loss as that of ADCC, SDMM results in an almost doubling of switching loss. SPS operates deeply inside the hard-switching zone with remarkably high conduction loss, making it the worst in terms of converter efficiency.

From the above evaluation, it can be concluded that the performance of the modulation schemes depends highly on working conditions. ADCC is good at light load where TRI-Buck mode is employed, but it performs less well when the power is higher, and then TRAP-Mode must be used. SPS is superior when near its boundary, but away from this, its performance declines rapidly. SDMM shows the best performance at the light-to-mid power range and has a particularly stable efficiency, ranging from 93.66% to 94.99% in all investigated cases.

## 5. Experimental Results

An experimental system was built to evaluate all the modulation methods. The key parameters are listed in Table 2. The DC-bus voltage at the input side was connected to a programmable power supply (MR50040 from BK Precision), whereas the output was linked to an electronic load (62120D from Chroma) configured in the constant-voltage mode. Due to the limitation of experimental equipment, scaled down experiments with specification of $V_1$ = 100 V, and $V_2$ = 60 to 100 V were conducted. SiC MOSFETs of C2M00025120D from CREE was used for both inverters. The three-phase transformer was constructed with three single-phase transformers. The equivalent leakage inductance seen from the inverter was thus about 4.16 µH. An STMicroelectronics NUCLEO-STM32G474RE board was used to generate the switching pattern of all modulation techniques. In the experiments, the input voltage was always fixed at 100 V (i.e., $P_m = V_1^2/(12 f_s L_k) = 4000$ W), whereas, the output

voltage was changed to test the modulation methods at various conversion ratios. Duty cycles and phase shift were set manually for open-loop tests. An image of the system is illustrated in Figure 10.

**Figure 10.** Prototype of the DAB3 converter.

**Table 2.** The key parameters of the DAB3 converter.

| Parameters | Symbol | Value |
|---|---|---|
| Input voltage | $V_1$ | 100 V |
| Output voltage | $V_2$ | 60–100 V |
| Scale down power | $P_{in}$ | 2 kW |
| Frequency | $f_s$ | 50 kHz |
| Turn ratio | $n$ | 1 |
| Leakage inductance | $L_k$ | 12.5 µH |
| Wire | | Lizt 1650AWG38 |
| Core | | EE42/21/15 (N87) |
| SiC MOSFET | | CREE C2M0025120D |

Figure 11 shows the measured voltage and current of the ADCC and SDM methods with $M = 0.8$. The measured waveform of ADCC TRI Buck, SDM Mode 2, and SDMM Mode 2 when transmitting 500 W ($P$ = 0.125 p.u.) are depicted in Figure 11a,c, and e, respectively. In all cases, ZCT was achieved. However, while the drain-source voltage obtained with the ADCC method was clear with low ringings, that obtained with SDM and SDMM contained ringings with a frequency of about 1 MHz due to the resonance between leakage inductances and parasitic capacitors of the FETs. Although the ringings occurred at zero current, causing no loss, they contributed to a louder noise emitted by the converter.

The current waveform shown in Figure 11c,e is symmetrical with a clear zero interval that ensures ZCT of the switches. The zero-current interval observed in Figure 11a, however, appears to have a small bias. This might be due to the magnetizing current, parasitic elements, and dead time [36]. Moreover, since the duty-cycle value used in the ADCC method is highly dependent on the voltage ratio $M$, a small mismatch on its determination may lead to the hard switching of the transistors modulated by ADCC. Nevertheless, ADCC-TRI-Buck performs better than do both SDM and SDMM at a light load, as shown in Figure 12b. At 500 W, the overall system efficiency obtained with ADCC is mostly 97.2%, whereas that with SDM is 95.4%. The diode conduction loss is responsible for the inferior performance of SDM against ADCC.

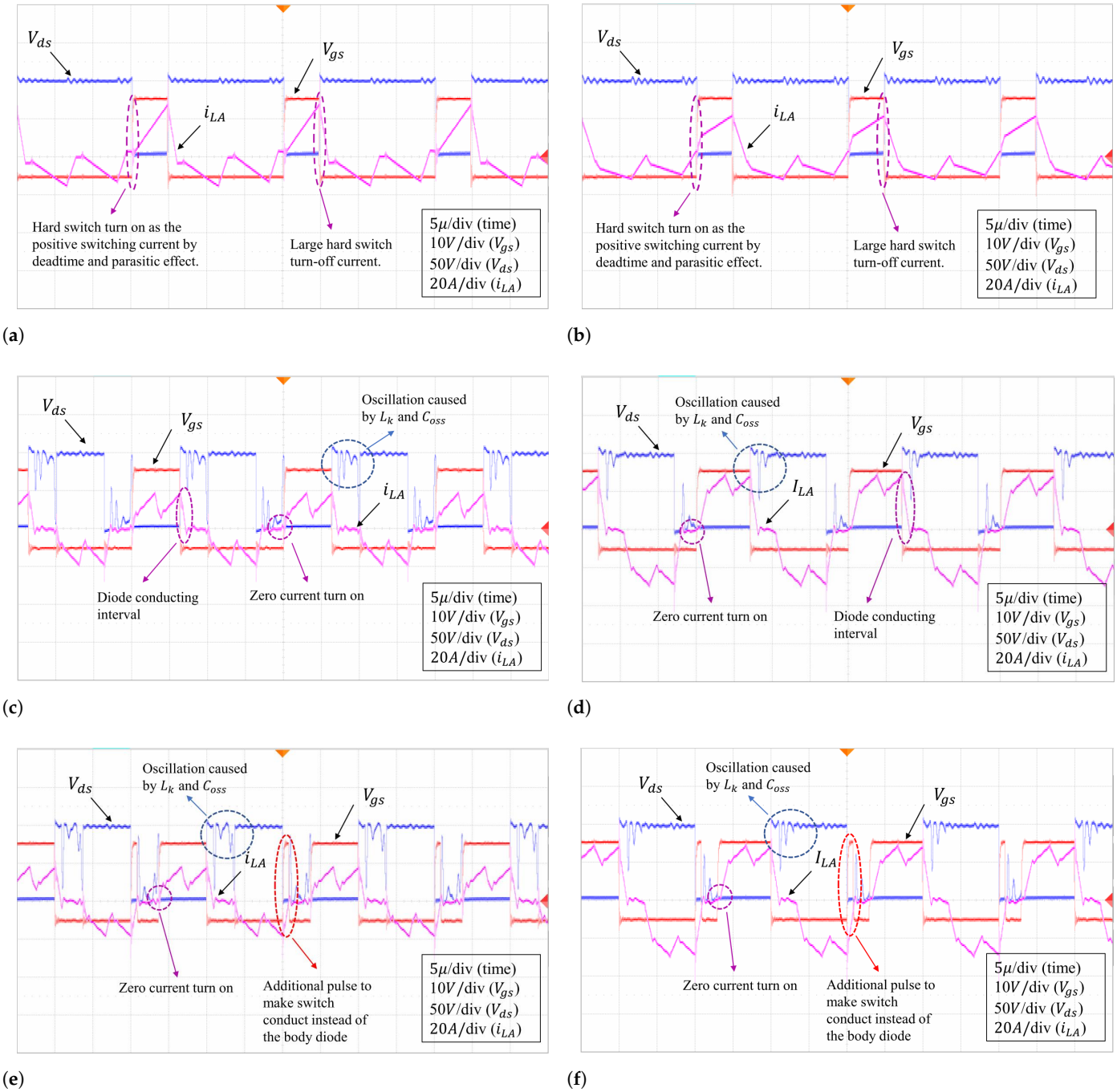
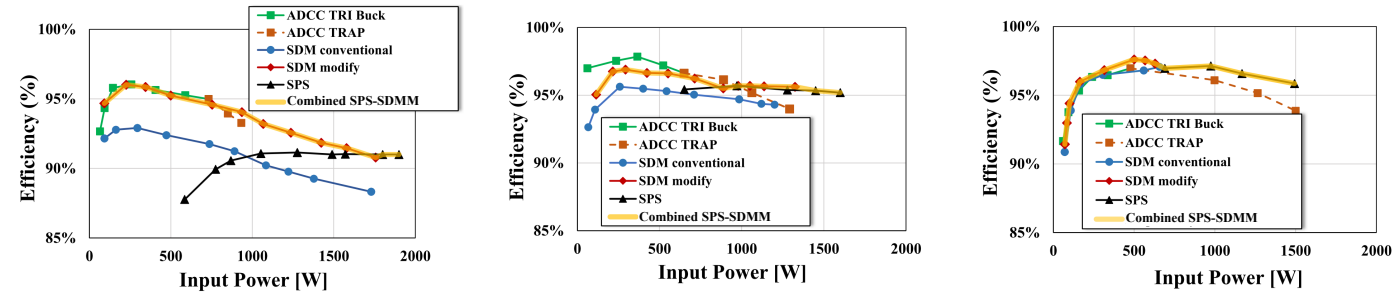



**Figure 11.** Current and voltage waveform: (**a**) ADCC Tri-Buck, (**b**) ADCC TRAP, (**c**) SDM Mode 2, (**d**) SDM Mode 1, (**e**) SDMM Mode 2, (**f**) and SDMM Mode 1.

The current waveform obtained with SDMM was the same as that obtained with SDM, as shown in Figure 11c,e. The additional pulse of the gate signal helps eliminate the diode conduction interval. As a result, the efficiency obtained with SDMM improves to about 96.7% at 500 W operation. Nonetheless, it is 0.5% less than that obtained with ADCC. The reason for this is that SDMM requires the switches to transit nine times in a half cycle (corresponding to nine switching states) compared to only six of the ADCC method. Therefore, at a low-power range, the lower switching loss of ADCC makes it slightly better than SDMM. This result confirms the conclusion of the loss breakdown analysis of case study 3 in the previous section.




(**a**) (**b**) (**c**)

**Figure 12.** The efficiency experiment results: (**a**) $M$ = 0.6, (**b**) $M$ = 0.8, and (**c**) $M$ = 0.9.

Figure 11b,d,f show the measured waveform obtained with ADCC TRAP, SDM Mode 1, and SDMM Mode 1, respectively, at $M = 0.8$ and 1.2 kW (i.e., 0.3 p.u.). This experiment was conducted to confirm the conclusion of case study 1 and 2 in the previous section. Analogous observations to those of the previous experiment were obtained. Ringings were still present in the drain-source voltage obtained with SDM and SDMM; however, its amplitude was smaller. At this power, conduction loss is dominant. As shown in Figure 12, at 1200 W, the overall system efficiency recorded with ADCC, SDM, SDMM, and SPS are 94.6%, 94.3%, 95.7%, and 95.4%, respectively. SDMM appears to be superior over the other methods. As the power increases, the performance of ADCC reduces dramatically, whereas SDMM can maintain the efficiency around 95.7%. Therefore, it can be concluded that at a high power range, SDMM outperforms ADCC in term of system efficiency.

Figure 12a–c show the system efficiencies at $M = 0.6$, $M = 0.8$, and $M = 0.9$, respectively. Observation from the figures reinforces the conclusions from the loss breakdown analysis. When $M = 0.6$, ADCC-TRI-Buck is superior under 800 W (i.e., 0.2 p.u.; this is also the upper boundary of ADCC-TRI-Buck mode) power transmission as predicted in case study 3 in Section 4.2. Efficiency declines rapidly when the power increases and the converter enters ADCC-TRAP mode. With SPS, since the system operates in the hard-switching zone, efficiency is remarkably low. When the converter enters the vicinity of the SPS soft-switching area (>1800 W), the converter is most benefited by SPS as observed in case study 1 of the previous section. Because of the diode loss, SDM appears to be the worst in most cases. However, owing to the elimination of the diode conduction interval, SDMM is shown to be the best in terms of efficiency when the power is greater than 800 W.

When $M = 0.8$, the above observation is still true. ADCC is still the best under the light-load condition with ADCC-TRI-Buck ($P < 700$ W or 0.175 p.u.—the upper boundary of the TRI-Buck mode) as shown in Figure 12b. However, the performance declines rapidly in the ADCC-TRAP mode when the power increases. SPS is still superior in its soft-switching area ($P > 1400$ W or 0.35 p.u.). In the mid-power range, SDMM appears to be the best. Interestingly, SDMM can maintain a quite stable performance throughout the power range with an average efficiency of about 96%. The same conclusion can also be drawn from the experiment results shown in Figure 12c when $M = 0.9$. In all cases, combining SDMM and SPS helps to cover the whole power range with high efficiency. The efficiency profile of the combined SPS-SDMM method is highlighted in yellow in Figure 12.

Figure 13 shows a current ripple comparison between ADCC and SDM. The ripple is measured at the output of the secondary bridge before the filter capacitors. Lower current ripple means lower loss on output caps and cleaner output current to the battery. As can be seen, SDM (and thus SDMM) provides better ripple characteristics. In the SDM method, although the phase current is discontinuous (Figure 3), except for Mode 3, the output current in all other modes is continuous with a low ripple. The current ripple obtained with SDM is always around 10% to 15% in all investigated cases, which is consistent with theoretical analysis shown in Figure 7. In contrast, the current ripple obtained with ADCC is always higher than that obtained with SDM. For instance, at 1200 W power transmission,

the measured current ripple with ADCC is almost 60%, which is nearly six times higher than that obtained with the proposed SDM method.

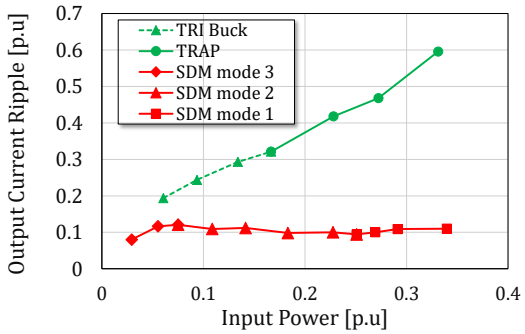



**Figure 13.** Output current ripple measurements.

Figure 14 summarizes the comparison across several areas. The larger area implies a better performance. In terms of current ripple, soft-switching, and power ranges, SDM (and thus SDMM) proved to be the best, as it generated the lowest current ripple. The combination of SPS and SDM can cover the whole power and soft-switching ranges. SDM and SPS methods occupy only one modulation variable; therefore, they are ranked highest in terms of robustness and feasibility. SDMM and ADCC, however, depend on the voltage conversion ratio to compute modulation parameters; therefore, they are less robust than are the other two methods. Compared to the other techniques, SDMM uses the most complicated modulation pattern; hence, it ranks the lowest in terms of feasibility. Efficiency is the weakest point of SDM due to the diode conduction loss. As SDMM can overcome this weakness, despite its inferior performance compared to ADCC under the light load, its performance is better under the heavy-load condition; thus, it is ranked the same as ADCC. To conclude, SDM has the largest area implying the best performance. SDMM ranks second overall, with the advantage of efficiency over SDM at the cost of feasibility and robustness.

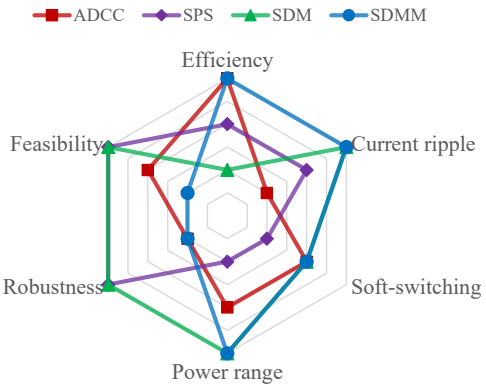



**Figure 14.** Summary of comparison results.

## 6. Conclusions

This paper proposes a new modulation method, SDM, as well as its improved version, to be applied for three-phase DAB converters. The performance of the proposed method was compared to other well-known methods, both in theoretical analysis and experiments. Results confirmed that SDM can extend the soft-switching area of DAB3 converters. In particular, a combination of SDM and SPS can cover the whole voltage and power range for the cases in which the voltage conversion ratio is less than the unity. Phase currents are symmetrical; thus, loss can be evenly distributed among switches and transformer winding. Furthermore, SDM can help reduce the output current ripple (up to six times less than that of the ADCC method), which is essential for battery charging applications. However, the original SDM is inferior due to the presence of the diode conduction period.

The SDMM method was thus proposed to solve this problem by modifying the switching pattern. Under this modified method, the converter efficiency could be improved up to 7%, and the SDMM technique was found to be the superior choice at the midrange of power for improving the converter efficiency. Therefore, a hybridization of SPS and SDMM is the best modulation method for overcoming most of the weaknesses of the other modulation techniques.

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## References

1. Kempton, W.; Tomić, J. Vehicle-to-grid power implementation: From stabilizing the grid to supporting large-scale renewable energy. *J. Power Sources* **2005**, *144*, 280–294. [CrossRef]
2. Ota, Y.; Taniguchi, H.; Nakajima, T.; Liyanage, K.M.; Baba, J.; Yokoyama, A. Autonomous distributed V2G (vehicle-to-grid) satisfying scheduled charging. *IEEE Trans. Smart Grid* **2011**, *3*, 559–564. [CrossRef]
3. Mouli, G.R.C.; Kaptein, J.; Bauer, P.; Zeman, M. Implementation of dynamic charging and V2G using Chademo and CCS/Combo DC charging standard. In Proceedings of the 2016 IEEE Transportation Electrification Conference and Expo (ITEC), Dearborn, MI, USA, 27–29 June 2016; pp. 1–6.
4. Mouli, G.R.C.; Schijffelen, J.; van den Heuvel, M.; Kardolus, M.; Bauer, P. A 10 kW solar-powered bidirectional EV charger compatible with chademo and COMBO. *IEEE Trans. Power Electron.* **2018**, *34*, 1082–1098. [CrossRef]
5. Inoue, S.; Akagi, H. A bidirectional DC–DC converter for an energy storage system with galvanic isolation. *IEEE Trans. Power Electron.* **2007**, *22*, 2299–2306. [CrossRef]
6. Ting, P.; Shenghua, H.; Shuanghong, W. A three phase ZVS bidirectional DC-DC converter. In Proceedings of the 2008 IEEE Vehicle Power and Propulsion Conference, Harbin, China, 3–5 September 2008; pp. 1–6.
7. De Doncker, R.W.; Divan, D.M.; Kheraluwala, M.H. A three-phase soft-switched high-power-density DC/DC converter for high-power applications. *IEEE Trans. Ind. Appl.* **1991**, *27*, 63–73. [CrossRef]
8. Zhao, B.; Song, Q.; Liu, W.; Sun, Y. Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system. *IEEE Trans. Power Electron.* **2013**, *29*, 4091–4106. [CrossRef]
9. He, P.; Khaligh, A. Comprehensive analyses and comparison of 1 kW isolated DC–DC converters for bidirectional EV charging systems. *IEEE Trans. Transp. Electrif.* **2016**, *3*, 147–156. [CrossRef]
10. Haghbin, S.; Alatalo, M.; Yazdani, F.; Thiringer, T.; Karlsson, R. The design and construction of transformers for a 50 kW three-phase dual active bridge dc/dc converter. In Proceedings of the 2017 IEEE Vehicle Power and Propulsion Conference (VPPC), Belfort, France, 11–14 December 2017; pp. 1–5.
11. Baars, N.H.; Everts, J.; Wijnands, C.G.; Lomonova, E.A. Performance evaluation of a three-phase dual active bridge DC–DC converter with different transformer winding configurations. *IEEE Trans. Power Electron.* **2015**, *31*, 6814–6823. [CrossRef]
12. Zhang, J.; Wang, Z.; Shao, S. A three-phase modular multilevel DC–DC converter for power electronic transformer applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *5*, 140–150. [CrossRef]
13. Segaran, D.; Holmes, D.G.; Mcgrath, B.P. Comparative analysis of single and three-phase dual active bridge bidirectional DC-DC converters. In Proceedings of the 2008 Australasian Universities Power Engineering Conference, Sydney, NSW, Australia, 14–17 December 2008; pp. 1–6.
14. van Hoek, H.; Neubert, M.; Kroeber, A.; De Doncker, R.W. Comparison of a single-phase and a three-phase dual active bridge with low-voltage, high-current output. In Proceedings of the 2012 International Conference on Renewable Energy Research and Applications (ICRERA), Nagasaki, Japan, 11–14 November 2012; pp. 1–6.
15. Chakraborty, S.; Vu, H.N.; Hasan, M.M.; Tran, D.D.; Baghdadi, M.E.; Hegazy, O. DC-DC converter topologies for electric vehicles, plug-in hybrid electric vehicles and fast charging stations: State of the art and future trends. *Energies* **2019**, *12*, 1569. [CrossRef]
16. Wang, Y.C.; Ni, F.M.; Lee, T.L. Hybrid modulation of bidirectional three-phase dual-active-bridge DC converters for electric vehicles. *Energies* **2016**, *9*, 492. [CrossRef]

17. Riedel, J.; Holmes, D.G.; McGrath, B.P.; Teixeira, C. ZVS soft switching boundaries for dual active bridge DC–DC converters using frequency domain analysis. *IEEE Trans. Power Electron.* **2016**, *32*, 3166–3179. [CrossRef]
18. CHAdeMO Association. *Technical Specifications of Quick Charger for Electric Vehicles*; CHAdeMO 2.0; CHAdeMO Association: Paris, France, 2018; 84p.
19. Chen, L.R.; Wu, S.L.; Shieh, D.T.; Chen, T.R. Sinusoidal-ripple-current charging strategy and optimal charging frequency study for Li-ion batteries. *IEEE Trans. Ind. Electron.* **2012**, *60*, 88–97. [CrossRef]
20. Bessman, A.; Soares, R.; Vadivelu, S.; Wallmark, O.; Svens, P.; Ekström, H.; Lindbergh, G. Challenging sinusoidal ripple-current charging of lithium-ion batteries. *IEEE Trans. Ind. Electron.* **2017**, *65*, 4750–4757. [CrossRef]
21. Uddin, K.; Moore, A.D.; Barai, A.; Marco, J. The effects of high frequency current ripple on electric vehicle battery performance. *Appl. Energy* **2016**, *178*, 142–154. [CrossRef]
22. Zhao, B.; Yu, Q.; Sun, W. Extended-phase-shift control of isolated bidirectional DC–DC converter for power distribution in microgrid. *IEEE Trans. Power Electron.* **2011**, *27*, 4667–4680. [CrossRef]
23. Shi, H.; Wen, H.; Chen, J.; Hu, Y.; Jiang, L.; Chen, G.; Ma, J. Minimum-backflow-power scheme of DAB-based solid-state transformer with extended-phase-shift control. *IEEE Trans. Ind. Appl.* **2018**, *54*, 3483–3496. [CrossRef]
24. Zhao, B.; Song, Q.; Liu, W. Efficiency characterization and optimization of isolated bidirectional DC–DC converter based on dual-phase-shift control for DC distribution application. *IEEE Trans. Power Electron.* **2012**, *28*, 1711–1727. [CrossRef]
25. Krismer, F.; Kolar, J.W. Closed form solution for minimum conduction loss modulation of DAB converters. *IEEE Trans. Power Electron.* **2011**, *27*, 174–188. [CrossRef]
26. van Hoek, H.; Neubert, M.; De Doncker, R.W. Enhanced modulation strategy for a three-phase dual active bridge–Boosting efficiency of an electric vehicle converter. *IEEE Trans. Power Electron.* **2013**, *28*, 5499–5507. [CrossRef]
27. Hu, J.; Soltau, N.; De Doncker, R.W. Asymmetrical duty-cycle control of three-phase dual-active bridge converter for soft-switching range extension. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016; pp. 1–8.
28. Hu, J.; Yang, Z.; Soltau, N.; De Doncker, R.W. A duty-cycle control method to ensure soft-switching operation of a high-power three-phase dual-active bridge converter. In Proceedings of the 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), Kaohsiung, Taiwan, 3–7 June 2017; pp. 866–871.
29. Huang, J.; Li, Z.; Shi, L.; Wang, Y.; Zhu, J. Optimized modulation and dynamic control of a three-phase dual active bridge converter with variable duty cycles. *IEEE Trans. Power Electron.* **2018**, *34*, 2856–2873. [CrossRef]
30. Jiang, H.; Wei, J.; Dai, X.; Zheng, C.; Ke, M.; Deng, X.; Sharma, Y.; Deviny, I.; Mawby, P. SiC MOSFET with built-in SBD for reduction of reverse recovery charge and switching loss in 10-kV applications. In Proceedings of the 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Sapporo, Japan, 28 May–1 June 2017; pp. 49–52.
31. Sung, W.; Baliga, B.J. On developing one-chip integration of 1.2 kV SiC MOSFET and JBS diode (JBSFET). *IEEE Trans. Ind. Electron.* **2017**, *64*, 8206–8212. [CrossRef]
32. Sung, W.; Baliga, B.J. Monolithically integrated 4H-SiC MOSFET and JBS diode (JBSFET) using a single ohmic/Schottky process scheme. *IEEE Electron Device Lett.* **2016**, *37*, 1605–1608. [CrossRef]
33. Nguyen, D.D.; Yukitta, K.; Katou, A.; Yoshida, S. A comparison study of modulation methods for three-phase dual-active-bridge converters in battery charging applications. In Proceedings of the 2021 IEEE 12th Energy Conversion Congress & Exposition-Asia (ECCE-Asia), Singapore, 24–27 May 2021; pp. 1033–1038.
34. Nguyen, D.D.; Yukita, K.; Katou, A.; Yoshida, S. A new method to extend the soft-switching area of three-phase dual-active-bridge converters. In Proceedings of the 2021 IEEE 12th Energy Conversion Congress & Exposition-Asia (ECCE-Asia), Singapore, 24–27 May 2021; pp. 736–742.
35. Nguyen, D.D.; Bui, N.T.; Yukita, K. Design and optimization of three-phase dual-active-bridge converters for electric vehicle charging stations. *Energies* **2019**, *13*, 150. [CrossRef]
36. Hu, J.; Yang, Z.; Cui, S.; De Doncker, R.W. Closed-form asymmetrical duty-cycle control to extend the soft-switching range of three-phase dual-active-bridge converters. *IEEE Trans. Power Electron.* **2021**, *36*, 9609–9622. [CrossRef]
37. McLyman, C.W.T. *Transformer and Inductor Design Handbook*; CRC Press: Boca Raton, FL, USA, 2004.