

## Article

# A Single Source Self-Balanced Boost MLI with Reduced Part Count for EV Applications

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**Abstract:** As the use of inductor-based topologies demands a large amount of space, capacitor-based topologies have garnered attention. Electric Vehicles (EVs) are usually equipped with two-level inverters, which require separate control strategies for each level and synchronizing the strategies increases the complexity of operation and makes them unreliable. Therefore, a single-stage converter with boost and conversion abilities with better power quality at optimal component count and efficiency is needed. A novel capacitor-based boost multilevel inverter (CB-MLI) topology is proposed in this paper as it is found suitable for EV and HEV applications. It is capable of generating an eleven-level waveform with only eleven switches, three capacitors, and a single isolated source. The self-balancing property of the capacitors makes the topology one of a kind. A constant carrier PWM-based control strategy is utilized to switch the IGBTs. Testing results from hardware setup confirm the proposed capacitor-based CB-MLI topology operating modes and potentiality. Lastly, by highlighting the proposed and existing MLI circuits, the benefits of the recommended configuration are outlined by component count and total cost. Additionally, it is a simplified design that needs fewer footprint areas and space.

**Keywords:** single-stage; multilevel inverter; switched capacitor; loss calculation; boosting gain; self-balancing



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## 1. Introduction

Demand for EVs [1] has been increasing rapidly as a result of the environmental issues and fuel scarcity associated with combustion engine vehicles. First-generation EVs use DC motors [2] to produce the tractive effort required by the vehicle to advance [3]. It did not take many years for the DC motors to lose their significance in the EV domain when researchers found AC motors offer more desirable characteristics than DC motors with better efficiency. Almost all EVs are equipped with distributed AC motors for vehicle propulsion nowadays. It is a well-established fact that all EVs are powered by battery systems [4], a DC form of electricity [5]. The voltage level of the battery systems [6] is at a low level, thus forcing us to introduce a voltage boost and DC-to-AC conversion before feeding the battery unit power to AC MOTOR.

Power semiconductor devices were revolutionized in the early 1990s because of their efficient conversion [7] and control abilities [8]. The extensive power handling capability at compact sizes is a significant advantage. The major problem associated with the use of power semiconductor devices is harmonics. The harmonics are imposed over the fundamental cause wave shape to deviate from the sinusoidal. Smoothing the deviated waveform demands large inductance and capacitance values in order to filter out harmonics. The EV power source is a DC form of electricity, and EV motors demand AC supply at a high frequency. It incorporates a need for a DC-AC converter (essentially, an inverter [9]), along

with the voltage boost [10] capability in EV [11]. The Inverter topologies are advancing in such a way as to nullify filter requirements completely in the converter. The first step towards achieving that was the invention of multilevel inverters (MLI).

The basic H-bridge inverter [12] produces a square waveform that contains all the odd harmonics with a total THD of 48.3%. In the same H-bridge converter, when operated with the three-level waveform (with a pulse width of 120), the THD value tumbles to 31.1%. With a single-step waveform, it even eliminated the triplen harmonics out of the waveform essentially without any use of filter, and the THD value further decreases as the number of levels in the waveform increases. We can say the THD value of a waveform is inversely proportional to the number of steps in the waveform. In addition to the output wave shape, MLIs offer additional advantages such as reduced  $dv/dt$  stress on switches, lower common mode voltage, lower input current distortion, and reduced filter ratings.

The problem with the conventional MLIs, such as cascaded H-bridge, are the multi-source requirements which are an unlikely case in the practical world. To avoid the isolated source requirement, we shifted to diode-clamped MLI, where we use a cascaded capacitor technique for voltage division, which also demands a large device count as the number of levels increases. Clamping of levels is achieved with the help of diodes. In flying capacitor MLI topology [12], capacitors are used to maintain levels instead of diodes. All the basic topologies [13,14] demand a large switch count, and a large number of capacitors is required in NPC. This forces us to look into new topologies with all the advantages of MLIs but with a reduced component count.

Boost and inversion of voltage with multiple stages [15] make the conversion circuit bulky and unreliable. Thus, a topology that boosts and inverts the DC supply in a single stage offers better results with compact and economic advantages. The boost MLIs [15] are finding recognition in the recent trend as the advantages offered are far superior to those of the conventional systems. The circuit compactness and lower THD with boosting capability are major among them.

High device count and voltage stress in the converter are the significant shortcomings of circuits as the boosting gain increases. These limitations influence the overall cost of the converter significantly. Therefore, the converter should not undergo a greater component count and total standing voltage (TSV) for a cost-effective solution. Hence, a topology of capacitor-based 2.5 times boost, 11-level inverter is proposed. The topology demands only 11 switches, out of which 2 are complimentary, and there are three capacitors with a single DC-voltage source. The maximum blocking voltage of the switch decides the ratings and economics of the circuit. The topology demands four switches with a blocking voltage of  $1.5V_{dc}$  and the all remaining switches with the voltage of  $V_{dc}$ . The total standing voltage of the topology is  $12.5V_{dc}$ . The voltage boost is achieved by significant charging and discharging of capacitors. The capacitors with a rating of  $0.5V_{dc}$  are required. As all the capacitors are used in aiding with the source, the circuit delivers a maximum boost, which is  $2.5V_{dc}$ .

One of the major advantages associated with the proposed topology is the capacitors' self-balancing property. During the charging of capacitors, the source feeds supply to capacitors through switches, whose on-state resistances are very low, thus making the charging time of capacitors low in value, but when the capacitors start to feed load, the resistance seen by the capacitors is of a high value. This makes the capacitors' charging time far faster than the discharging time. As the charging time is far lesser than the discharging time, even before it discharges, the capacitor becomes charged, thus causing the capacitor to maintain its voltage at around  $0.5 V_{dc}$  with lower ripple. The essential aspects of the recommended topology are:

- Smaller part count;
- The eleven-level load voltage generation with 2.5-times boost capability;
- Inherent self-balance ability and being simple to control;
- There are no limitations on the power factor or modulation index;
- To generate bipolar levels, no extra H-bridge is required;

- Lower total standing voltage (TSV).

This work aims to develop a novel voltage boost inverter circuit with a smaller component count and low TSV by mitigating the shortcomings. A thorough analysis of the working principle is discussed in Section 2. Section 3 presents modulation, capacitor size, and power loss calculations. The corresponding simulation results for the proposed circuit are provided in Section 4. To support the claims of the proposed inverter, sufficient hardware verification is presented in Section 5. Additionally, quantitative and cost analyses are performed to distinguish the merits of the proposed converter in Section 6. Finally, the conclusions are presented in Section 7.

## 2. Proposed Topology

### 2.1. Description of Proposed Topology

The proposed boost-MLI structure based on the switched capacitors is shown in Figure 1. This design pattern has a leg on two ends to produce load voltages with both negative and positive waveforms. The suggested circuit contains 11 semiconductor-switching devices ( $S_1$  and  $\bar{S}_1$ ,  $S_9$  and  $\bar{S}_9$ ,  $S_2, S_3, S_4, S_5, S_6, S_7$ , and  $S_8$ ), and an isolated DC-voltage source ( $V_{dc}$ ). Additionally, the suggested structure includes three boosting capacitors ( $C_1, C_2$ , and  $C_3$ ) to minimize the requirement of the number of sources.  $V_{C_1}, V_{C_2}$ , and  $V_{C_3}$  are the voltages across the capacitors  $C_1, C_2$ , and  $C_3$ , respectively. The recommended boost-MLI topology uses the fundamental frequency PWM (FF-PWM) control switching method to provide eleven voltage levels at the load end. The possible magnitude of voltage levels are  $+2.5V_{dc}, +2V_{dc}, +1.5V_{dc}, +V_{dc}, +0.5V_{dc}$ , zero ( $0V_{dc}$ ), and  $-0.5V_{dc}, -V_{dc}, -1.5V_{dc}, -2V_{dc}, -2.5V_{dc}$ . The significant switching sequence needed to build the eleven levels of the proposed boost-MLI topology is shown in Table 1.

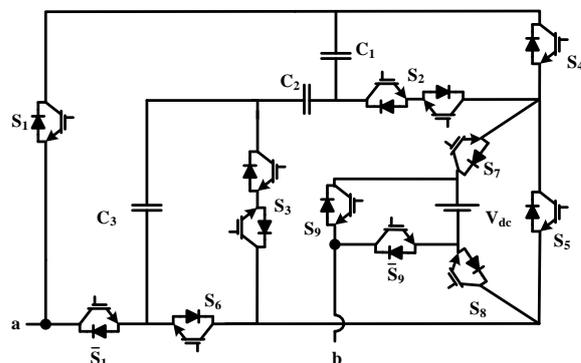


Figure 1. Proposed boost-MLI Structure.

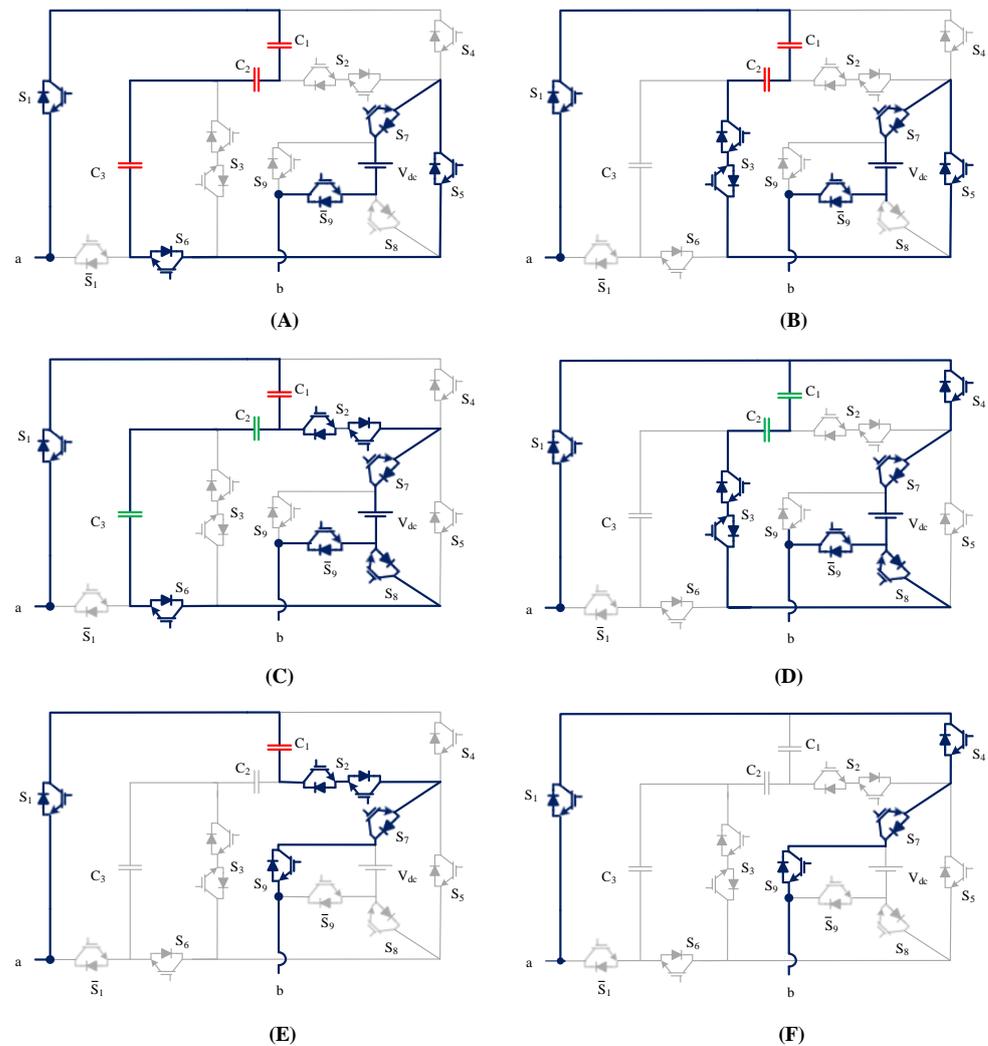
Table 1. Switching states for Proposed CB-MLI.

$V_o$	$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$	$S_7$	$S_8$	$S_9$	$V_{C_1}$	$V_{C_2}$	$V_{C_3}$
$2.5V_{dc}$	1	0	0	0	1	1	1	0	0	D	D	D
$2V_{dc}$	1	0	1	0	1	0	1	0	0	D	D	-
$1.5V_{dc}$	1	1	0	0	0	1	1	1	0	D	C	C
$1V_{dc}$	1	0	1	1	0	0	1	1	0	C	C	-
$0.5V_{dc}$	1	1	0	0	0	0	1	0	1	D	-	-
0	1	0	0	1	0	0	1	0	1	-	-	-
0	0	0	0	0	0	1	0	1	0	-	-	-
$-0.5V_{dc}$	0	0	1	0	0	0	0	1	0	-	-	D
$-1V_{dc}$	0	0	1	0	0	0	0	1	0	-	C	C
$-1.5V_{dc}$	0	0	1	1	0	0	1	1	1	C	C	D
$-2V_{dc}$	0	1	0	0	1	0	0	1	1	-	D	D
$-2.5V_{dc}$	0	0	0	1	1	0	0	1	1	D	D	D

C: Charging; D: Discharging; -: No effect.

## 2.2. Modes of Operation

For the proposed CB-MLI topology, the different levels of output waveforms are developed by firing appropriate switches, as mentioned in Table 1. The conduction paths of the topology are illustrated graphically in Figures 2 and 3.  $V_{C_1}$ ,  $V_{C_2}$ , and  $V_{C_3}$  are the voltages across the capacitors  $C_1$ ,  $C_2$ , and  $C_3$ , respectively. The operating modes of the proposed topology are as follows.



**Figure 2.** Suggested boost-MLI operating modes: (A)  $2.5V_{dc}$ , (B)  $2V_{dc}$ , (C)  $1.5V_{dc}$ , (D)  $V_{dc}$ , (E)  $0.5V_{dc}$ , (F) 0.

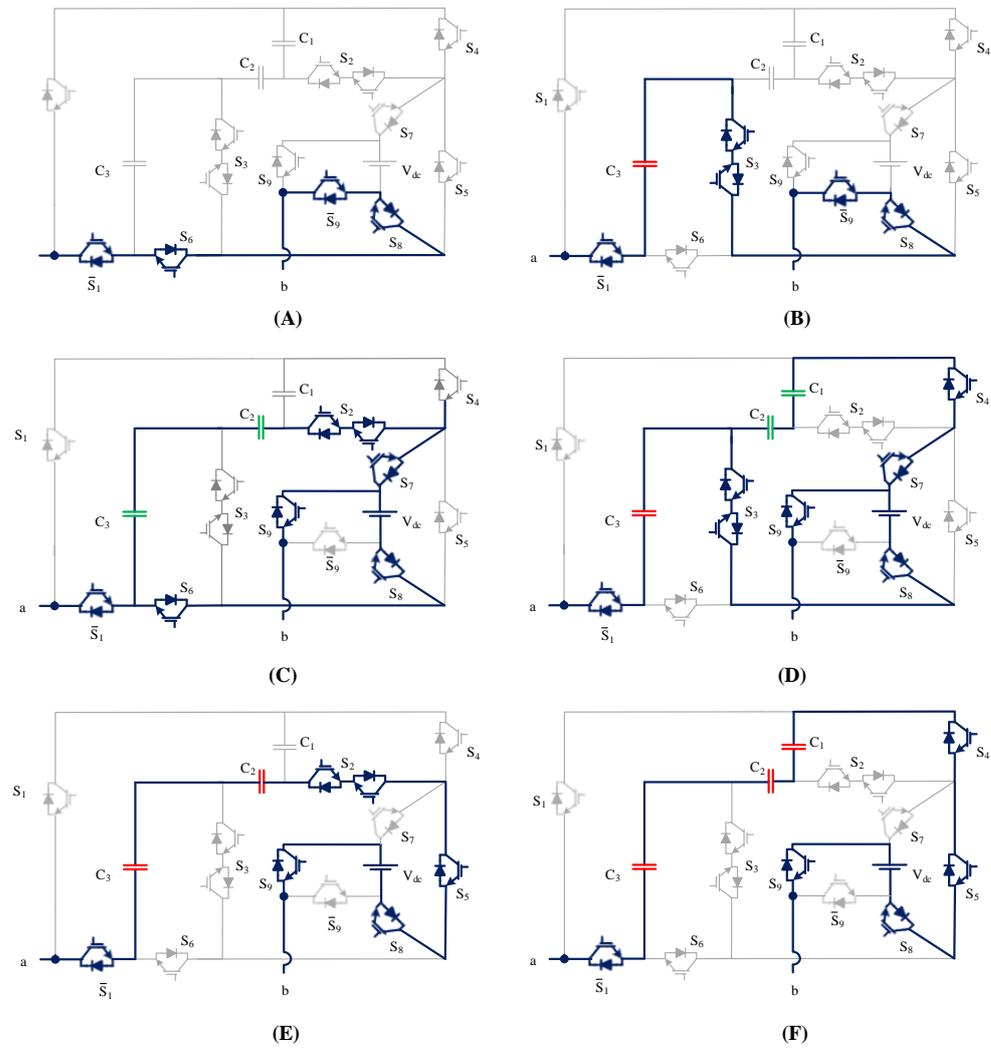
(1)  $+2.5V_{dc}$  Mode [Figure 2A]: The switches  $S_1$ ,  $S_5$ ,  $S_6$ ,  $S_7$ , and  $\bar{S}_9$  are triggered to achieve the output as  $2.5V_{dc}$ . During this state source, the capacitors  $C_1$  and  $C_2$  and  $C_3$  feed the load. The corresponding flow path is depicted in Figure 2A. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C_1} = 0.5V_{dc} \\ V_{C_2} = 0.5V_{dc} \\ V_{C_3} = 0.5V_{dc} \\ V_0 = V_{C_1} + V_{C_2} + V_{C_3} + V_{dc} = 2.5V_{dc}. \end{cases} \quad (1)$$

(2)  $+2V_{dc}$  Mode [Figure 2B]: The switches  $S_1$ ,  $S_3$ ,  $S_5$ ,  $S_7$ , and  $\bar{S}_9$  are triggered to achieve the output as  $2V_{dc}$ . During this state source, the capacitors  $C_1$  and  $C_2$  feed the load.

The corresponding flow path is depicted in Figure 2B. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C1} = 0.5V_{dc} \\ V_{C2} = 0.5V_{dc} \\ V_0 = V_{C1} + V_{C2} + V_{dc} = 2V_{dc}. \end{cases} \quad (2)$$



**Figure 3.** Operating states of proposed boost-MLI: (A) 0, (B)  $-0.5V_{dc}$ , (C)  $-V_{dc}$ , (D)  $-1.5V_{dc}$ , (E)  $-2V_{dc}$ , (F)  $-2.5V_{dc}$ .

(3)  $+1.5V_{dc}$  Mode [Figure 2C]: The switches  $S_1, S_2, S_7,$  and  $\bar{S}_9$  are triggered to achieve the output as  $1.5V_{dc}$ . In this state, the capacitor  $C_1$  is made to support the source, feed the load, and thus achieve the desired  $1.5V_{dc}$  as output. The capacitors  $C_2$  and  $C_3$  are charged through switches  $S_6$  and  $S_8$  to  $0.5V_{dc}$  each during this level. The corresponding flow path is depicted in Figure 2C. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C1} = 0.5V_{dc} \\ V_{C2} = 0.5V_{dc} \\ V_{C3} = 0.5V_{dc} \\ V_0 = V_{C1} + V_{dc} = 1.5V_{dc}. \end{cases} \quad (3)$$

(4)  $+V_{dc}$  Mode [Figure 2D]: The switches  $S_1, S_4, S_7,$  and  $\bar{S}_9$  are turned ON to achieve  $V_{dc}$  output. Source, along with load feed, will charge the capacitors  $C_1$  and  $C_2$  through

switches  $S_3$ , and  $S_8$ . As the resistances of switches during on-state is low, the charging time constant of capacitors is very low. The corresponding flow path is depicted in Figure 2D. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C1} = 0.5V_{dc} \\ V_{C2} = 0.5V_{dc} \\ V_0 = V_{dc}. \end{cases} \quad (4)$$

(5)  $+0.5V_{dc}$  Mode [Figure 2E]: The output  $0.5V_{dc}$  can be achieved by firing the gates of  $S_1$ ,  $S_2$ ,  $S_7$ , and  $S_9$  switches, thus making the capacitor  $C_1$  to feed power demanded by the load during this mode. As the discharging time constant is a far greater value than the charging time, the voltage fall across the capacitor is small. The capacitors  $C_2$  and  $C_3$  remain idle during this mode. All remaining switches are in blocking state. The corresponding flow path is depicted in Figure 2E. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C1} = 0.5V_{dc} \\ V_0 = V_{C1} = 0.5V_{dc}. \end{cases} \quad (5)$$

(6) ZERO Mode [Figures 2F and 3A]: During the output, zero modes have two sets of switching combinations. One involves the switches  $S_1$ ,  $S_4$ ,  $S_7$ , and  $S_9$  being triggered, and the other combination is the switches  $\bar{S}_1$ ,  $S_6$ ,  $S_8$ , and  $\bar{S}_9$  being triggered. This shortens the load through the path, as depicted in Figures 2F and 3A. The rest of the switches are in blocking state, and three capacitors remain idle during this mode, i.e., neither charging, nor discharging.

$$\begin{cases} V_{C1} = 0 \\ V_{C2} = 0 \\ V_{C3} = 0 \\ V_0 = 0. \end{cases} \quad (6)$$

(7)  $-0.5V_{dc}$  Mode [Figure 3B]: The output  $-0.5V_{dc}$  can be achieved by firing the gates of  $\bar{S}_1$ ,  $S_3$ ,  $S_8$ , and  $\bar{S}_9$  switches, thus making the capacitor  $C_3$  feed power demanded by the load during this mode. As the discharging time constant has a far greater value than the charging time, the voltage fall across the capacitor is small. The capacitors  $C_1$  and  $C_2$  remains idle during this mode. All remaining switches will be in blocking state. The corresponding flow path is depicted in Figure 3B. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C3} = 0.5V_{dc} \\ V_0 = -V_{C3} = -V_{dc}/2. \end{cases} \quad (7)$$

(8)  $-V_{dc}$  Mode [Figure 3C]: The switches  $\bar{S}_1$ ,  $S_6$ ,  $S_8$ , and  $S_9$  are turned ON to achieve  $-V_{dc}$  output. Source, along with load feed, will charge the capacitors  $C_2$  and  $C_3$  through switches  $S_2$ , and  $S_7$ . As the resistances of switches during on-state is low, the charging time constant of capacitors is very low. The corresponding flow path is depicted in Figure 3C. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C2} = 0.5V_{dc} \\ V_{C3} = 0.5V_{dc} \\ V_0 = -V_{dc}. \end{cases} \quad (8)$$

(9)  $-1.5V_{dc}$  Mode [Figure 3D]: The switches  $\bar{S}_1$ ,  $S_3$ ,  $S_8$ , and  $S_9$  are triggered to achieve the output as  $-1.5V_{dc}$ . During this state, the capacitor  $C_1$  is made to support the source, feed the load, and thus achieve the desired  $-1.5V_{dc}$  as output. The capacitors  $C_2$  and  $C_3$

are charged through the switches  $S_4$  and  $S_7$  at this level. The corresponding flow path is depicted in Figure 3D. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C1} = 0.5V_{dc} \\ V_0 = -V_{C1} - V_{dc} = -3V_{dc}/2. \end{cases} \quad (9)$$

(10)  $-2V_{dc}$  Mode [Figure 3E]: The switches  $\bar{S}_1$ ,  $S_2$ ,  $S_5$ ,  $S_8$ , and  $S_9$  are triggered to achieve the output as  $-2V_{dc}$ . During this state source, the capacitors  $C_2$  and  $C_3$  feed the load. The corresponding flow path is depicted in Figure 3E. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C2} = 0.5V_{dc} \\ V_{C3} = 0.5V_{dc} \\ V_0 = -V_{C2} - V_{C3} - V_{dc} = -2V_{dc}. \end{cases} \quad (10)$$

(11)  $-2.5V_{dc}$  Mode [Figure 3F]: The switches  $\bar{S}_1$ ,  $S_4$ ,  $S_5$ ,  $S_8$  and  $S_9$  are triggered to achieve the output as  $-2.5V_{dc}$ . During this state source, the capacitors  $C_1$ ,  $C_2$ , and  $C_3$  feed the load. The corresponding flow path is depicted in Figure 3F. Thus, the resulting load voltage is expressed as

$$\begin{cases} V_{C1} = 0.5V_{dc} \\ V_{C2} = 0.5V_{dc} \\ V_{C3} = 0.5V_{dc} \\ V_0 = -V_{C1} - V_{C2} - V_{C3} - V_{dc} = -2.5V_{dc}. \end{cases} \quad (11)$$

### 3. Modulation Technique

Space vector, sinusoidal, selective harmonic elimination pulse width modulation (SV-, S-, SHE-PWM), and basic fundamental frequency switching are a few of the controlled modulation techniques [16] employed by power converters to produce a multilevel output, which is in the sinusoidal shape of voltage waveforms. Numerous different control techniques are stated in [17]. Here, the fundamental frequency PWM (FF-PWM) control technique [18] is employed to provide gating signals for semiconductor switches. Level-shifted constant carrier signals with similar phases are coupled with an ideal reference sinusoidal pulse to produce gating signals to drive the semiconductor switching devices. This control technique requires  $(N_l - 1)/2$  constant carrier signals to obtain the required output voltage with  $N_l$  levels. In Figure 4, the designing model of the output voltage waveform at any given load is illustrated. At the output terminals, eleven voltage levels are produced using four constant carrier pulses ( $car_1 - car_4$ ) with the same frequency but different offset values for the voltage parameter. These higher-frequency constant carrier signals are frequently compared with an absolute value of sinusoidal reference pulse ( $V_{ref} = |V_m \sin(\omega t)|$ ) to generate gating signals for the semiconductor switches. Table 1 lists the different operating modes described by the recommended control switching strategy for semiconductor switches. The amplitude modulation index ( $m_a$ ) for triangular carrier pulses is determined as

$$m_a = \frac{V_m}{\left(\frac{N_l-1}{2}\right) \times \hat{V}_{Car}} \quad (12)$$

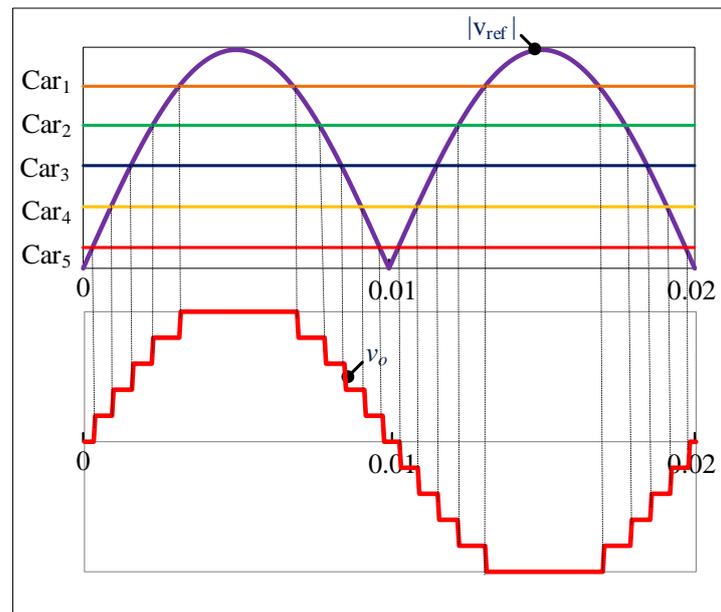
Here,  $\hat{V}_{Car}$ , and  $V_m$  are peak magnitudes of carrier and reference pulses, respectively.

The recommended capacitor-based CB-MLI structure uses one reference signal with 50 HZ frequency, a fundamental sinusoidal frequency, and four carrier pulses. Numerous carrier signal patterns, such as triangular, ramping, trapezoidal, sinusoidal, etc., can also be

used. The root mean square (RMS) value of the resultant output for eleven-level voltage at different  $m_a$  values is expressed as follows:

$$V_{ab} \simeq m_a \frac{V_{dc}}{\sqrt{2}} \quad (13)$$

The suggested structure has the feasibility that it can operate with all the control modulation techniques. There is no impact on capacitor voltage balancing when the circuit performs at the lower range of frequencies. However, the capacitor size negligibly depends on the switching frequency. When the switching frequency rises, the desired output waveform of the voltage chops more frequently. Consequently, it will only obtain limited time intervals to gain charge.



**Figure 4.** Modulation control method for proposed CB-MLI Topology.

The final switching equations derived from the above Figure 5 are as given for all semiconductor switches as follows:

$$S_1 = P \quad (14)$$

$$S_2 = (A_1 \cdot \bar{A}_2 + A_3 \cdot \bar{A}_4) \cdot P + [(A_2 \cdot \bar{A}_3 + A_4 \cdot \bar{A}_5) \cdot \bar{P}] \quad (15)$$

$$S_3 = (A_1 \cdot \bar{A}_2 + A_3 \cdot \bar{A}_4) \cdot \bar{P} + [(A_2 \cdot \bar{A}_3 + A_4 \cdot \bar{A}_5) \cdot P] \quad (16)$$

$$S_4 = (A_1 \cdot \bar{A}_2 + A_3 \cdot \bar{A}_4 + A_5) \cdot \bar{P} + [(A_2 \cdot \bar{A}_3 + \bar{A}_1) \cdot P] \quad (17)$$

$$S_5 = A_4 + A_5 \quad (18)$$

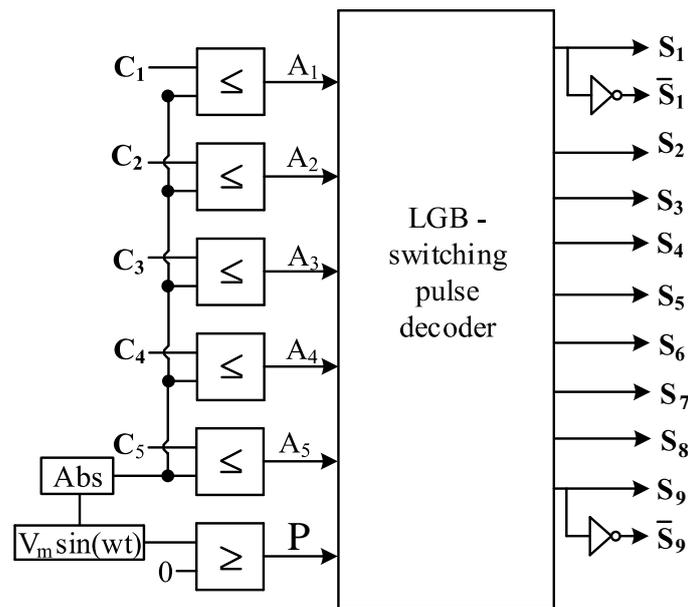
$$S_6 = (A_3 \cdot \bar{A}_4 + A_5) \cdot P + [(A_2 \cdot \bar{A}_3 + \bar{A}_1) \cdot \bar{P}] \quad (19)$$

$$S_7 = A_1 \cdot \bar{A}_2 + A_2 \cdot \bar{A}_3 + A_3 \cdot \bar{A}_4 + (\bar{A}_1 + A_4 + A_5) \cdot P \quad (20)$$

$$S_8 = A_2 \cdot \bar{A}_3 + A_3 \cdot \bar{A}_4 + (\bar{A}_1 + \bar{A}_2 + A_4 + A_5) \cdot \bar{P} \quad (21)$$

$$S_9 = (\bar{A}_1 + \bar{A}_2) \cdot P + [(A_2 + A_3 + A_4 + A_5) \cdot \bar{P}] \quad (22)$$

Logic gate-based (LGB) switching pulse decoder is a function block which contains the switching pattern of all semiconductors. Boolean Equations (3)–(11) are programmed in this decoder block to generate the required voltage level.



**Figure 5.** Switching scheme for eleven-level generation.

### 3.1. Determination of Capacitance

Estimating capacitance is essential in capacitor-based inverters, especially switched capacitor-based MLIs, to maintain the ripples below acceptable bounds. The smaller voltage ripple content in the capacitor causes fewer losses, leading to more inverter efficiency [19]. The large discharge period, allowable ripples, and maximum current of the capacitors are considered while calculating the capacitance value. Figure 6 indicates the time durations ( $t_1$ ,  $t_2$ ,  $t_3$ , etc.) on every step change. Whereas a loading is entirely resistive, output current and voltage are in perfect harmony. At this resistive load (unity power factor (UPF)), the peak current at the middle of the integration leads to maximum discharge in the capacitor. This means that if designed for UPF, the capacitor retains fewer ripples for other loads. Considering UPF ( $m_a = 1$ ), the longest discharging period of boosting capacitor ( $C_1$ ) in Figure 4 occurs between  $[t_3, t_8]$ , and  $[t_1 - t_2, t_9 - t_{10}, t_{15} - t_{16}]$  respectively. As the load waveform adheres to the property of symmetry, positive and negative cycles have equal periods. Accordingly, the time interval between  $[t_9, t_{10}]$  is similar to  $[t_1, t_2]$  and duration between  $[t_7, t_8]$  is similar to  $[t_3, t_4]$  because of quarter wave symmetry. Additionally, each capacitor's maximum discharge is computed [17] using the following equations:

$$\Delta Q_{C_n} = \int_{t_3}^{t_8} I_{load} \sin(\omega t) dt \quad (23)$$

where  $I_{load}$  is peak current of the capacitor, and  $\omega$  is the fundamental frequency in rad/s.

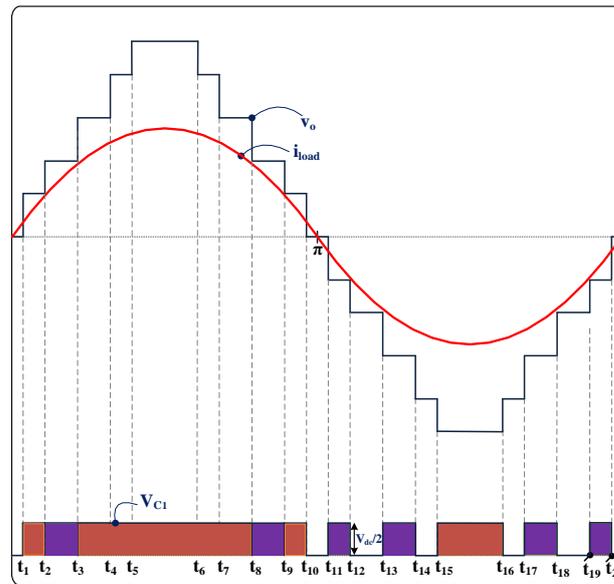


Figure 6. Key waveforms of proposed eleven-level inverter.

The time duration ( $t_1 - t_{10}$ ) is estimated as

$$t_1 = \frac{\sin^{-1}(Car_5/V_{ref})}{2\pi f_{ref}} = 2.8944 \times 10^{-4} \text{ sec} \quad (24)$$

$$t_2 = \frac{\sin^{-1}(Car_4/V_{ref})}{2\pi f_{ref}} = 8.788 \times 10^{-4} \text{ sec} \quad (25)$$

$$t_3 = \frac{\sin^{-1}(Car_3/V_{ref})}{2\pi f_{ref}} = 1.499 \times 10^{-3} \text{ sec} \quad (26)$$

$$t_4 = \frac{\sin^{-1}(Car_2/V_{ref})}{2\pi f_{ref}} = 2.19 \times 10^{-3} \text{ sec} \quad (27)$$

$$t_5 = \frac{\sin^{-1}(Car_1/V_{ref})}{2\pi f_{ref}} = 3.05 \times 10^{-3} \text{ sec} \quad (28)$$

$$t_6 = \frac{\pi - \sin^{-1}(Car_1/V_{ref})}{2\pi f_{ref}} = 6.9494 \times 10^{-3} \text{ sec} \quad (29)$$

$$t_7 = \frac{\pi - \sin^{-1}(Car_2/V_{ref})}{2\pi f_{ref}} = 7.804 \times 10^{-3} \text{ sec} \quad (30)$$

$$t_8 = \frac{\pi - \sin^{-1}(Car_3/V_{ref})}{2\pi f_{ref}} = 8.5 \times 10^{-3} \text{ sec} \quad (31)$$

$$t_9 = \frac{\pi - \sin^{-1}(Car_4/V_{ref})}{2\pi f_{ref}} = 9.1211 \times 10^{-3} \text{ sec} \quad (32)$$

$$t_{10} = \frac{\pi - \sin^{-1}(Car_5/V_{ref})}{2\pi f_{ref}} = 9.7105 \times 10^{-3} \text{ sec} \quad (33)$$

Therefore, the minimum value of capacitance required for capacitor voltage with allowable ripples proportion ( $x\%$ ) is given as:

$$C_n = \frac{\Delta Q_{C_n}}{x\% \times V_{C_n}} \quad (34)$$

The desired capacitance value for a 50 V supply at UPF (R-load (30  $\Omega$ )) with 3% of allowable voltage ripple content is determined as

$$C_1 = \frac{1}{x\% \times V_{CB}} \int_{t_3}^{t_6} I_o \sin(\omega t) dt \quad (35)$$

$$C_1 = \frac{1}{0.03 \times 25} \int_{1.499 \times 10^{-3}}^{8.5 \times 10^{-3}} 3 \sin(2\pi f t) dt \quad (36)$$

$$C_1 = 2.132 \text{ mF} \quad (37)$$

Similarly, the capacitance values of the capacitors ( $C_2$  and  $C_3$ ) are calculated, and those are almost equal to  $C_1$ .

### 3.2. Power Loss Calculation

The suggested methodology in [20] is used to determine approximated output total power losses. There are two types of electrical power losses caused by semiconductor switches: 1. conduction loss ( $P_{cd}$ ) and 2. switch loss ( $P_{sw}$ ). The mathematical formula for switching loss ( $P_{sw}$ ) of the proposed structure is defined as:

$$P_{sw} = f \left[ \sum_{i=1}^{10} \left( \sum_{k=1}^{N_{ON,i}} E_{ON,ik} + \sum_{k=1}^{N_{OFF,i}} E_{OFF,ik} \right) \right] \quad (38)$$

where  $E_{ON}$  = Power loss during ON-state, and  $E_{OFF}$  = Power loss during OFF-state.

The total energy loss during the ON-state of a switch is expressed as

$$E_{ON} = \int_0^{t_{ON}} v(t) i(t) dt \quad (39)$$

The total energy loss during the OFF-state of a switch is expressed as

$$E_{OFF} = \int_0^{t_{OFF}} v(t) i(t) dt \quad (40)$$

The conduction losses for an IGBT ( $P_{c,t}(t)$ ) and a diode ( $P_{c,d}(t)$ ) within the ON-state are calculated as follows:

$$P_{c,t}(t) = V_s(t) i(t) \quad (41)$$

$$P_{c,d}(t) = V_d(t) i(t) \quad (42)$$

The following equation represents the extensive conductive switching losses ( $P_c$ ):

$$P_c(t) = P_{c,t}(t) + P_{c,d}(t) \quad (43)$$

The overall conduction losses of the suggested capacitor-based CB-MLI circuit are the sum of  $P_c$  for all semiconductor switches in a given operating state, which includes  $N_d(t)$  diodes, and  $N_i(t)$  IGBTs.

$$P_c = \frac{1}{\pi} \int_0^\pi (N_i(t) V_s(t) + N_d(t) V_d(t)) i(t) dt \quad (44)$$

Additionally, losses are caused by ripple current in the voltage waveform and the capacitor's intrinsic resistance. While in the charging state, the change between the volt-

age across capacitors and the reference input supply will create voltage ripple losses. The amount of ripple content across each capacitor is determined as follows:

$$\Delta V_{C_n} = \frac{1}{C_n} \int_t^{t'} i_{C_n}(t) dt. \quad (45)$$

The current ( $i_{C_n}$ ) flows through the  $n$ th capacitor during the time interval, which is obtained in the suggested circuit. As a result, the capacitor ripple loss ( $P_{C_{rpl}}$ ) can always be defined by including capacitance, fundamental frequency, and ripple content in the voltage waveform as parameters

$$P_{C_{rpl}} = \frac{f_{ref}}{2} \sum_{n=1}^2 (C_n \times \Delta V_{C_n}^2) \quad (46)$$

$$P_{C_{rpl}} = \frac{f_{ref}}{2} (C_{LD} \times \Delta V_{C_{LD}}^2 + C_B \times \Delta V_{C_B}^2) \quad (47)$$

The proposed CB-MLI circuit total losses are mathematically expressed as follows:

$$P_T = P_{sw} + P_c + P_{C_{rpl}} \quad (48)$$

Hence, the proposed capacitor-based CB-MLI efficiency is calculated as

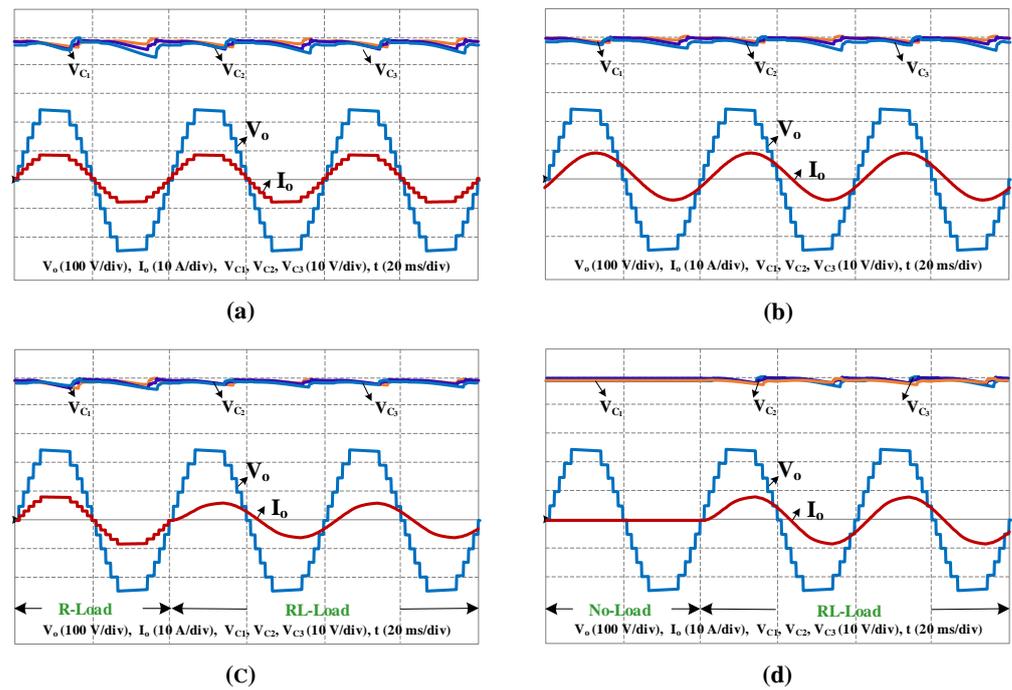
$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_T} \quad (49)$$

#### 4. Simulations

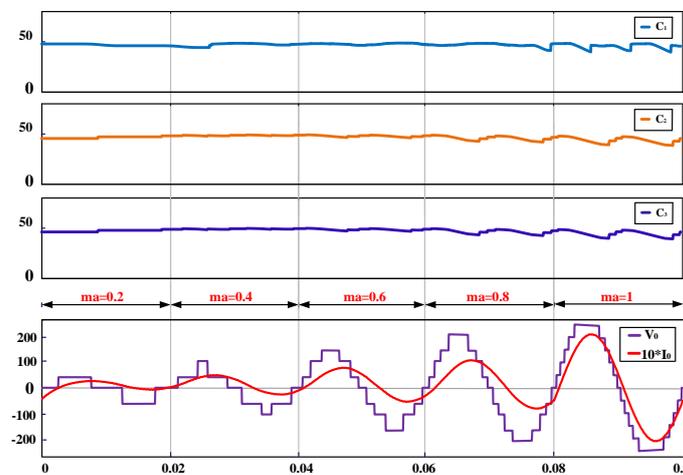
Simulations were performed in MATLAB/SIMULINK to validate the proposed switched capacitor-based CB-MLI structure and FF-PWM-based switching pattern. In this case, the amplitude modulation index ( $m_a$ ) is 1. The configuration presented in this study has three boosting capacitors ( $C_1$ ,  $C_2$ , and  $C_3$ ) with 2.2 mF each value, and an isolated 100 V dc source is used. In the present case, they provide a 30  $\Omega$  R-load and a 30  $\Omega$ -50 mH RL-load, assuming that the converter's parts will be nearly ideal. In Section 4, it is stated that the FF-PWM approach is used to generate gate pulses to create an eleven-level output voltage.

The proposed CB-MLI configuration generates the eleven-level output voltage waveform, shown in Figure 7 at different load conditions. Additionally, the corresponding output currents waveforms are depicted in Figure 7. Both output voltage and output current are achieved using the FF-PWM switching technique. The proposed topology is tested for an R-Load of 30  $\Omega$ ; the corresponding results, i.e., output voltage, current, and capacitor voltages, are shown in Figure 7a. Similarly, Figure 7b shows the output results at RL-Load of 30  $\Omega$ -50 mH. To test the proposed inverter at transient conditions, here, we consider the load variations as R to RL-Load and No-Load to RL-Load. The corresponding outcomes are shown in Figure 7c,d, respectively.

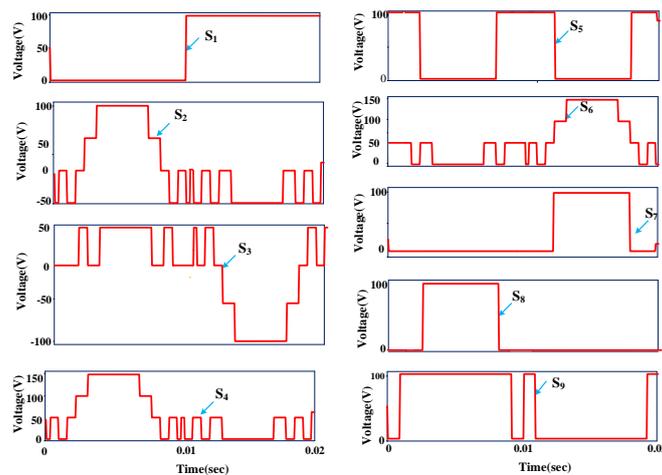
In Figure 7, the waveform of voltage across capacitors ( $C_1$ ,  $C_2$ , and  $C_3$ ) are also shown, and it is observed that the voltage ripples are maintained at low value. Additionally, the output voltage, current, and voltage across the capacitors variations at different modulation index values ( $m_a = 0.2$ ,  $m_a = 0.4$ ,  $m_a = 0.6$ ,  $m_a = 0.8$ , and  $m_a = 1$ ) are presented in Figure 8, and noticed that at  $m_a = 0.2$ ,  $m_a = 0.4$ ,  $m_a = 0.6$ ,  $m_a = 0.8$ , and  $m_a = 1$ , the proposed CB-MLI provides three-, five-, seven-, nine-, eleven-level output voltage waveforms, respectively. The individual switch stress for proposed CB-MLI topology is illustrated in Figure 9. As shown in Figure 7b, the recommended CB-MLI circuit converts a 100 V dc input supply voltage into a eleven-level output voltage of 176.78 Vrms and gives a 8.33A peak current. The proposed circuit's estimated output power is 922.82 W at RL-Load (30  $\Omega$ -50 mH), while the total loss of suggested CB-MLI is estimated to be 20.56 W. Using the FF-PWM control switching method for recommended CB-MLI circuit, the efficiency is calculated as 97.82%.



**Figure 7.** Simulation Results of load voltage, current, and the capacitor voltage waveforms with dynamic change: (a) R-Load (30  $\Omega$ ), (b) RL-Load (30  $\Omega$ -50 mH), (c) R-Load (30  $\Omega$ ) to RL-Load (30  $\Omega$ -50 mH), (d) NO-Load to RL-Load (30  $\Omega$ -50 mH).



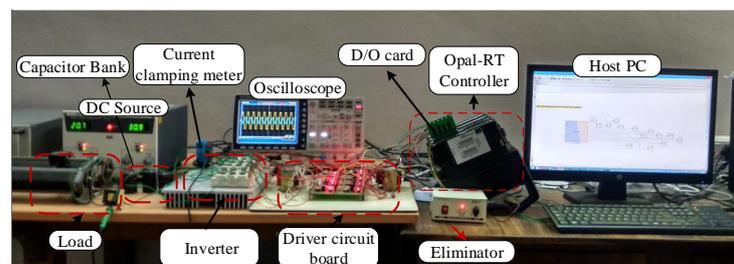
**Figure 8.** Simulation outputs: Load voltage, current, and the voltage across all capacitor ( $C_1$ ,  $C_2$ , and  $C_3$ ) waveforms at different modulation indices.



**Figure 9.** Voltage stress for individual switches of proposed boost-MLI topology.

## 5. Laboratory Results

After extensive investigation and testing, the suggested capacitor-based CB-MLI topology was verified to be practical. An insulated-gate bipolar transistor (IGBT) with an anti-parallel diode is employed for each of the switching devices  $S_1$  to  $S_9$ . Each module is rated at 1200 V/75 A and has two IGBTs/diodes. In a hardware implementation, HGTG11N120CND IGBT modules, pulse drivers (TLP250), and capacitors (electrolytic) were used to provide gating signals for the power switches, and for controlling the gating pulses, a real-time simulator (OPAL-RT4200) was used as a controller. A schematic diagram for the computer interface and additional controlling devices are also shown in Figure 10. A reference modulating signal (sine) and four triangular carrier signals with the same features described in the earlier section are utilized for CB-MLI modulation. The constant carrier pulses are sent as a digital pulse from the computer to the controller OPAL-RT unit, which transmits the digital signals as output to the gate driving circuit through the optocoupler.

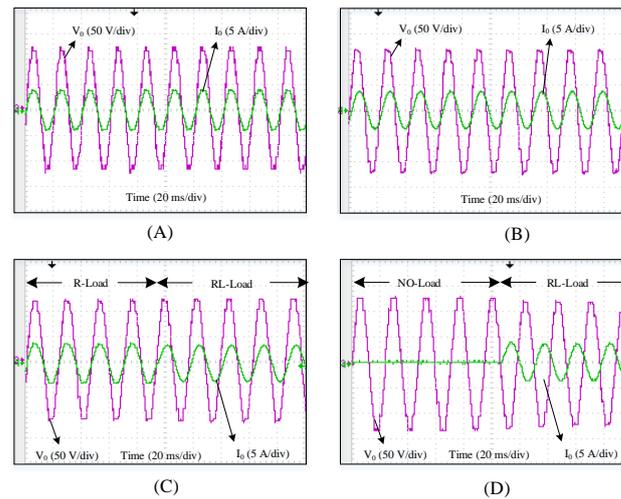
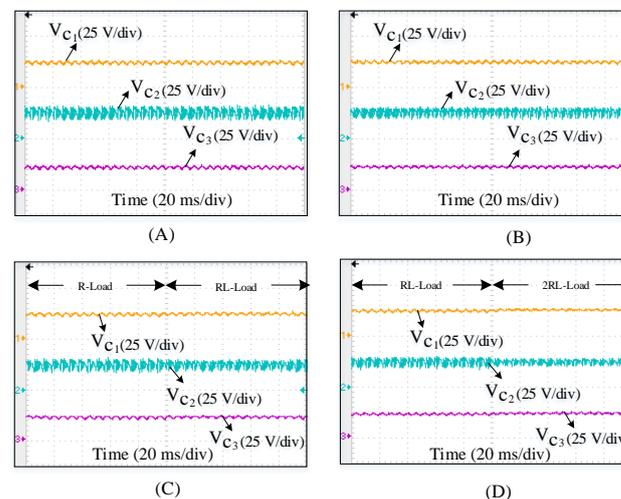


**Figure 10.** Hardware prototype.

The hardware prototype components and requirements are listed in Table 2. The suggested CB-MLI's load voltage and current are shown in Figure 11A,B. The self-balanced voltage across each capacitor waveform is depicted in Figure 12A,B with different load changes, i.e., R-load ( $30 \Omega$ ) and RL-load ( $30 \Omega$ -50 mH). Furthermore, the dynamic load variations, which are no-load to full load corresponding voltage and current, are illustrated in Figure 11D. For the load variation of R-load ( $30 \Omega$ ) to RL-load ( $30 \Omega$ -50 mH), the corresponding load voltage and current waveforms are shown in Figure 11C, the capacitor voltages are shown in Figure 12C. The suggested CB-MLI has three capacitors, and the corresponding capacitor voltage waveforms with a dynamic change of R-load ( $30 \Omega$ -50 mH) to 2RL-load ( $60 \Omega$ -50 mH) are shown in Figure 12D.

**Table 2.** Prototype implementing parameters.

Elements	Units	Specifications
Input DC-source	V	50
output frequency	Hz	50
Capacitors ( $C_1 = C_2 = C_3$ )	mF	2.2
Load resistance	$\Omega$	30
Load inductance	mH	50

**Figure 11.** Hardware Results of output Voltage and Current with dynamic changes: (A) R-Load (30  $\Omega$ ), (B) RL-Load (30  $\Omega$ -50 mH), (C) R-Load (30  $\Omega$ ) to RL-Load (30  $\Omega$ -50 mH), and (D) No-Load to RL-Load (30  $\Omega$ -50 mH).**Figure 12.** Hardware results for capacitor voltages ( $V_{C1}$ ,  $V_{C2}$ , and  $V_{C3}$ ) with dynamic changes: (A) R-Load (30  $\Omega$ ), (B) RL-Load (30  $\Omega$ -50 mH), (C) R-Load (30  $\Omega$ ) to RL-Load (30  $\Omega$ -50 mH), and (D) RL-Load to 2RL-Load (60  $\Omega$ -50 mH).

Additionally, the proposed capacitor-based CB-MLI FFT spectrum analysis of the derived output voltage and current are illustrated in Figure 13a,b. Consequently, the CB-MLI circuit can identify when  $ma = 1$ , the harmonic components of odd-order suppressing a comprehensive change in a THDs of 9.12% and 1.52% for eleven levels. The capacitor-based CB-MLI circuit provides medium-range power applications due to various attributes, including decreased voltage stress on switches, reduced component count, and electromagnetic interference (EMI).

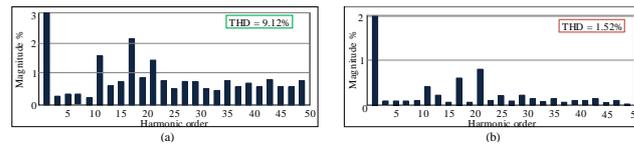


Figure 13. Hardware Results of proposed boost-MLI for THD: (a) Output Voltage and (b) Output Current.

## 6. Comparative Analysis

Any practical voltage balancing approach must be evaluated by looking at the methodology processing time, which can be expressed in CPU clock pulses. To organize another method, the simplest approach to assess a method's speed is to consider the number of CPU pulses required by a processor, such as a DSP, dSPACE, OPAL-RT, or the FPGA, which is used in the prototype implementation. Lower CPU clock periods make the algorithms run more quickly. Here, the proposed capacitor-based CB-MLI circuit is implemented using the OPAL-RT controller, which is the more accurate and advanced controller to give gating pulses to drive the circuit.

Additionally, quantitative and cost assessments of recently existing isolated DC-voltage source MLIs are presented. There are several issues with MLIs, such as having both passive and active component quantities and the rating of the devices. For a collated study, the blocking voltage, required capacitors, and switching devices for capacitor-based MLIs are all assessed in Table 3. Table 3 shows that the recommended CB-MLI circuit has the smallest part count. Existing structures required more semiconductor switching devices, diodes, and capacitors than the proposed design, and in the suggested configuration, no diodes are necessary. Since capacitors in the circuit are the most sensitive part of an inverter, their quantity should be reduced to a minimum. The number of capacitors is thus among the most widely used MLI measures of competent quality. In the suggested structure, merely three capacitors are required (throughout all inverter circuits, this circuit is the least expensive). Therefore, the recommended design is more compact and cheaper. Additionally, it must evaluate the H-bridge stress and blocking voltage of an inverter circuit since they represent the price of an inverter and the requirement for a heat sink. The proposed design shows that it has a lower TSV value when compared to existing architectures, and there is no H-bridge stress. Hence, the recommended capacitor-based CB-MLI structure has less components and reduced blocking voltage, and is cheaper than the MLIs mentioned in Table 3, making it best suited for a wider range of applications.

Table 3. Collation of recommended CB-MLI topology with currently evolved structures.

Topology	[21] (2018)	[22] (2021)	[23] (2020)	[24] (2021)	[25] (2021)	[26] (2018)	[27] (2018)	[28] (2022)	[29] (2018)	Proposed
$N_L$	11	11	11	9	7	11	11	9	9	11
$N_{sw}$	14	21	20	10	12	20	24	10	12	11
$N_{Cap}$	4	6	4	2	4	5	4	2	4	3
$N_{diode}$	2	2	-	1	-	-	-	-	4	-
$N_{dc}$	1	1	1	1	1	1	1	1	2	1
$PIV \times V_{dc}$	2.5	2.5	4	2	1	4	1	1	16	1.5
TSV	26	21	20	14	10	33	24	7	26	12.5

$N_L, N_{sw}, N_{Cap}, N_{diode}, N_{dc}$ —No. of—levels, power switches, capacitors, power diodes, DC sources, respectively.

Finally, an economic benefit comparison is conducted to verify the recommended financial gains of the multilevel inverter. Table 4 displays the costs of the investigated configurations, and an illustration situation of 250 W (100 V, 5 A peak) is assessed. The expense of the device's standardized rating is considered. It is challenging to compare the capacitance of the capacitor in capacitor-based configurations because it is impacted by frequency, load, and ripple percentage. Consequently, the comparative study is founded on similar capacitance values but with different voltage amplitudes. According to Table 4, the recommended capacitor-based CB-MLI structure is indeed less expensive when collated with earlier configurations. In conclusion, the proposed design is economical and is executed impressively while collating with existing converter topologies.

**Table 4.** Cost estimation of the proposed CB-MLI circuit with recently developed capacitor-based topologies.

Component	Series	Rating	Unit Price (\$)	Topology								
				[25]	[26]	[27]	[28]	[29]	[22]	[23]	[24]	P
MOSFET	IRFP350PBF	400 V	2.98	-	-	4	-	-	-	-	-	-
	IRFP240PBF	200 V	2.31	-	9	-	4	4	-	-	-	-
	IRFP9140NPBF	100 V	1.89	-	8	15	6	8	2	2	4	2
	IRFZ20PBF	50 V	1.63	8	-	-	-	-	4	6	6	9
	IRF1404	25 V	1.16	4	-	-	-	-	5	8	-	-
Gate driver	IR2110SPBF	-	1.92	12	14	19	10	12	11	16	10	11
Capacitor	B41231A9128M	2.2 mF	1.51	4	4	3	2	4	4	3	2	3
Diode	SDT10A100P5	100 V	0.61	-	4	3	0	4	2	-	1	-
Total price (\$)				47.84	71.27	83.11	45.22	55.88	44.48	58	45.5	44.1

Courtesy: [www.element14.com](http://www.element14.com), [mouser.in](http://mouser.in), [digikey.com](http://digikey.com).

## 7. Conclusions

A novel capacitor-based boost MLI circuit with fewer semiconductor switching devices and gate signals is developed. The maximum blocking voltage value of the individual switch lies within the limits of  $1.5V_{dc}$ . Moreover, the boost capacitors are equally charged and discharged in the positive and negative half of the cycle, resulting in the smallest amount of capacitance needed. As the devised PWM technique contains only logic gates and does not need any sensing devices to control the boosting capacitors, the proposed CB-MLI configuration is significantly cost-effective. In addition, an explanation of the proposed CB-MLI topology, operating states, FF-PWM scheme, and the capacitor designs are provided. Both the hardware and simulator findings achieved here have validated the principle of operation and assessed the proposed structure's ability to withstand various load conditions. Furthermore, a comprehensive commensurate study indicates the suggested CB-MLI circuit benefits compared to quondam study results, proving its suitability for a wide range of applications, especially in electric vehicles.

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## References

- Cherif, R.; Hasanov, F.; Pande, A. Riding the energy transition: Oil beyond 2040. *Asian Econ. Policy Rev.* **2021**, *16*, 117–137. [[CrossRef](#)]
- Lai, J.S.; Peng, F.Z. Multilevel converters—a new breed of power converters. *IEEE Trans. Ind. Appl.* **1996**, *32*, 509–517.
- Schuch, L.; Rech, C.; Hey, H.; Grundlinggrundling, H.; Pinheiro, H.; Pinheiro, J. Analysis and Design of a New High-Efficiency Bidirectional Integrated ZVT PWM Converter for DC-Bus and Battery-Bank Interface. *IEEE Trans. Ind. Appl.* **2006**, *42*, 1321–1332. [[CrossRef](#)]
- Wang, C.; Li, D.; Wang, S.; Huang, B.; Tian, Y. Communication—A Self-Contained Temperature Sensing Approach for Ultrafast Microwelding. *J. Electrochem. Soc.* **2018**, *165*, B220. [[CrossRef](#)]
- Zhang, H.; Wang, S.; Wu, B.; Zhang, W.; Hang, C.; Tian, Y. Ultrafast Parallel Micro-Gap Resistance Welding of an AuNi9 Microwire and Au Microlayer. *Micromachines* **2021**, *12*, 51. [[CrossRef](#)] [[PubMed](#)]

6. Park, S.H.; Park, K.B.; Kim, H.S.; Moon, G.W.; Youn, M.J. Single-magnetic cell-to-cell charge equalization converter with reduced number of transformer windings. *IEEE Trans. Power Electron.* **2011**, *27*, 2900–2911. [[CrossRef](#)]
7. Rahman, K.; Patel, N.; Ward, T.; Nagashima, J.; Caricchi, F.; Crescimbin, F. Application of Direct-Drive Wheel Motor for Fuel Cell Electric and Hybrid Electric Vehicle Propulsion System. *IEEE Trans. Ind. Appl.* **2006**, *42*, 1185–1192. [[CrossRef](#)]
8. Rivetta, C.; Emadi, A.; Williamson, G.; Jayabalan, R.; Fahimi, B. Analysis and control of a buck DC-DC converter operating with constant power load in sea and undersea vehicles. *IEEE Trans. Ind. Appl.* **2006**, *42*, 559–572. [[CrossRef](#)]
9. Aditya, K.; Suresh, Y.; Naik, B.S.; Rao, B.N. A Fault Tolerant Nine-level Inverter Topology With Full DC Utilization for Electric Vehicle Application. In Proceedings of the 2022 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE), Trivandrum, India, 2–5 January 2022; pp. 1–6.
10. Shiva Naik, B.; Suresh, Y.; Venkataramanaiah, J. Experimental verification of a hybrid multilevel inverter with voltage-boosting ability. *Int. J. Circuit Theory Appl.* **2020**, *48*, 420–434. [[CrossRef](#)]
11. Nageswar Rao, B.; Suresh, Y.; Shiva Naik, B.; Venkataramanaiah, J.; Aditya, K.; Kumar Panda, A. A novel single source multilevel inverter with hybrid switching technique. *Int. J. Circuit Theory Appl.* **2022**, *50*, 794–811. [[CrossRef](#)]
12. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Pérez, M.A.; Leon, J.I. Recent advances and industrial applications of multilevel converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2553–2580. [[CrossRef](#)]
13. Abdullah, R.; Rahim, N.A.; Raihan, S.R.S.; Ahmad, A.Z. Five-level diode-clamped inverter with three-level boost converter. *IEEE Trans. Ind. Electron.* **2014**, *61*, 5155–5163. [[CrossRef](#)]
14. Dargahi, V.; Sadigh, A.K.; Abarzadeh, M.; Eskandari, S.; Corzine, K.A. A new family of modular multilevel converter based on modified flying-capacitor multicell converters. *IEEE Trans. Power Electron.* **2014**, *30*, 138–147. [[CrossRef](#)]
15. Chattopadhyay, S.K.; Chakraborty, C. A New Multilevel Inverter Topology With Self-Balancing Level Doubling Network. *IEEE Trans. Ind. Electron.* **2014**, *61*, 4622–4631. [[CrossRef](#)]
16. Ghosh, G.; Rathi, A.; Chowdhury, A.R.; Dutta, P.; Preeti, S.; Shri, D.; Krishna, S.; Das, A.; Saha, P.; Singh, N. Comparison of different techniques for selective harmonic elimination in PWM inverters—A review. In Proceedings of the 2017 8th IEEE Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON), Vancouver, BC, Canada, 3–5 October 2017; pp. 509–515. [[CrossRef](#)]
17. Naik, B.S.; Suresh, Y.; Aditya, K.; Rao, B.N. A novel nine-level boost inverter with a low component count for electric vehicle applications. *Int. Trans. Electr. Energy Syst.* **2021**, *31*, e13172. [[CrossRef](#)]
18. Naik, B.S.; Suresh, Y.; Venkataramanaiah, J.; Panda, A.K. A hybrid nine-level inverter topology with boosting capability and reduced component count. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *68*, 316–320. [[CrossRef](#)]
19. Hinago, Y.; Koizumi, H. A switched-capacitor inverter using series/parallel conversion with inductive load. *IEEE Trans. Ind. Electron.* **2012**, *59*, 878–887. [[CrossRef](#)]
20. Hurley, W.G.; Wölfle, W.H. *Transformers and Inductors for Power Electronics: Theory, Design and Applications*; John Wiley & Sons: Hoboken, NJ, USA, 2013.
21. Liu, J.; Wu, J.; Zeng, J. Symmetric/Asymmetric Hybrid Multilevel Inverters Integrating Switched-Capacitor Techniques. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 1616–1626. [[CrossRef](#)]
22. Daula Siddique, M.; Reddy, B.; Iqbal, A.; Mekhilef, S. A new family of boost active neutral point clamped inverter topology with reduced switch count. *IET Power Electron.* **2021**, *14*, 1433–1443. [[CrossRef](#)]
23. Daula Siddique, M.; Reddy, B.; Iqbal, A.; Mekhilef, S. Reduced Switch Count Based N-Level Boost Inverter Topology for Higher Voltage Gain. *IET Power Electron.* **2020**, *13*, 3505–3509. [[CrossRef](#)]
24. Iqbal, A.; Siddique, M.D.; Reddy, B.P.; Maroti, P.K. Quadruple Boost Multilevel Inverter (QB-MLI) Topology With Reduced Switch Count. *IEEE Trans. Power Electron.* **2021**, *36*, 7372–7377. [[CrossRef](#)]
25. Khoshkbar-Sadigh, A.; Dargahi, V.; Khorasani, R.R.; Corzine, K.A.; Babaei, E. Simple Active Capacitor Voltage Balancing Method Without Cost Function Optimization for Seven-Level Full-Bridge Flying-Capacitor-Multicell Inverters. *IEEE Trans. Ind. Appl.* **2021**, *57*, 1629–1643. [[CrossRef](#)]
26. Khenar, M.; Taghvaie, A.; Adabi, J.; Rezanejad, M. Multi-level inverter with combined T-type and cross-connected modules. *IET Power Electron.* **2018**, *11*, 1407–1415. [[CrossRef](#)]
27. Taghvaie, A.; Adabi, J.; Rezanejad, M. A self-balanced step-up multilevel inverter based on switched-capacitor structure. *IEEE Trans. Power Electron.* **2018**, *33*, 199–209. [[CrossRef](#)]
28. Aditya, K.; Suresh, Y.; Shiva Naik, B.; Nageswar Rao, B.; Panda, A.K. A capacitor based single source MLI with natural balancing and less component for EV/HEV application. *Int. J. Circuit Theory Appl.* **2022**, *50*, 3551–3566. [[CrossRef](#)]
29. Saeedian, M.; Hosseini, S.M.; Adabi, J. Step-up switched-capacitor module for cascaded MLI topologies. *IET Power Electron.* **2018**, *11*, 1286–1296. [[CrossRef](#)]

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