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Experimentation of Multi-Input Single-Output Z-Source Isolated DC–DC Converter-Fed Grid-Connected Inverter with Sliding Mode Controller

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Abstract: Converting devices are quickly becoming the most important part of renewable energy-producing systems that are linked to the grid. Applications that are linked to the grid are the most common place to find usage for two-port power converters that are built using single-input and single-output (SISO) ports. The incorporation of SISO power converters into the grid-connected hybrid system results in an increase in both its size and its cost. Multiple power sources may be connected to a single DC bus by means of hybrid power systems, which make use of multi-input power converters. To combine the hybrid wind and PV system with a common DC bus, this study suggests an isolated multi-input single-output (IMISO) Z-Source converter. It has been determined that the suggested system performs well in spite of dynamic load fluctuations and shifting input voltage circumstances. The sliding mode controller (SMC) has also been used to control a single-phase five-level (SPFL) inverter. The purpose of developing the laboratory prototype model was to verify the proposed IMISO Z-source converter-fed single-phase five-level (SPFL) inverter in the context of the circumstance that is being investigated.

Keywords: IMISO Z-source converter; sliding mode controller (SMC); SPFL inverter; multi-input power converter; hybrid power generation system; grid-connected hybrid system

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1. Introduction

The ever-increasing need for electricity may be traced back to a variety of sources, including population growth, industrial output, the construction of more commercial buildings, and the development of the IT sector. According to the current scenario, 70% of the world's energy demand is met using power plants that are fueled by fossil fuels [1]. Fossil fuel combustion hastens global warming and the greenhouse effect [2]. A renewable power generation system (RPGS) is the best alternative strategy for mitigating the effects of global warming and greenhouse emissions. In the realm of renewable energy, photovoltaic (PV) and wind sources play a significant role because they are the most accessible, adaptable, and efficient energy sources, and have the potential to solve a significant number of global energy and environmental problems [3,4]. As of July 2023, renewable energy sources, including large hydropower, had a combined installed capacity of 179.322 GW. This installed capacity for renewables is as follows: wind power: 42.8 GW; solar power: 67.07 GW; biomass/co-generation: 10.2 GW; small hydro power: 4.94 GW; waste to energy: 0.55 GW; and large hydro: 46.85 GW [5]. When used on a large scale, the hybrid wind-photovoltaic power-generating system has a number of technological challenges that must be overcome. One of these problems is connecting many renewable power sources to a single DC bus. In the typical hybrid layout, many power converters are used to link various power supplies to a DC bus. This causes a loss of efficiency in the conversion process, a massive rise in

volume, and higher overall expenses [5]. Over the course of the past several decades, numerous academics and engineers have worked to advance the state-of-the-art power electronic converters. There is a continuing need for novel approaches and architectures [6] because of the possibility that doing so will improve the robustness and performance of the conversion system while decreasing its price, size, and weight. To boost a low and fluctuating input voltage, a Z-source converter is often used, since this is the most tried and tested method. In 2002, Peng created the first Z-source converter (ZSC), which aimed to overcome some of the restrictions of conventional power electronics converters. In order to implement this concept as a DC–DC converter, the newly introduced Z-source impedance network must be short-circuited at each switching point according to a predetermined duty ratio. The converter would not work without this, so it must be present. The fundamentals of operation are otherwise unaffected; all that has changed is the use of a different converter bridge in the back to facilitate DC–DC transformations. Only this one thing has changed significantly.

The series Z-source network [7] was designed to increase the output voltage of power electronic inverters by extending the well-known concept of the Z-source DC connection. To achieve this, the notion of the Z-source DC connection was developed further. The buck and boost functionalities are provided by a new transformer-isolated DC–DC converter with a distributed impedance-source network [8]. This device is used to switch from DC–DC power sources. The distributed impedance source network DC–DC converter is a one-of-a-kind because it may be open and short-circuited without harming the switching devices, unlike conventional V-source or I-source converters. These capabilities are exclusive to this kind of converter. For grid-connected solar power systems, switching Z-source or quasi-Z-source DC–DC converters are recommended [9]. In contrast to conventional matrix converters, Z-source matrix converters (ZSMCs) may perform buck and boost operations with a reduced switch count [10], freeing them from the voltage gain limitation. A Z-source converter with a linked transformer and high boost gain has been developed for this purpose. Any increase in the transformer's turn ratio also results in a better gain factor. A topology formed by a moderate transformer turn ratio is more realistically relevant for specific voltage improvements [11]. The converter is simple to design, and less money is spent on its manufacturing as a consequence. High step-up DC–DC converters are required in photovoltaic applications to boost the low-source voltages to a specified grid voltage. The goal of this project was to create a hybrid Z-source boost DC–DC converter that could be used in solar systems.

Hybrid topologies that combine several types of current Z-source networks may increase the boost capabilities of the traditional Z-source networks [12]. The Z-source network is combined with other networks in the converter's hybrid design. This is necessary due to the fact that standard Z-source network boost capabilities are inadequate for the task at hand. An isolated bidirectional DC–DC converter, or qZIBDC, based on a quasi-Z source has been developed for use in systems that make use of renewable energy. This converter is bidirectional, meaning it may change a direct current to another kind of direct current. The dual active bridge circuit used in the converter allows it to function as both a buck and a boost converter, depending on the perspective [13]. The converter is able to do this because of the usage of a pair of active bridges. A new generation of Z-source DC–DC converters has been developed to provide higher voltage pumping and a high power density [14]. Three distinct topologies for Z-source DC–DC boost converters using switched capacitors have been developed to maximize the boost factor [15]. The suggested converter design has a number of advantages over other topologies, including those listed below:

1. The notion of a Z-Source converter is presented with the suggested multi-port converter in order to give a larger boost factor than the standard Z-source boost converter. This is done in order to meet the requirements set out by the IEEE. It is beneficial to provide a stronger boost factor while maintaining an extremely low duty ratio.
2. The architecture that was suggested may be expanded to incorporate an N-number of additional input sources using a centralized DC bus. It dispenses with the requirement

for a number-independent DC–DC converter to be utilized. It contributes to a rise in the conversion efficiency, which in turn serves to minimize the system's total cost.

3. Isolation between the input and output is achieved in the proposed converter by virtue of its design, which incorporates an isolation transformer.

A common configuration for a standard Z-source converter with two outputs is shown in Figure 1. A diode, a switch, and an impedance network make up this kind of converter [16].

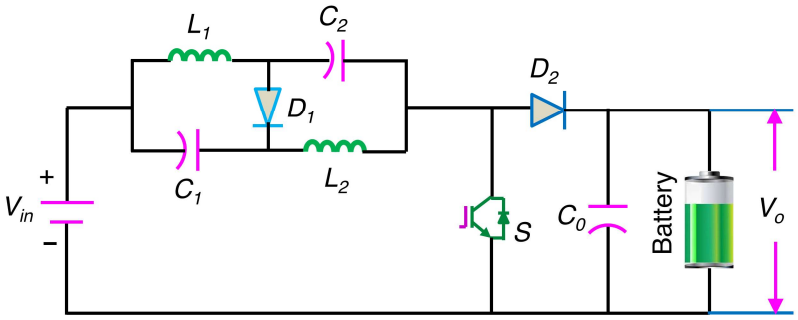


Figure 1. Impedance source converter using a conventional two-port configuration.

Figure 2 is an illustration of the usual interleaved-boost full-bridge three-port converter-supplied gird-connected single-phase inverter [17]. In order to implement the proposed isolated multi-input single-output (IMISO) isolated Z-source DC–DC converter depicted in Figure 3, this component is put to use.

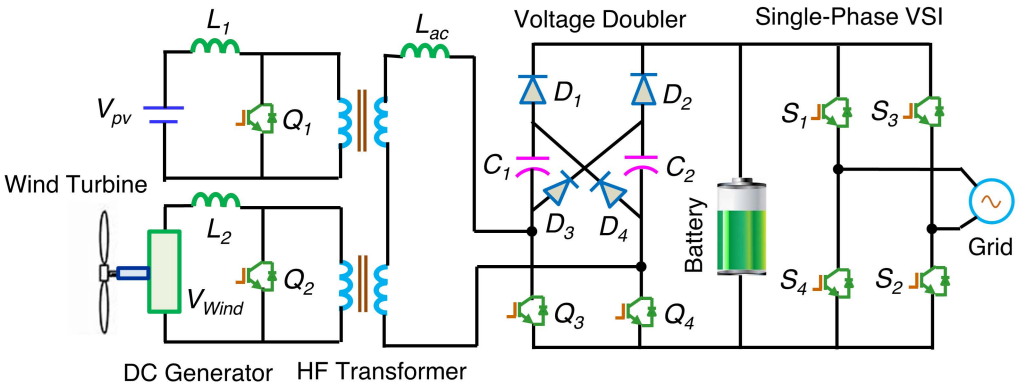


Figure 2. Conventional interleaved-boost full-bridge three-port converter.

Conventional topologies, such as those shown in Figures 1 and 2, have limited voltage gain and need a large step-up high-frequency transformer; this was discovered during research into the Z-Source and interleaved DC–DC converter topologies. This research aims to develop a novel and efficient isolated multi-input single-output (IMISO) Z-source DC–DC converter for combining several energy sources into a single DC bus. This paper dissects and analyzes in depth the architecture, modes of operation, and implementation of a single-phase five-level (SPFL) inverter based on the IMISO Z-source converter. The dynamic behavior of the proposed design is tested and verified by constructing a software and hardware model of the 1500 W, 230 V, 50 Hz system. Both the modeling and experimental findings demonstrated that the IMISO Z-source converter-based single-phase five-level (SPFL) inverter controlled using the sliding mode controller (SMC) provided better performance.

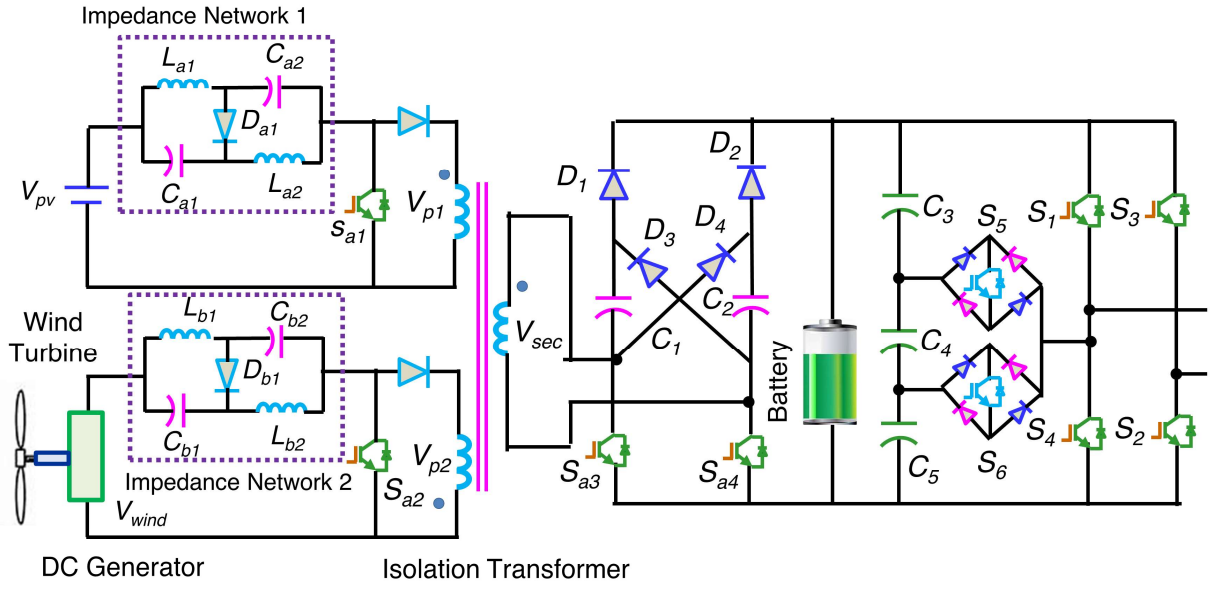


Figure 3. Proposed IMISO Z-source converter fed single-phase five-level (SPFL) inverter.

2. System Description and Modes of Operation

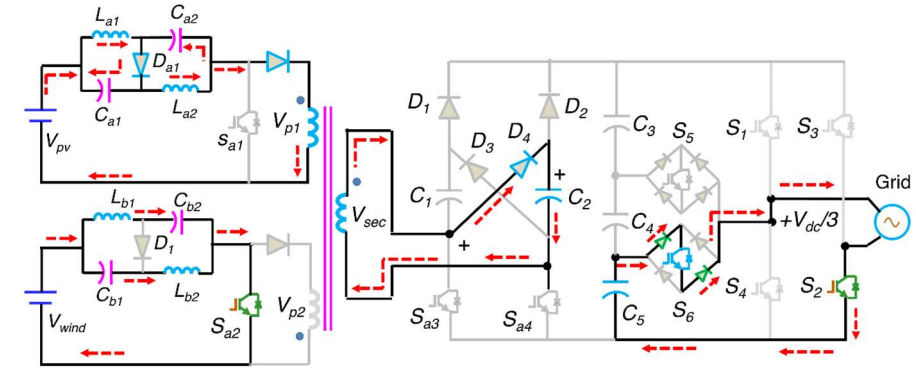
Figure 3 depicts the proposed grid-connected hybrid PV-wind system, which utilizes an isolated multi-input single-output (IMISO) Z-source converter-fed single-phase five-level (SPFL) inverter. It consists of a single-phase five-level (SPFL) inverter, a voltage doubler rectifier, a multi-input high-frequency transformer, and two impedance networks. Connecting the different renewable energy sources to the DC bus was made easier with the help of the high-frequency multi-input transformer. Using high-frequency transformers with two windings increases the physical footprint and financial commitment of the system. The DC–DC converter's price and size were reduced by using a high-frequency transformer with many inputs. The proposed converter has similarities with both Z-source converters and active interleaved flybacks in that it offers benefits to the user. The proposed converter has the ability to amplify the inputs separately to provide the necessary boost factor.

2.1. Positive Half-Cycle Operation of the Proposed IMISO Z-Source Converter

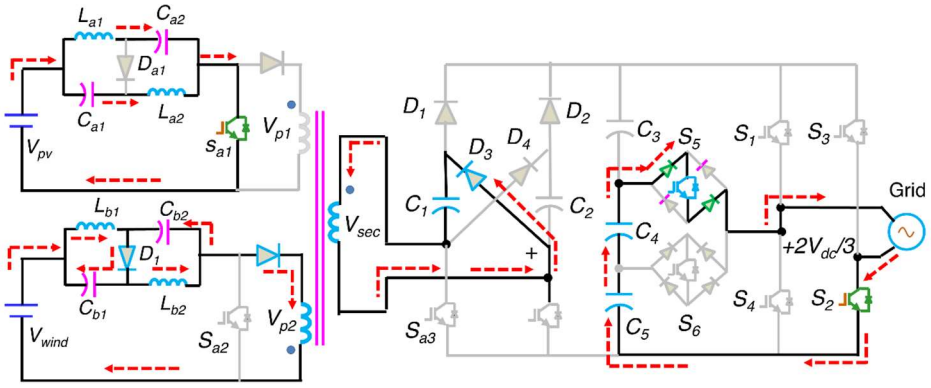
In Figure 4a, S_{a2}, S_2, and S_6 are turned on at t_0, and the inductors L_{a1} and L_{a2} in the impedance network, as well as the input source V_{pv}, charge the capacitors C_{a1} and C_{a2}. The input voltage V_{pv} is added to the voltages across inductors L_{a1} and L_{a2} in the impedance network to arrive at the voltage across the transformer primary, V_{p1}. The capacitor C_2 is charged using the secondary of the transformer through diode D_4, while the voltage across the transformer V_{p2} is clamped at zero during this period. The SPFL inverter's output voltage, V_{inv}, determines the drain slope of the capacitor C_5. To calculate the voltage across the capacitors in the impedance network, we used the following formula:

$$V_{Ca1} = V_{La1} = V_{Ca2} = V_{La2} \tag{1}$$

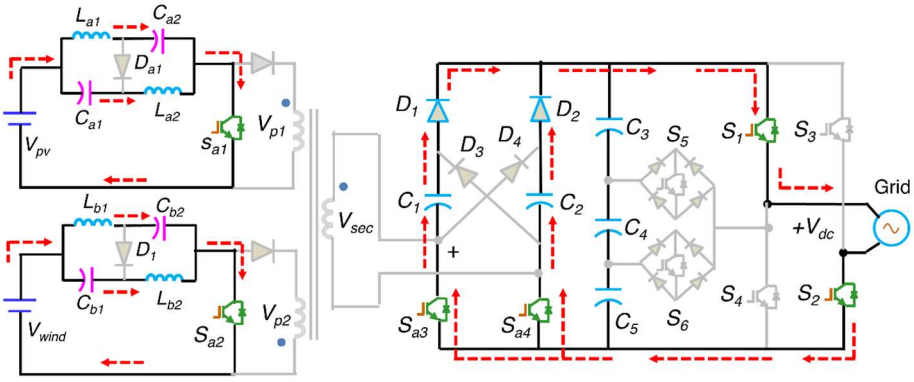
$$V_{Ca1} = V_{Ca2} = \frac{d_{sa1}}{1 - 2d_{sa1}} V_{pv} \tag{2}$$



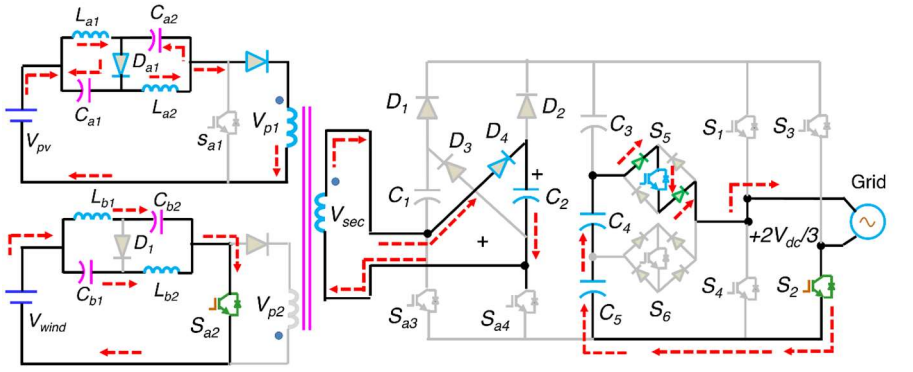
(**a**) First interval of a positive half cycle



(**b**) Second interval of a positive half cycle

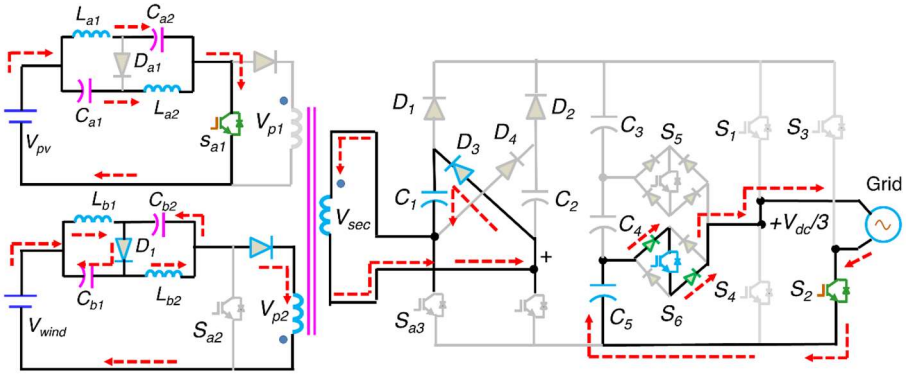


(**c**) Third interval of a positive half cycle



(**d**) Fourth interval of a positive half cycle

Figure 4. *Cont.*



(**e**) Fifth interval of a positive half cycle

Figure 4. Positive half-cycle modes of operation for the proposed IMISO Z-source converter-fed SPFL inverter.

The voltage across the impedance network inductors can be expressed as follows:

$$V_{Lb1}^{I} = V_{Cb2}^{I} + V_{wind}^{I} \tag{3}$$

$$V_{Lb2}^{I} = V_{Cb1}^{I} + V_{wind}^{I} \tag{4}$$

The voltage equations of the transformer and SPFL inverter are expressed as follows:

$$V_{p1} = V_{pv} + V_{La1} + V_{La2} \tag{5}$$

$$V_{\text{sec}} = V_{c2} = (V_{pv} + V_{La1} + V_{La2})n = nV_{p1} \tag{6}$$

$$V_{inv} = +\frac{V_{dc}}{3} \tag{7}$$

During the second subinterval, represented by [t_1–t_2] in Figure 4b, switches S_{a1}, S_2, and S_5 all conduct simultaneously. Therefore, at this moment, L_{b1} and L_{b2} are being discharged while L_{a1} and L_{a2} are being charged. Since this is a multiple of n and the total input voltage of primary 2, C_1 is charged with $n(V_{wind} + V_{Lb1} + V_{Lb2})$. The current through the secondary of the transformer flows negatively, as illustrated in Figure 4b. The slope used to discharge capacitors C_4 and C_5 is calculated from the voltage at the SPFL inverter's output. In its default configuration, the SPFL inverter circuit outputs $+2V_{dc}/2$ at its terminals. To calculate the voltage across the capacitors in the impedance network, we used the following formula:

$$V_{Cb1} = V_{Lb1} = V_{Cb2} = V_{Lb2} \tag{8}$$

$$V_{Cb1} = V_{Cb2} = \frac{d_{sa2}}{1 - 2d_{sa2}} V_{wind} \tag{9}$$

The voltage across the impedance network inductors can be expressed as follows:

$$V_{La1}^{II} = V_{Ca2}^{II} + V_{PV}^{II} \tag{10}$$

$$V_{La2}^{II} = V_{Ca1}^{II} + V_{PV}^{II} \tag{11}$$

The voltage equations of the transformer and SPFL inverter are expressed as

$$V_{p2} = V_{pv} + V_{Lb1} + V_{Lb2} \tag{12}$$

$$V_{\text{sec}} = V_{c1} = (V_{wind} + V_{Lb1} + V_{Lb2})n = nV_{p2} \tag{13}$$

$$V_{inv} = +\frac{2V_{dc}}{3} \tag{14}$$

As can be seen in Figure 4c, the impedance network inductors L_{a1}, L_{a2}, L_{b1}, and L_{b2} will remain charged during the whole subinterval [t_2–t_3], right up until S_{a1} and S_{a2} are disabled. At the same time, the electrostatic charge in capacitors C_1 and C_2 is completely discharged. Capacitors C_3, C_4, and C_5 are charged by capacitors C_1 and C_2, and then provide electricity to the AC load/grid. The terminals of the SPFL inverter are set up for a $+V_{dc}$ reading, as determined using the inverter's circuit. The following formulas represent the voltage measured across the inductors of an impedance network.

$$V_{La1}^{III} = V_{Ca2}^{III} + V_{PV}^{III} \tag{15}$$

$$V_{La2}^{III} = V_{Ca1}^{III} + V_{PV}^{III} \tag{16}$$

$$V_{Lb1}^{III} = V_{Cb2}^{III} + V_{wind}^{III} \tag{17}$$

$$V_{Lb2}^{III} = V_{Cb1}^{III} + V_{wind}^{III} \tag{18}$$

$$V_{inv} = +V_{dc} \tag{19}$$

Figures 4 and 5 depict an equivalent circuit and the important operating waveforms of the positive half cycle, respectively. Subintervals 4 and 5 of the IMISO Z-source converter operate similarly to intervals 1 and 2, except the SPFL inverter. The SPFL inverter switches S_5 and S_2 are activated to produce $+2V_{dc}/3$ throughout the time period [t_3–t_4]. Between times t_4 and t_5, the SPFL inverter's S_6 and S_2 switches are activated, producing a $+V_{dc}/3$ output. In Figure 5, the gate pulses, transformer waveforms, and SPFL inverter output for the first five-time intervals are shown. Table 1 displays the switching table for the SPFL inverter output during the positive half cycle.

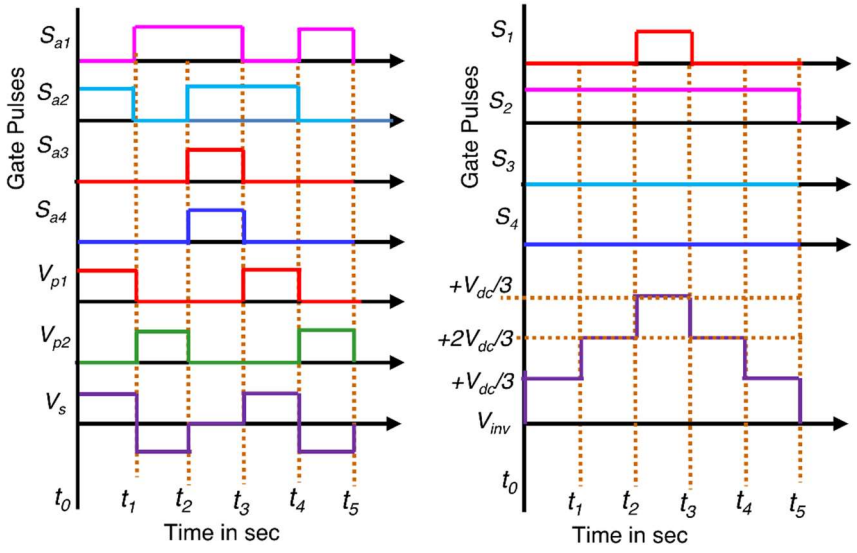


Figure 5. IMISO Z-source converter and SPFL inverter switching patterns and output.

Table 1. Switching pattern for positive half cycle of operation.

Interval	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_1	S_2	S_3	S_4	S_5	S_6	V_{inv}
t_0–t_1	0	1	0	0	0	1	0	0	0	1	$+V_{dc}/3$
t_1–t_2	1	0	0	0	0	1	0	0	1	0	$+2V_{dc}/3$
t_2–t_3	1	1	1	1	1	1	0	0	0	0	$+V_{dc}$
t_3–t_4	1	0	0	0	0	1	0	0	1	0	$+2V_{dc}/3$
t_4–t_5	0	1	0	0	0	1	0	0	0	1	$+V_{dc}/3$

2.2. Negative Half-Cycle Operation of IMISO Z-Source Converter

The input source V_{pv} and the impedance network's inductors L_{a1} and L_{a2} charge the capacitors C_{a1} and C_{a2} when the switches S_{a2}, S_3, and S_5 are activated at time t_0 as presented in Figure 6a. The voltages measured across the impedance network inductors L_{a1} and L_{a2} are added to obtain the voltage across the primary of the transformer. The V_{p2} or voltage across the transformer is kept constant at 0 V throughout this period. Capacitor C_2 is charged to a magnitude of nV_{sec} through the secondary winding of the transformer via diode D_4. The SPFL inverter's output voltage V_{inv} determines the value of the drain of the capacitor C_3. The voltage across the IMISO Z-source converter's components may be expressed using a similar subinterval 1 to that which is described in Section 2.1. The output of the SPFL inverter may be modeled as

$$V_{inv} = -\frac{V_{dc}}{3} \tag{20}$$

The second subinterval is shown in Figure 6b, and it includes the conducting states of switches S_{a1}, S_3, and S_6 across the time interval [t_1–t_2]. Thus, L_{b1} and L_{b2} are being discharged at the moment when L_{a1} and L_{a2} are being charged. To the power of $n(V_{wind} + V_{Lb1} + V_{Lb2})$, C_1 is negatively charged.

Negative current flows through the secondary of the transformer, as shown in Figure 6b. The discharge slope of capacitors C_2 and C_3 is calculated using the SPFL inverter's output voltage. The terminals of the SPFL inverter circuit are set up to provide the output voltage in Equation (21).

$$V_{inv} = -\frac{2V_{dc}}{3} \tag{21}$$

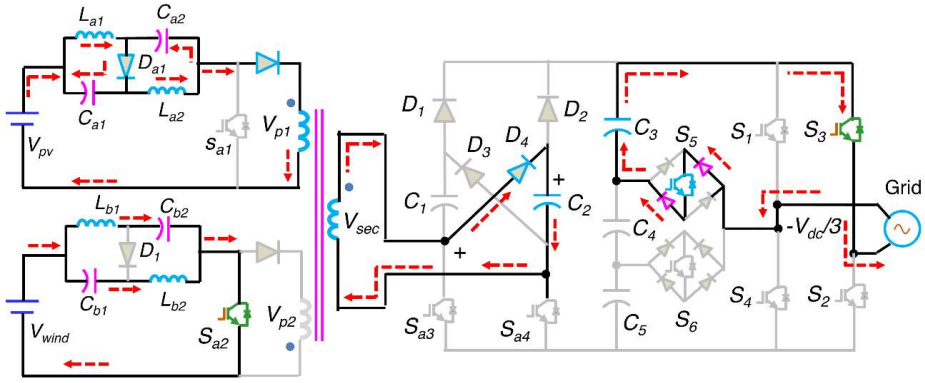
As can be seen in Figure 6c, until S_{a1} and S_{a2} are turned off at t_3, the impedance network inductors L_{a1}, L_{a2}, L_{b1}, and L_{b2} will continue to be charged during the whole subinterval [t_2–t_3]. At the same moment, the electrostatic charges in capacitors C_1 and C_2 are discharged to zero. Capacitors C_3, C_4, and C_5 are charged by capacitors C_1 and C_2, and they then feed power into the AC load and grid. The SPFL inverter circuit is wired in a manner that allows $-V_{dc}$ to be read from the terminals when the device is functioning. The following expressions may be used to represent the inverter voltage.

$$V_{inv} = -V_{dc} \tag{22}$$

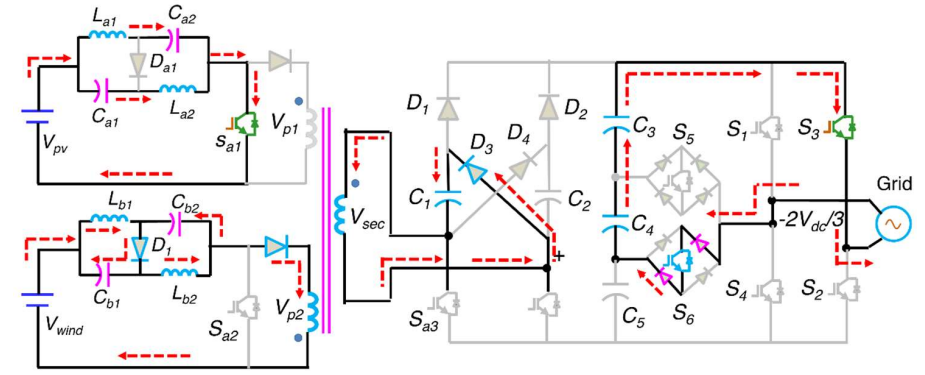
In Figures 6 and 7, the circuits and the essential waveforms of operation that are associated with the negative half cycle are shown. Subintervals 4 and 5 are similar to subintervals 1 and 2, with the exception being the SPFL inverter. During the subinterval from t_3 to t_4, the SPFL inverter switches S_3 and S_6 are activated to allow the output to be set to $-2V_{dc}/3$. During the time period t_4–t_5, the SPFL inverter switches S_3 and S_5 are activated, leading to a $-V_{dc}/3$ output. The gate pulses, transformer waveforms, and SPFL output for the next five periods are shown in Figure 7. The SPFL inverter's negative half-cycle output is reflected in Table 2, which shows the corresponding switching configuration. The table below shows the multiple subintervals that make up the SPFL inverter's output voltage.

Table 2. Switching pattern corresponds to the negative half-cycle of output.

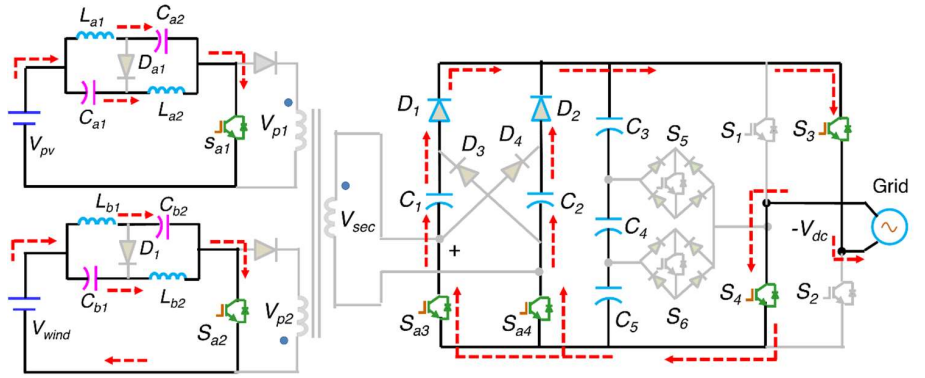
Interval	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_1	S_2	S_3	S_4	S_5	S_6	V_{inv}
t_0–t_1	0	1	0	0	0	0	1	0	1	0	$-V_{dc}/3$
t_1–t_2	1	0	0	0	0	0	1	0	0	1	$-2V_{dc}/3$
t_2–t_3	1	1	1	1	0	0	1	1	0	0	$-V_{dc}$
t_3–t_4	1	0	0	0	0	0	1	0	0	1	$-2V_{dc}/3$
t_4–t_5	0	1	0	0	0	0	1	0	1	0	$-V_{dc}/3$



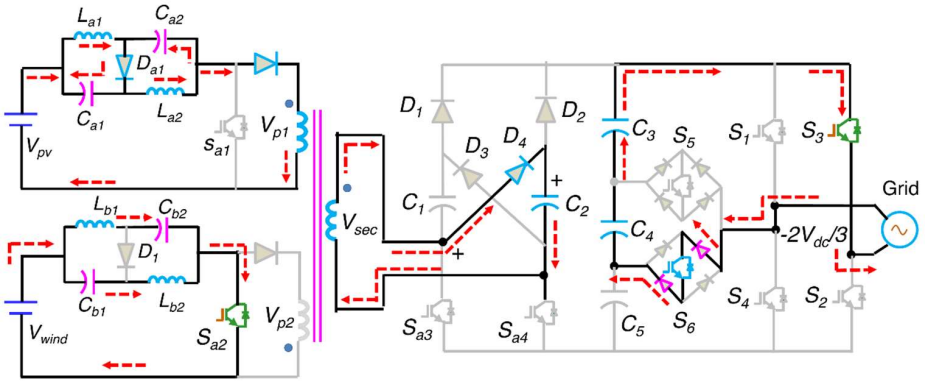
(**a**) First interval of a negative half cycle



(**b**) Second interval of a negative half cycle

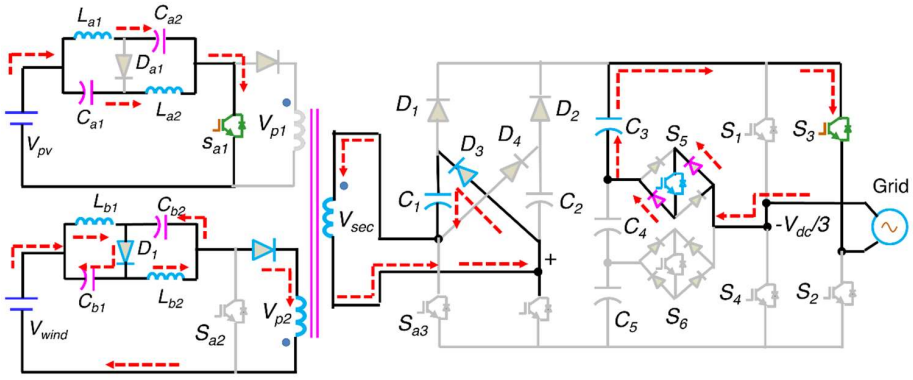


(**c**) Third interval of a negative half cycle



(**d**) Fourth interval of a negative half cycle

Figure 6. *Cont.*



(**e**) Fifth interval of a negative half cycle

Figure 6. Modes of operation of proposed IMISO Z-source converter-fed SPFL inverter under negative half cycle.

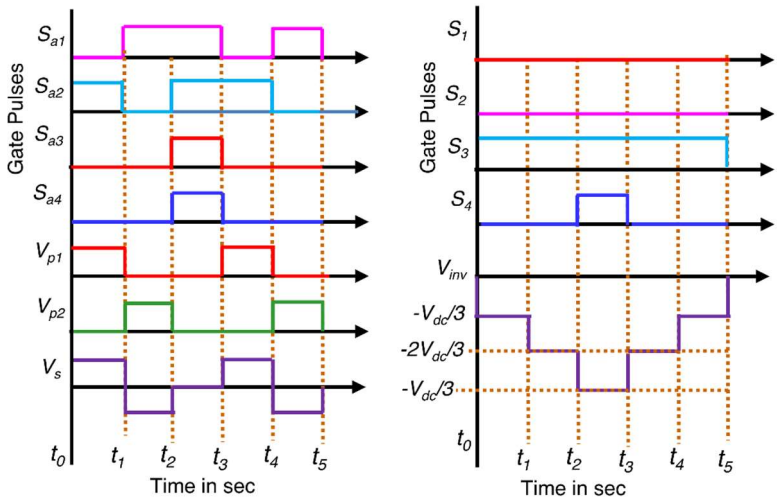


Figure 7. IMISO Z-source converter and SPFL inverter negative half-cycle switching patterns and output.

3. Voltage Gain and Duty Ratio Relation

The following simplifications were made during the steady-state examination of the proposed converter to aid in comprehension. All components, including the power switches S_{a1} and S_{a2}, diodes, load resistors, inductors, and capacitors, were in good working order; thus, the parasitic impact was disregarded. The quasi-Z-source network makes it such that $L_{a1} = L_{a2} = L_{b1} = L_{b2}$ and $C_{a1} = C_{a2} = C_{a3} = C_{a4}$ are all deemed to have the same value. In continuous conduction mode, the IMISO converter may operate in two distinct modes, shown by the analogous circuits in Figures 4 and 6. In the analogous circuits of the various modes, the diodes D_{a1}, D_{a2}, D_{a3}, and D_{a4} are all shown to be off while the switches S_{a1} and S_{a2} are both on. The steady-state equations $V_{La1} = V_{pv} + V_{Ca2}$, $V_{La2} = V_{pv} + V_{Ca1}$, and $V_p = V_{pv} + V_{La1} + V_{La2}$ may be derived from Kirchoff's voltage law. From Figure 4, it is clear that when S_{a1} and S_{a2} are turned off, D_{a1} and D_{b1} are activated, D_{a2} and D_{b2} become reverse blockers, L_{a1} charges C_{a2}, L_{a2} charges C_{a1}, and V_{pv} and L_{a1} are linked in series with L_{a2} to feed the charges to primary 1 of the transformer. Capacitors C_1 and C_2 receive electricity from the secondary. This leads us to the following set of equations:

$$V_{Ca1} = V_{Ca2} = \frac{V_{pv} D_{sa1}}{1 - D_{sa1}} \tag{23}$$

$$V_{Cb1} = V_{Cb2} = \frac{V_{wind} D_{sa2}}{1 - D_{sa2}} \tag{24}$$

The input voltage of the primaries of the transformer may be calculated using Equations (25) and (26).

$$V_{p1} = V_{pv} + V_{La1} + V_{La2} = \frac{2 - D_{sa1}}{1 - D_{sa1}} V_{pv} \tag{25}$$

$$V_{p2} = V_{wind} + V_{Lb1} + V_{Lb2} = \frac{2 - D_{sa2}}{1 - D_{sa2}} V_{pv} \tag{26}$$

$$V_{\text{sec}} = (\frac{2 - D_{sa1}}{1 - D_{sa1}} V_{pv})2 = (\frac{2 - D_{sa2}}{1 - D_{sa2}} V_{wind})2 \tag{27}$$

The output voltage of the proposed IMISO Z–source converter can be expressed as presented in Equation (28), where D_{sax} is the duty ratio of S_{a1} or S_{a2}, V_{p1} is the primary 1 voltage, V_{p2} is the primary 2 voltage, V_{sec} is the secondary voltage, D_{sa1} is the duty ratio of S_{a1}, and D_{sa2} is the duty ratio of S_{a2}.

$$V_o = (\frac{4 - 2D_{sax}}{1 - D_{sax}} V_{in}) \tag{28}$$

The voltage gain (Vgain) of the proposed IMISO Z-source converter can be expressed as presented in Equation (29).

$$V_{gain} = \frac{V_o}{V_{in}} = (\frac{4 - 2D_{sax}}{1 - D_{sax}}) \tag{29}$$

4. Control Schemes of the Proposed Hybrid PV-Wind System

The provision of a controlled and regulated AC voltage to the utility grid is the primary objective of an SPFL inverter that is linked to the utility grid. In addition to this, it is in charge of ensuring that the grid and the SPFL inverter remain in synchronization with one another. For the purpose of carrying out the regulating action against the flow of power, two control loops were constructed. These loops were designed so that the DC bus voltage could be regulated, and the inverter could be synchronized with the grid. The first is an internal voltage control loop, and the second is a PI controller-based synchronous reference frame (SRF) theory with a hysteresis band pulse generator. Both of these are considered to be integral parts of the system.

4.1. Control Strategy of IMISO Z-Source Converter

The malfunction of linked loads is brought on by fluctuations in the DC-bus voltage of a grid-connected inverter. To solve this particular issue, a more conventional kind of controller known as the inner voltage control loop with PI controller is utilized in order to maintain a consistent DC-link voltage. Gains for the PI controller may be determined based on the step responsiveness of the transfer function. Figure 8 depicts the closed-loop control system with the PI controller used for the generation of gate pulses for the IMISO Z-source converter. When the voltage of the DC-link feedback circuit V_{dc} is compared to the voltage of the reference circuit V_{dc^*}, an error voltage V_e is produced. In order to correct the erroneous signal, that error voltage is sent into the PI controller. The PI controller is responsible for issuing a duty cycle order to the gate pulse generator, which in turn supplies pulses to the switches Q_{a1}, Q_{a2}, Q_{a3}, and Q_{a4}.

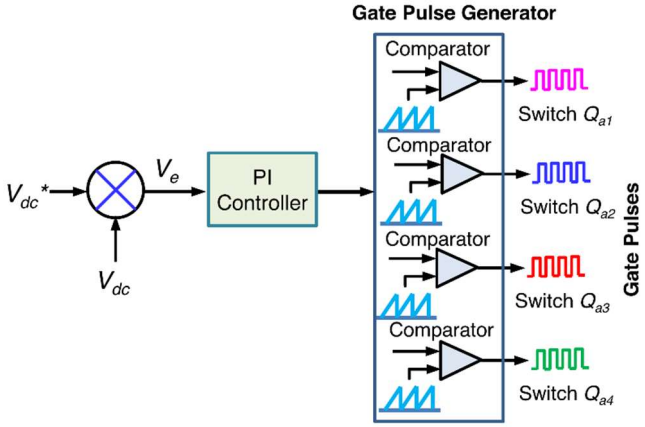


Figure 8. Voltage control of IMISO Z-source converter.

The proper functioning of the controller is essential to achieving the desired results in terms of both the performance and the output regulation of the converters. The overall control functions are as follows:

$$V_c(t) = k_p V_e(t) + k_i \int_0^t V_e(t)dt \tag{30}$$

4.2. Sliding Mode Controller (SMC) for SPFL Inverter

A sliding mode controller (SMC) is a nonlinear control method that alters the dynamics of a nonlinear system. The control rule based on state feedback breaks the continuity of time. Instead, it may transition between several continuous structures depending on its location in the state space. Therefore, the SMC is a means of controlling a changeable structure. In order to ensure that the final trajectory does not reside only inside one control structure, many control structures are built such that the trajectories always travel towards an adjacent area with a different control structure. Instead, it will creep around the periphery of the regulatory mechanisms. The SMC consists of a state-feedback discontinuous control rule that rapidly transitions between several continuous structures depending on the values of the state variables at any given moment. The goal is to ensure that the manipulated system's dynamics take the form that was described previously. The ON–OFF behavior of power switches makes the SMC especially intriguing because of its recognized resilience and system order reduction. A hysteresis band SMC is simple to implement since it does not need any extra calculations or ancillary circuitries. When using a hysteresis modulation-based SMC, there are essentially three ways to maintain a constant switching frequency. The design of this SMC first takes into account the sliding surface that will be used and then the control law which is used to drive the state of the system onto the chosen sliding surface. The hysteresis modulation approach is used to create the gate signals. The sliding mode controller (SMC) with hysteresis modulation is presented in Figure 9.

In this configuration, the inverter is controlled using bipolar modulation, and its output may take on one of two possible levels: −1 or +1. In each interval, two switches are activated, while the other four switches will remain in their off positions. If the switching frequency is denoted by f_{sw}, then the switching loss experienced during each on–off cycle will be proportional to f_{sw} and can be calculated using the formula $P_{inv} = kf_{sw}$. A variable structure control, denoted by the letter u, is defined as

$$u = \begin{cases} +1 \rightarrow V_c > +HB \\ -1 \rightarrow V_c < -HB \end{cases} \tag{31}$$

where V_d* represents the amount of deviation that exists between the actual value of the state variable and the reference that corresponds to it. An error voltage V_{d*} is generated as

a result of a comparison between the voltage of the DC-link Vdc and the reference voltage V_{dc*}. The SMC criteria are satisfied whenever S_k crosses the switching surface. The dq to a conversion block process the I_{d*} and I_{q*} and convert the inputs into I_a. The reference wave I_{a*}, obtained from the grid current I_g, is processed through a product block to generate the V_c. The equation used for the conversion of I_g into I_d and I_q is presented in Equation (32).

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} I_{real} \\ I_{image} \end{bmatrix} \tag{32}$$

Equations (33) and (34) may be used to represent the real and imaginary components of the grid current, respectively.

$$I_{real}(t) = I_m \sin\theta \tag{33}$$

$$I_{image}(t) = -I_m \cos\theta \tag{34}$$

Equation (35), shown below, provides a way to transform *dq* variables into *a* and *a**.

$$\begin{bmatrix} I_{real} \\ I_{image} \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \cos(\theta) \\ -\cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{35}$$

To create the time-locked gate pulses for the SPFL inverter, a hysteresis band pulse generator is utilized. The gate pulse generation through the hysteresis band pulse generator is illustrated in Figure 10.

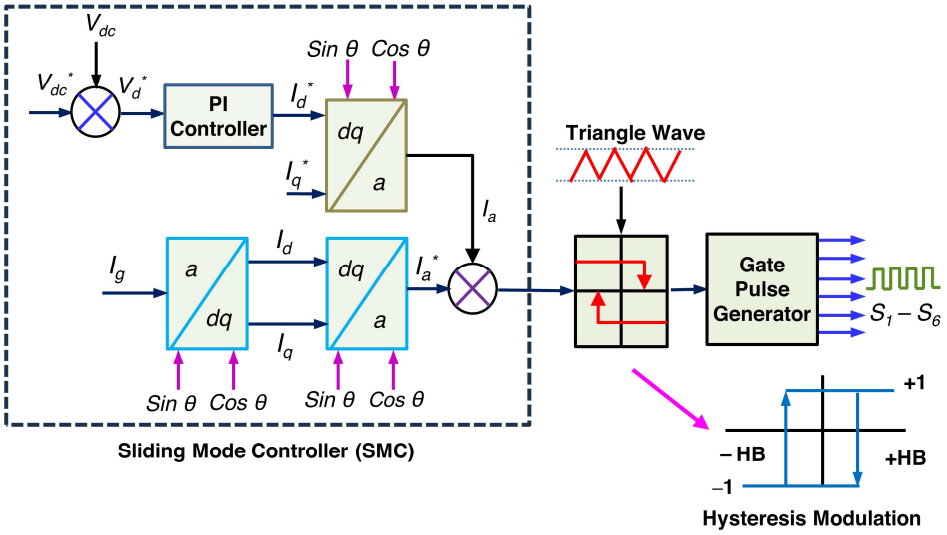


Figure 9. Sliding mode controller (SMC) with hysteresis modulation.

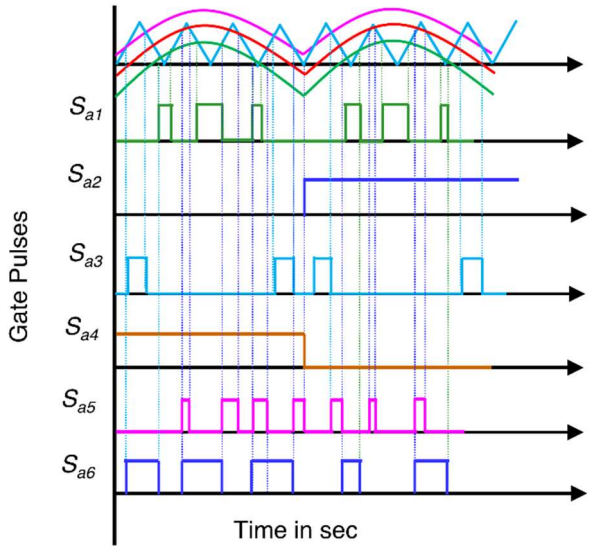


Figure 10. Gate pulse generation through hysteresis band.

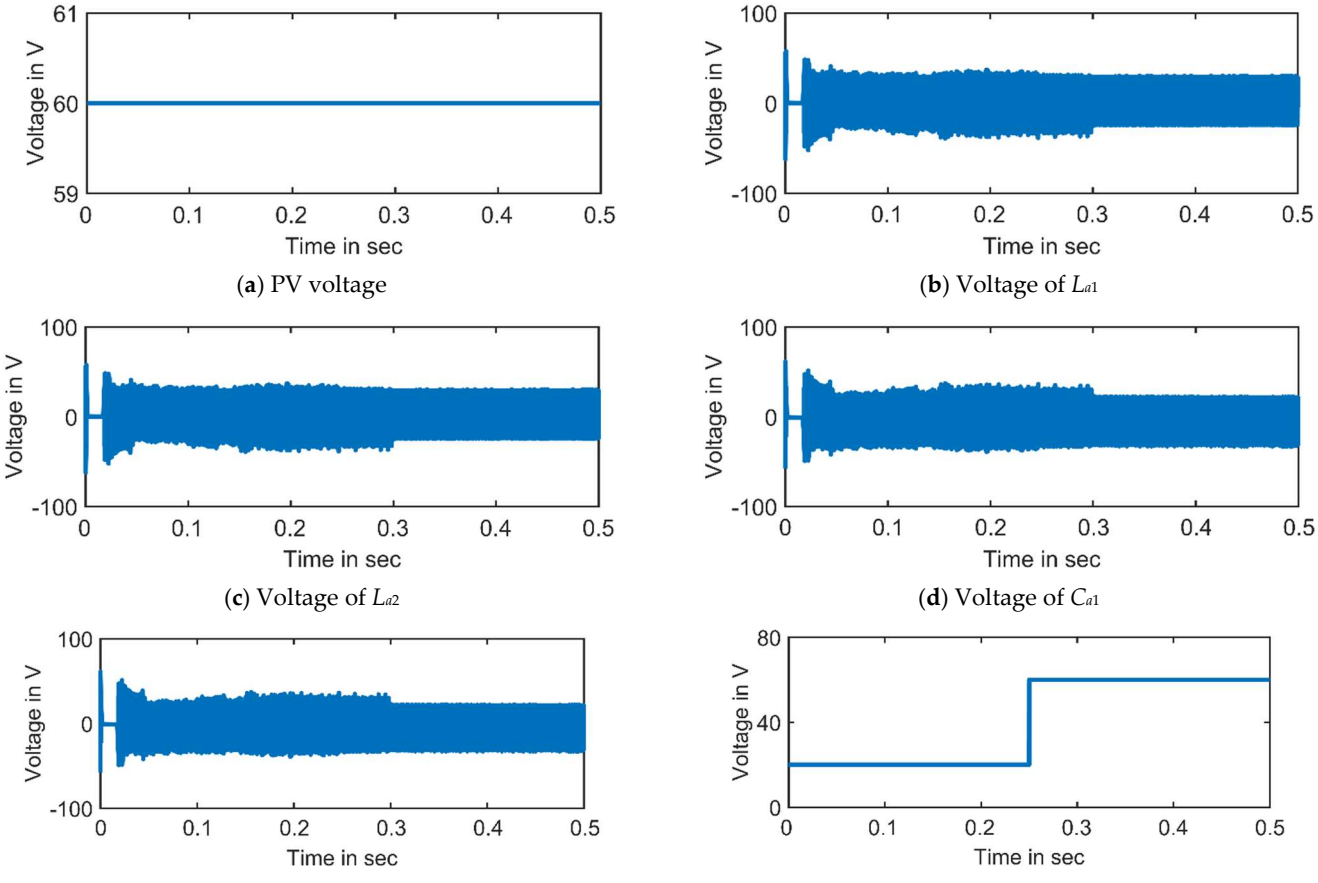
5. Results and Discussion

This section describes the experimental findings of a scaled down model with the specifications of 1500 W, 230 V (RMS), and 50 Hz. The purpose of this model was to investigate the possible benefits and downsides of the IMISO-Z source converter-fed SPFL inverter that was described before. The findings of the scaled-down model will be reported, which will allow us to fulfil this goal. During the process of carrying out the evaluation, several aspects, such as the boost factor, capability of producing a regulated DC output, and its ability to transmit power, are all taken into consideration. This is performed in order to ensure that the proposed IMISO-Z source converter may be evaluated in an appropriate manner. With the aid of MATLAB/Simulink and hardware implementation, analyses of the functioning of a single-phase SPFL inverter that was connected to the grid and was supplied using a scaled-down IMISO-Z source converter have been carried out. In order for it to be possible to assess it as part of the process of evaluating the simulated model, the discrete sample time of the simulated system was set to a value of 50 µs. The input ports of the proposed IMISO Z-source converter were powered using a combination of a pair of solar modules and a wind system, each of which was rated at 750 W and 60 V. A model that was developed in MATLAB Simulink is responsible for driving these input ports. Verification was performed on the recommended system, and the results were analyzed in light of the design parameters presented in Table 3. During the course of the experiment, a simulated photovoltaic (PV) array that had a power output of 750 W and a voltage of 60 V was exposed to a constant light intensity of 1000 W/m^2. The wind turbine that was connected to the terminals of the unregulated three-phase rectifier was subjected to varying wind velocities that were imposed on the device. The wind speed was increased from 5 m per second to 10 m per second so that a varied voltage could be produced. In addition to this, the terminals of an SPFL inverter were connected with a dynamic load that consisted of a resistance of 230 Ω and an inductance of 0.114 mH. The functionality of an IMISO Z-source converter-powered SPFL inverter was examined during this phase of the testing while it was subjected to the effects of a dynamic load. This test was carried out while the inverter was kept in a state where it was connected to the grid. This method produces the most trustworthy results; thus, completing the test in this manner is standard practice. When they are working at a voltage of 60 volts, the solar cells that made up the PV array have a combined output power that is equal to 750 W.

Table 3. Design parameters of simulated and experimental model.

Component	Value and Unit	Component	Value and Unit
L_{a1}, L_{a2}, L_{b1}, and L_{b2}	40 µH	Grid Voltage	230 V (RMS)
C_{a1}, C_{a2}, C_{b1}, and C_{b2}	100 µF, 400 V	Grid Frequency	50 HZ
Rating of transformer	1.5 kVA	Type	Single Phase
Primary voltage	200 V	Maximum Power	150 W/12 V
Secondary voltage	400 V	Open-circuit Voltage	22.5 V
Turns Ratio	1:2	Short-circuit Current	8.81 A
C_1 and C_2	100 µF, 400 V	Voltage at maximum power	17.96 V
C_3, C_4, and C_5	0.114 µF, 400 V	Current at maximum power	8.36 A
Load Resistance	230 Ω	Load Inductance	0.114 mH

The PV voltages are passed to L_{a1} and L_{a2} even after the switches S_{a1} and S_{a2} have been set to their closed positions. This occurs even if the switches are in their closed positions. This procedure will go on until the voltage hits the highest possible input voltage it can attain. The photovoltaic source and the wind sources may both discharge the energy that they have stored in series with one another because of the way that they are linked to the inductors L_{a1}, L_{a2}, L_{a3}, and L_{a4} in the system. Based on the test, it was determined that the primary voltage detected across the impedance network inductors was 50 V. Waveforms similar to those shown in Figure 11 were produced during the simulations. The output voltage of the simulated solar panel was shown to be 60 V in Figure 11a when it was exposed to an intensity of solar irradiation of 1000 W/m^2. When the variable wind velocity was applied to the wind source, as shown in Figure 11f, the source generated 30 V between 0 and 0.25 s, and then produced 60 V between 0.25 and 0.5 s.



(**a**) PV voltage

(**b**) Voltage of L_{a1}

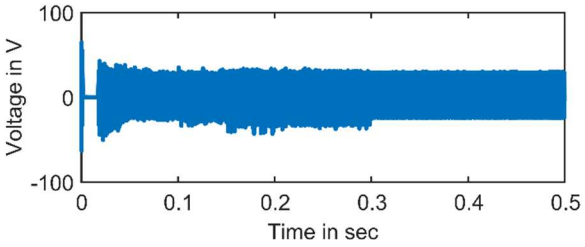
(**c**) Voltage of L_{a2}

(**d**) Voltage of C_{a1}

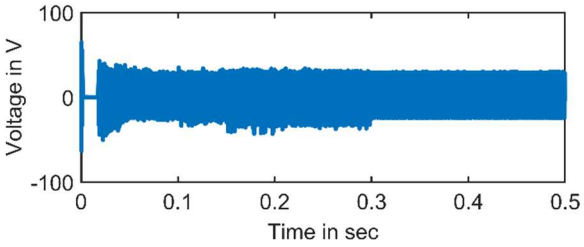
(**e**) Voltage of C_{a2}

(**f**) Wind rectifier output voltage

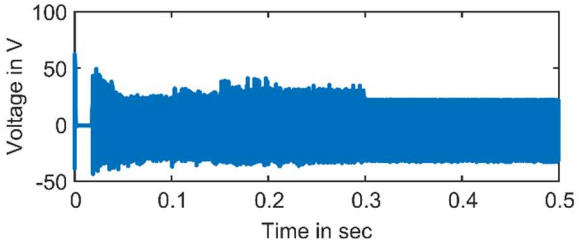
Figure 11. *Cont.*



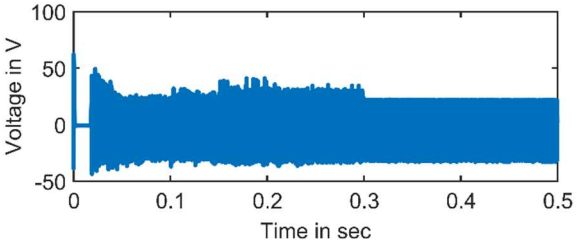
(**g**) Voltage of L_{b1}



(**h**) Voltage of L_{b2}



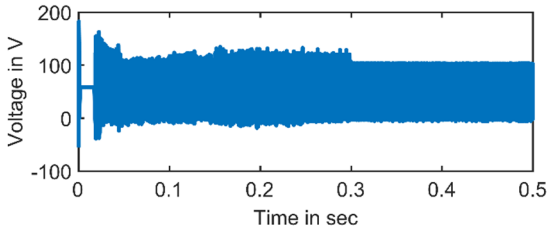
(**i**) Voltage of C_{b1}



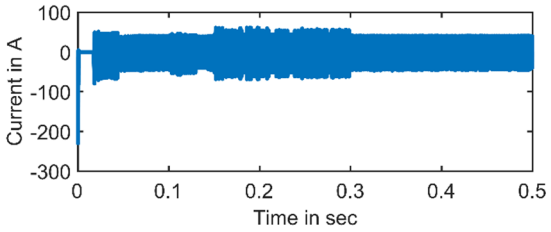
(**j**) Voltage of C_{b2}

Figure 11. Simulation results of active and passive elements of impedance network.

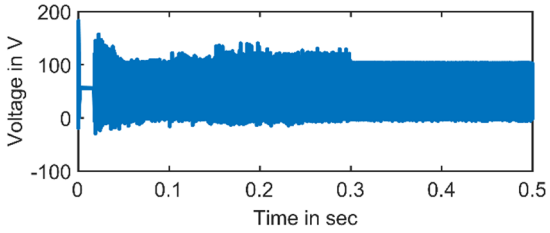
Figure 12 depicts the voltage that was present across the main and secondary windings of the transformer, the voltage that was present across capacitors C_1 and C_2, and the voltage that was present at the output of the IMISO Z–source converter. The primary winding of the transformer was tested as having a voltage of 100 V. The voltage control loop that is described in Section 4.1 was responsible for keeping the DC bus voltage at 326 V at all times.



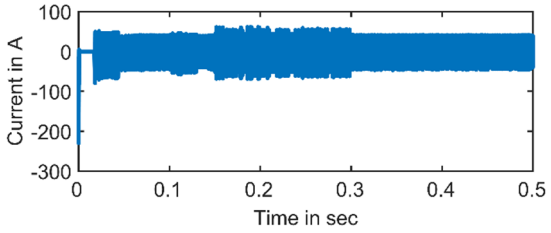
(**a**) Primary 1 voltage



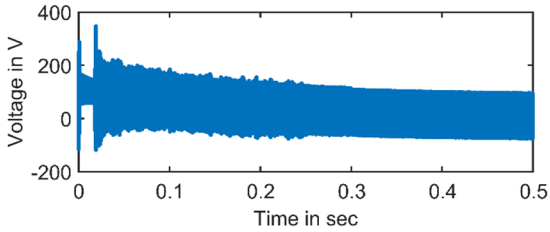
(**b**) Primary 1 current



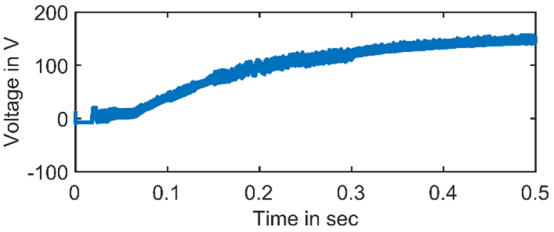
(**c**) Primary 2 voltage



(**d**) Primary 2 current

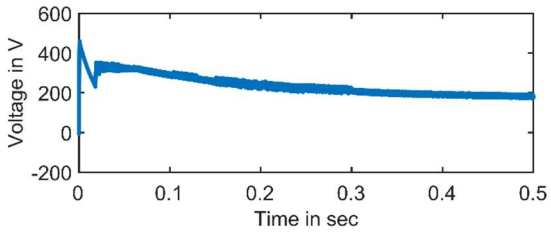


(**e**) Secondary voltage

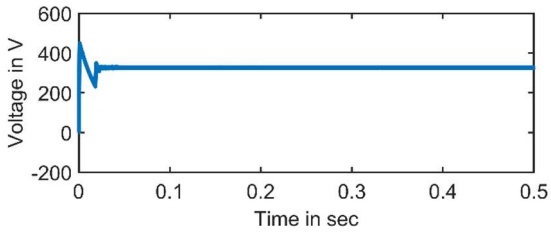


(**f**) Voltage of C_1

Figure 12. *Cont.*



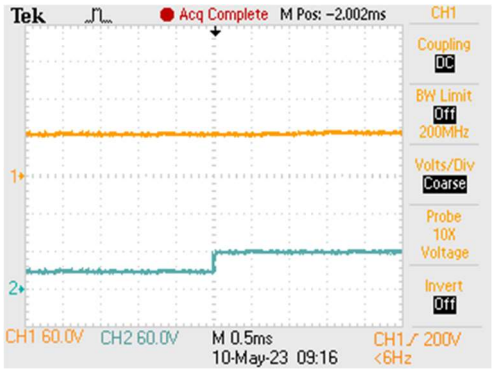
(**g**) Voltage of C_2



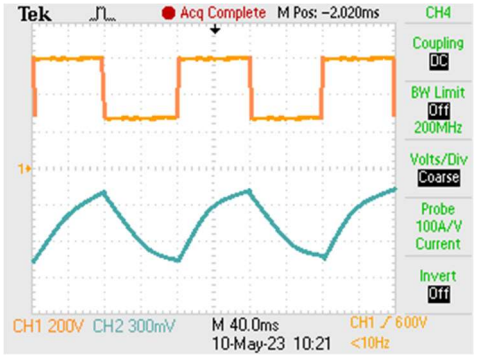
(**h**) Output voltage of IMISO ZSC

Figure 12. Simulation results of transformer and output terminal.

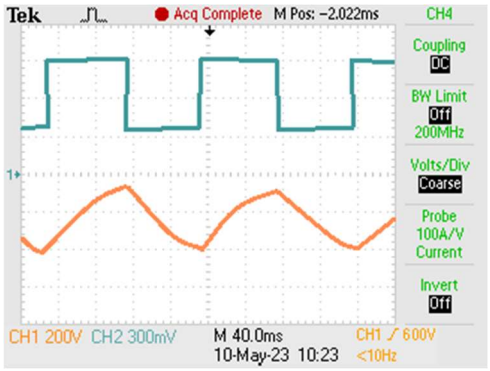
To assess the practical implementation of the suggested IMISO Z–source converter-fed SPFL inverter, the experimental data measured using the six-phase power analyzer are shown here. Figure 13 displays the results of measurements used to determine the voltage that exists between the active and passive components of an IMSO Z-source converter. The output voltage of the solar photovoltaic array and the wind system is shown in Figure 13a. In order to test the capacity of the converter to maintain a constant voltage, the output voltage of source 2 was raised from 30 V to 60 V.



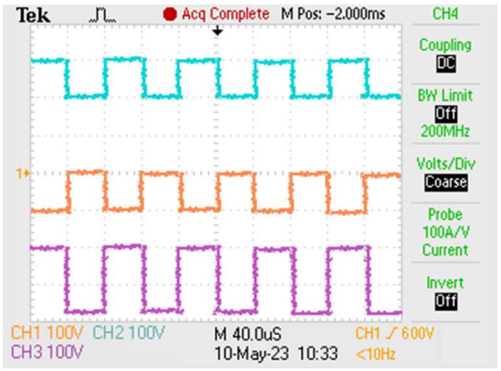
(**a**) PV and Wind output voltage



(**b**) Voltage and current of L_{a1} and L_{a2}



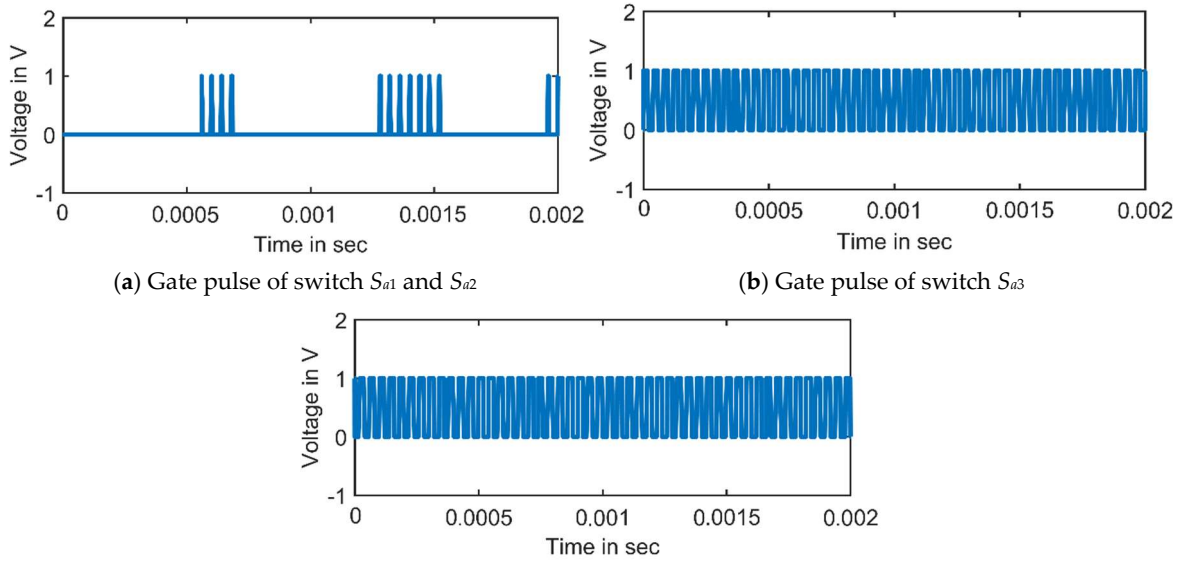
(**c**) Voltage and current of L_{b1} and L_{b2}



(**d**) Transformer primary and secondary voltage

Figure 13. Experimental results of active and passive elements of IMSO-ZSC.

The voltage and current readings for the impedance network inductors L_{a1}, L_{a2}, L_{a3}, and L_{a4} are shown in Figure 13b and Figure 13c, respectively. The charging and discharging curves of the inductor are represented by the waveform of the current. The voltage that was measured across the transformer's primary was approximately 200 V in each direction. The secondary voltage was somewhere in the neighborhood of 400 V. Figure 14 illustrates the gate pulses that were generated by the power switches S_{a1}, S_{a2}, S_{a3}, and S_{a4}.



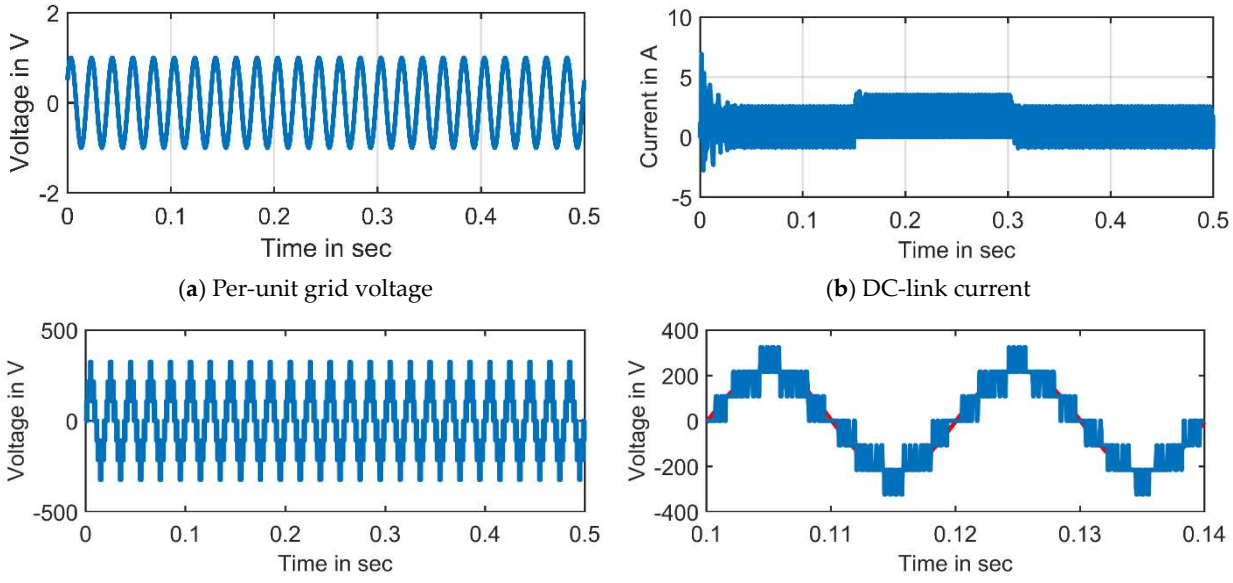
(**a**) Gate pulse of switch S_{a1} and S_{a2}

(**b**) Gate pulse of switch S_{a3}

(**c**) Gate pulse of switch S_{a4}

Figure 14. Gating signal of active switches.

Figure 15 depicts the utility's per–unit cost, the SPFL inverter's DC bus current, the inverter's five–level voltage waveform and its expanded voltage waveform, and the current and active and reactive power taken by the load. The simulation validation included applying varying input voltages and loads to evaluate the system's overall performance. The experimental model was adjusted to accommodate the increased demand. There was a 1.5 A increase in the AC load, for a total of 3 A. The prototype could still run a 230 V, 3 A load in this other scenario.



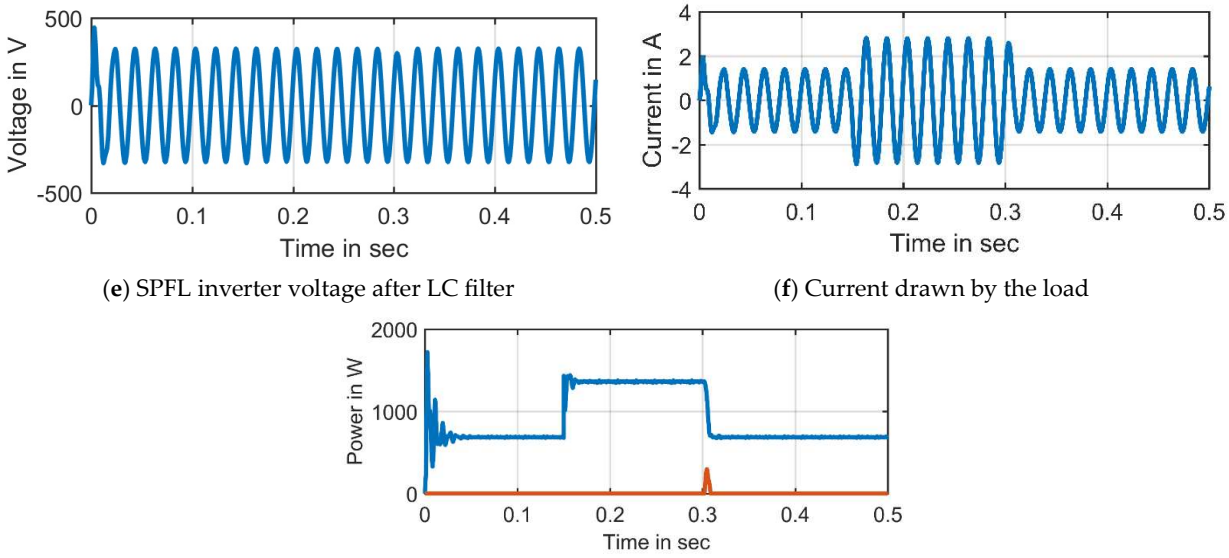
(**a**) Per-unit grid voltage

(**b**) DC-link current

(**c**) SPFL inverter output voltage

(**d**) Enlarged SPFL inverter voltage

Figure 15. *Cont.*



(**e**) SPFL inverter voltage after LC filter

(**f**) Current drawn by the load

(**g**) Power drawn by the load

Figure 15. Simulation results of SPFL inverter and load.

The SPFL inverter added total harmonic distortion (THD) to the grid power, and an FFT analysis was used to quantify this effect. Figure 16 shows the THD content of the SPFL inverter voltage as calculated from the simulation data. The voltage and current waveforms produced by the prototype SPFL inverter are shown in Figure 17.

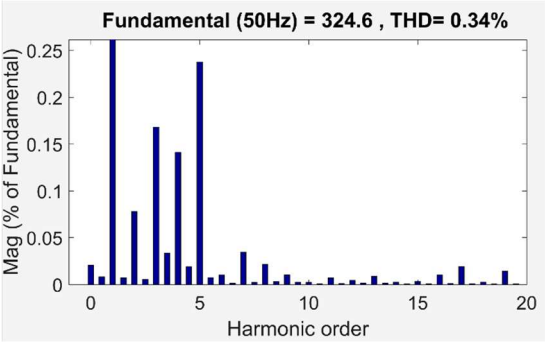
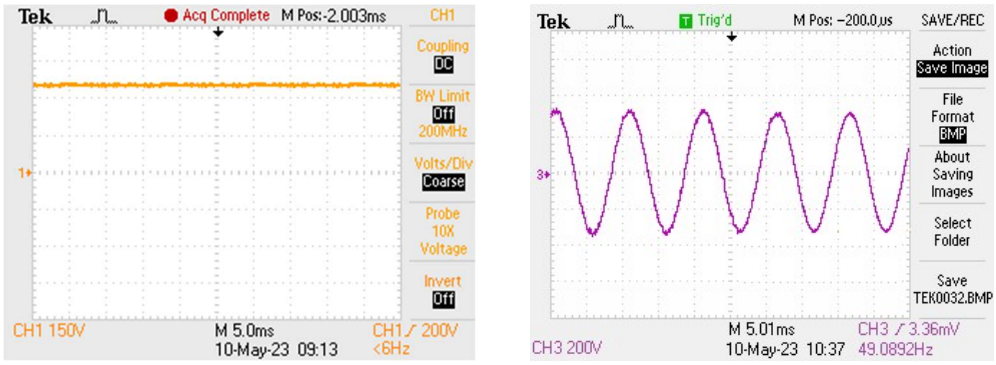


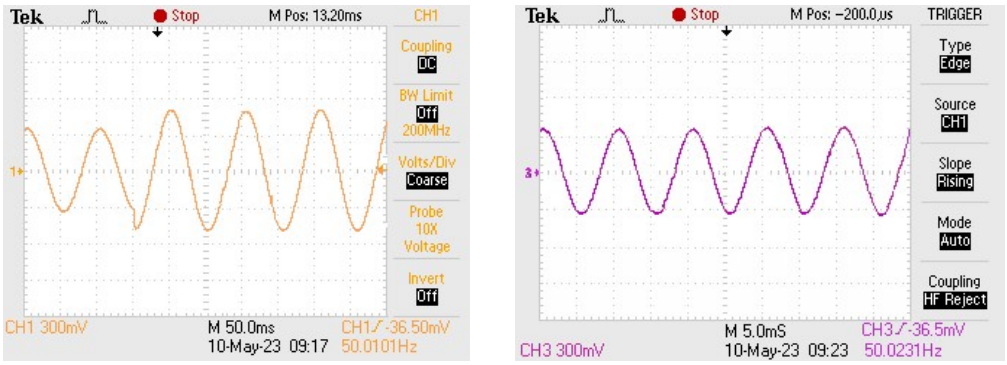
Figure 16. Simulation results of voltage THD analysis.



(**a**) DC bus voltage of SPFL inverter

(**b**) SPFL inverter voltage after filter

Figure 17. *Cont.*



(**c**) Load current under dynamic load (**d**) Load current under constant load

Figure 17. Experimental results of SPFL inverter and load.

The proportion of THD in the SPFL inverter's output voltage after utility connections were made was calculated using power quality measurement devices. As can be seen in Figure 18, the load voltage THD determined using the power quality measuring equipment was 2.2%.

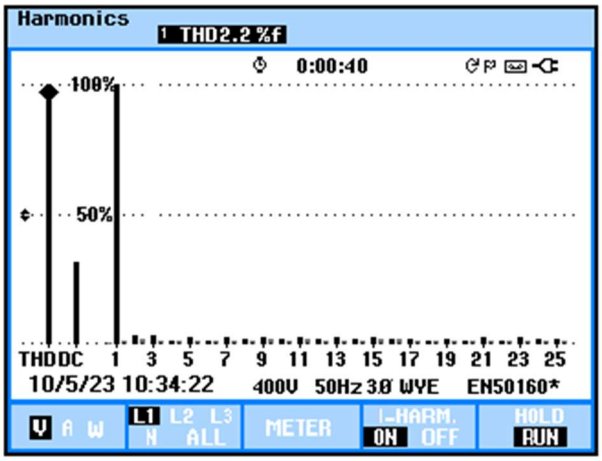


Figure 18. Experimental results of voltage THD analysis.

Figure 19 provides a comparison between the proposed IMISO Z-source converter and the standard converter described in references [18–20]. The suggested IMISO Z-source converter outperformed the other conventional converters in terms of gain.

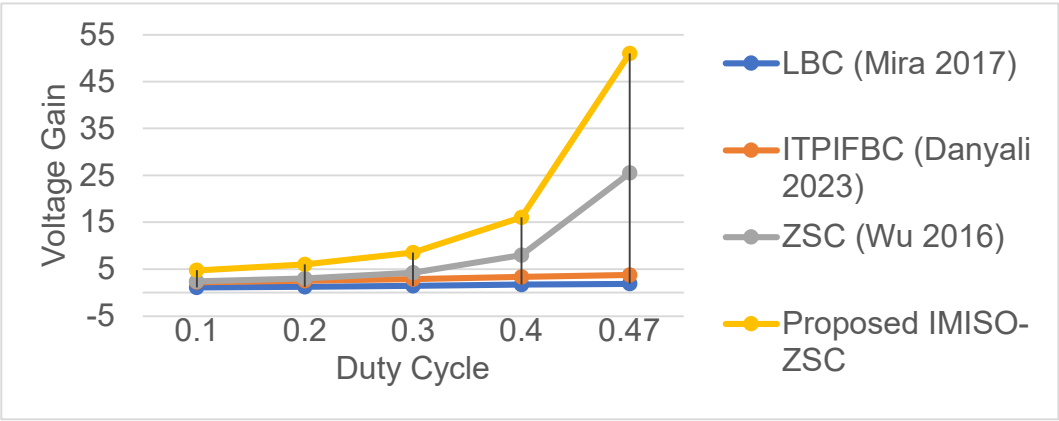


Figure 19. Comparison between the proposed IMISO Z–source converter and the standard converter [18–20].

6. Conclusions

In this research, a unique switching impedance network for a high step-up isolated multi–input single–output (IMISO) Z–source DC–DC converter is proposed. Comparing the features of the Z–source converter with the interleaved-boost full-bridge three-port converter led to the proposal of this particular converter. The working principle analysis, parameter selection, and a comparison with other comparable high step–up DC–DC converters on the market have all been covered at length. Finally, the computational and experimental findings were shown to validate the potential benefits of the proposed converter. The proposed IMISO–Z–source converter exhibited a lower current stress and lower voltage stress across the switches compared to previously suggested high step-up DC–DC converters. All of these advantages resulted from the converter's superior construction. As a result, the suggested converter's boost factor and reliability may be enhanced, suggesting it is well–suited for high step-up voltage conversion tasks. PV systems, wind systems, hybrid wind–solar systems, and grid connectivity of renewable energy sources are all examples of such uses.

7. Future Scope

In the proposed topology, IGBT has been utilized as a switching device. Gallium nitride (GaN) and silicon carbide (SiC) FETs are enabling higher levels of power density and efficiency compared to traditional silicon metal-oxide semiconductor field-effect transistors (MOSFETs). Although both technologies are wide bandgap, there are fundamental differences between GaN and SiC that makes one a better fit than the other in certain topologies and applications. In the proposed topology, the replacement of traditional IGBTs can give a better conversion efficiency.

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