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A High Step-up DC-DC Converter Based on the Voltage Lift Technique for Renewable Energy Applications

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Abstract: High gain DC-DC converters are getting popular due to the increased use of renewable energy sources (RESs). Common ground between the input and output, low voltage stress across power switches and high voltage gain at lower duty ratios are desirable features required in any high gain DC-DC converter. DC-DC converters are widely used in DC microgrids to supply power to meet local demands. In this work, a high step-up DC-DC converter is proposed based on the voltage lift (VL) technique using a single power switch. The proposed converter has a voltage gain greater than a traditional boost converter (TBC) and Traditional quadratic boost converter (TQBC). The effect of inductor parasitic resistances on the voltage gain of the converter is discussed. The losses occurring in various components are calculated using PLECS software. To confirm the performance of the converter, a hardware prototype of 200 W is developed in the laboratory. The simulation and hardware results are presented to determine the performance of the converter in both open-loop and closed-loop conditions. In closed-loop operation, a PI controller is used to maintain a constant output voltage when the load or input voltage is changed.

Keywords: high gain; low voltage stress; voltage lift (VL); renewable energy sources (RESs); equivalent series resistance (ESR)

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1. Introduction

The present alarming situation of depletion of non-renewable energy sources presents an opportunity to look for alternative energy sources. RESs are a good option to replace fossil fuel energy and nuclear energy for electrical power generation. In recent years, the share of RESs in power generation has increased significantly. Distributed generation (DG) technologies utilize RESs in the form of solar cells, fuel cells and wind turbines etc. [1,2]. To tackle the problem of environmental pollution and global warming caused by fossil fuels, sustainable energy production can be achieved by renewable [3,4] energy sources. Renewable energy systems and energy storage systems are going to play an important role in the future of low-carbon energy emission systems [5].

RESs are integrated with battery energy storage systems (BESSs), are not only environmentally friendly but also result in the wide use of DC (Direct Current) systems, i.e., DC generation and DC storage units. To inject this power into the alternating current (AC) Distribution Grid, DC-AC power electronic converters are used. Similarly, AC–DC and DC–AC conversion are used in AC drives. Moreover, the DC loads such as electric vehicles (EVs), light-Emitting Diode systems (LED), DC motors, data centres, and other battery-based devices are penetrating the market with a rising curve [6]. These systems require AC–DC conversion systems, so there are multiple stages of AC–DC conversion,

which reduce the overall efficiency and reliability of the systems. The increasing demand for DC power at load has challenged the conventional AC distribution system, while the DC power systems are used for the transfer of DC power over long distances, mostly in high-voltage applications. The advantages of DC power systems have not been exploited in low voltage (LV) (1.5 kV) and medium voltage (MV) (50 kV), leaving the power system domain to AC architecture [6,7]. To solve this problem, the concept of a DC microgrid is derived to meet local demands. Microgrids are interconnected to LV and MV distribution networks via direct connection or a power electronic interface. Easier integration of RESs and BESSs with DC microgrid means that the supply does not need to be converted into AC; instead of the multiple AC–DC and DC–AC converter, DC power could be supplied by a DC-DC converter, resulting in the reduction of primary energy consumption, leading to efficient and smaller systems. Therefore, it is more efficient to have a DC distribution, including DC-DC converters, than AC counterparts [8].

Figure 1 shows the arrangement for RESs, which generate low output voltage (12–48 V), so output voltage has to be lifted to level (200–500 V) for DC microgrid or battery set applications.

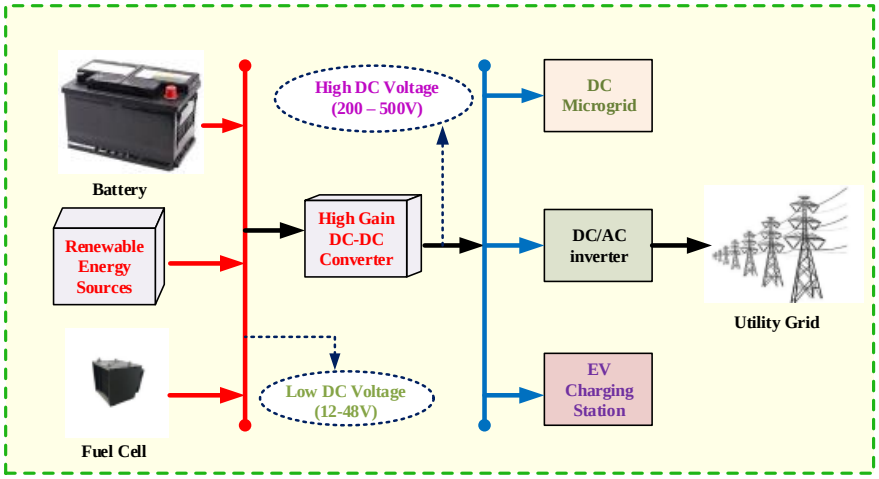


Figure 1. High Gain DC–DC converter for RES-relevant schematic arrangement.

DC–DC converters act as a medium between the load and the source. They are broadly classified into two types in the literature: isolated and non-isolated. Traditional boost converters (TBC), as shown in Figure 2a, if deployed in microgrids, would have to be operated at high values of the duty ratio which causes high current and voltage stress on the power devices of the converter. The voltage drop across the parasitic resistance (ESR) of capacitors and inductors increases substantially at higher duty ratios, leading to the decrease in voltage gain and efficiency of the conventional boost converter [9–11].

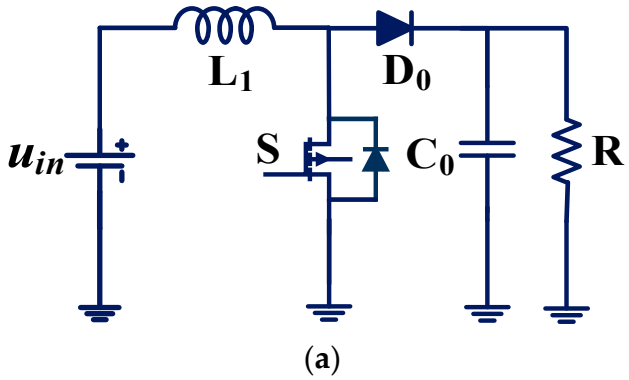


Figure 2. *Cont.*

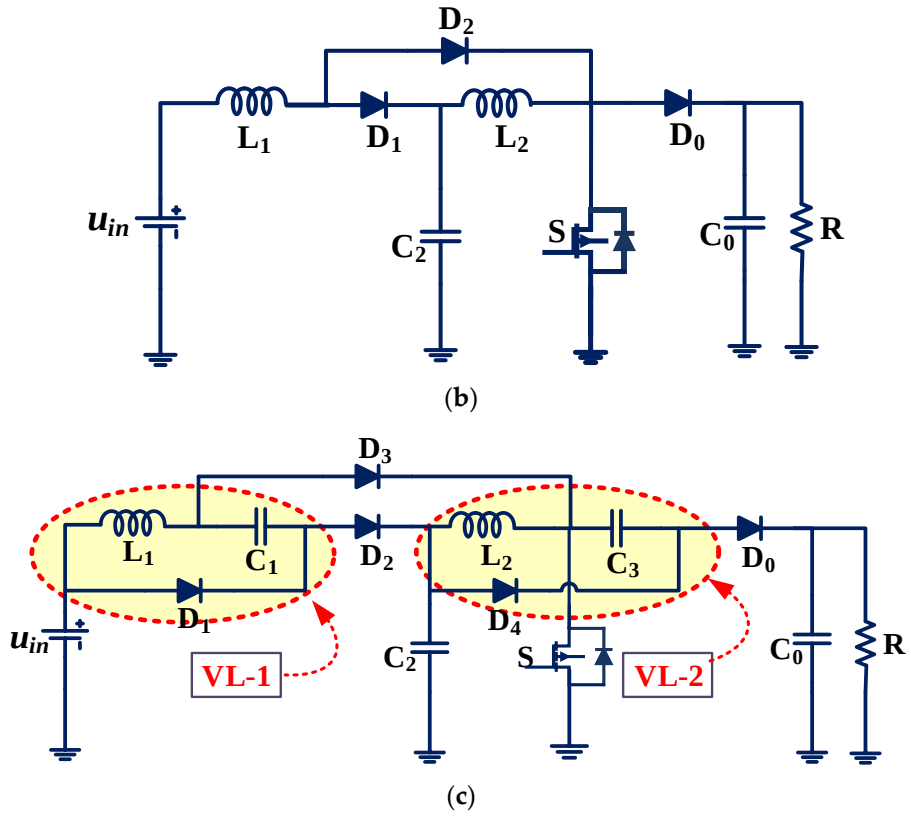


Figure 2. (**a**). Traditional boost converter. (**b**). A traditional quadratic boost converter (TQBC). (**c**). Proposed dual-voltage lift (D-VL) topology.

To address these problems, several DC-DC converters topologies have been proposed. In [10] a review of o various boosting techniques such as the use of voltage multipliers to multiply the boost factor, and switched inductor, switched capacitor, magnetic coupling, and multistage techniques. Several high-gain DC-DC converters are proposed using these techniques. In [11] the converter uses a voltages doubler to increase the voltage gain. Several converters use isolated high-frequency transformers to obtain voltage gain by increasing the turns ratio of the transformer. However, such circuits are bulky, costly, and more complex., Moreover, the leakage inductance of the transformer would interfere with switch operation [10,11].

Non-isolated converters are further classified into two types, namely, coupled inductor and non-coupled [12]. In the coupled-inductor-based converters, the output can be boosted by selecting a suitable turn ratio of the inductor coil. The leakage inductance of the coupled inductor is inexorable, which generates a spike in switch current and demands clamping [13]. Several applications do not require an isolated converter; in such cases, non-isolated DC-DC converters are preferred to achieve high voltage gains [14–16]. A modified structure of the quadratic boost converter is obtained by using a switched inductor module in place of the inductor to obtain the voltage gain twice the TQBC [17,18]. Additionally, the combination of different converters can give rise to new converters. A modified SEPIC converter is used to achieve higher gain by amalgamating the conventional SEPIC with the boosting module [19]. A novel buck-boost topology is derived in [20] by combining one traditional boost converter, one traditional buck converter, and one traditional buck-boost converter using only one power switch to obtain quadratic voltage gain. Another buck-boost topology is presented in [21]. Hybrid switched-capacitor quadratic boost converters with very high DC gain and low voltage stress on power devices are presented in [22]. A larger gain is obtained by a hybrid switched-capacitor technique in [23]. The low voltage stress on power semiconductor devices allows using lower-rated MOSFET

with low on-resistance to obtain better efficiency by reducing conduction and switching loss [23].

The voltage lift (VL) technique is a well-known method widely used in electronic circuit design. In recent years, it has been successfully used in DC-DC converter applications and paved the way for the design of high voltage gain converters. The use of the VL technique was confirmed by Luo by developing DC-DC converters [24]. It uses extra energy storage elements inductors and capacitors to enhance the voltage gain of the circuit. Luo proposed a series of positive output Luo converters, such as a self-lift circuit, re-lift circuit, triple-lift, and quadruple-lift boost converters. This technique was used to overcome the effects of the parasitic elements and to boost the voltage at the output. In [25] a high-gain converter using the VL technique to achieve gain equal to twice the traditional boost converter using two inductors, but this converter has switch stress equal to the output voltage. A voltage doubler circuit such as Cockroft–Walton can be used to increase the output voltage [26], and it reduces the voltage stress across the switch. Additionally, the VL technique is used in [25–28] with a voltage doubler. A non-isolated DC-DC converter based on the VL technique was used to obtain a negative voltage concerning the ground [29]. The isolated category of converter bases on interleaving technique is proposed in ref. [30]

In this paper, the proposed non-isolated quadratic boost converter utilizes the dual voltage lift (VL) technique to increase the gain of the converter. The proposed topology has the following advantages.

1. The voltage gain is greater than TBC and QBC.
2. The voltage stress on the power switch is lower than the output voltage.
3. The voltage doubler is avoided to increase the voltage gain.
4. A single power switch that makes control easy reduces gate drive requirements.
5. The low voltage stress on power devices reduces the power losses, hence the converter efficiency is increased.
6. A common ground connection is available between the source and load.

2. Operating Principle of the D-VL Converter

The proposed schematic illuminated in Figure 2c uses two voltage lift cells. The combination of L_1, C_1, and D_1 is the first voltage lift cell (VL-1), whereas the similar combination of L_2, C_2, and D_2 is (VL-2). The proposed converter has two inductors, four capacitors, and five diodes. The converter utilizes a single power switch, so the control is very easy. Taking a single voltage lift cell (VL-1), when Switch S is ON, the additional capacitor C_1 is connected in parallel with Inductor L_1 and charged by an input DC source. When the switch is OFF, the energy storage capacitor C_1 is connected in series with DC input, and Inductor L_1 discharges energy to pure resistive load R. Same situation occurs in VL-2. This way, voltage gain improvement is achieved and reduced switch stress over a traditional quadratic boost converter (TQBC), as depicted in Figure 2b.

2.1. Continuous Conduction Mode (CCM) of the D-VL Converter

The continuous conduction mode of the D-VL converter can be analyzed in two modes of operation.

Mode 1 ($t_1 < t < t_0$): The equivalent circuit related to this mode is shown in Figure 3a. inductor L_1 is charged by input source U_{in} through D_3 and S. Moreover, inductor L_2 is charge by capacitors C_1 and C_2 through S. In this interval, inductor currents have a positive slope and store energy. The output DC load is fed by output capacitor voltage U_{C0}. Waveform's profile of the proposed converter is shown in Figure 4. The governing voltage equations are as follows

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = u_{L1} = u_{in} \\ L_2 \frac{di_{L2}}{dt} = u_{L2} = u_{C3} \\ u_{C1} = u_{C3} - u_{C2} + u_{in} \\ u_{C2} = u_{C3} \\ u_{C1} = u_{in} \end{cases} \quad (1)$$

where u_x represents the voltage across the corresponding components.

Mode 2($t_1 < t < _S$): Switch S is turned off in this mode. The equivalent circuit of this mode is shown in Figure 3b. Inductors L_1 and L_2 discharge through D_2, C_2, and D_0, C_0, respectively. Waveform's profile of the proposed converter is shown in Figure 4. The governing voltage equations are as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = u_{L1} = u_{in} + u_{C1} - u_{C2} \\ L_2 \frac{di_{L2}}{dt} = u_{L2} = u_{C2} + u_{C3} - u_0 \end{cases} \quad (2)$$

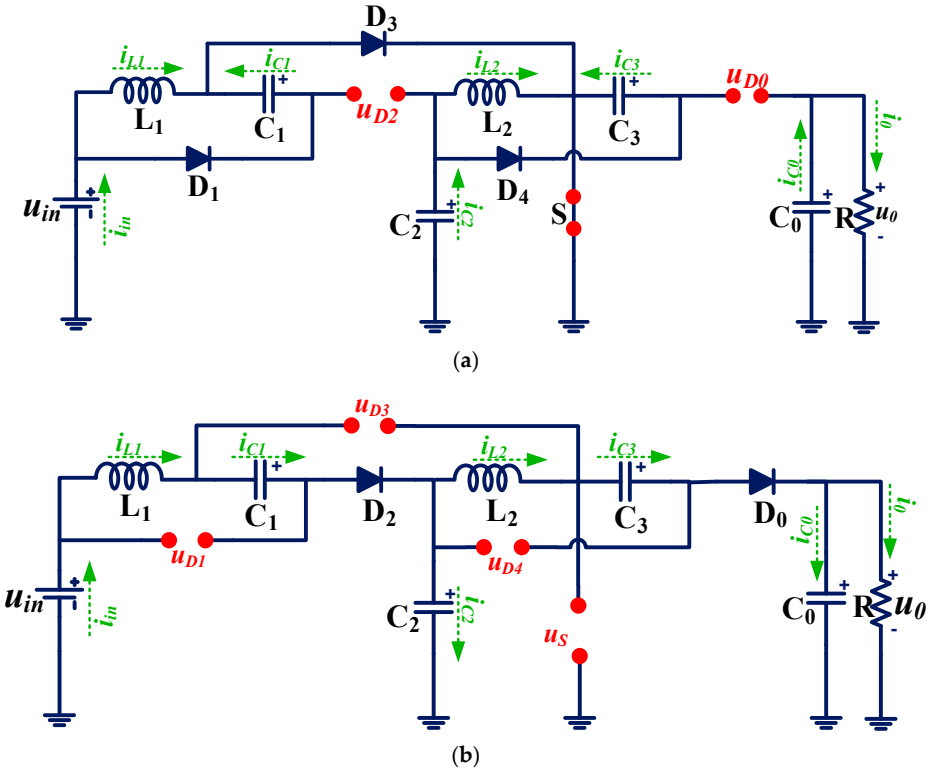


Figure 3. D-VL CCM operation: (**a**) Mode I (**b**) Mode II.

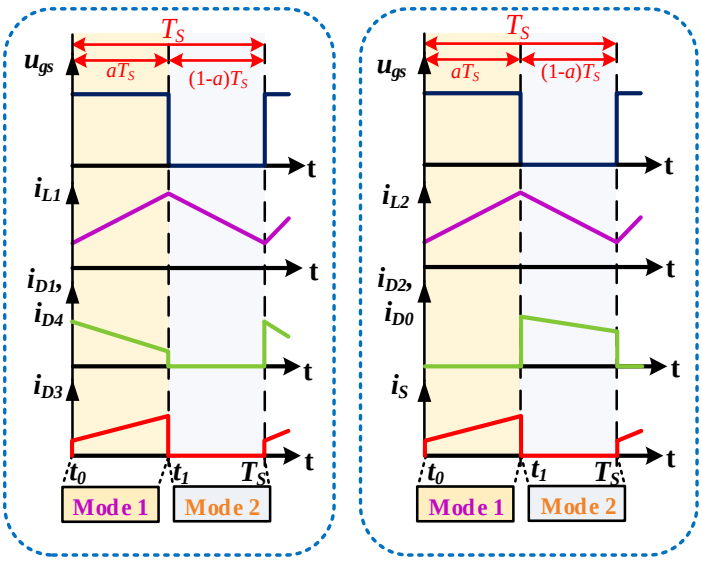


Figure 4. Important waveforms of the converter in CCM.

Voltage Gain Calculation

During steady-state conditions, the average voltage across an inductor is zero, i.e., $\int_0^{T_s} u_L dt = 0$.

Using the derived voltage Equations (1) and (2), we can extract the volt-second balance equations as

$$\begin{cases} u_{in}\alpha + (u_{in} + u_{C1} - u_{C2})(1-\alpha) = 0 \\ u_{C3}\alpha + (u_{C2} + u_{C3} - u_0)(1-\alpha) = 0 \end{cases} \quad (3)$$

where α is the duty ratio.

Using Equations (1)–(3), the following results are obtained:

$$\begin{cases} u_{C3} = \left(\frac{2-\alpha}{1-\alpha}\right)u_{in} \\ u_{C3} = \left(\frac{1-\alpha}{2-\alpha}\right)u_0 \end{cases} \quad (4)$$

Using (4) voltage gain K_{ccm} for the proposed converter, the results are:

$$K_{ccm} = \frac{u_0}{u_{in}} = \left(\frac{2-\alpha}{1-\alpha}\right)^2 \quad (5)$$

2.2. Mismatch Operating Modes of the Inductors of the Proposed D VL Converter

The converter enters the DCM mode of operation when the inductor current goes to zero at any time of interval. Consider two cases of operation:

2.2.1. Case I: Inductor L_1 Operating in DCM and L_2 into CCM

Inductor L_1 is sufficiently high so that ripple is neglected. A low value of inductance of L_2 makes the ripple high in inductor current L_2, and the current goes to zero before the time interval T_S. The waveform of the considered operation is shown in Figure 5a.

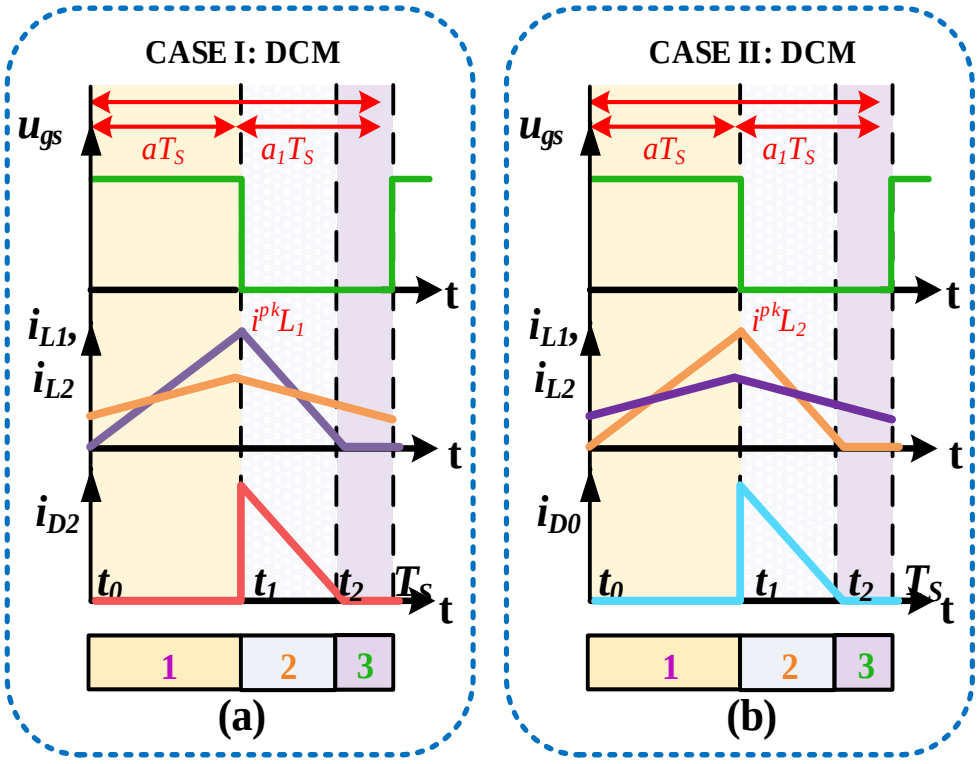


Figure 5. DCM waveforms (**a**) Case I: Inductor L_1 operating in DCM and L_2 into CCM (**b**) Case II: Inductor L_2 operating in DCM and L_1 into CCM.

Mode 1($t_0 < t < t_1$):

The power switch is ON for this duration. Inductor L_1 starts to magnetize from zero and reaches the maximum at the end at time DT_S. This mode is the same as CCM Mode I. The governing relations in this mode is given by Equation (1).

Mode 2($t_1 < t < t_2$):

The power switch is OFF in this time interval. Inductor L_1 starts to demagnetize, and the current falls to null at the end of the interval $\alpha_1 T_s$. The governing relations in this interval are given by (2).

Mode 3($t_2 < t < T_S$):

The power switch is OFF. In this interval, the Inductor L_1 current is zero. The voltage across Inductor L_1 is zero. The equivalent circuit diagram is shown in Figure 6.

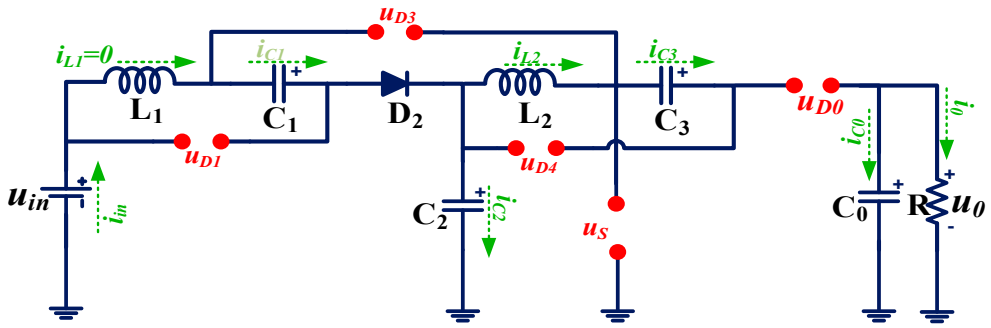


Figure 6. Mode 3 of Case I of DCM.

The average voltage across an inductor is zero, i.e., $\int_0^{T_s} u_L dt = 0$ in equilibrium. Therefore,

$$\begin{cases} u_{in}\alpha + (u_{in} + u_{C1} - u_{C2})\alpha_1 = 0 \\ u_{C3}\alpha + (u_{C2} + u_{C3} - u_0)(1-\alpha) = 0 \end{cases} \quad (6)$$

Using Equations (4) and (6), the voltage gain can be derived as

$$K_{dcm} = \frac{u_0}{u_{in}} = \frac{(\alpha + 2\alpha_1)(2-\alpha)}{\alpha_1(1-\alpha)} \quad (7)$$

Additionally, the value of α_1 can be calculated as below:

$$\frac{1}{2}\alpha_1 i^{pk}{}_{L1} = \langle i_{D2} \rangle = \left(\frac{2-\alpha}{1-\alpha}\right)\langle i_0 \rangle \quad (8)$$

$$i^{pk}{}_{L1} = \frac{u_{in}\alpha}{L_1 f_s}\ ;\ \langle i_0 \rangle = \frac{u_0}{R} \quad (9)$$

From (7), (8), and (9), the resulting quadratic equation has roots that give a voltage gain relation in the DCM mode of operation.

$$K^2{}_{dcm} - \frac{2(2-\alpha)}{(1-\alpha)}K_{dcm} - \frac{\alpha^2}{\beta} = 0 \quad (10)$$

where $\beta = 2L_1/RT_S$ is defined as a normalized inductor time constant.

The positive solution gives the required solution, i.e.,

$$K_{dcm} = \left(\frac{2-\alpha}{1-\alpha}\right)\left[1 + \sqrt{1 + \frac{\left(\frac{\alpha(1-\alpha)}{2-\alpha}\right)^2}{\beta}}\right] \quad (11)$$

Boundary Condition Mode:

In Mode 2, the inductor current of L_1 becomes zero at the end of αT_S. This mode is termed a boundary condition mode (BCM). In this mode, the voltage gain of CCM mode and DCM mode are equal, i.e.,

$$K_{dcm} = K_{ccm} = \left(\frac{2-\alpha}{1-\alpha}\right)^2 = \left(\frac{2-\alpha}{1-\alpha}\right)\left[1+\sqrt{1+\frac{\left(\frac{\alpha(1-\alpha)}{2-\alpha}\right)^2}{\beta}}\right] \quad (12)$$

The following relation is yielded from (12):

$$\beta = \beta^{L_1}{}_{BCM} = \frac{\alpha(1-\alpha)^4}{(2-\alpha)^3} \quad (13)$$

The derived $\beta^{L_1}{}_{BCM}$ is defined as the normalized boundary inductor time constant for Inductor L_1. If $\beta > \beta^{L_1}{}_{BCM}$, the converter operates in CCM mode; otherwise, the converter operates in DCM mode, as shown in Figure 8a.

2.2.2. Case II: Inductor L_2 Operating in DCM and L_1 into CCM

Inductor L_2 is sufficiently high so that ripple is neglected. A low value of inductance of L_1 makes ripple high in inductor current L_1, and the current goes to zero before the time interval T_S. The waveform of the considered operation is shown in Figure 5b.

Mode 1($t_0 < t < t_1$):

The power switch is ON for this duration. Inductor L_1 starts to magnetize from zero value and reach the maximum at the end at time DT_S. This mode is the same as CCM Mode I. The governing relations in this mode are given by Equation (1):

Mode 2($t_1 < t < t_2$):

The power switch is OFF in this time interval. Inductor L_2 starts to demagnetize, and the current falls to zero at the end of the interval $\alpha_1 T_s$. The governing relations in this interval are given by Equation (2).

Mode 3($t_2 < t < T_S$):

The power switch is OFF. In this interval, the Inductor L_2 current is zero. The voltage across Inductor L_2 is zero. The equivalent circuit diagram is shown in Figure 7:

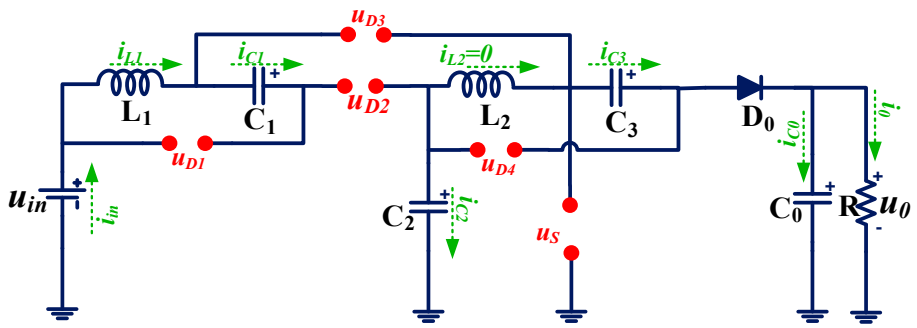


Figure 7. Mode 3 of Case II of DCM.

The average voltage across an inductor is zero, i.e., $\int_0^{T_s} u_L dt = 0$ in equilibrium. Therefore,

$$\begin{cases} u_{in}\alpha + (u_{in} + u_{C1} - u_{C2})(1-\alpha) = 0 \\ u_{C3}\alpha + (u_{C2} + u_{C3} - u_0)\alpha_1 = 0 \end{cases} \quad (14)$$

Using Equations (4) and (14), the voltage gain can be derived as

$$K_{dcm} = \frac{u_0}{u_{in}} = \frac{(\alpha + 2\alpha_1)(2-\alpha)}{\alpha_1(1-\alpha)} \tag{15}$$

Additionally, the value of α_1 can be calculated as below:

$$\frac{1}{2}\alpha_1 {i^{pk}}_{L2} = \langle i_0 \rangle \tag{16}$$

$${i^{pk}}_{L2} = \frac{u_{in}\alpha}{L_2 f_s} \; ; \; \langle i_0 \rangle = \frac{u_0}{R} \tag{17}$$

From (7), (8), and (9), the resulting quadratic equation has roots that give a voltage gain relation in the DCM mode of operation.

$${K^2}_{dcm} - \frac{2(2-\alpha)}{(1-\alpha)} K_{dcm} - \frac{2\left(\frac{2-\alpha}{1-\alpha}\right)^2}{\beta} = 0 \tag{18}$$

where $\beta = 2L_2/RT_S$ is defined as a normalized inductor time constant. The positive solution gives the required solution, i.e.,

$$K_{dcm} = \left(\frac{2-\alpha}{1-\alpha}\right)\left[1 + \sqrt{1 + \frac{\alpha^2}{\beta}}\right] \tag{19}$$

Boundary Condition Mode:

In Mode 2, the inductor current of L_2 becomes zero at the end of αT_S. This mode is termed a boundary condition mode (BCM). In this mode, the voltage gains of the CCM mode and DCM mode are equal, i.e.,

$$K_{dcm} = K_{ccm} = \left(\frac{2-\alpha}{1-\alpha}\right)^2 = \left(\frac{2-\alpha}{1-\alpha}\right)\left[1 + \sqrt{1 + \frac{\alpha^2}{\beta}}\right] \tag{20}$$

The following relation is yielded from (20):

$$\beta = \frac{\alpha(1-\alpha)^2}{(2-\alpha)} \tag{21}$$

The derived ${\beta^{L_2}}_{BCM}$ is defined as the normalized boundary inductor time constant for Inductor L_2. If $\beta > {\beta^{L_1}}_{BCM}$, the converter operates in the CCM mode; otherwise, the converter operates in the DCM mode, as shown in Figure 8b.

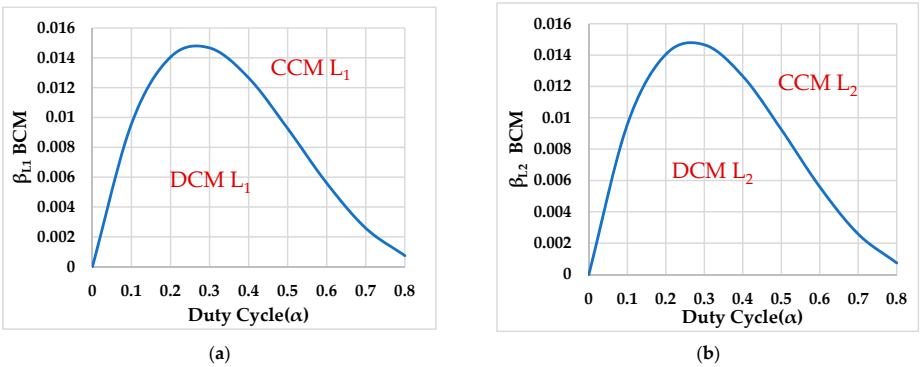


Figure 8. Boundary-normalized inductor time constants of (**a**) Inductor L_1 and (**b**) Inductor L_2 versus duty cycle.

2.3. Effect of ESR of Inductor on Voltage Gain

Parasitic resistance ESR r_L is considered. Inductor L in Figure 2 is replaced by this arrangement, as shown in Figure 9. The voltage across Inductor L can be determined in both modes as follows:

$$\text{Switch-ON mode} \Rightarrow \begin{cases} u_{L1} = u_{in} - i_{L1}r_{L1} \\ u_{L2} = u_{C2} - i_{L2}r_{L2} \end{cases} \quad (22)$$

$$\text{Switch-OFF mode} \Rightarrow \begin{cases} u_{L1} = u_{in} + u_{C1} - u_{C2} - i_{L1}r_{L1} \\ u_{L2} = u_{C2} + u_{C3} - u_0 - i_{L2}r_{L2} \end{cases} \quad (23)$$

The average value of voltage across the inductor is zero. Therefore, the following expressions are derived:

$$\begin{cases} u_{C2} = \frac{(2-\alpha)u_{in} - i_{L1}r_{L1}}{(1-\alpha)} \\ u_{C3} = \frac{(2-\alpha)u_{C2} - i_{L2}r_{L2}}{(1-\alpha)} \end{cases} \quad (24)$$

Therefore, the effect of ESR on voltage gain can be calculated using (24):

$$\left.\frac{V_0}{V_{in}}\right|_{r_{L1},rL2} = \frac{(2-\alpha/1-\alpha)^2}{\left(1 + \frac{(2-\alpha)^2}{(1-\alpha)^4}\frac{r_{L1}}{R} + \frac{(2-\alpha)}{(1-\alpha)^2}\frac{r_{L2}}{R}\right)} \quad (25)$$

If $r_{L1} = r_{L2} = r_L$, then

$$\left.\frac{V_0}{V_{in}}\right|_{r_{L1}=rL2} = \frac{(2-\alpha/1-\alpha)^2}{\left(1 + \frac{(2-\alpha)(3-3\alpha+\alpha^2)}{(1-\alpha)^4}\frac{r_L}{R}\right)} \quad (26)$$

The effect of ESR of inductors on voltage is shown in Figure 10.

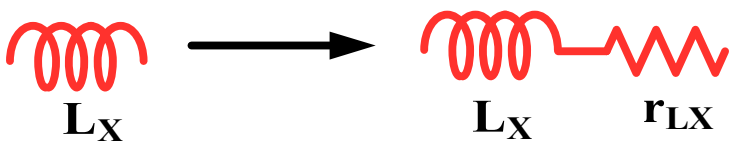


Figure 9. Non-ideal model of an inductor with ESR.

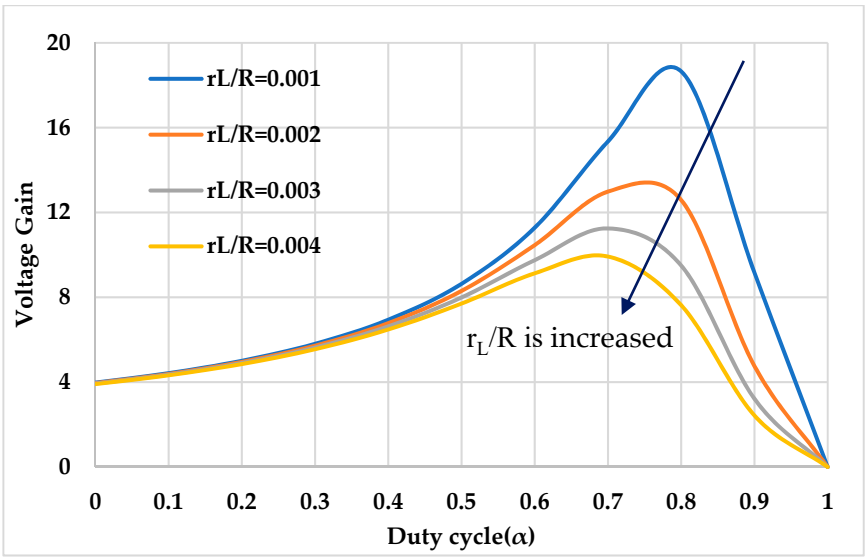


Figure 10. Effect of inductor resistance on voltage gain.

2.4. Current Stress of Components

If the converter is assumed loss-free, then

$$\begin{cases} P_{in} = P_{out} \\ u_{in}\langle i_{in}\rangle = u_0\langle i_0\rangle \\ \frac{\langle i_{in}\rangle}{\langle i_0\rangle} = \frac{u_0}{u_{in}} = K_{ccm} = \left(\frac{2-\alpha}{1-\alpha}\right)^2 \end{cases} \tag{27}$$

where $\langle i_x\rangle$ is the average current of any element of the proposed converter. According to the modes of operation of the proposed converter, $i_{C1_{on}}$, $i_{C0_{on}}$ are the capacitor currents when S is turned ON and $i_{C1_{off}}$, $i_{C0_{off}}$ are the capacitor currents when S is turned OFF. The current expressions are shown in (28).

$$\begin{cases} i_{C1_{on}} = i_{L1} - i_{D3} \\ i_{C0_{on}} = -\langle i_0\rangle \\ i_{C1_{off}} = i_{L1} \\ i_{C0_{off}} = i_{L2} - \langle i_0\rangle \end{cases} \tag{28}$$

Applying current–second balance on capacitor C_1 and C_0:

$$i_{C1_{on}}\alpha + i_{C1_{off}}(1-\alpha) = 0 \tag{29}$$

$$i_{C0_{on}}\alpha + i_{C0_{off}}(1-\alpha) = 0 \tag{30}$$

Using Equations (28)–(30), the average inductor currents $\langle i_{L1}\rangle$ and $\langle i_{L2}\rangle$ can be drawn out as

$$\begin{cases} \langle i_{L1}\rangle = \left(\frac{2-\alpha}{(1-\alpha)^2}\right)\langle i_0\rangle \\ \langle i_{L2}\rangle = \left(\frac{1}{1-\alpha}\right)\langle i_0\rangle \end{cases} \tag{31}$$

Likewise, applying current–second balance on capacitor C_2 and C_3, the average current through power diodes (D_0 to D_4) and power Switch (S) can be obtained as

$$\begin{cases} \langle i_{D1}\rangle = \langle i_{D2}\rangle = \left(\frac{2-\alpha}{1-\alpha}\right)\langle i_0\rangle \\ \langle i_{D3}\rangle = \left(\frac{2-\alpha}{(1-\alpha)^2}\right)\langle i_0\rangle, \ \langle i_{D4}\rangle = \langle i_{D0}\rangle = \langle i_0\rangle \\ \langle i_S\rangle = \left(\frac{3-2\alpha}{(1-\alpha)^2}\right)\langle i_0\rangle \end{cases} \tag{32}$$

3. Design of Circuit Components

Inductors are designed based on current ripple, and capacitors are designed based on voltage ripple.

(A) Inductor Design:

Using Equation (1), the value of inductors L_1 and L_2 can be extracted as follows:

$$\begin{cases} L_1 = \frac{u_{in}\alpha}{\Delta i_{L1} f_s} \\ L_2 = \frac{u_{in}(2-\alpha)\alpha}{(1-\alpha)\Delta i_{L2} f_s} \end{cases} \tag{33}$$

where Δi_{L1} and Δi_{L2} are the ripples in inductor currents L_1 and L_2, and fs is the switching frequency.

(B) Capacitor Design:

The capacitor value depends upon its charging current, the voltage ripple Δu_{Cx} across it, duty ratio, and switching frequency f_s.

Using Equation (7), we can obtain the value of C_0 and C_1 as follows:

$$C_0 = \frac{\alpha\langle i_0\rangle}{\Delta u_{C0} f_s}, \ C_1 = \frac{(2-\alpha)\langle i_0\rangle}{(1-\alpha)\Delta u_{C1} f_s} \tag{34}$$

Likewise, the rest capacitor value can be drawn out as

$$C_2 = \frac{\langle i_0 \rangle}{(1-\alpha)\Delta u_{C2} f_s}, \; C_3 = \frac{\langle i_0 \rangle}{\Delta u_{C3} f_s} \tag{35}$$

where Δu_{Cx} is the voltage ripple in capacitor voltage.

(C) Selection of Diodes and Switch:

The voltage across power diodes (D_0 to D_4) and the power Switch (S) are as follows:

$$u_{D0} = \begin{cases} \left(\frac{2-\alpha}{(1-\alpha)^2}\right) u_{in}, \; 0 < t < \alpha T_s \\ 0 \quad , \quad 0 < t < \alpha T_s \end{cases}, \tag{36}$$

$$u_{D1} = \begin{cases} 0, & 0 < t < \alpha T_s \\ \left(\frac{1}{1-\alpha}\right) u_{in}, & 0 < t < \alpha T_s \end{cases} \tag{37}$$

$$u_{D2} = \begin{cases} \left(\frac{1}{1-\alpha}\right) u_{in}, \; 0 < t < \alpha T_s \\ 0 \quad , \quad 0 < t < \alpha T_s \end{cases}, \tag{38}$$

$$u_{D3} = \begin{cases} 0, & 0 < t < \alpha T_s \\ \left(\frac{1}{(1-\alpha)^2}\right) u_{in}, & 0 < t < \alpha T_s \end{cases} \tag{39}$$

$$u_{D4} = \begin{cases} 0, & 0 < t < \alpha T_s \\ \left(\frac{2-\alpha}{(1-\alpha)^2}\right) u_{in}, & 0 < t < \alpha T_s \end{cases} \tag{40}$$

$$u_S = \begin{cases} 0, & 0 < t < \alpha T_s \\ \left(\frac{2-\alpha}{(1-\alpha)^2}\right) u_{in}, & 0 < t < \alpha T_s \end{cases} \tag{41}$$

where T_s is the switching period.

4. Power Loss Calculation in the Proposed Dual VL Converter

The equivalent circuit, including parasitic resistors, is also considered to analyze the proposed converter circuit. In a non-ideal equivalent circuit, all components are replaced with their parasitic resistances, as shown in Figure 11, where r_S is the switch on-resistance, r_D is the diode on-resistance, and uF is the diode's threshold voltage. The ESR of the inductor is taken as r_L. The ESR of the capacitor is taken as r_C. Assuming that the inductor current has no ripple. The power output is given as

$$P_0 = u_0 i_0 = \langle i_0 \rangle^2 R$$

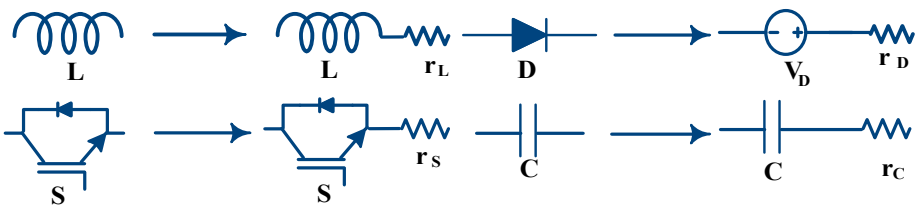


Figure 11. Equivalent non-ideal model of components.

(a) Switch Losses

The root mean square value of the current passing through the switch is $i_{S_{rms}}$, and $P_{S_{SW}}$ and $P_{S_{con}}$ are the switching loss and conduction loss of switch S.

$$\begin{cases} i_{S_{rms}} = \left(\frac{3-2\alpha}{(1-\alpha)^2\sqrt{\alpha}}\right)\langle i_0\rangle \\ P_{S_{con}} = {i_{S_{rms}}}^2 r_S = \left(\frac{(3-2\alpha)^2}{(1-\alpha)^4\alpha}\right)\langle i_0\rangle^2\, r_S = \left(\frac{(3-2\alpha)^2}{(1-\alpha)^4\alpha}\right)\frac{r_S}{R}P_0 \\ P_{S_{SW}} = \frac{1}{2T_S}(\langle i_s\rangle u_S)\,(t_r + t_f) \end{cases} \tag{42}$$

where the rising and falling times of S are given by t_r and t_f, respectively. Total loss by the switch is calculated as

$$P_{S_{total}} = P_{S_{con}} + P_{S_{SW}} \tag{43}$$

(b) Power losses in diodes

The root mean square current of the diode is notified by $i_{Dx_{rms}}$. The power loss due to ON resistance of diodes is P_{rDx} and $P_{u_{Fx}}$ is the loss due to forward voltage drop u_{Fx} of the diodes. Diode loss is calculated as

$$P_{Dx} = u_{Fx}\langle i_{Dx}\rangle + {i_{Dx_{rms}}}^2 r_{Dx} \tag{44}$$

$$\begin{cases} i_{D1_{rms}} = \frac{(2-\alpha)\langle i_0\rangle}{(1-\alpha)\sqrt{\alpha}} \\ P_{D1} = \left(\frac{2-\alpha}{1-\alpha}\right)u_{F1}\langle i_0\rangle + \left(\frac{(2-\alpha)^2}{\alpha(1-\alpha)^2}\right)\langle i_0\rangle^2 r_{D1} = \left(\frac{2-\alpha}{1-\alpha}\right)\frac{u_{F1}}{u_0}P_0 + \left(\frac{(2-\alpha)^2}{\alpha(1-\alpha)^2}\right)\frac{r_{D1}}{R}P_0 \\ i_{D2_{rms}} = \frac{(2-\alpha)\langle i_0\rangle}{\sqrt{(1-\alpha)^3}} \\ P_{D2} = \left(\frac{2-\alpha}{(1-\alpha)}\right)u_{F2}\langle i_0\rangle + \left(\frac{(2-\alpha)^2}{(1-\alpha)^3}\right)\langle i_0\rangle^2 r_{D2} = \left(\frac{2-\alpha}{1-\alpha}\right)\frac{u_{F2}}{u_0}P_0 + \left(\frac{2-\alpha}{(1-\alpha)^3}\right)\frac{r_{D2}}{R}P_0 \\ i_{D3_{rms}} = \frac{(2-\alpha)\langle i_0\rangle}{(1-\alpha)^2\sqrt{\alpha}} \\ P_{D3} = \left(\frac{2-\alpha}{(1-\alpha)^2}\right)u_{F3}\langle i_0\rangle + \left(\frac{(2-\alpha)^2}{\alpha(1-\alpha)^4}\right)\langle i_0\rangle^2 r_{D3} = \left(\frac{2-\alpha}{(1-\alpha)^2}\right)\frac{u_{F3}}{u_0}P_0 + \left(\frac{(2-\alpha)^2}{\alpha(1-\alpha)^4}\right)\frac{r_{D3}}{R}P_0 \\ i_{D4_{rms}} = \frac{\langle i_0\rangle}{\sqrt{\alpha}} \\ P_{D4} = u_{F4}\langle i_0\rangle + \left(\frac{1}{\alpha}\right)\langle i_0\rangle^2 r_{D4} = \frac{u_{F4}}{u_0}P_0 + \left(\frac{1}{\alpha}\right)\frac{r_{D4}}{R}P_0 \\ i_{D0_{rms}} = \frac{\langle i_0\rangle}{\sqrt{1-\alpha}} \\ P_{D0} = u_{F0}\langle i_0\rangle + \left(\frac{1}{1-\alpha}\right)\langle i_0\rangle^2 r_{D4} = \frac{u_{F4}}{u_0}P_0 + \left(\frac{1}{1-\alpha}\right)\frac{r_{D4}}{R}P_0 \end{cases} \tag{45}$$

Total diode loss can be drawn out as follows:

$$P_{D_{total}} = \sum_{i=0}^{4} P_{Di} \tag{46}$$

(c) Power loss in inductors due to ESRs

The root mean square current of the diode is notified by $i_{Lx_{rms}}$. The power loss due to ESRs and the r_{Lx} of the inductor is P_{Lx}.

$$\begin{cases} i_{L1_{rms}} = \left(\frac{2-\alpha}{(1-\alpha)^2}\right)\langle i_0\rangle, \quad i_{L2_{rms}} = \left(\frac{1}{1-\alpha}\right)\langle i_0\rangle \\ P_{L1} = {i_{L1_{rms}}}^2 r_{L1} = \left(\frac{(2-\alpha)^2}{(1-\alpha)^4}\right)\langle i_0\rangle^2 r_{L1} = \left(\frac{(2-\alpha)^2}{(1-\alpha)^4}\right)\frac{r_{L1}}{R}P_0 \\ P_{L2} = {i_{L2_{rms}}}^2 r_{L2} = \left(\frac{1}{1-\alpha}\right)^2\langle i_0\rangle^2 r_{L2} = \left(\frac{1}{1-\alpha}\right)^2\frac{r_{L2}}{R}P_0 \end{cases} \tag{47}$$

Total loss due to ESR of inductors can be obtained as

$$P_{L_{total}} = \sum_{i=1}^{2} P_{Li} \tag{48}$$

(d) Power losses in capacitors

The root mean square current of the diode is denoted by $i_{Cx_{rms}}$. The power loss due to the ESRs and r_{Cx} of the inductor is P_{Cx}.

$$\begin{cases} i_{C1_{rms}} = \frac{(2-\alpha)\langle i_0\rangle}{\sqrt{\alpha}\sqrt{(1-\alpha)^3}}, i_{C2_{rms}} = \frac{\langle i_0\rangle}{\sqrt{\alpha}\sqrt{(1-\alpha)^3}} \\ i_{C3_{rms}} = \frac{\langle i_0\rangle}{\sqrt{\alpha}\sqrt{(1-\alpha)}}, i_{C0_{rms}} = \frac{\sqrt{\alpha}\langle i_0\rangle}{\sqrt{(1-\alpha)}} \\ P_{C1} = {i_{C1_{rms}}}^2 r_{C1} = \left(\frac{(2-\alpha)^2}{\alpha(1-\alpha)^3}\right)\langle i_0\rangle^2 r_{C1} = \left(\frac{(2-\alpha)^2}{\alpha(1-\alpha)^3}\right)\frac{r_{C1}}{R}P_0 \\ P_{C2} = {i_{C2_{rms}}}^2 r_{C2} = \left(\frac{1}{\alpha(1-\alpha)^3}\right)\langle i_0\rangle^2 r_{C2} = \left(\frac{1}{\alpha(1-\alpha)^3}\right)\frac{r_{C2}}{R}P_0 \\ P_{C3} = {i_{C3_{rms}}}^2 r_{C3} = \left(\frac{1}{\alpha(1-\alpha)}\right)\langle i_0\rangle^2 r_{C3} = \left(\frac{1}{\alpha(1-\alpha)}\right)\frac{r_{C3}}{R}P_0 \\ P_{C0} = {i_{C0_{rms}}}^2 r_{C0} = \left(\frac{\alpha}{(1-\alpha)}\right)\langle i_0\rangle^2 r_{C0} = \left(\frac{\alpha}{(1-\alpha)}\right)\frac{r_{C0}}{R}P_0 \end{cases} \quad (49)$$

For all capacitors, the loss can be calculated as

$$P_{C_{total}} = \sum_{i=0}^{3} P_{Ci} \quad (50)$$

The expression for the efficiency of the proposed converter circuit can be obtained from Equations (43), (46), (48) and (50) as

$$\eta = \frac{P_0}{P_0 + P_{S_{total}} + P_{D_{total}} + P_{L_{total}} + P_{C_{total}}} \quad (51)$$

5. Comparative Study

A detailed analysis of the proposed converter with similar non-isolated structures is carried out in this section. The comparison is based on voltage gain, voltage stress, and the number of components in the converters, as listed in Table 1. Voltage gain is an important index to determine the performance of the converter. The voltage gain curve is shown in Figure 12. The proposed converter can achieve the highest voltage gain till duty ratio (α) of 0.6 after $\alpha > 0.6$; topologies two and eight are greater than the proposed converter. Topology nine uses coupled inductors to boost the voltage gain up to eight times (not shown in Figures 12 and 13) because of the isolated category of DC-DC converters but has the maximum number of components compared to other converters listed in Table 1.

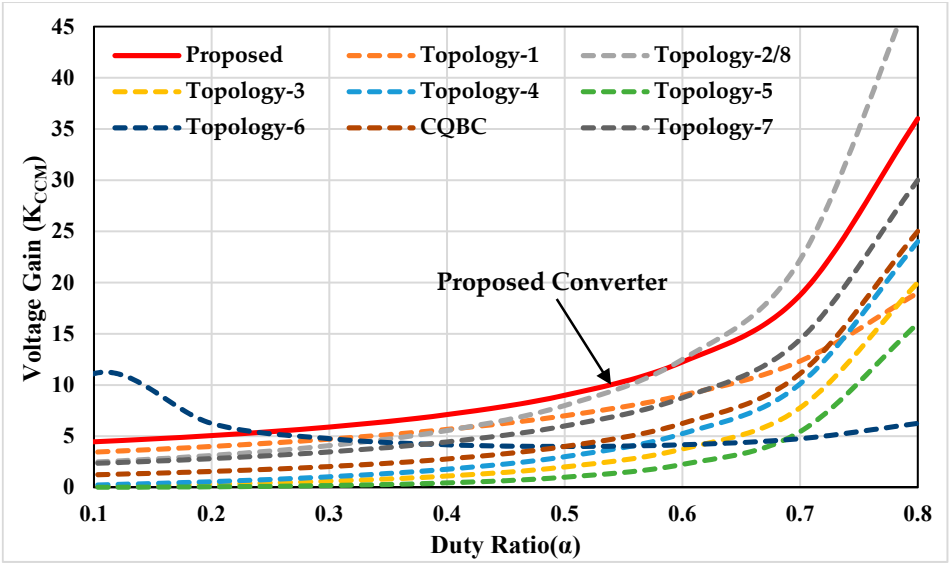


Figure 12. Voltage gain curve of the different topologies listed in Table 1.

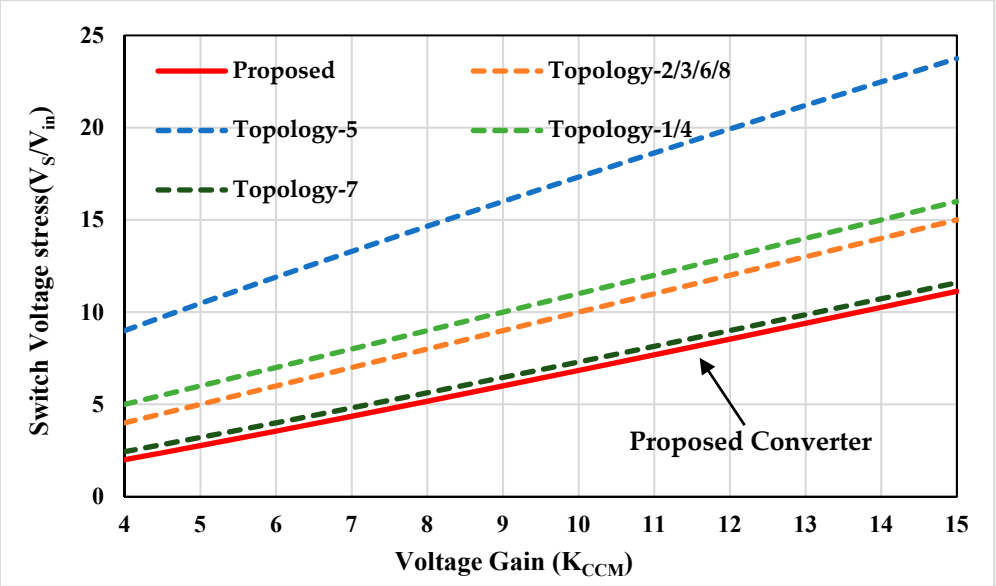


Figure 13. Normalized switch voltage stress curve of the different topologies listed in Table 1.

Table 1. Comparison with similar non-isolated converters.

Converter	N_L	N_S	N_D	N_C	Voltage Gain (K_{ccm})	Voltage Stress (V_S/V_{in})	Continuous Input Current	Common Ground
Topology 1	2	1	5	4	$\frac{3+\alpha}{1-\alpha}$	$\frac{4}{1-\alpha}$	No	No
Topology 2	3	1	5	3	$\frac{2}{(1-\alpha)^2}$	$\frac{2}{(1-\alpha)^2}$	Yes	Yes
Topology 3	3	1	3	3	$\frac{\alpha}{(1-\alpha)^2}$	$\frac{\alpha}{(1-\alpha)^2}$	Yes	Yes
Topology 4	2	1	3	2	$\frac{\alpha(2-\alpha)}{(1-\alpha)^2}$	$\frac{1}{(1-\alpha)^2}$	No	Yes
Topology 5	3	1	5	3	$\frac{\alpha^2}{(1-\alpha)^2}$	$\frac{1}{(1-\alpha)^2}$	Yes	Yes
Topology 6	2	2	3	2	$\frac{1}{\alpha(1-\alpha)}$	$\frac{1}{1-\alpha}$	Yes	Yes
Topology 7	2	1	4	3	$\frac{2-\alpha}{(1-\alpha)^2}$	$\frac{1}{(1-\alpha)^2}$	Yes	Yes
Topology 8	3	1	5	3	$\frac{2}{(1-\alpha)^2}$	$\frac{2}{(1-\alpha)^2}$	Yes	Yes
Topology 9	2	2	7	6	$\frac{8}{1-\alpha}$	$\frac{1}{1-\alpha}$	Yes	No
TQBC	2	1	3	2	$\frac{1}{(1-\alpha)^2}$	$\frac{1}{(1-\alpha)^2}$	Yes	Yes
Proposed Converter	2	1	5	3	$\frac{(2-\alpha)^2}{(1-\alpha)^2}$	$\frac{2-\alpha}{(1-\alpha)^2}$	Yes	Yes

N_L: number of inductors, Ns: number of switches, N_D: number of diodes, N_C: number of capacitors, topology 1: A. A. Fardoun et al., topology 2: Javed et al., topology 3: Maroti et al., topology 4: Gorji et al., topology 5: Zhang et al., topology-6: F. M. Shahir et al., topology 7: Manxin et al., topology 8: Rezaie et al., topology 9: M.L. Alghaythi et al.

The component counts of the proposed converter are less than topologies 1, 2, 5, and 8. Another important criterion is the voltage stress on the semiconductor devices. For this, a plot of normalized switch voltage stresses against the voltage gain of the proposed converter is shown in Figure 13. The proposed converter has the least voltage stress on the switch, which is less than the output voltage. Topologies two and eight have higher voltage gain, but they have greater voltage stress than the proposed converter. Moreover, topologies two and eight both have a greater number of components than the proposed converter. Topologies 2, 3, 6, and 8 have voltage stress equal to the output voltage. The high voltage stress on the devices increases the chance of the failure of the devices, so devices with a higher rating will be required. The components with the higher rating will have

increased costs and will deteriorate the efficiency of the converter due to high power loss. Topology 1 and topology 9 have a non-common ground structure, while other topologies, including the proposed converter, have a common ground structure.

The proposed topology can achieve higher gain with low stress on the components. The components with lower ratings will have low ON resistance, which will improve the overall efficiency of the converter. Moreover, the converter utilizes a single switch, so control is easy. The interleaved converter, presented in topology 9, utilizes two switches with a 180-degree phase difference. Further, the use of the coupled inductor makes the circuit complex. The proposed converter also provides a common ground structure between input and output, which mitigates electromagnetic interference problems. The volume of components is mainly decided by the magnetic components in the converter; the proposed converter uses only two inductors such as TQBC, so volume is low as compared to topologies 2, 3, 5, and 8 which utilizes three inductors. The use of more inductors makes the circuit bulkier.

6. Simulation Results at α = 0.4

In this section, simulation results of the proposed converter are discussed. The parameter values taken for simulation are presented in Table 2. The simulation is carried out at an input voltage of 36 volts at a frequency of 50 kHz. Equivalent series resistance (ESR) of inductors and capacitors is also considered for the simulation on Piecewise Linear Electrical Circuit Simulation (PLECS) software. The duty cycle is maintained at 0.4. Figure 14 shows the output voltage results of the proposed converter. The output voltage is obtained is 256 V, which is more than seven times the input voltage. The deviation obtained is due to a parasitic resistance drop in the proposed converter. The average current of inductors of L_1 and L_2 are 3.7 Ampere and 1.4 Ampere, as shown in Figure 15. In the same figure, the ripple observed in the inductor current is very low, with a fixed duty ratio of 0.4. When the switch is OFF, it blocks the positive voltage equal to 159 V which is 62% of the V_o in Figure 16. In the same figure, the average capacitor voltage V_{C3} is 96 V. Figure 17 presents the capacitor voltages of C_1 and C_2, equal to 36 V and 96 V, respectively. The simulation results obtained by using parameters mentioned in Table 2 are in agreement with the theoretical results. It is to be mentioned that the converter is operated in the CCM mode.

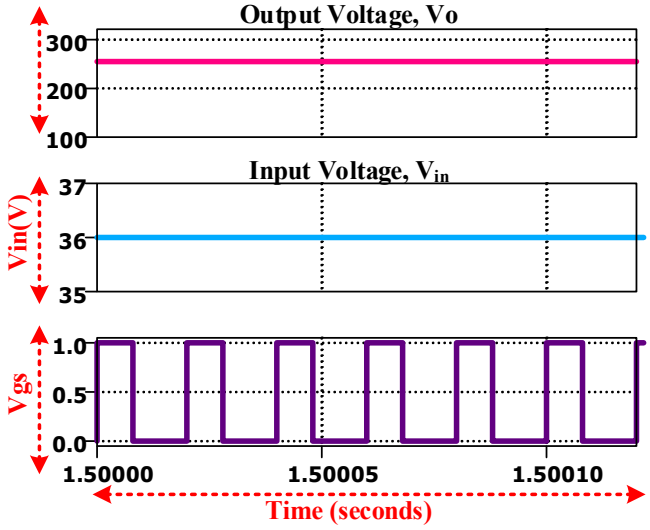


Figure 14. Simulated output voltage (V_O), input voltage (V_{in}), and duty cycle (α).

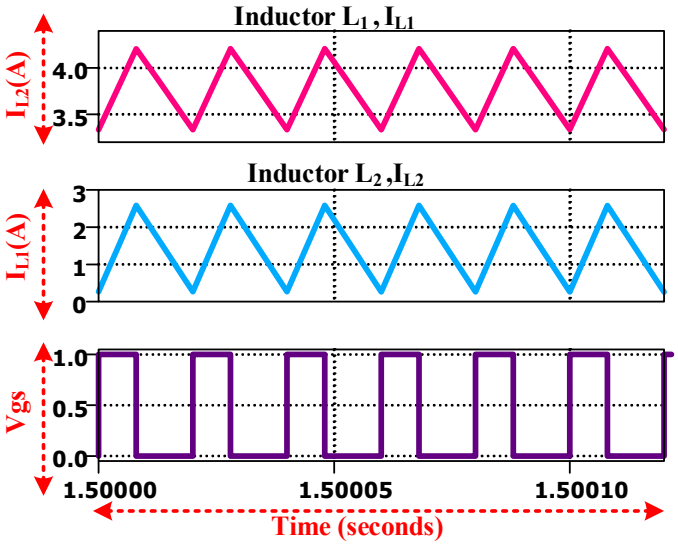


Figure 15. Simulated inductor current I_{L1}, I_{L2} and duty cycle (α).

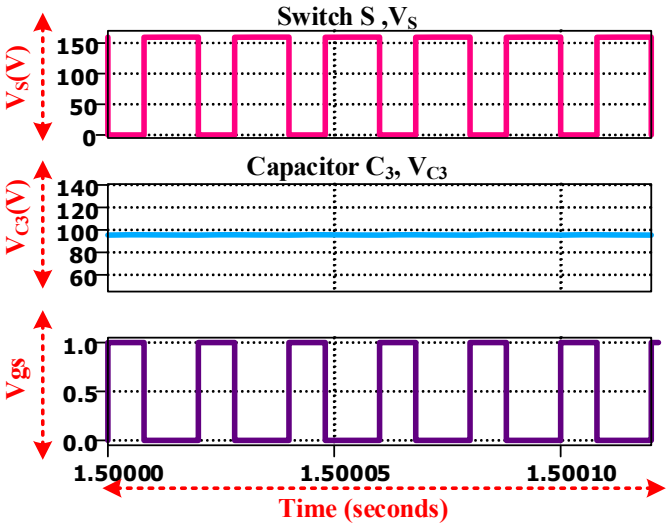


Figure 16. Simulated switch voltage stress (V_S), capacitor (C_3) voltage, and duty cycle (α).

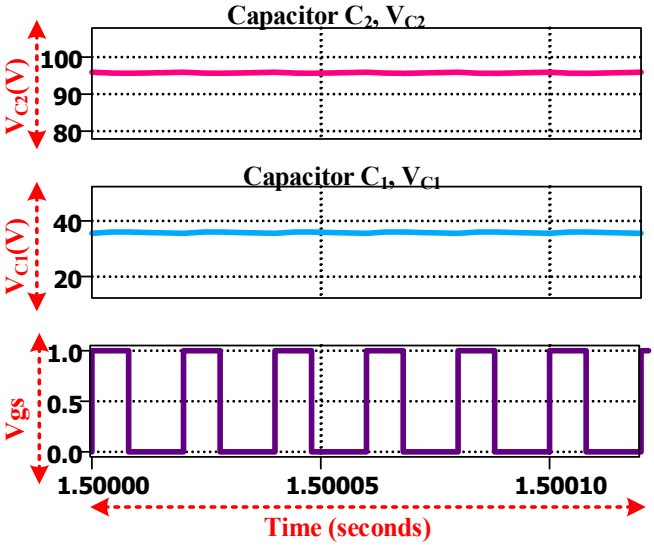


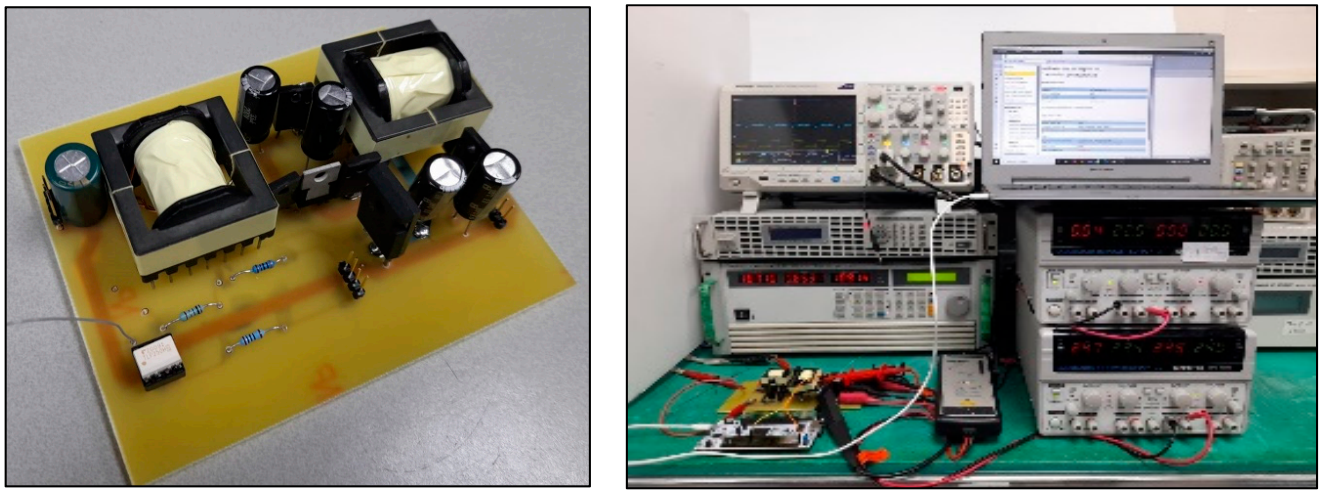
Figure 17. Simulated capacitor (C_2) voltage, capacitor (C_1) voltage, and duty cycle (α).

Table 2. Simulation parameters.

Parameters	Value
Input Voltage (V_{in})	36 V
Duty Cycle (α)	0.4
Frequency (f_S)	50 kHz
Inductor (L_1, L_2)	330 µH, ESR = 0.92 Ω
Capacitors (C_1, C_2, C_3, andC_0)	33 µF(each), ESR = 0.25 Ω
Power MOSFET	SPW52N50C3, 0.07 Ω
Diodes	SF8L60USM
Load Resistance	R = 300 Ω

7. Experimental Verification at α = 0.4

To verify the operating principles and boost the capability of the proposed converter, a hardware prototype of 200 W is developed and tested under laboratory conditions. The hardware prototype is shown in Figure 18a and the hardware setup in Figure 18b. The experimental waveforms are presented and demonstrated in this section.



(**a**) (**b**)

Figure 18. (**a**) Hardware prototype developed in the lab. (**b**) Hardware setup of the proposed converter.

The hardware parameters are the same as the simulation parameters given in Table 3. The DC input supply is taken to be 10 V for the CCM mode operation of the proposed hardware prototype. The experimental gate pulse for the power MOSFET (SPW52N50C3) is 40 per cent. Figure 19 captures the input (V_{in}) and output voltages (V_o) of the experimental prototype. The output voltage (V_O) obtained is 70 volts, where V_{gs} is the gate drive signal. When the MOSFET is ON, inductors L_1 and L_2 magnetize and the current through the inductors (I_{L1} and I_{L2}) increases linearly. I_{L1} increases from 0.15 Ampere to a peak value of 0.7 Ampere, whereas I_{L2} increases from 1.0 Ampere to a peak value of 1.2 Ampere. The average current of inductors of L_1 and L_2 are 1.04 Ampere and 0.4 Ampere, as shown in Figure 20. During the OFF state, the voltage across the switch is 40 V, which is less than V_O, as shown in Figure 21. The capacitor voltages V_{C1}, V_{C2}, and V_{C3} are 10 V, 26 V, and 26 V, respectively, captured in Figures 20 and 21 with very low voltage ripple.

Table 3. Hardware specification of the proposed converter.

Elements	Specification
Input Power	200 W
Input Voltage	10 V
Switching Frequency	50 kHz
Load Resistance	R = 300 Ω, Chroma electronic load simulator model 63,202
Inductors	$L_1 = L_2$ = 330 µH, ESR = 0.92 Ω
Capacitors	$C_1 = C_2 = C_3 = C_O$ = 33 µF 200 V 0.25 Ω,
Power MOSFET	SPW52N50C3, 0.07 Ω
Diodes	SF8L60USM
Gate Drivers IC	TLP250H
Microcontroller	STM32 Nucleo H743ZI2

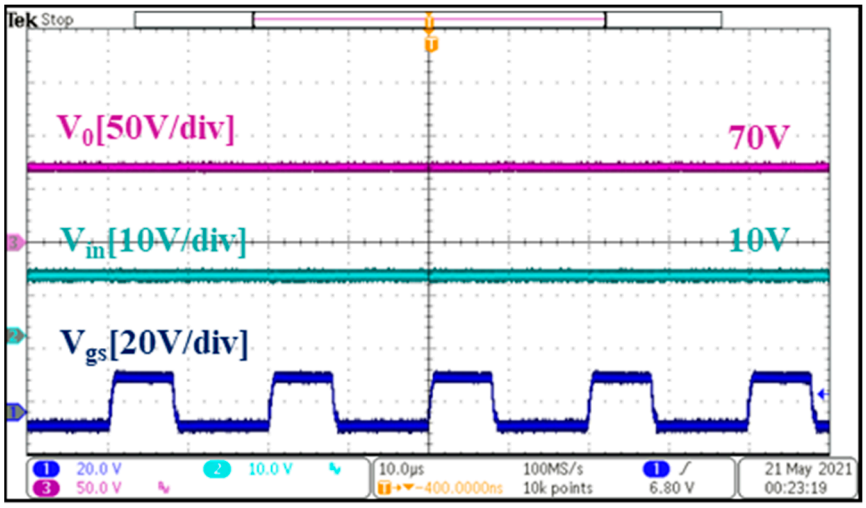


Figure 19. Top to bottom: experimental output waveforms (V_O), input voltage (V_{in}), and gate pulse (V_{gs}).

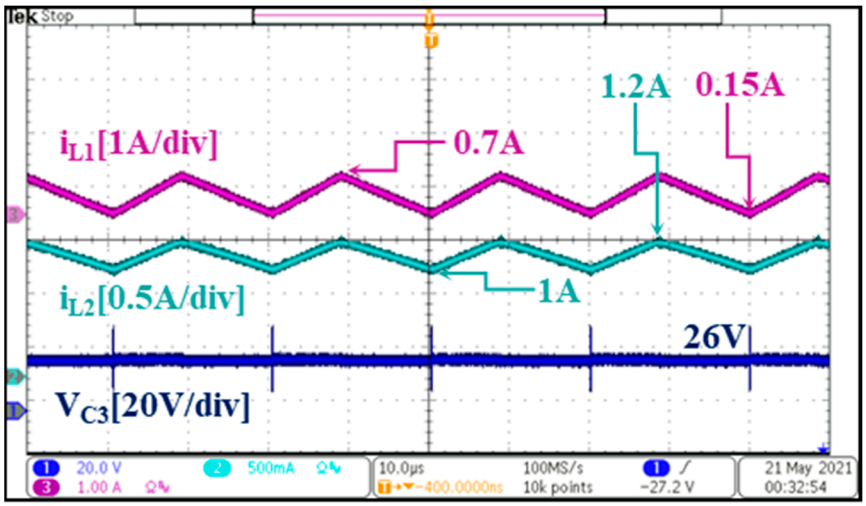


Figure 20. Top to bottom: experimental inductor current L_1 waveforms (I_{L1}), inductor current L_1 waveforms (I_{L2}), and capacitor C_3 voltage (V_{C3}).

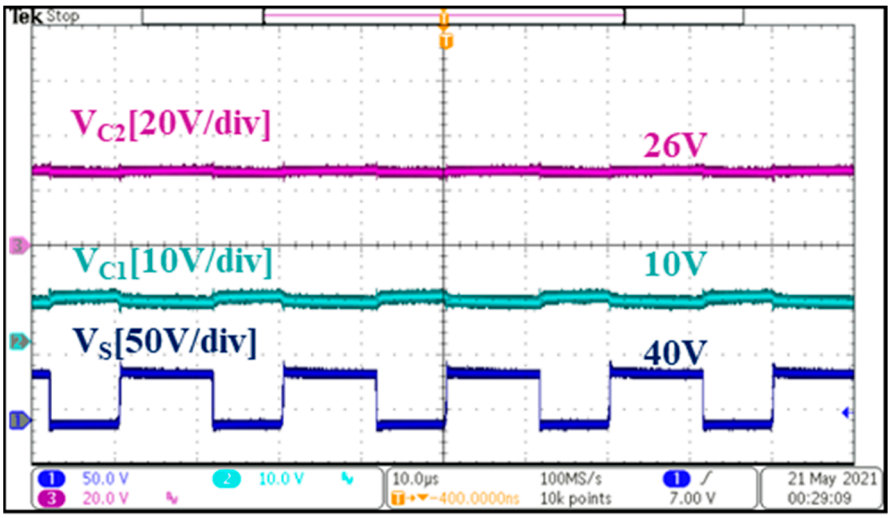


Figure 21. Top to bottom: experimental capacitor C_2 voltage (V_{C2}), capacitor C_1 voltage (V_{C1}), and the voltage waveform of Switch (S).

The closed-loop performance of the converter is illustrated in Figures 22 and 23. The output voltage V_o is regulated at 45 V when the input voltage is varied from 10 volts to 14 V to 8 V. Similarly, when the load resistance is changed the output voltage should be held constant by the PI controller. As the load is changed from 300 Ω to 800 Ω, the output voltage is held constant at the set reference value of 60 V, as shown in Figure 24. It shows that the PI controller is working satisfactorily. The values of proportional constant (K_p) and integral constant (K_i) for the PI controller are set to be 0.05 and 0.01 respectively. TMS320F28335 controller is used for implementation of closed-loop control.

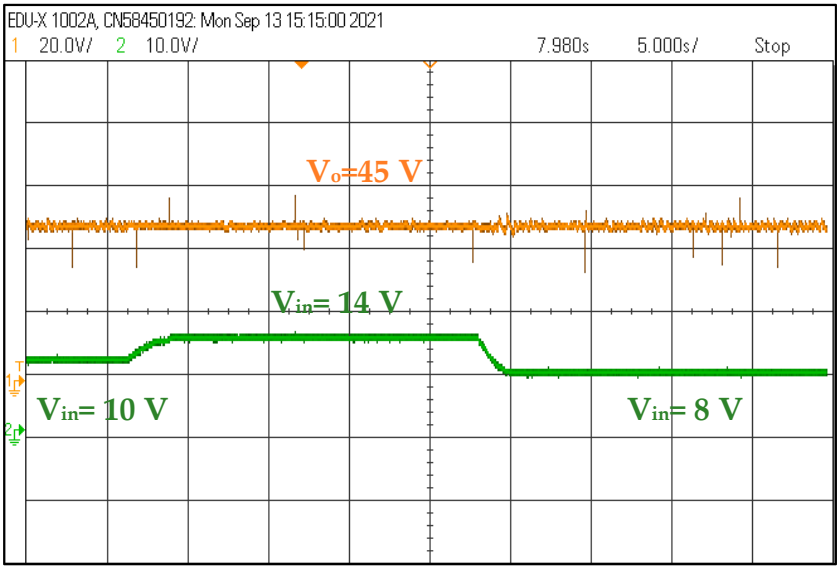


Figure 22. Output Voltage with change in input from 10 volts to 14 volts to 8 volts.

The efficiency at different power levels is shown in Figure 24. It can be seen from the plot that for a constant output power as the voltage increased from 10 V to 20 V, the efficiency of the converter increased. This is because to achieve the same power level, the current decreases with the increase in output voltage. As a result, the conduction losses in the converter decreases and efficiency increases. The percentage losses in the components as calculated from the PLECS software by incorporating the real loss values from the datasheet of different component. 47% of the total loss, occurs in diodes, as shown

in Figure 25. The switch losses are around 19%. Losses in the inductors and capacitors are found to be 20% and 14% respectively. The diode losses can be reduced by the selection of diodes with a low value of parasitic resistances. The capacitor ESR depends on the frequency and hence capacitor losses increase with an increase in frequency.

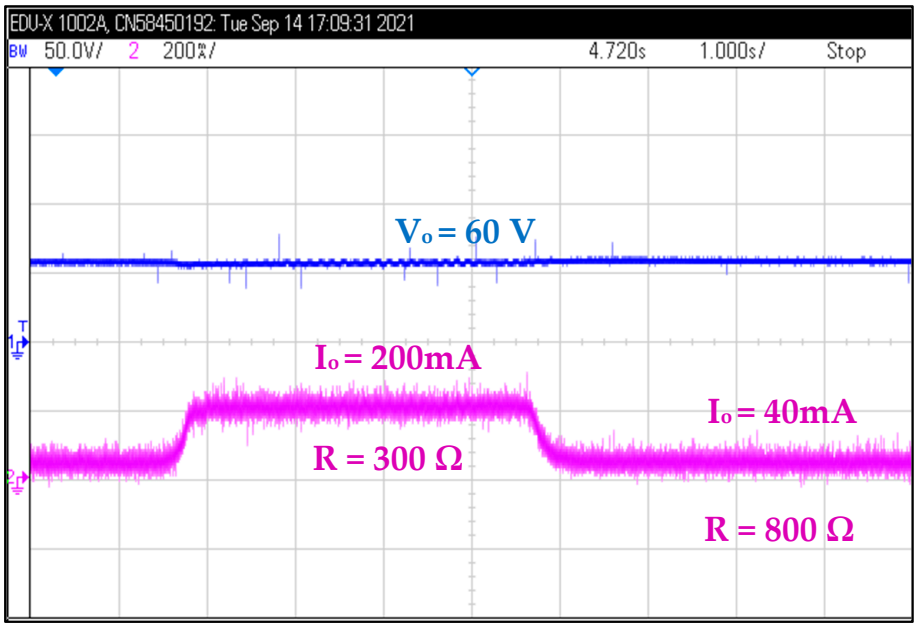


Figure 23. Output Voltage with change in the load from 300 ohms to 800 ohms.

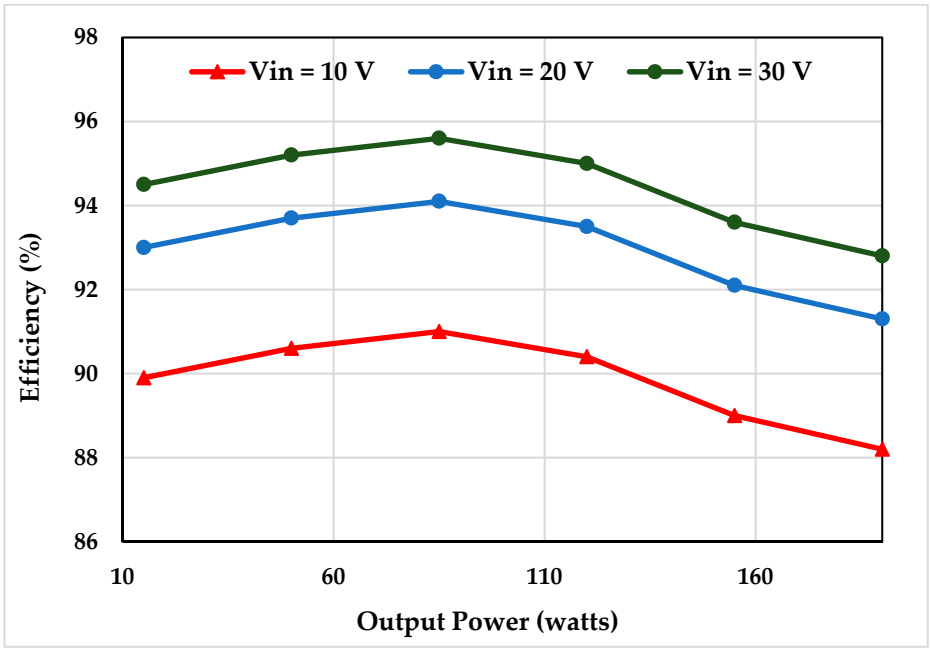


Figure 24. Experimental efficiency at various power levels.

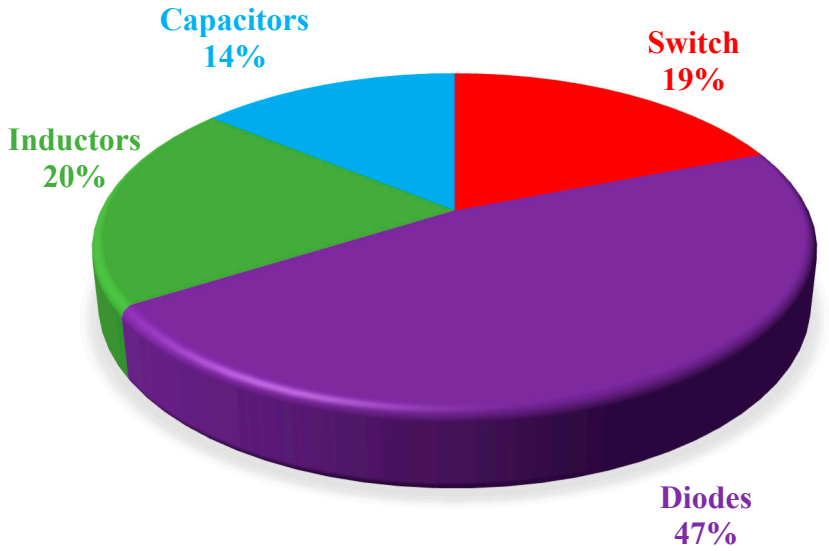


Figure 25. Power loss bifurcation of various components.

8. Discussion and Conclusions

The proposed converter can achieve a voltage gain of more than 10 times at a duty ratio of 0.6. The topology has a common ground structure with a single switch, so control is very easy with a reduced number of components. Due to parasitic resistances of components, the voltage gain of the proposed converter is severely affected at higher duty ratios. The total number of the elements in the proposed converter is less than the other converters for the same value of voltage gain. The maximum efficiency obtained was 94% at an input voltage of 20 V. The converter performance is found to be good in a closed-loop situation also with the PI controller. The PI controller is tuned to maintain a constant output voltage when the load or the input voltage changes. The converter is suitable for renewable energy applications for medium power applications due to the presence of continuous input current and common ground between the input and the output sides.

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