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Real-Time Implementation of an Optimized Model Predictive Control for a 9-Level CSC Inverter in Grid-Connected Mode

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Abstract: The Crossover Switches Cell (CSC) is a recent Single DC-Source Multilevel Inverter (SDCS-MLI) topology with boosting abilities. In grid-connected PV applications, the CSC should be controlled to inject a sinusoidal current to the grid with low THD% and unity power factor, while balancing the capacitor voltage around its reference. These two objectives can be met through the application of a finite control set model predictive control (FCS-MPC) method. Thus, this paper proposes a design of an optimized FCS-MPC for a 9-level grid-tied CSC inverter. The switching actions are optimized using the redundant switching states. The design is verified through simulations and real-time implementation. The presented results show that the THD% of the grid current is 1.73%, and the capacitor voltage is maintained around its reference with less than 0.5 V mean error. To test the reliability of the control design, different scenarios were applied, including variations in the control reference values as well as the AC grid voltage. The presented results prove the good performance of the designed controller in tracking the reference values and minimizing the steady-state errors.

Keywords: crossover switches cell; CSC; multilevel inverter; Packed-U-Cell; model predictive control; grid connection

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1. Introduction

The capacity of global renewable energy (RE) has witnessed an increase of 261 GW in 2020, which leads to 2799 GW of the total global RE capacity, where PV systems dominate, with around 25.3% of this total capacity [1]. In order to connect the PV strings to the utility grid, the DC output of the PV modules should be converted to AC, which is the function of the inverters stage. Several research works reviewed the inverter technologies for PV applications [2–5].

In the literature, it has been reported that multilevel inverters (MLIs) ensure a higher power quality compared to conventional 2-level inverters, which make them a good candidate for RE applications [5]. In various MLI topologies, the design mainly consists of the use of DC voltage sources, capacitors, and medium power semiconductor devices that operate at a reduced voltage rating. These topologies, which generate multiple DC voltage levels at the output terminals, have several advantages compared to the conventional two-level inverters such as lower switching losses, lower voltage stress on the power semiconductor devices, reduced electromagnetic interference, higher efficiency, and lower harmonic pollution and filter size [6–8]. On the other hand, the complexity of the inverter's design increases and the overall reliability of the system decreases with the increase in the number of levels. That is because each switch used in the design requires a related gate driver and a protection circuit. As a result, the increase in the power semiconductor

switches in the design leads to increases in the system's cost and the control complexity [8,9]. Moreover, using multiple DC sources in MLIs topologies raises concerns regarding the increase in the power losses and malfunctioning in the system due to the unbalanced power sharing among the isolated DC sources [10]. In PV systems, the increase in the required DC sources implies an excessive number of DC-DC converters.

Therefore, interest is increasing in the reduced switches MLIs and in single DC sources MLIs (SDCS-MLIs) [11]. One of the recently developed SDC-MLIs is the Packed U cells (PUC) topology, which is classified as an asymmetric Flying Capacitors inverter (FCI) that could be used as a compromise between the cascaded H-bridges and the flying capacitor topologies [12,13]. The PUC MLI generates more voltage levels with high-power quality, while using a lower number of passive/active components and DC sources (single DC source) compared to other MLI topologies. These PUC-MLI features result in cost reductions and a smaller compact power conversion unit compared to even 2-level topologies. However, the maximum voltage level generated by PUC-MLI equals the DC source voltage which limits its employment to low power applications and makes it unsuitable for applications that require an output voltage greater than the input DC source. Furthermore, the topology provides the capacitor with one path for charging. Hence, problems may occur if there is a lack of energy and a long interval between the discharging and charging states [14].

These limitations are overcome by modifying the PUC MLI to have two crossover switches between the DC link and the capacitor; the new topology is called the Crossover Switches Cell (CSC) [14]. This modification provides another way of charging the capacitor and increases the number of levels from seven levels in PUC to nine levels in CSC. The maximum voltage level is the sum of the DC source and the capacitor's voltage; CSC has a boosting ability.

Voltage/current controllers are required in MLIs to deliver green energy/power from the source to the load/grid. Control schemes with modulators such as sinusoidal pulse width modulation (SPWM) and space vector (SVPWM) are commonly used with MLIs in general and in PV applications [15–17]. These methods are compatible with high switching frequencies. SPWM is easy to implement and does not require any optimization technique. SVPWM generates low current ripples and is easy to implement, while its complexity increases with the number of levels [6,18]. Space vector control is a fundamental frequency method that is effective for a high number of levels cases, but the lower-order harmonic components cannot be eliminated [6,7]. The selective harmonic elimination method generates signals with a low total harmonic distortion (THD%) and is suitable for high-power applications, but suffers with offline calculations. Additionally, adaptive controllers, sliding mode controllers, artificial intelligent controllers and Fuzzy logic controllers are designed for MLIs in the PV systems [19–22].

Model predictive control (MPC) schemes are based on the predicted states obtained by systems' model. MPC was applied effectively in systems with MLIs and in PV applications [23–28]. One of the main advantages of MPC is that the control action is applied directly to the system, without the need for a modulation stage [29]. Furthermore, MPC is a multi-objective control technique; several objectives can be designed in its cost function by specifying their priorities according to the application. This makes MPC a good candidate for MLIs in PV systems where the capacitors' voltage needs to be regulated according to their references in order to generate the required voltage levels and maintain a low THD% in the current that is fed to the grid.

In this paper, a finite control set MPC (FCS-MPC) is proposed for a nine-level, single phase, grid-connected CSC-MLI. The objective of the controller is to generate a synchronized grid current with a minimized THD%, while maintaining the capacitor voltage at around its reference value. The topology and the switching patterns of the CSC inverter are described in detail. Then, the mathematical model of the system and the control design steps are explained. The proposed controller is verified through simulation and real-time

implementation and the results are shown and discussed to prove the acceptable dynamic performance of the designed controller.

2. CSC Topology and Mathematical Modelling

2.1. CSC Topology

The studied nine-level CSC-inverter is shown in Figure 1. The topology consists of a DC voltage source (representing the the output of the DC-DC converter fed by the solar panels in PV applications), a capacitor, and eight switches (S_i, $i = 1 \ldots 8$), where two of them are bidirectional (S_2 and S_5). The switches between the DC link and the positive output terminal of the inverter, S_1 and S_4, work in a complementary manner, in which one of them is ON at a time. The same concept applies to the switches between the capacitor link and the negative output terminal of the inverter, S_3 and S_6. The four switches between the DC link and the capacitor link also work in a complementary way. All the valid switching patterns are presented in Table 1, where $s_i \in \{0, 1\}$ represents the switching state of the switch S_i. In order to have nine DC levels at the output terminal of the inverter, the capacitor voltage (V_2) is maintained at one third of the DC link voltage (V_1). Table 1 shows the V_{AB} value when V_1 is set to 150 V and V_2 is set to 50 V. It is clear that the maximum and minimum output voltage will be $\pm$200 V. Hence, CSC inverter has a boosting ability.

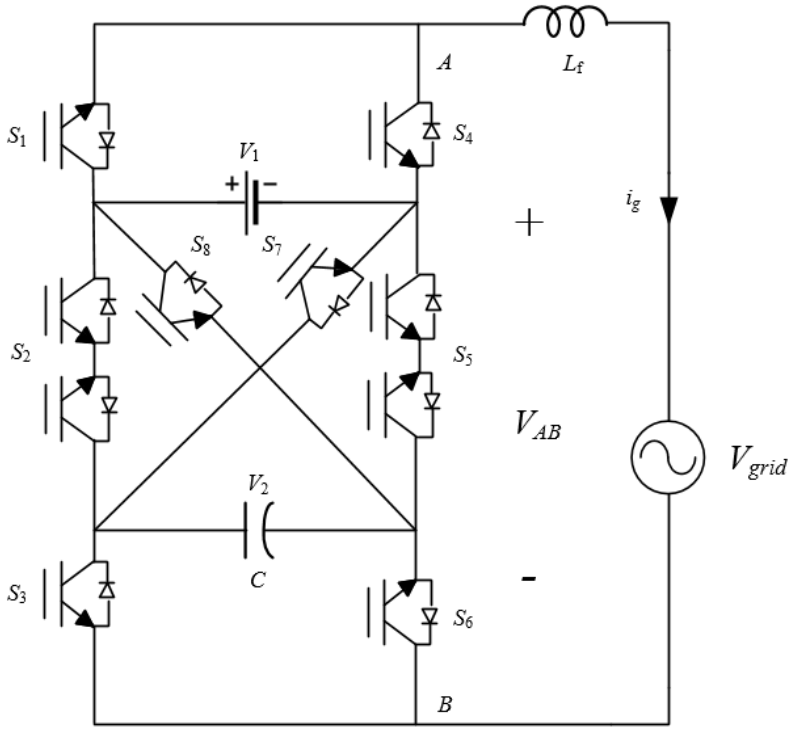

Figure 1. The Crossover Switches Cell (CSC) Inverter Topology.

2.2. Modelling

Given that C is the CSC capacitor, L_f is the filtering inductor. By using Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) on the topology shown in Figure 1, the model state equations can be written as:

$$\dot{V}_2(t) = \frac{1}{C}(s_3 - s_2 - s_7) i_g(t) \quad (1)$$

$$\dot{i}_g(t) = \frac{1}{L_f}(V_{AB}(t) - V_g(t)) \quad (2)$$

where $\dot{V}_2(t) = \frac{dV_2}{dt}$, $\dot{i}_g(t) = \frac{di_g}{dt}$,

$$V_{AB}(t) = (s_1 - s_2 - s_8)V_1(t) + (s_2 - s_3 + s_7)V_2(t), \quad (3)$$

$V_1(t)$ is the DC voltage and $V_2(t)$ is the capacitor voltage.

Table 1. Switching states and the corresponding output voltage level of the CSC inverter.

s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	V_{AB}	V_{AB} (V)	Cell Capacitor
1	0	0	0	0	1	1	0	$V_1 + V_2$	200	Charged
1	0	0	0	1	1	0	0	V_1	150	Bypassed
1	0	1	0	0	0	1	0	V_1	150	Bypassed
1	0	1	0	1	0	0	0	$V_1 - V_2$	100	Discharged
0	0	0	1	0	1	1	0	V_2	50	Charged
1	1	0	0	0	1	0	0	V_2	50	Charged
0	0	1	1	0	0	1	0	0	0	Bypassed
1	1	1	0	0	0	0	0	0	0	Bypassed
0	0	0	1	1	1	0	0	0	0	Bypassed
1	0	0	0	0	1	0	1	0	0	Bypassed
0	0	1	1	1	0	0	0	$-V_2$	−50	Discharged
1	0	1	0	0	0	0	1	$-V_2$	−50	Discharged
0	1	0	1	0	1	0	0	$-V_1 + V_2$	−100	Charged
0	0	0	1	0	1	0	1	$-V_1$	−150	Bypassed
0	1	1	1	0	0	0	0	$-V_1$	−150	Bypassed
0	0	1	1	0	0	0	1	$-V_1 - V_2$	−200	Discharged

3. Control Scheme

MPC is divided into three steps: Predicting the model, calculating the cost function and minimizing the cost function. The details of the control scheme are given in Figure 2.

Prediction of the model's state equations step depends on the discrete version of the state equations, in which the (k + 1) state is predicted from the (k) state. Since the state variables' trajectory is assumed to be rectlinear over a small sampling time, the state equations can be discretized using the following relationship:

$$x(k+1) = x(k) + \frac{dx(t)}{dt}.T_s \quad (4)$$

where $x(k+1)$ is the predicted state at $(k+1)$, $x(k)$ is the measured state at (k), T_s is the sampling time.

At (k) step, V_g, i_g, V_1, and V_2 are measured. By applying Equation (4) on Equations (1) and (2), respectively, the prediction of the capacitor voltage and the grid current values at $(k+1)$ can be found using the following equations:

$$V_2(k+1) = V_2(k) + \frac{T_s}{C}(s_3 - s_2 - s_7)i_g(k) \quad (5)$$

$$i_g(k+1) = i_g(k) + \frac{T_s}{L_f}(V_{AB}(k) - V_g(k)) \quad (6)$$

where $V_{AB}(k) = (s_1 - s_2 - s_8)V_1(k) + (s_2 - s_3 + s_7)V_2(k)$. The model is predicted for the 16 switching states given in Table 1.

For the grid-tied CSC inverter, the objective is to minimize the grid current THD% and the error between the capacitor voltage and its reference value. Hence, the cost function is designed as

$$g = \lambda_v \|V_2^*(k+1) - V_2(k+1)\|^2 + \lambda_i \|i_g^*(k+1) - i_g(k+1)\|^2, \quad (7)$$

where λ_v and λ_i are weighting factors, and (i_g^*,V_2^*) are the desired values for the grid current and the capacitor voltage, respectively. The cost function implies that the reference values

are obtained at $(k+1)$ sample. According to [30,31], it can be assumed that $i_g^*(k+1) \approx i_g^*(k)$. Since the DC voltage ($V_1$) is assumed to be constant, then $V_2^*(k)$ is equal to $V_2^*(k+1)$. Hence, the cost function is calculated using the following:

$$g = \lambda_v \|V_2^*(k) - V_2(k+1)\|^2 + \lambda_i \|i_g^*(k) - i_g(k+1)\|^2. \quad (8)$$

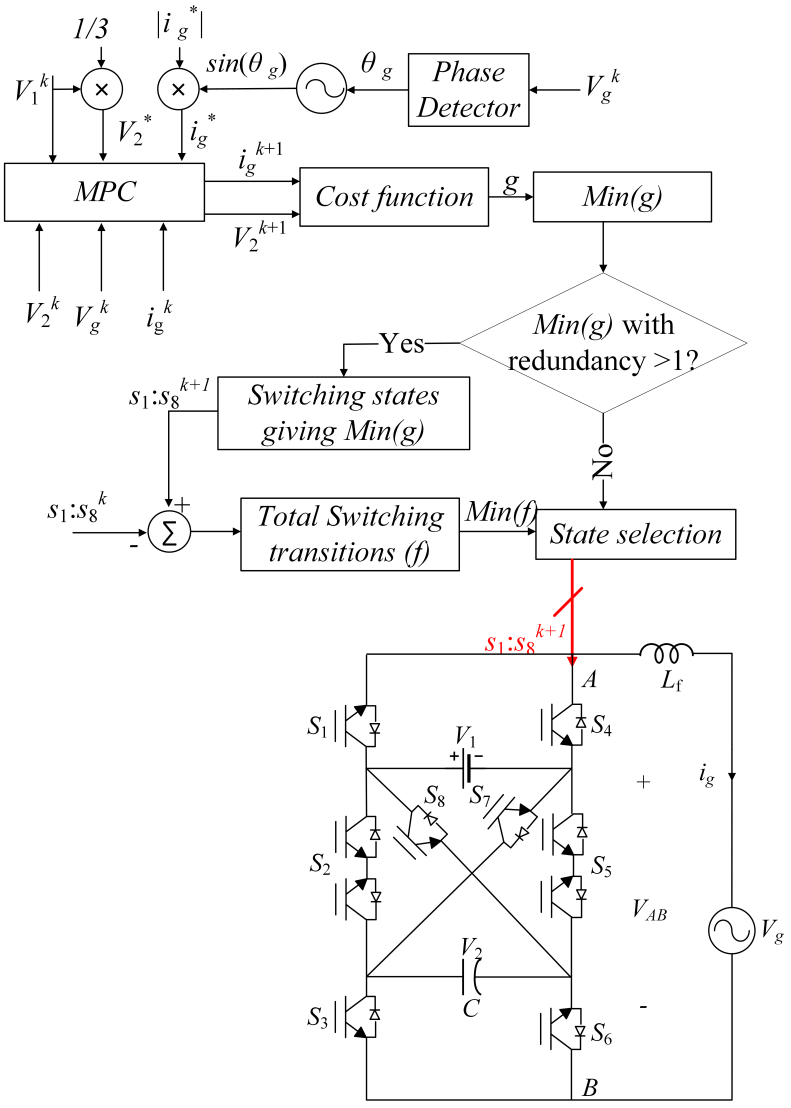

Figure 2. The synoptic of the proposed optimized FCS-MPC for the grid-tied 9-Level CSC inverter.

The cost function is calculated for the 16 switching states, and the switching state that will give the minimum g is chosen for $(k+1)$ time step. However, in CSC inverter, as shown in Table 1, there are several redundant states that will lead to the same minimum g. To reduce the switching losses, the (k) switching state $(s_1^k : s_8^k)$ is compared with all switching states that give (g_{min}), $(s_1^{k+1} : s_8^{k+1})$. The total switching transitions from $(s_1^k : s_8^k)$ to $(s_1^{k+1} : s_8^{k+1})$ are calculated, f. The one with the minimum switching transitions is sent to the inverter.

The weighting factors, λ_v and λ_i are chosen based on the objectives' priorities. In the CSC grid-connected case, a higher priority is given to the grid current THD% over the capacitor's voltage error. In our previous work [32], it was shown that to compromise between the two objectives, λ_i is set to 10 and λ_v is set to 5. The simulation results showed that the current THD% is 1.73% and the mean voltage error is 0.53 V.

4. Results and Discussion

The presented MPC for CSC inverter is tested via simulation and real-time implementation. The simulation was carried out using MATLAB/Simulink. The real-time implementation of the system was carried out using an OPAL-RT 5600 real-time simulator, enabling dynamic RT simulation responses.

The system parameters used for simulation and real-time implementation are listed in Table 2.

Table 2. System's parameters.

Parameters	Value
Fundamental frequency f_0	60 Hz
Sampling time T_s	20 µs
Grid voltage peak V_g	170 V
Grid current peak $\lvert i_g^* \rvert$	5 A
DC source voltage V_1	150 V
Capacitor voltage V_2^*	50 V
Capacitor C	2500 µF
Filtering inductor L_f	6 mH
Current weighting factor λ_i	10
Voltage weighting factor λ_v	5

4.1. Simulation Results

The effectiveness of the proposed controller in generating low-grid-current THD% is shown in Figure 3, where the THD% is 1.73%. This result is below the stated limit in IEEE 929-2000 standard for grid-connected PV systems (THD < 5%). The synchronization between the grid current and the grid voltage, the unity power factor, is shown in Figure 4. Additionally, the quality of the grid current is presented by plotting it against its reference.

Figure 5 shows the DC voltage, V_1, set as 150 V during the simulation. The capacitor voltage, V_2, is maintained at around its reference, 50 V, as shown in the same figure. The mean error of V_2 is 0.44 V. The third part of Figure 5 shows the generated nine levels of the inverter , V_{AB}, with the grid voltage, V_g. The results show the boosting ability of the CSC inverter, where the maximum voltage level (200 V) is the sum of the DC voltage and the capacitor voltage.

Figures 6 and 7 show the switching transitions for the eight switches ($S_1 : S_8$) of the CSC inverter. In Figure 6, the switching optimization algorithm (f) was used to reduce the total switching transitions, while in Figure 7, the switching optimization algorithm was skipped. Applying the switching optimization algorithm reduces the number of total switching transitions by an average of 85 transitions per cycle, and for a one-second simulation, the difference was more than 4500 transitions which is 9.3% transitions reduction. This reduction affects the conduction and switching losses in multilevel inverters, which depend on the frequency with which the switches are turned ON and OFF [33,34].

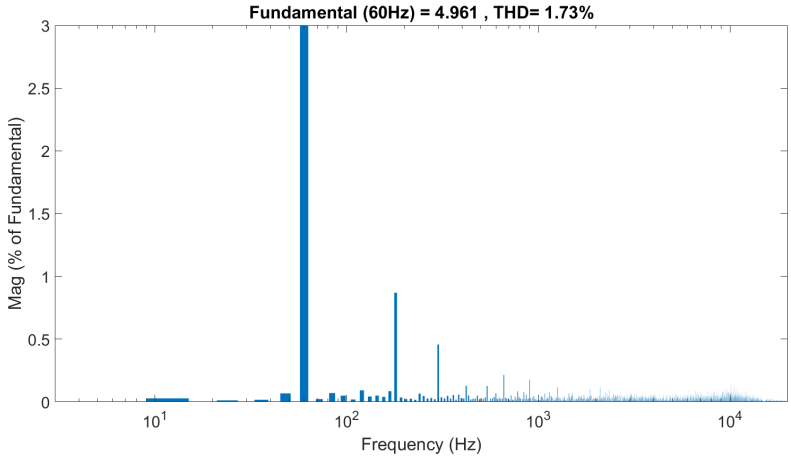

Figure 3. Grid current (i_g) THD%.

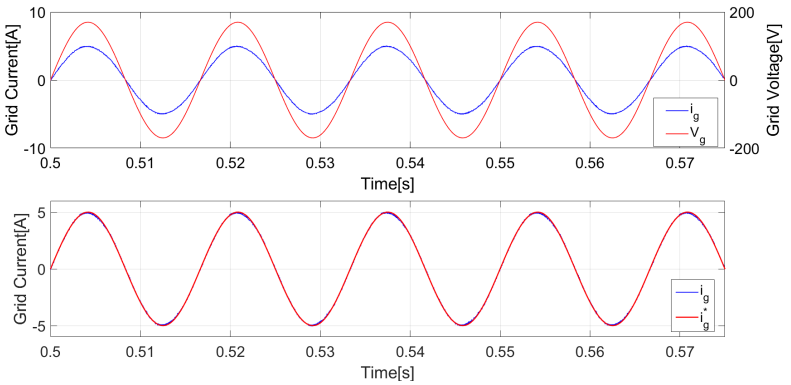

Figure 4. (**Upper**): The grid current (i_g) and the grid voltage (V_g), showing the synchronization between the two signals. (**Lower**): the generated grid current (i_g) versus its reference (i_g^*).

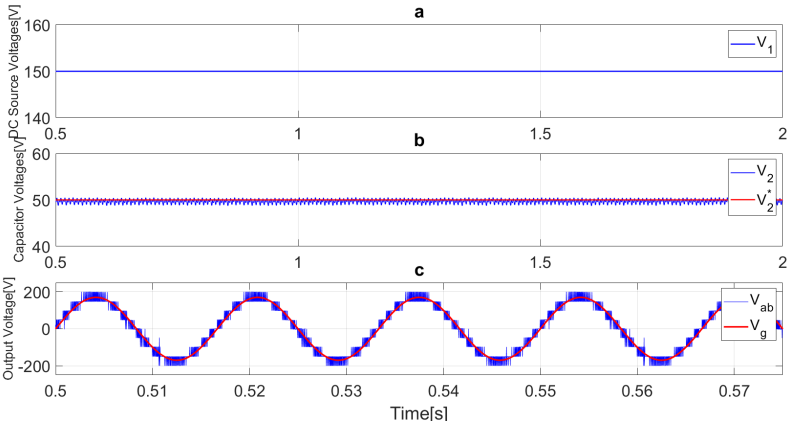

Figure 5. (**a**) The DC voltage (V_1), (**b**) The capacitor voltage (V_2) against its reference (V_2^*), and (**c**) The inverter output voltage V_{AB} and the grid voltage (V_g).

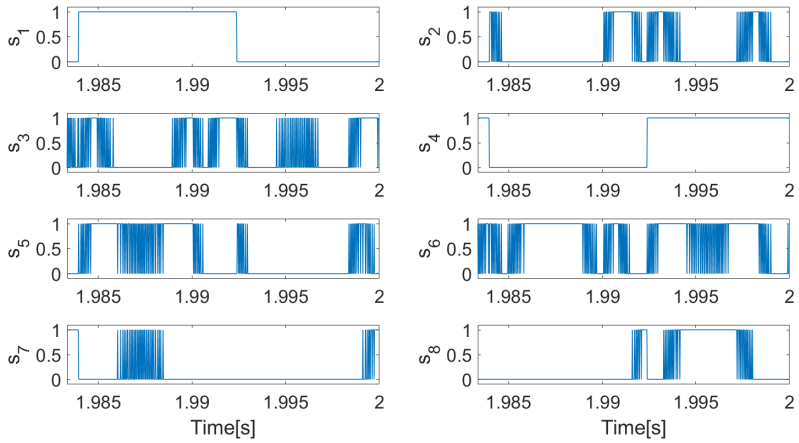

Figure 6. The transitions of the eight switches ($S_1 : S_8$) for one steady-state cycle when the switching optimization algorithm is used.

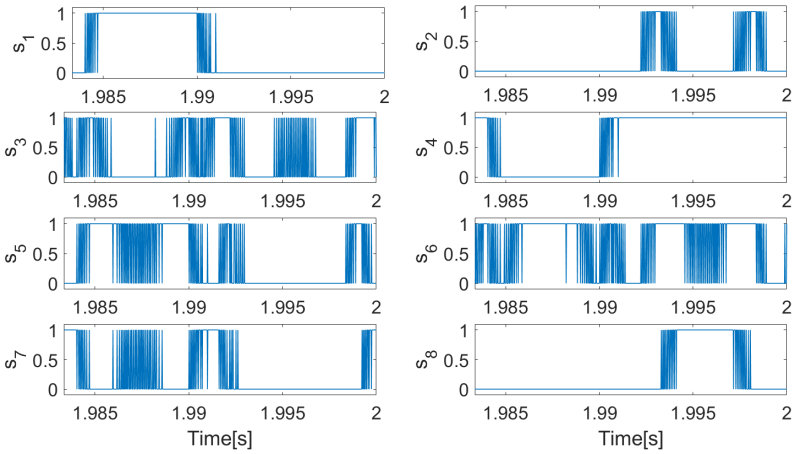

Figure 7. The transitions of the eight switches ($S_1 : S_8$) for one steady-state cycle without using the switching optimization algorithm.

4.2. Implementation Results

The setup of the system's real-time implementation is shown in Figure 8. Figures 9–11 demonstrate the steady-state operation of the system. The nine voltage levels of the CSC inverter (V_{AB}) are shown in Figure 9 along with the grid voltage (V_g). The MPC objective is to ensure that the generated grid current (i_g) follows its reference (i_g^*). This is clearly shown in Figure 10. The phase angle that is used to generate the reference current signal (i_g^*) is obtained from the grid voltage signal. That is, the generated grid current (i_g) is synchronized with the grid voltage with unity power factor. This synchronization is demonstrated in Figure 11.

To represent the importance of choosing the proper weighting factors, a distorted case is shown through real-time implementation. In Figure 10 ($\lambda_v = 5$) and ($\lambda_i = 10$) are chosen to give a higher priority to the current error in the cost function. However, in Figure 12, high distortion is shown in the grid current when the weighting factors were chosen as ($\lambda_v = 5$) and ($\lambda_i = 1$).

Since the MPC control strategy is based on predictions of the new state value using the system's model, any mismatch between the model and the real value of the system may affect the controller's effectiveness. Therefore, the capacitor and inductor values were changed by 50% to test the robustness of the controller. Figure 13 shows the accommodation of the generated grid current by the inverter, with its reference.

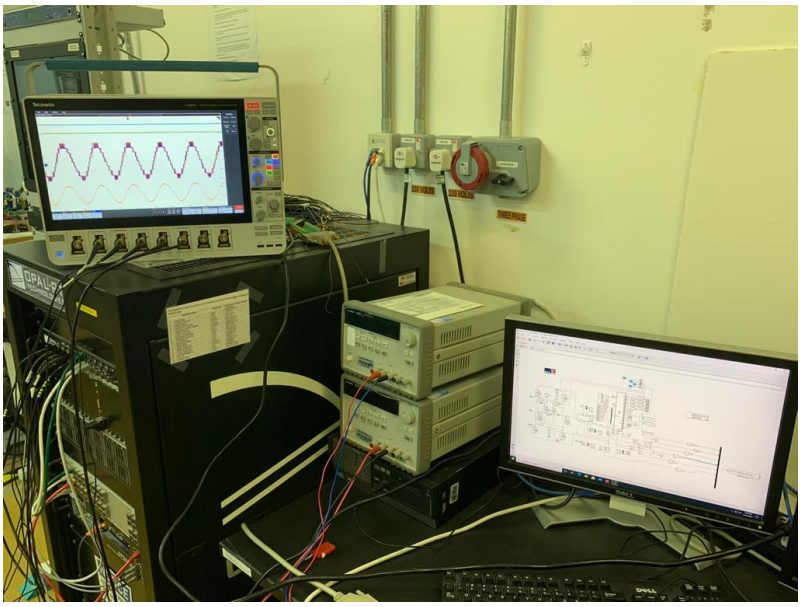

Figure 8. The setup of the FCS-CSC real-time implementation.

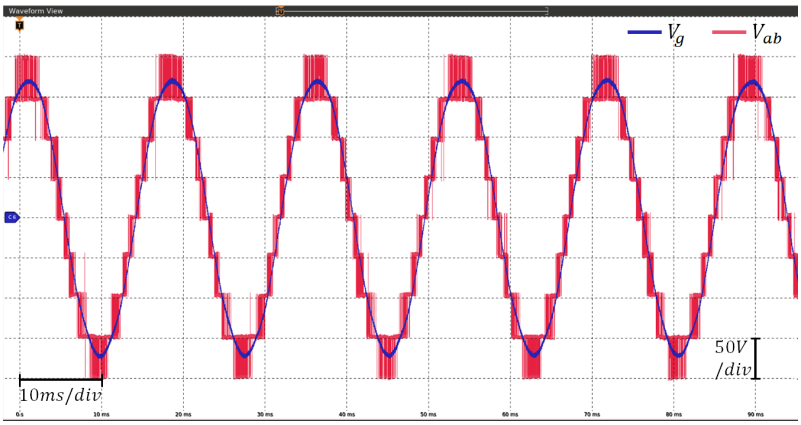

Figure 9. The output voltage of the CSC terminals showing the nine levels and the grid voltage.

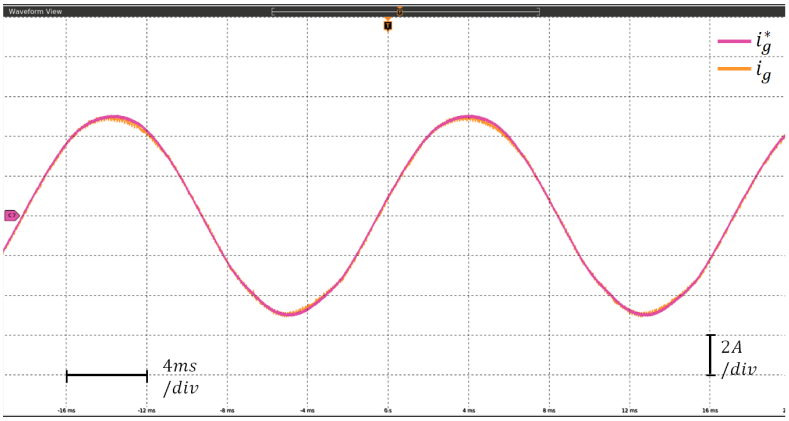

Figure 10. The grid currents (i_g) and its reference i_g^* for $\lambda_v = 5$ and $\lambda_i = 10$ case.

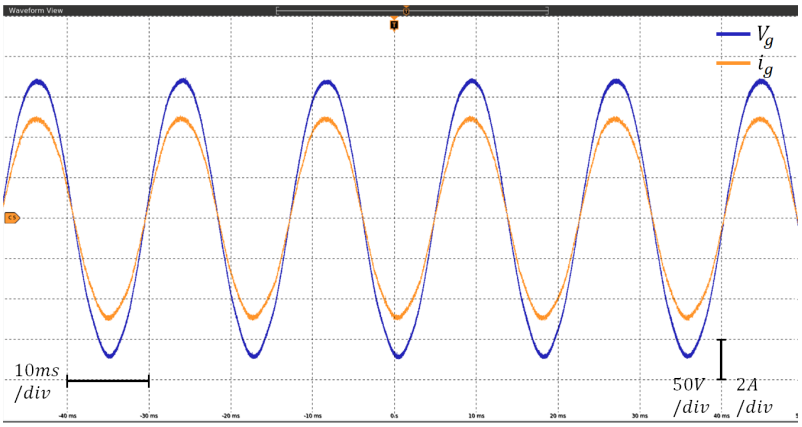

Figure 11. The synchronization between the grid currents (i_g) and the grid voltage v_g.

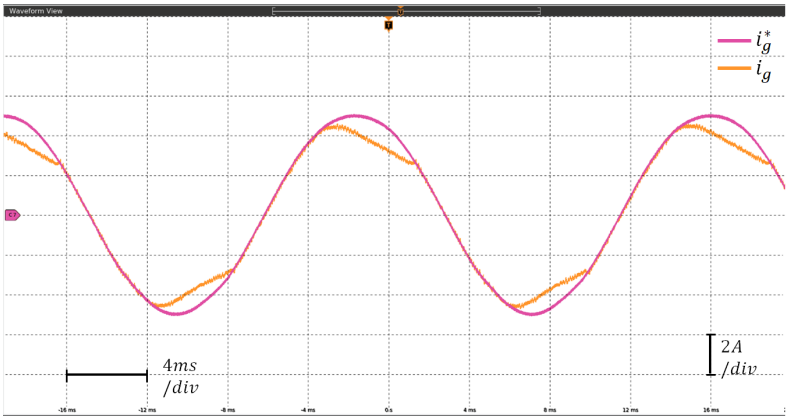

Figure 12. The grid current (i_g) and its reference i_g^* for $\lambda_v = 5$ and $\lambda_i = 1$ case.

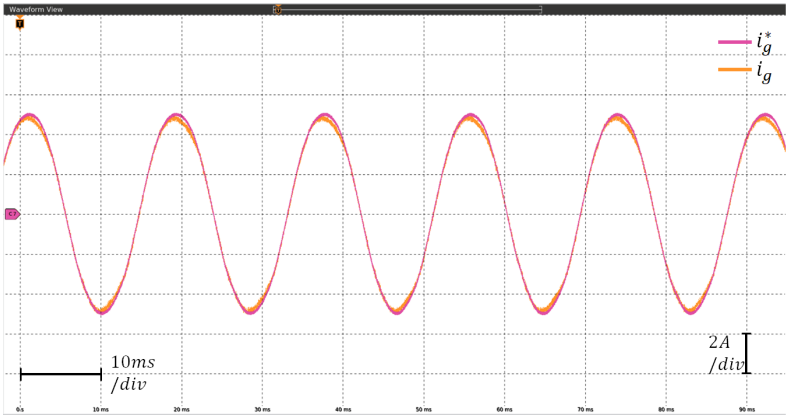

Figure 13. The grid current (i_g) and its reference (i_g^*) when the inductor and the capacitor values varied by ±50%.

The real-time implementation of the proposed MPC was extended to include several dynamic variation tests. Figure 14 illustrates the dynamic performance during a step-up change in the current reference peak from 5 A to 10 A. The generated grid current followed the new reference and maintained the unity power factor. In the second dynamic test, the DC voltage source was increased by (40%), i.e., V_1 is increased from 150 V to 210 V. As shown in Figure 15, V_2 accommodated the changes and increased from 50 V to 70 V ($V_2 = V_1/3$).

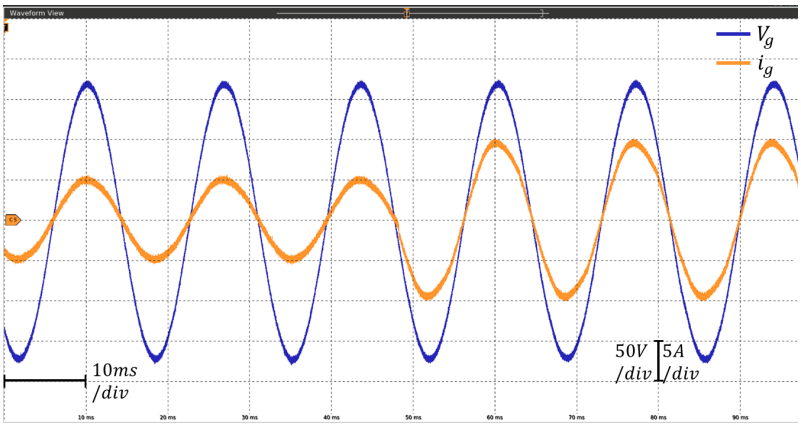

Figure 14. The grid voltage V_g and the generated grid current i_g when the grid current reference (i_g^*) is increased from 5 A to 10 A.

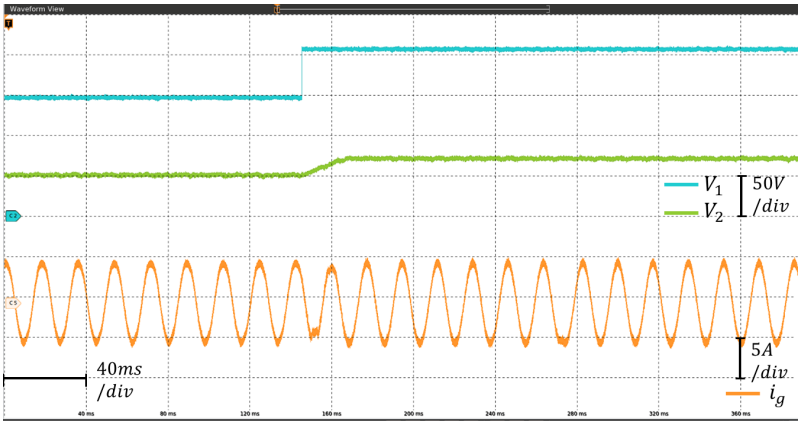

Figure 15. V_1, V_2, and i_g when the DC Source (V_1) varies from 150 V to 210 V.

To ensure the reliability of the systems tied to grids and the quality of the power distribution, some power quality disturbances were introduced to systems under testing [35]. Additionally, several standards describe the criteria of the accepted electric power quality, such as EN 50160-2000 and IEC 61000-2-8-2002. Voltage sag and voltage swell are common power-quality disturbances, which were introduced to the proposed FCS-MPC for 9-level CSC inverter in this work. Voltage sag can result from short-circuit faults, a change in the load, or a sudden change in the power source [35]. To implement the system under the effect of grid voltage sag, the grid voltage V_g was stepped-down by 10% from 170 V to 153 V, as shown in Figure 16. However, faults in the electrical distribution systems lead to voltage swell disturbances. Although voltage swell is less likely to occur than voltage sag, the damage it causes is greater on devices that cannot handle a voltage above their rating values [35]. To implement the voltage swell disturbance on the proposed system, the grid voltage V_g was increased from 170 V to 185 V, as shown in Figure 17.

Reactive power variation was tested by introducing phase shift between the grid voltage and the grid current in two scenarios: $\pi/4$ and $\pi/6$, as shown in Figures 18 and 19, respectively.

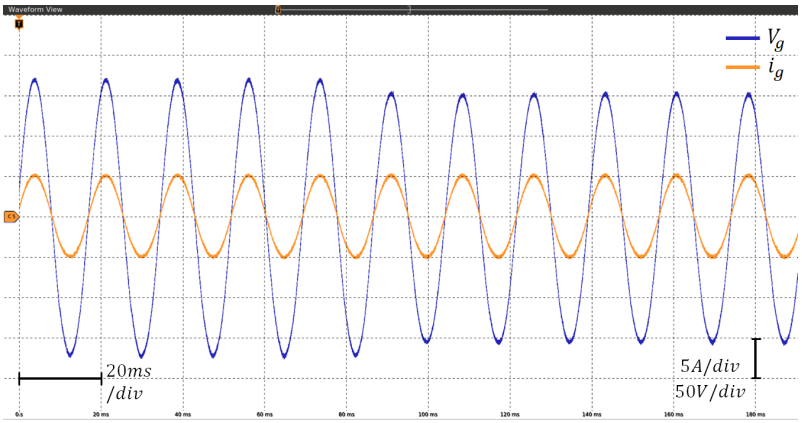

Figure 16. Voltage Sags—Grid Voltage (V_g 170 V to 153 V), V_g and i_g.

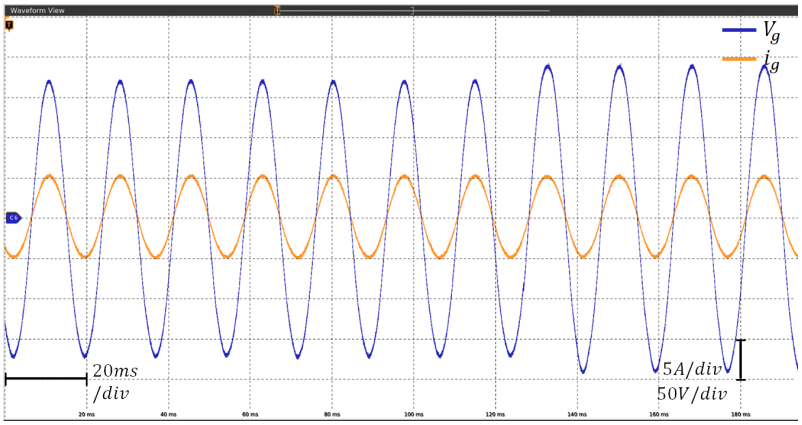

Figure 17. Voltage swell—Grid Voltage (V_g 170 V to 185 V), V_g and i_g.

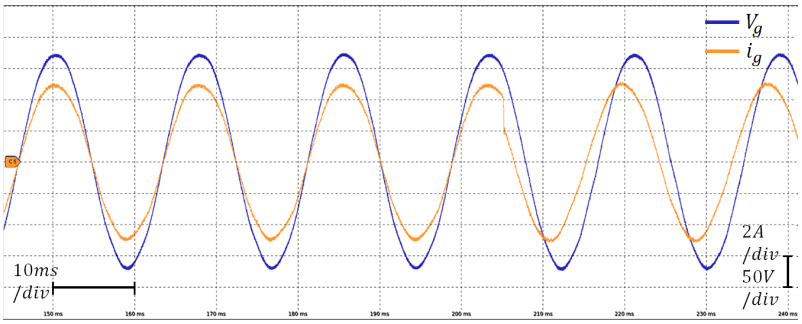

Figure 18. The phase shift between the grid voltage and current is $\pi/4$.

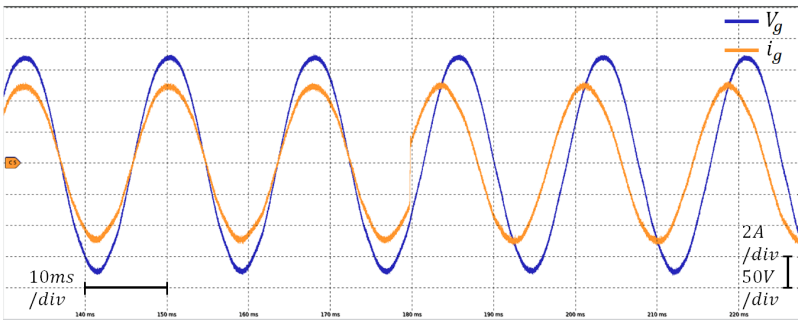

Figure 19. The phase shift between the grid voltage and current is $\pi/6$.

5. Conclusions

This paper proposes a finite control set–model predictive control (FSC-MPC) for a nine-level grid-connected single-phase crossover switches cell (CSC) multilevel inverter (MLI).

The results clearly showed the generated nine voltage levels, where the maximum voltage level was the sum of the DC source and the capacitor voltages. The cost function was designed to minimize the THD% of the generated grid current and regulate the capacitor's voltage around its reference. The simulation results showed that the current THD% is 1.73% and the mean error of the capacitor's voltage is less than 0.5 V. To connect the system to the grid, the grid current and the grid voltage should be synchronized; the power factor (PF) is one. Simulation results and real-time implementation results showed the synchronization between the two signals. The transient response of the system was tested in real-time implementation by changing the reference values of the capacitor voltage and the grid current amplitude. In both cases, the system showed a fast response to the changes and reached the new steady state. Furthermore, the results showed the ability of the system to accommodate different changes in the grid conditions, such as the grid voltage sag case, grid voltage swell case and the need for a reactive power. The control algorithm was designed to benefit from the redundant switching states in the CSC patterns by choosing, at each time step, the state that minimizes the cost function with the fewest total switching transitions. This algorithm decreased the switching transitions by 9.3% for a one-second steady-state simulation.

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Abbreviations

The following abbreviations are used in this manuscript:

MLI	Multilevel Inverter
THD	Total harmonic distortion
CSC	Crossover switches Cell
FCS-MPC	Finite control set-model predictive control
s_i (i 1 to 8)	CSC switches
V_1	DC link voltage
V_2	Capacitor voltage
V_{AB}	CSCoutput Voltage
V_g	Grid voltage
i_g	Grid current
T_s	Sampling time

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