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Analyzing the Effect of Parasitic Capacitance in a Full-Bridge Class-D Current Source Rectifier on a High Step-Up Push–Pull Multiresonant Converter

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Abstract: This paper presents an analysis on the effect of a parasitic capacitance full-bridge class-D current source rectifier (FB-CDCSR) on a high step-up push–pull multiresonant converter (HSPPMRC). The proposed converter can provide high voltage for a 12 V_{DC} battery using an isolated transformer and an FB-CDCSR. The main switches of the push–pull and diode full-bridge rectifier can be operated under a zero-current switching condition (ZCS). The advantages of this technique are that it uses a leakage inductance to achieve the ZCS for the power switch, and the leakage inductance and parasitic junction capacitance are used to design the secondary side of the resonant circuit. A prototype HSPPMRC was built and operated at 200 kHz fixed switching frequency, 340 V_{DC} output voltage, and 250 W output power. In addition, the efficiency is equal to 96% at maximum load. Analysis of the effect of the parasitic junction capacitance on the full-bridge rectifier indicates that it has a significant impact on the operating point of the resonant tank and voltage. The proposed circuit design was verified via experimental results, which were found to be in agreement with the theoretical analysis.

Keywords: parasitic capacitance; high step-up; zero-current switching; multiresonant; converter; current source rectifier

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1. Introduction

Currently, fossil fuel sources are being depleted owing to the considerable increase in the need for energy sources. To overcome this problem, efforts have been invested to develop renewable energy systems in the energy production field. In recent years, high step-up converters have been widely used in distributed power generators based on battery energy storage (BES) and module-integrated converters (MIC) with a DC link, and in stand-alone/grid-connected renewable energy systems such as photovoltaic cells, wind turbines, and fuel cells. These systems, which can be single or hybrid, use energy sources to generate electricity [1–4]. As these are low-voltage systems, the output voltage can be varied. For maintaining system voltage, a battery system is generally used to back-up the system with a constant DC-link in the inverter state. Therefore, to increase the low voltage of the battery to a suitable value, a high step-up converter is employed to step-up the low input voltage to a high output voltage. High step-up topologies are classified into nonisolated and isolated DC/DC converters. The nonisolated topology typically uses a boost converter

structure to provide a higher output voltage from low input sources by varying the duty cycle of the pulse width modulation (PWM) [5]. At high voltage/frequency, the converter generates a high voltage spike at the power switch and high electromagnetic interference increases the switching loss and the loss due to the passive element. A significant issue with the boost converter is that when considering a low input voltage source, it is difficult to obtain a high voltage conversion ratio. To overcome this problem, the gain conversion ratio is modified to maximize the gain voltage using several techniques such as interleaved positive/negative coupling; cascading, n-stage cascading, or integrated cascading; and using multilevel cells and switch capacitors [6–17]. The overall family of high step-up converters is depicted in Figure 1. Isolated DC/DC converter topologies that include the flyback and forward converters are considered more suitable for low-voltage/-power applications because these converters only have a single switch that results in lower cost and significantly lower circuit losses during operation. High-voltage step-up techniques require high-frequency transformers.

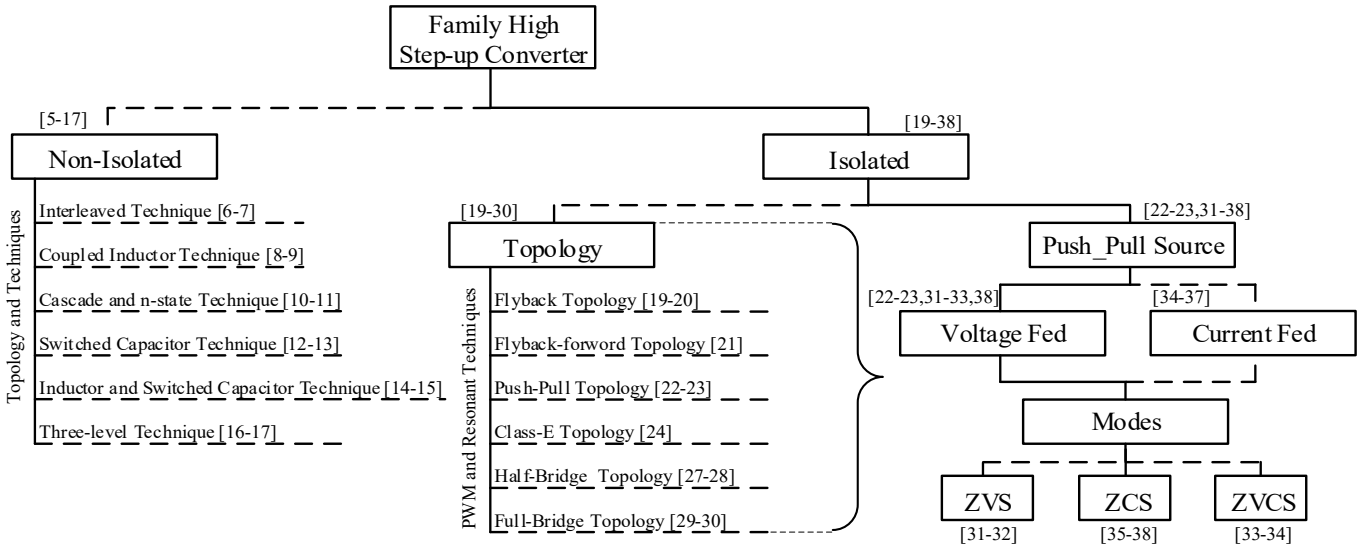


Figure 1. Family of high step-up converters and the proposed high step-up push–pull resonant converter.

Asymmetric pattern waveforms have disadvantages such as flux saturation and voltage/power issues on the primary side of the high-frequency transformer. However, the leakage inductance at the primary side of the transformer can place high-voltage stress on the power switch during the turn-on and turn-off states [18–23]. A Class-E inverter is a topology with the advantages of using a single switch, a simple gate driving circuit, and all its parameters can be calculated. However, the high voltage across the power switch has a limitation as it is approximately three ranges higher than that of the input voltage [24–26]. Therefore, two switch converters among half-bridge, push–pull, and Class-D converters are preferred when applying high power. The half-bridge and full-bridge topologies can easily achieve zero-voltage switching (ZVS). The reverse–recovery of the main power switches in the body diodes is an important problem as it causes a significant drop in overall efficiency owing to the electromagnetic interference from the high output voltage. The source can be categorized as either a voltage-fed source or a current-fed source. The current-fed source consists of an inductor input connected in series with a power switch to reduce the current ripple and to limit the current input. This structure, with an active switch clamp, is used to reduce the voltage spike on the power switch generated by the inductor input side [27–30]. The push–pull converter is more effective for low to medium power operations owing to its two switches, low component count, and simple gate driving circuit [18–38]. For this converter, both the current-fed and voltage-fed topologies can be employed in either the PWM or the resonant modes to achieve the ZVS, ZCS, or ZVCS conditions [31–38]. For low-voltage high-current input applications, ZVS is not particularly

important, whereas zero-current switching (ZCS) is critical to eliminate switching losses. In the resonant mode, a resonant tank is connected to a half-wave/full-wave bridge or a center-tap and to voltage double rectifiers [39–41]. However, a diode with a common rectifier in a low-frequency range with parallel parasitic capacitance can affect the main state when we consider both the main factors in a high step-up application depending on voltage and switching frequency range. The resonant techniques enable a high step-up and frequency converter while operating simultaneously with high switching frequency, and the rectifier can be utilized to achieve parasitic capacitance in parallel and series–parallel resonant tanks. In terms of the rectifier circuit, the parasitic capacitance of the rectifier can be used for the resonant tank. In the literature, the parasitic capacitance can be used in parallel, and the series–parallel resonant tanks are mentioned to increase the load quality factor. However, a high output voltage under light-load conditions can occur, and this can possibly damage the diode rectifier [42–47].

The remainder of this paper is organized as follows. The proposed circuit is described in Section 2; Section 3 presents the circuit analysis; the analysis modeling resonant and parasitic capacitance rectifier is shown in Section 4; the design procedure for the component is shown in Section 5; experimental results are presented in Section 6; a discussion of the effected parasitic capacitance parameter and the experimental results are presented in Section 7; and, finally, the conclusion is provided in Section 8.

2. Circuit Description

The main circuit consists of power switches, a high-frequency center-tap transformer, a resonant tank, a full-bridge rectifier, an output capacitor, and a resistance load. The HSPPMRC consists of two switches, M_1, M_2, with a duty ratio of nearly 0.5; an antiparallel body diode; and a parasitic capacitance drain–source C_{M1}, C_{M2} of MOSFETs. The equivalent circuit model of the transformer consists of leakage inductances at the primary side L_{p1}, L_{p2} and a resonant inductance L_{lks} at the secondary side. The secondary-side leakage inductance of the high-frequency transformer is connected in series with capacitor C_r and in parallel with parasitic capacitance full-wave bridge rectifier C_e. The parameter values of the leakage inductance at the high-frequency transformer depend on the physical structure such as the magnetic material, air gap, and the coil-winding technique used. The equivalent circuit model of the center-tap transformer of the push–pull converter is shown in Figure 2. The parameter values of the transformer can be measured using the LCR meter. However, the magnetizing inductance of the transformer values is higher than the leakage inductance L_{lks} for both sides and, therefore, it can be ignored. The resonant capacitor C_r is a series capacitor that includes the leakage inductance and parallel parasitic junction capacitor C_e when the junction capacitor of each diode is $C_D = C_{D1} = C_{D2} = C_{D3} = C_{D4}$ of the FB-CDCSR. In the resonant circuit, each diode is operated under the ZCS condition. The output capacitance is very large; therefore, the output voltage V_o is constant and supplies a load R_o. The resonant circuit feeds a square-wave voltage and a sine-wave current to the secondary side. This high frequency is used to drive the FB-CDCSR.

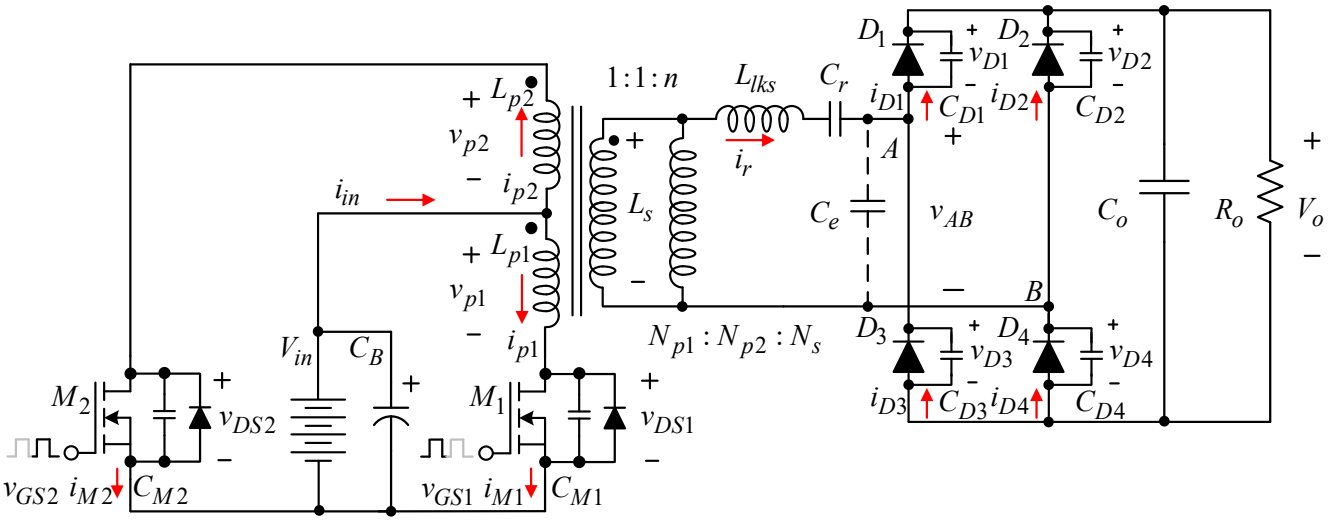


Figure 2. Proposed parasitic capacitance full-wave bridge class-D current source rectifier design in the high step-up push–pull multiresonant converter.

3. Circuit Analysis

The principles of the power state of HSPPMRC are explained as shown in Figure 2. The main power switch and the diode rectifier operate under the ZCS condition. It is appropriate to consider the secondary side of the transformer as a sinusoidal current source i_r, which is also a high-frequency current source of the full-bridge rectifier. Figure 3 shows that the key waveforms consist of a gate driven by switches v_{gs1}, v_{gs2}; voltage across v_{ds1}, v_{ds2}; current of switch i_{M1}, i_{M2}; voltage resonant v_{rec}; current of resonant i_r; overall voltage across v_{D1}-v_{D2}-v_{D3}-v_{D4}; and a current of the diode rectifier i_{D1}-i_{D2}-i_{D3}-i_{D4}. The proposed circuit can be operated under four modes, as shown in Figure 4. The analysis of the circuit begins with these following assumptions.

1. The main power switch and active/passive elements in the on and off state are equal to zero and have infinite resistance.
2. All passive components in the circuit are ideal and the initial condition is equal to zero.
3. The load quality factor is higher so that the current is sinusoidal.
4. The transformer is ideal and the value inductance of the primary side 1 is similar to the value of primary side 2.
5. The output capacitor is sufficiently large for the output voltage to be constant.

Mode 1: This mode is depicted in Figure 4a. First, the power switch M_1 is turned on while switch M_2 is off. The current flows from the DC input source V_{in} to the drain–source of MOSFET M_1 when switch M_1 is turned on and operated under the ZCS condition by the commutation of the leaked inductance, magnetizing current transformer, and the drain–source junction capacitance. Simultaneously, the junction capacitor C_{M1} of M_1 discharges the voltage and decreases to zero, and the junction capacitor voltage v_{ds2} of M_2 charges the voltage from zero to twice the voltage of the DC input source. Then, the energy is transferred to the secondary side, diodes D_1 and D_4 are turned on, and diodes D_2 and D_3 are turned off under the ZCS condition by the flow of current i_{D1} and i_{D4} through the diode rectifier and resonant circuit.

Mode 2: As depicted in Figure 4b, the commutation between M_1 and M_2 is turned off. The junction capacitor drain–source C_{M1} of M_1 charges the voltage v_{ds1} until it increases to twice that of the DC input source, and the junction capacitor drain–source C_{M2} of M_2 discharges voltage v_{ds2} until the voltage decreases from twice that of the DC input source to zero. At the same time, the junction capacitors C_{D1} and C_{D4} of diodes D_1 and D_4 discharge to the zero value, and the junction capacitor C_{D2} and C_{D3} of diodes D_2 and D_3 charge from zero to the negative output voltage, as shown in Figure 4b.

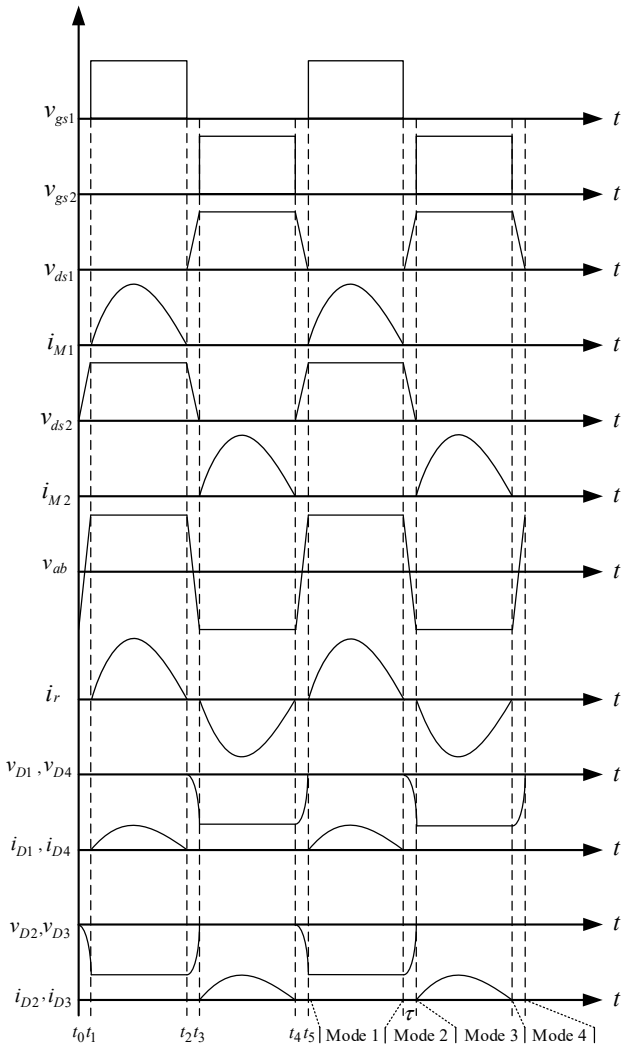


Figure 3. Key waveforms of the proposed circuit.

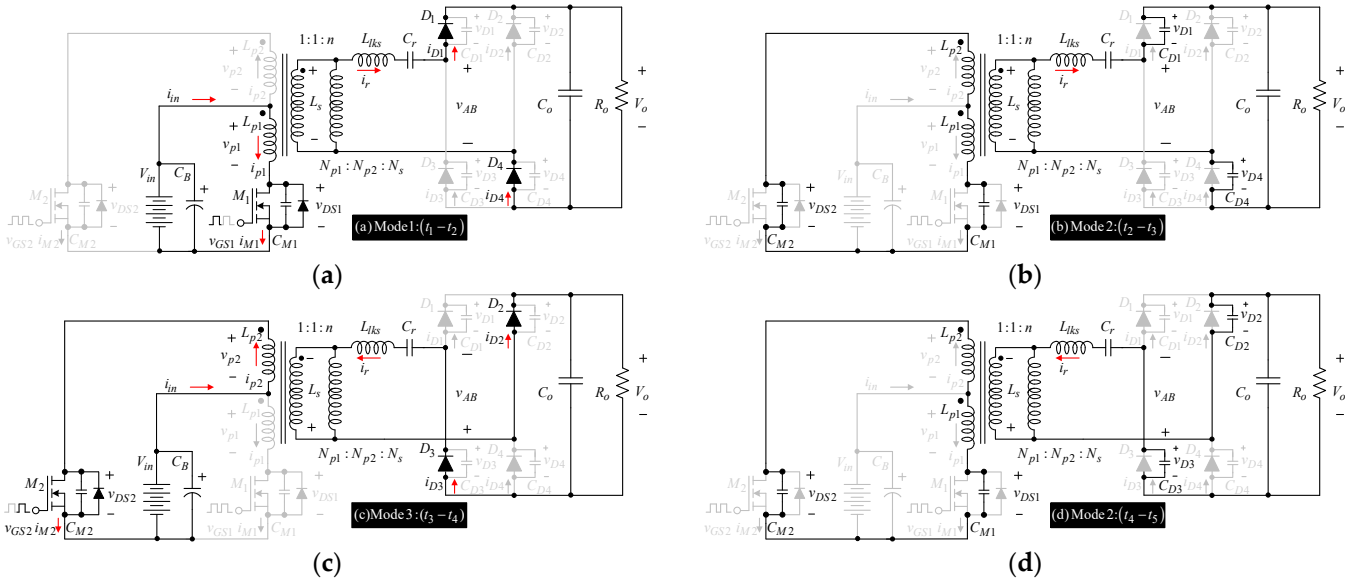


Figure 4. Operation modes of the proposed circuit. (**a**) Power switch M_1 is turned on while power switch M_2 is turned off; (**b**) commutation time of M_1 while M_2 is turned off; (**c**) power switch M_2 is turned on while power switch M_1 is turned off; (**d**) commutation time of M_2 while M_1 is turned off.

Mode 3: This mode is similar to Mode 1. As shown in Figure 4c, the gate driving circuit turns M_2 on and turns M_1 off. The current flows from the DC input V_{in} to the drain–source of MOSFET M_2 when M_2 is turned on and operated under the ZCS condition by the commutation of the leaked inductance, magnetizing current transformer, and drain–source junction capacitance. Simultaneously, the voltage of the junction capacitor C_{M2} in M_2 discharges to zero. At the same time, the junction capacitor voltage v_{ds1} of M_1 charges the voltage from zero to twice the voltage of the DC input source. Then, the energy is transferred to the secondary side, the diodes D_2 and D_3 are turned on, and diodes D_1 and D_4 are turned off under the ZCS condition under the flow of current i_{D2} and i_{D3} through the diode rectifier and resonant circuit.

Mode 4: This is depicted in Figure 4d. The junction capacitor drain–source C_{M2} of M_2 charges voltage v_{ds2} until the voltage increases to twice that of the input source and the junction capacitor drain–source C_{M1} of M_1; then, it discharges the voltage v_{ds1} until the voltage decreases from twice that of the input source to zero. Simultaneously, the junction capacitors C_{D2} and C_{D3} of diodes D_2 and D_3 discharge to a zero value. Then, diodes D_2 and D_3 are turned off by ZCS and the junction capacitors C_{D1} and C_{D4} of the diodes D_1 and D_4 charge from zero to the negative output voltage. In fact, there are four assumptions based on the analytical operation in FB-CDCSR, the input current source $i_r \sin \omega_s t$ has a sinusoidal waveform and is the same between the switching and resonant frequency, and each parasitic junction capacitance C_{D1}-C_{D2}-C_{D3}-C_{D4} of the full-wave rectifier has the same value.

All the parasitic junction capacitances C_e have an "equivalent parasitic capacitance", which operates as an equilibrium in the commutation range and at a constant value. The final assumption is used to simplify the analysis, and the parasitic junction capacitance with respect to the reverse bias voltage is not considered. From Figure 3, both the junction capacitors C_{D2} and C_{D3} of diodes D_2 and D_3 discharge to a zero value at the same time t_0-t_1. The top diode D_1 and cruciate diode D_4 turn on. At time t_1-t_2, when i_r is still charging C_{D2}-C_{D3} and discharging C_{D1}-C_{D4}, the conducting mode ends, C_{D2}-C_{D3} is fully charged, and C_{D1}-C_{D4} discharges to zero. In this section, we define commutation period $\tau = t_1$-t_0 and t_3-t_2 and the commutation angle, where f_s and ω_s are the switching and angular frequency, respectively. From the first harmonic approximation technique used to find the real and reactive voltage fundamental component of the FB-CDCSR, the real part value can be expressed as

$$v_{AB-real} = \frac{1}{\pi} \int_0^{2\pi} v_{AB} \sin(\omega_s t) d(\omega_s t) \tag{1}$$

We obtain the condition as shown:

$$v_{AB-real} \begin{cases} \frac{I_{rp}}{\omega_s C_D}(1 - \cos(\omega_s t)) - V_o \sin(\omega_s t) d(\omega_s t), t_0 - t_1 \\ V_o \sin(\omega_s t) d(\omega_s t), t_1 - t_2 \\ V_o \sin(\omega_s t) d(\omega_s t) - \frac{I_{rp}}{\omega C_D}(1 - \cos(\omega_s t)), t_2 - t_3 \\ V_o \sin(\omega_s t) d(\omega_s t), t_3 - t_4 \end{cases} \tag{2}$$

Voltage across the rectifier in a real term is shown below:

$$v_{AB-real} = \frac{I_{rp}}{\pi \omega_s C_D} \left(1 - 2\cos(\omega_s \tau) + \frac{\cos^2(\omega_s \tau)}{2} + \frac{1 + \cos(2\omega_s \pi + 2\omega_s \tau)}{4}\right) + 4V_o \cos(\omega_s \tau) \tag{3}$$

$$v_{AB-real} = \frac{1}{\pi} \left(\frac{I_{rp}}{\omega_s f_s C_D} \left(1 - \cos^2(\omega_s \tau)\right)\right) \tag{4}$$

Similarly, the reactive part fundamental component value can be expressed as

$$v_{AB-react} = \frac{1}{\pi} \int_0^{2\pi} v_{AB} \cos(\omega_s t) d(\omega_s t) \tag{5}$$

Afterwards, the condition under analysis for voltage across the rectifier in an imaginary term can be found.

$$v_{AB-react}\begin{cases} \frac{I_{rp}}{\omega_s C_D}(1-\cos(\omega_s t)) - V_o\cos(\omega_s t)d(\omega_s t), t_0 - t_1 \\ V_o\cos(\omega_s t)d(\omega_s t), t_1 - t_2 \\ V_o - \frac{I_{rp}}{\omega_s C_D}(1-\cos(\omega_s t))\cos(\omega_s t)d(\omega_s t), t_2 - t_3 \\ V_o\cos(\omega_s t)d(\omega_s t), t_3 - t_4 \end{cases} \tag{6}$$

Voltage across the rectifier in an imaginary term is shown below:

$$v_{AB-react} = \frac{1}{\pi}\left(\frac{I_{rp}}{\omega_s C_D}\left(2\sin(\omega_s\tau) - \frac{2\omega_s\tau}{2}\right)\right) - \frac{(\sin(2\omega_s\tau + 2\omega_s\pi) - \sin(2\omega_s\pi))}{4} + 4V_o\sin(\omega_s\tau) \tag{7}$$

$$v_{AB-react} = \frac{1}{\pi}\left(\frac{I_{rp}}{\omega_s C_D}\left(-\frac{2\omega_s\tau}{2} - \frac{\sin(2\omega_s\tau)}{2} + \sin(2\omega_s\tau)\right)\right) \tag{8}$$

Furthermore, the find section of output voltage V_o can have two conditions. In $t_0 - t_1$, the parasitic junction capacitance changes during the commutation time as

$$V_{o,t_0-t_1} = \frac{1}{C_D}\int_0^{\tau}\frac{I_{rp}}{2}\sin(\omega_s t)d(\omega_s t) \tag{9}$$

$$V_{o,t_0-t_1} = \frac{I_{rp}}{4\pi f_s C_D}(1-\cos(\omega_s t)) \tag{10}$$

From $t_1 - t_2$, during the commutation time, v_{D2} and v_{D3} are equal to output voltage. v_{D1} and v_{D4} are zero and both diodes conduct the following input current resonant i_r, which can be found using (11) and (12):

$$V_{o,t_1-t_2} = \frac{\omega_s R_o}{\pi}\int_0^{T/2} I_{rp}\sin(\omega_s t)d(\omega_s t) \tag{11}$$

$$V_{o,t_1-t_2} = \frac{R_o I_{rp}}{\pi}(\cos(\omega_s\tau) + 1) \tag{12}$$

(10) and (12) show the charge/discharge of the parasitic junction capacitance and during commutation. It can be rewritten as the characteristic commutation angular time, showing that

$$\frac{I_{rp}}{4\pi f_s C_D}(1-\cos(\omega_s\tau)) = \frac{R_o I_{rp}}{\pi}(\cos(\omega_s\tau) + 1) \tag{13}$$

$$\cos(\omega_s\tau) = \left(\frac{1 - 4R_o f_s C_D}{1 + 4R_o f_s C_D}\right) \tag{14}$$

In (4), (8), and (14), when considering an ideal case, the parasitic junction capacitance C_D equals to zero, in which the input voltage and current resonant in phase are a simplified real and reactive part of the fundamental component as divided into

$$V_{ab,CD_0} = \frac{8R_o I_{rp}}{\pi^2} \tag{15}$$

$$v_{ab-real,CD_0} = \frac{I_{rp}}{2\pi^2 f_s C_D}\sin^2(\omega_s\tau) = \frac{V_{ab,CD_0}}{(1 + 4f_s R_o C_D)^2} \tag{16}$$

$$v_{ab-react,CD_0} = \frac{I_{rp}}{4\pi^2 f_s C_D}(\sin(2\omega_s\tau) - 2\omega_s\tau) = \frac{V_{ab,CD_0}}{32 f_s R_o C_D}(\sin(2\omega_s\tau) - 2\omega_s\tau) \tag{17}$$

4. Analysis Modeling Resonant and Parasitic Capacitance Rectifier

In this section, we analyze the parasitic capacitance of FB-CDCSR in a resonant tank circuit. In the first step, the model combines the HSPPMR and FB-CDCSR circuits. The MOSFETs are modeled by both switches with turned-on resistances. Resistances and inductances are parasitic equivalent circuits of the transformer. The main switch M_1 operates in the positive half-cycle, whereas the main switch M_2 operates in the negative half-cycle. From Figure 5a, the high-frequency square-wave voltage source v'_{in} is transferred from two windings on the primary side to the secondary side. The leakage inductance L_r is connected in series to the resonant capacitor C_r and is calculated from the transferred inductances L_{lk11} and L_{lk12} in the primary side, as per $(L_{lk11} + L_{lk12})(n/2)^2 + L_{lks}$. The parasitic junction capacitance in the FB-CDCSR for the HSPPMRC, where diodes D_1 and D_4 of the rectifier operate during the positive cycle of a high-frequency square-wave voltage source, is a fundamental component amplitude that equals to $v'_{in} \sin \omega_s t$, where v'_{in} is the voltage across the secondary side. This amplitude is similar to that of diodes D_2 and D_3 of the rectifier, which operate during the negative cycle. The equivalent circuit affects the parasitic junction capacitance of the FB-CDCSR diode under a high voltage and high switching frequency operation. Owing to the short circuit of the AC voltage source on the secondary side, the junction capacitor $C_{DA}/2$ is derived from diodes D_1 and D_3, whereas the junction capacitor $C_{DB}/2$ is obtained from diodes D_2 and D_4, as demonstrated in Figure 5b. In this circuit, capacitor C_D is a parallel combination of the junction capacitor C_{DA} of diodes D_1 and D_3 and the junction capacitor C_{DB} of diodes D_2 and D_4, which can be considered as one capacitor $C_{DAB} = C_{DA}/2 + C_{DB}/2$. The C_{DAB} parameter is parallel with the AC resistance R_{ac} transformed from the DC resistance of the output side. The final model between the parasitic junction capacitor of the push–pull resonant converter is illustrated in Figure 5c. The output voltage equals the voltage of the AC resistor parallel with the parasitic junction capacitors, and the input voltage equals the voltage on the secondary side.

$$\left.\begin{aligned} Z_i &= sL_r + \left(\frac{1}{sC_r}\right) + \left(\frac{R_{ac}}{sC_eR_{ac}+1}\right) \\ Z_o &= \frac{R_{ac}}{sC_e\left(R_{ac}+\frac{1}{sC_e}\right)} \end{aligned}\right\} \tag{18}$$

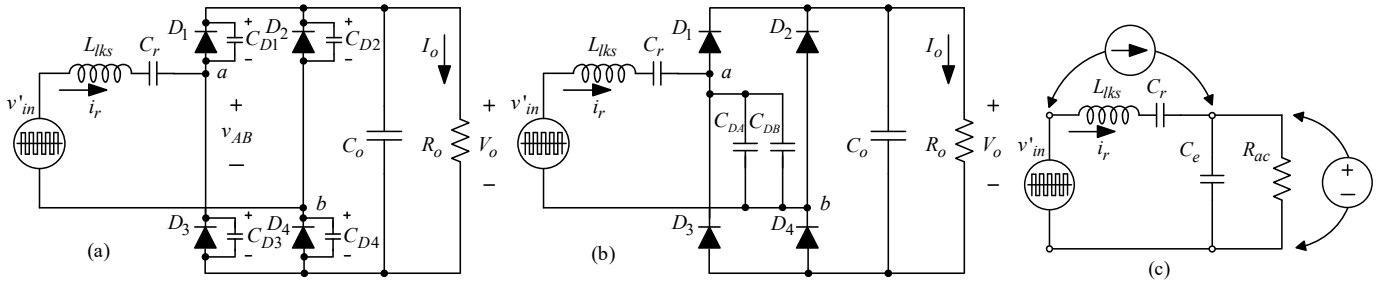


Figure 5. Equivalent circuit for the parasitic capacitance of FB-CDCSR. (**a**) Equivalent circuit of the FB-CDCSR including parasitic capacitance; (**b**) equivalent square-wave voltage source circuit is connected, affecting parasitic capacitance; (**c**) semi- and final equivalent resonant circuit including parasitic capacitance of the FB-CDCSR.

From (18), we can rewrite the transfer function as

$$\frac{v_{AB}}{v'_{in}}(s) = \left(\frac{1}{sL_r + \frac{1}{sC_r} + \frac{R_{ac}}{sC_eR_{ac}+1}}\right) \times \left(\frac{R_{ac}}{sC_eR_{ac}+1}\right) \tag{19}$$

Hence, the normalized voltage gain of the resonant circuit can be described as

$$tf(s) = \frac{sC_rR_{ac}}{s^3L_rC_rC_eR_{ac} + s^2L_rC_r + s(C_eR_{ac} + C_rR_{ac}) + 1} \tag{20}$$

Further, the input impedance Z_i of the resonant circuit with the variable parasitic junction capacitors can be written as

$$Z_i(s) = \frac{s^3 L_r C_r C_e R_{ac} + s^2 L_r C_r + s(C_e R_{ac} + C_r R_{ac}) + 1}{s^2 C_r C_e R_{ac} + s C_r} \tag{21}$$

where R_{ac} and C_r are the normalized resistance and capacitance resonance, respectively.

The value of the AC resistance R_{ac} and the combination of the parasitic junction capacitors C_e that can be plotted to adjust the switching frequency are shown in Figures 6–9.

$$R_{ac} = \frac{8R_o}{\pi^2} \tag{22}$$

$$\tau = \frac{1}{\omega_s} \cos^{-1}\left(\frac{1 - 4f_s R_o C_D}{1 + 4f_s R_o C_D}\right) \tag{23}$$

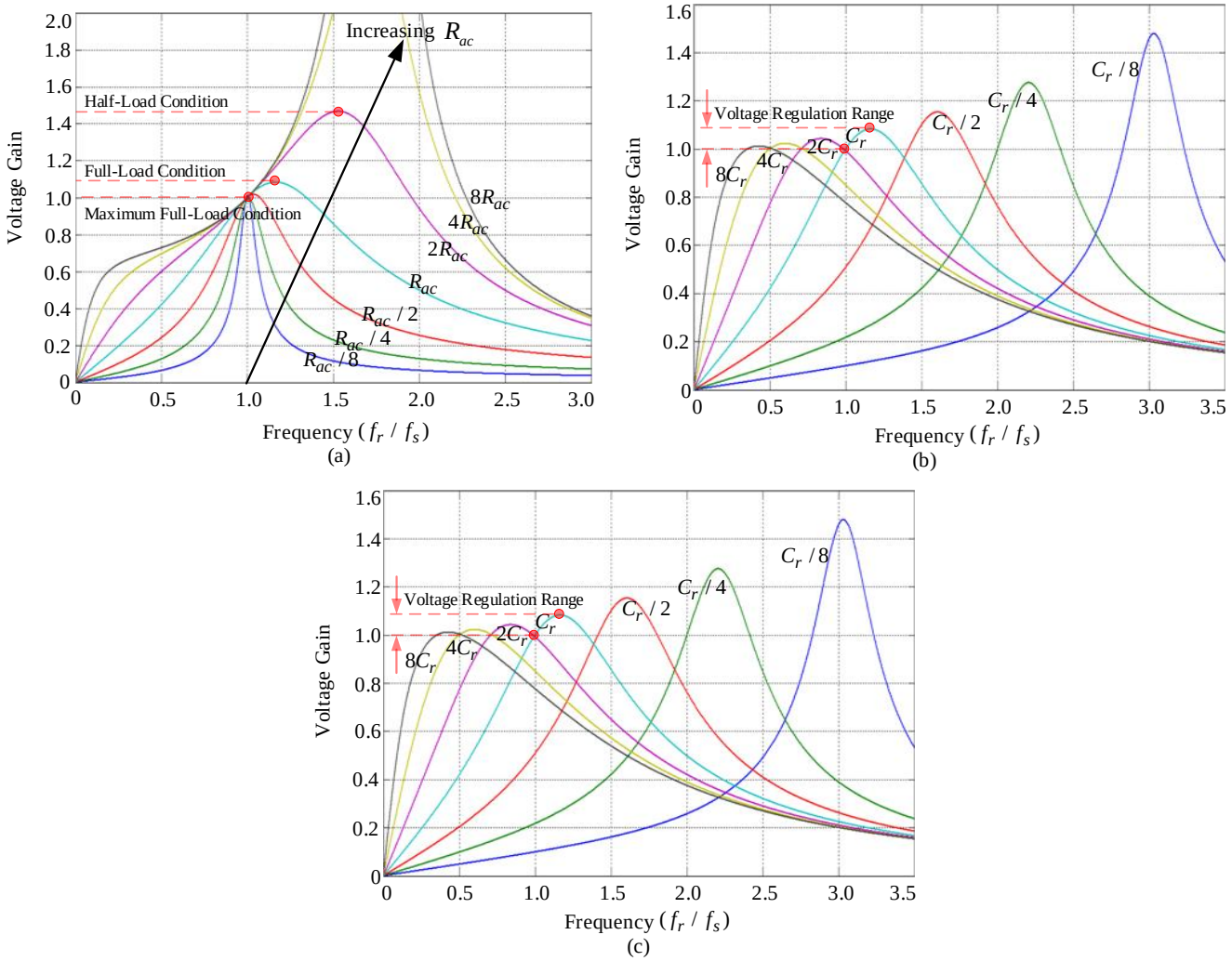


Figure 6. Relationships of the matching resonant tank of the proposed circuit. (**a**) Normalized voltage gain of resonant circuit versus frequency at varied AC resistance; (**b**) normalized voltage gain of resonant circuit versus frequency at varied AC capacitor resonant load; and (**c**) input impedance of the resonant circuit versus the frequency at a variable parasitic junction capacitance.

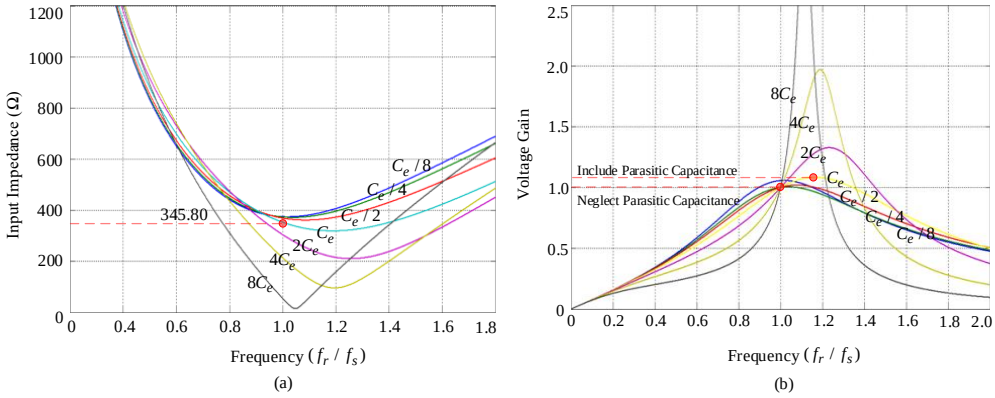


Figure 7. Relationships affecting parasitic junction capacitance on the matching resonant tank of proposed circuit. (**a**) Input impedance of the resonant circuit versus the frequency at a variable parasitic junction capacitance and (**b**) normalized voltage gain of resonant circuit versus frequency at a varying capacitor resonant C_e load.

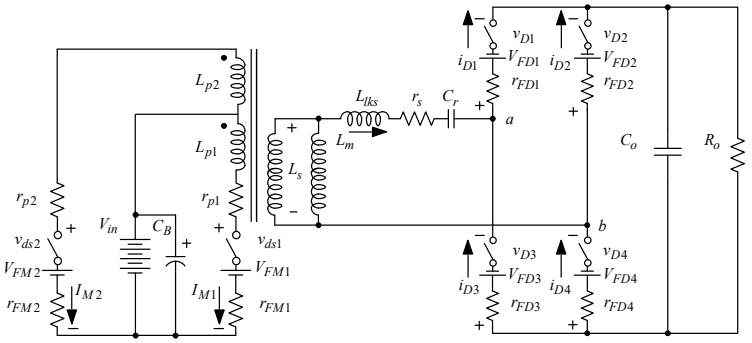


Figure 8. Equivalent circuit for the conduction loss analysis.

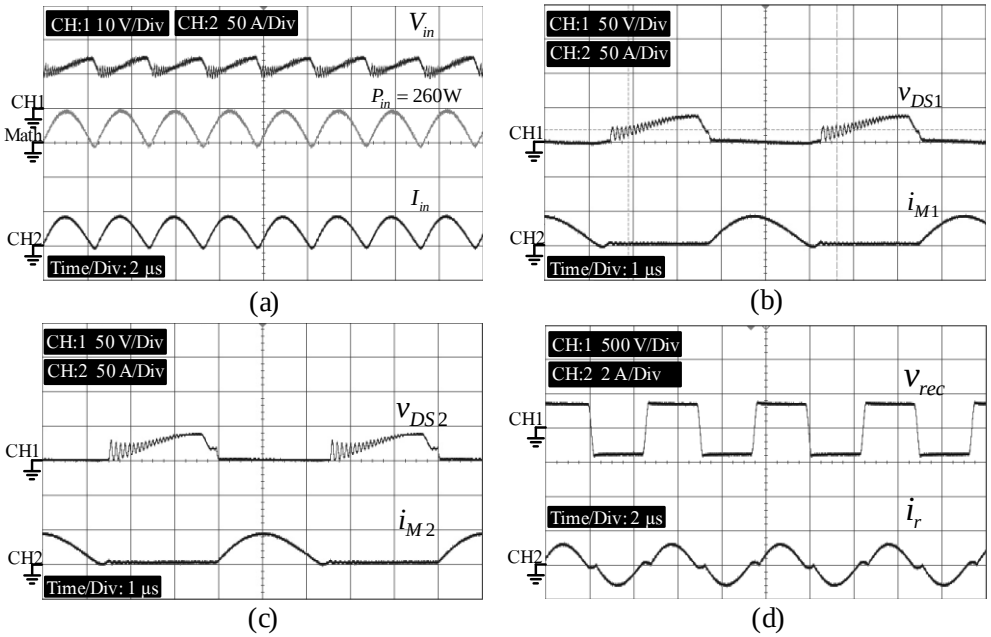


Figure 9. Experimental results. (**a**) Measured voltage V_{in}, current I_{in}, and power P_{in} waveform on the input side; (**b**) measured switch voltage v_{ds1} and current waveform i_{M1} of MOSFET M_1; (**c**) measured switch voltage v_{ds2} and current waveform i_{M2} of MOSFET M_2; and (**d**) measured input voltage rectifier v_{rec} and resonant current i_r waveforms.

In terms of the commutation stages of the parasitic junction capacitors on the rectifier circuit, the fundamental current is sinusoidal and the voltage is a square wave in the analysis of diode commutation time τ during the final time period when the junction capacitors are charged to the output voltage and discharged to zero. Therefore, the equivalent capacitance of the full-bridge rectifier C_e is related to the parallel resistance and the connected series resonant L_r and C_e, which can be found using (5), (11), and (15) as

$$C_e = \left(\frac{\pi}{16R_o f_s}\right)\left(\frac{\sin 2\omega_s\tau - 2\omega_s\tau/32f_sR_oC_D}{\left(\sin^2\omega_s\tau/16f_sR_oC_D\right)^2 + \left(\sin 2\omega_s\tau - 2\omega_s\tau/32f_sR_oC_D\right)^2}\right) \quad (24)$$

The plots of the normalized voltage gain of the resonant circuit versus the operating frequency at different values of the AC resistance are shown in Figure 6a. The range of the AC resistance varies from $R_{ac}/8$ to $8R_{ac}$ of the load R_{ac}. In our design, the switching frequency can be operated from the nearly resonant operating point until the full load for all values of output resistance. When the capacitance varies from $C_r/8$ to $8C_r$ of load C_r, the operating point of the circuit increases from half to threefold in Figure 6b. This frequency increases proportionally with the regulated output voltage. Figure 7a shows the input impedance of the resonant circuit versus the frequency while the parasitic junction capacitance is varied. It can be seen that under the high frequency range, the input impedance changes dramatically with the increasing parasitic junction capacitance, and this leads to output voltage variation. When the resistance load is constant, the operating resonance frequency point increases more than the switching frequency. The changes, with an increase in the parasitic junction capacitance, vary from $C_{e/8}$ to $C_{e/2}$ and can be noticed in the series resonant tank, where varying C_e results in the operating point switching and voltage gain moving on less than unity, and the operating point of the resonance moves from low to high frequencies. Then, the next simulation step changes from the C_e to $8C_e$ operating point from series to series–parallel resonant models. The parasitic junction capacitance affects the voltage transfer function gain and the type of resonant tank topologies, as shown in Figure 7b.

5. Design Procedure

The analysis and design of the HSPPSC for FB-CDCSR was divided into two parts. The first part involves the design of the power state and the parasitic junction capacitance in the FB-CDCSR, whereas the second part involves the analysis of the overall power loss. The design procedure for the power state and the analysis of the effect of the junction capacitance, as described in Figure 2, Figure 5, and Figure 9, are provided below.

1. Choose the voltage output V_o and the output power P_o to determine the DC side-load resistance; it is then transferred to the resistance of the AC R_{ac} side.
2. Find the load quality factor Q_L value at full load, when the switching frequency f_s is approximately equal to the resonant frequency.
3. Find the junction capacitance C_e in the FBCSR from the characteristic diode.
4. Find the equivalent resonant capacitance C_r.
5. Find the value of the output capacitor C_o and choose the ripple output to be less than 2%.
6. Finally, calculate the conduction loss in the power switch P_{rds}; the power loss in the diode rectifier P_{DB}; the loss in transformer P_{rp}, P_{rs}; and the gate driving circuit loss P_{gs}.

5.1. High Step-up Push–Pull Multiresonant Converter

The proposed HSPPSC circuit is shown in Figure 2. In the steady-state operation, the circuit was designed to be operated at a 200 kHz fixed switching frequency, 12 V_{DC}

input voltage, and a maximum power output of 250 W at an output voltage of 340 V_{DC}. Therefore, at the full load condition, the output resistance R_o is given by

$$R_o = \frac{{V_o}^2}{P_o} = \frac{(340)^2}{250} = 462.4\ \Omega \tag{25}$$

The AC resistance calculated from (13) is $R_{ac} = 8R_o/\pi^2 = 374.80\ \Omega$, which is the transferred resistance from the DC output side to the AC input side of the rectifier. When considering the voltage waveform as a high-frequency square wave and the current input of a full-bridge rectifier as a sinusoidal waveform, the maximum output power is 250 W; further, it is assumed that the total efficiency η is equal to 0.95. The peak input current $I_{in\text{-}peak}$ is given by

$$I_{in-peak} = \frac{\pi P_o}{2\eta V_{in}} = \frac{\pi \times 250}{2 \times 0.95 \times 12} = 34.44\ \text{A} \tag{26}$$

The equivalent capacitance C_e and diode commutation time τ are expressed in (23) and (24). The calculated commutation time is $\tau = 0.263$. µs when ω_s is an angular switching frequency, f_s is a switching frequency, and C_D is the combined parasitic capacitance of FB-CDCSR. The equivalent circuit in Figure 5c includes the parasitic capacitance diodes. The circuit method suggests an absolute capacitance $C_e = 0.4$ nF. Next, the design parameters of the leakage inductance from the primary side to the secondary side were determined, as listed in Table 1. The resonant inductance L_r is 389.80 µH. Then, assuming that the switching frequency is the same as the resonant frequency $f_s = f_r$ at full load, the loaded quality factor Q_L is given as

$$Q_L = \frac{2\pi f_r L_r}{R_{ac}} = \frac{2\pi \times 200 \times 10^3 \times 389.80 \times 10^{-6}}{345.80} = 1.416 \tag{27}$$

Table 1. Circuit parameters of the prototype.

Parameter	Symbol	Value/Part Number	Type
Input voltage	V_{in}	12 V_{DC}	-
Output voltage	V_o	340 V_{DC}	-
Output power	P_o	250 W	-
Output capacitor	C_o	0.33 µF	Polypropylene
Switching frequency	f_s	200 kHz	SG3525 Gate Driver
Power MOSFETs	M_1, M_2	IRFP 3205	N-Chanel MOSFETs
Fast recovery diode	D_1–D_4	MUR 860	Fast-Recovery Diode
Resonant capacitance	C_r	1.8 nF	Polypropylene
Resonant inductance	L_r	389.8 µH	EE42/13/7 N87-EPCOS
Inductance primary	L_{p1}, L_{p2}	12.07 µH, 12.02 µH	EE42/13/7 N87-EPCOS
Inductance secondary	L_s	14.50 mH	EE42/13/7 N87-EPCOS
Leakage inductance primary	L_{lk1}, L_{lk2}	0.41 µH, 0.43 µH	EE42/13/7 N87-EPCOS
Parasitic junction capacitor diode	C_{D1}-C_{D4}	75 pF	-

From (19), the resonant capacitor is obtained as

$$C_r = \frac{1}{2\pi f_r Q_L R_s} = \frac{1}{2\pi \times 200 \times 10^3 \times 1.416 \times 248.23} = 2.2\ \text{nF} \tag{28}$$

The calculation of the resonant capacitance C_r is derived from (28) and composed between the resonant capacitance and equivalent capacitance of the FB-CDCSR. Therefore, equivalent resonant capacitance $C_{eq} = C_r - C_e = 1.8$ nF. Finally, the value of the output

capacitor C_o, which is used for energy storage and regulation of the output voltage to obtain a ripple voltage V_{rip} less than 2%, is given as

$$C_o \geq \frac{V_o}{2f_s R_o V_{rip}} = \frac{340}{2 \times 200 \times 10^3 \times 612.5 \times 6.8} = 0.270\ \mu\text{F} \tag{29}$$

From the calculation, C_o = 0.270 µF. Then, the standard capacitor value of 0.33 µF/600 V was chosen for C_o.

5.2. Analysis Conduction Power Loss and Efficiency

The main power loss in the proposed circuit can occur in three major parts: power MOSFET push–pull converter, high-frequency push–pull transformer, and power diode full-bridge rectifier. The MOSFETs were modeled using switches with turn-on resistances r_{ds1} and r_{ds2}. Resistances r_{p1}, r_{p2}, and r_s represent the parasitic equivalent resistance of the physical structure of the primary and secondary leakage inductors L_{lkp1}, L_{lkp2}, and L_{lks} of the high-frequency transformer, respectively. The power diodes were modeled using switches for a constant voltage source; forward voltage drop V_{FD}; and on-resistance of four diodes r_{D1}-, r_{D2}-, r_{D3}-, r_{D4}. The push–pull converter main switches employ IRFP 3205 (International Rectifier), and each switch has an on-resistance r_{ds} = 8 mΩ. Therefore, the power loss in each switch of the MOSFETs turn-on resistance r_{ds} can be obtained by (30).

$$P_{rds} = \frac{{I_{in-peak}}^2 rds}{4} = \frac{34.44^2 \times 8 \times 10^{-3}}{4} = 2.37\ \text{W} \tag{30}$$

Then, the full-wave bridge rectifier used the MUR 860 (Intersil) as a fast recovery diode with a forward voltage drop of 1.5 V. The power loss in the diode rectifiers D_1-, D_2-, D_3-, D_4 due to the forward voltage drop V_{FD} for two diodes, $2V_{FD}$, is given as

$$P_D = \frac{2V_{FD}P_o}{V_o} = \frac{2 \times 1.5 \times 250}{340} = 2.20\ \text{W} \tag{31}$$

The electrical series resistance of the primary side of the leakage inductor $r_p = r_{p1} = r_{p2}$ is equal to 12 mΩ, and the parasitic resistance of the secondary side of the leakage inductor r_s = 3.26 Ω, which was measured by an LCR meter. Therefore, the conduction loss in the resonant inductor primary side $L_p = L_{p1} = L_{p2}$ and secondary side L_s can be determined by (32) and (33), respectively.

$$P_{rp} = \frac{{I_{in-peak}}^2 r_p}{4} = \frac{34.44^2 \times 12 \times 10^{-3}}{4} = 3.55\ \text{W} \tag{32}$$

$$P_{rs} = \frac{{I_{r-peak}}^2 r_s}{2} = \frac{1.424^2 \times 3.26}{2} = 3.30\ \text{W} \tag{33}$$

The maximum value of the resonant current I_{r-peak} can be obtained as

$$I_{r-peak} = \frac{\pi V_o}{R_{ac}(\cos\omega\tau + 1)} = \frac{\pi \times 340}{374.80(\cos(2\pi \times 200 \times 10^3 \times 0.263 \times 10^{-6}) + 1)} = 1.424\ \text{A} \tag{34}$$

The gate-driven power loss of each MOSFET is that of the push–pull multiresonant converter at high frequency. This loss can be calculated by

$$P_G = 2f_s V_{gs-peak} Q_g = 2 \times 110 \times 10^3 \times 15 \times 146 \times 10^{-9} = 0.48\ \text{W} \tag{35}$$

where $V_{gs\text{-}peak}$ is the peak voltage gate-driven between the gate–source terminal of the MOSFETs and Q_g is the value gate charge of a power switch. Hence, the total efficiency of FBCSR and HSPPMRC can be obtained as

$$\eta = \frac{P_o}{P_o + \left(P_{rds} + P_D + P_{rp} + P_{rs} + P_G\right)} = \frac{250}{250 + (2.37 + 2.20 + 3.55 + 3.30 + 0.48)} = 0.954 \tag{36}$$

6. Experimental Results

A prototype of the HSPPSC for the FB-CDCSR was simulated and built. The circuit parameters presented in Table 1 were used in the experiment. The switching frequency was fixed at approximately 200 kHz. The overall experimental results are shown in Figures 9–11. The voltage, current, and power at the input side were measured and the input power was approximately 260 W, as shown in Figure 9a. Figure 9b,c shows the switch voltages and current, and it can be seen that both power MOSFET switches operate under the ZCS condition. The input voltage waveform of the FB-CDCSR is a high-frequency square-wave voltage v_{rec} and the current resonant i_r is a sinusoidal waveform, as shown in Figure 9d. The waveform and zoom-in of a diode voltage v_{D1}, current i_{D1}, and all the diodes are operated under the ZCS condition are shown in Figure 10a,b. The measured waveform's voltage, current, and power at the output side has a maximum value equal to 250 W, as shown in Figure 10c. Figure 10d shows the experimental results of the proposed circuit under a no-load condition. In the output voltage waveform, the measured value is approximately 580 V_{DC}. Figure 12a shows the regulation of the output voltage when the switching frequency is varied from 150 to 250 kHz. The minimum and maximum output voltages at full load are approximately 340 V_{DC} at a switching frequency of 200 kHz, and both output voltages are equal to 320 and 360 V_{DC} at switching frequencies of 150 and 250 kHz, respectively. It can be seen that the output voltage change narrows the switching frequency range. The measured efficiency of the HSPPSC for the FB-CDCSR was approximately 95% at the full-load condition, and the maximum efficiency was 96% at approximately 250 W. The overall relationship values of the efficiency, output voltage, and output power are shown in Figure 12b.

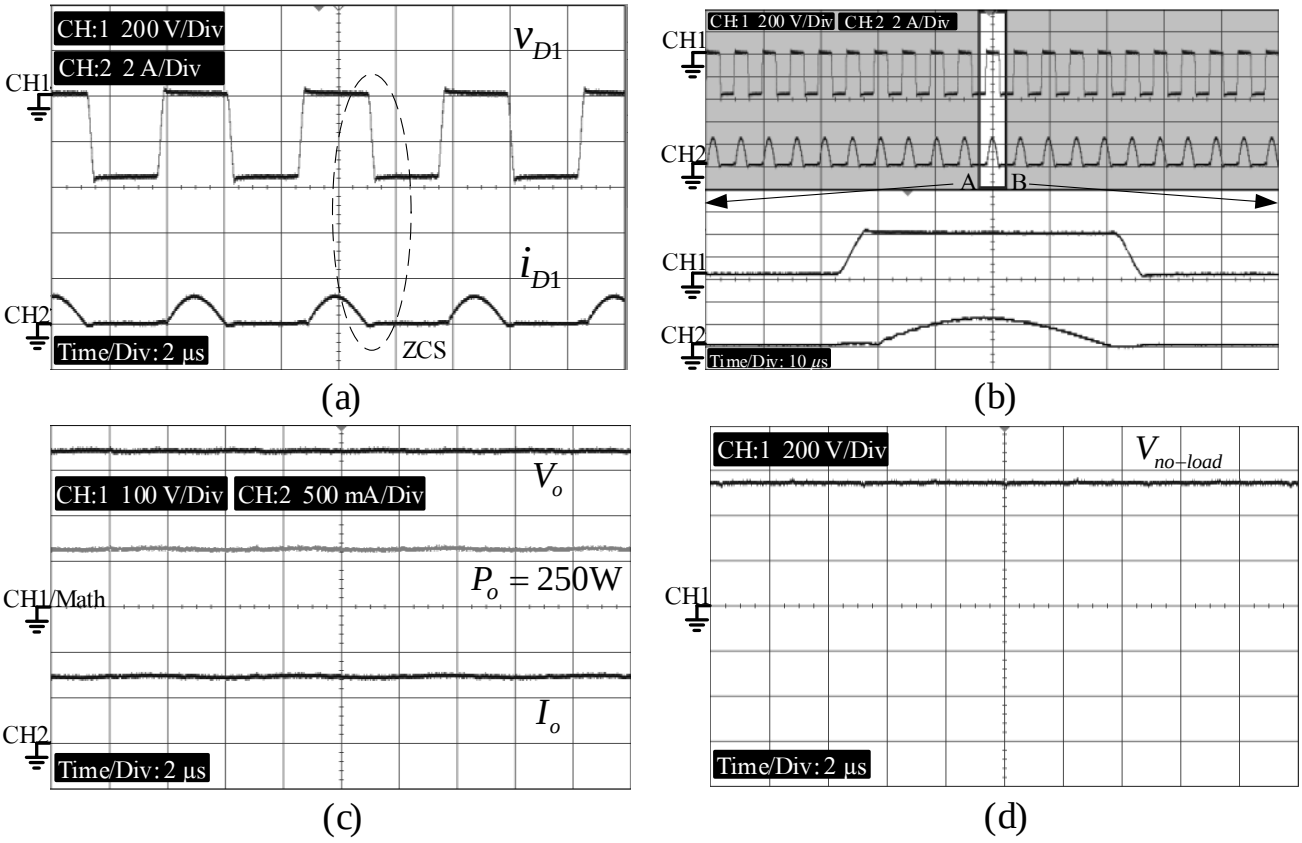


Figure 10. Experimental results of FB-CDCSR. (**a**) Measured voltage v_{D1} and current i_{D1} of the diode; (**b**) measured zoomed-in top view of voltage v_{D1} and current i_{D1} of the diode; (**c**) measured voltage V_o, current I_o, and power P_o waveforms on the output side; and (**d**) measured output voltage V_o under a no-load condition.

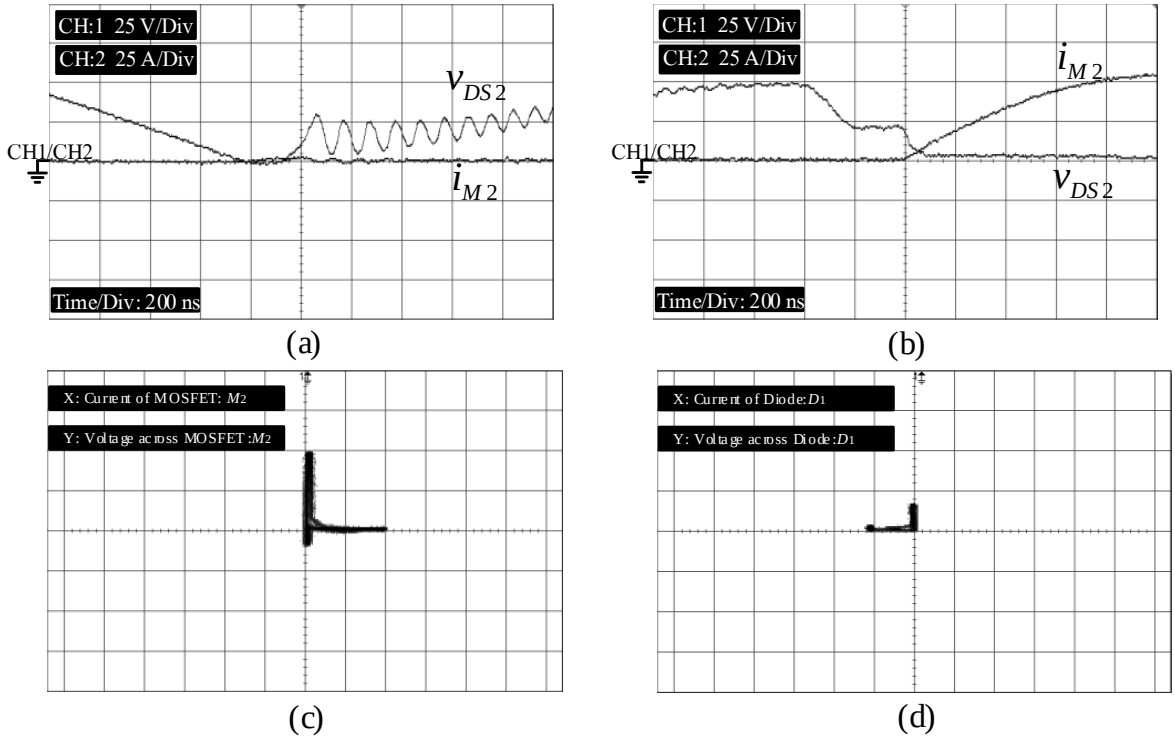


Figure 11. Experimental results of power loss. (**a**) Measured zoom-in voltage v_{ds2} and current waveform i_{M2} of MOSFET M_2 under the turn-off condition; (**b**) measured zoom-in voltage v_{ds2} and current waveform i_{M2} of MOSFET M_2's turn-on condition; (**c**) relationship power loss of route switch voltage v_{ds2} and current waveform i_{M2} of MOSFET M_2; and (**d**) relationship power loss of route voltage v_{D1} and current i_{D1} of the diode.

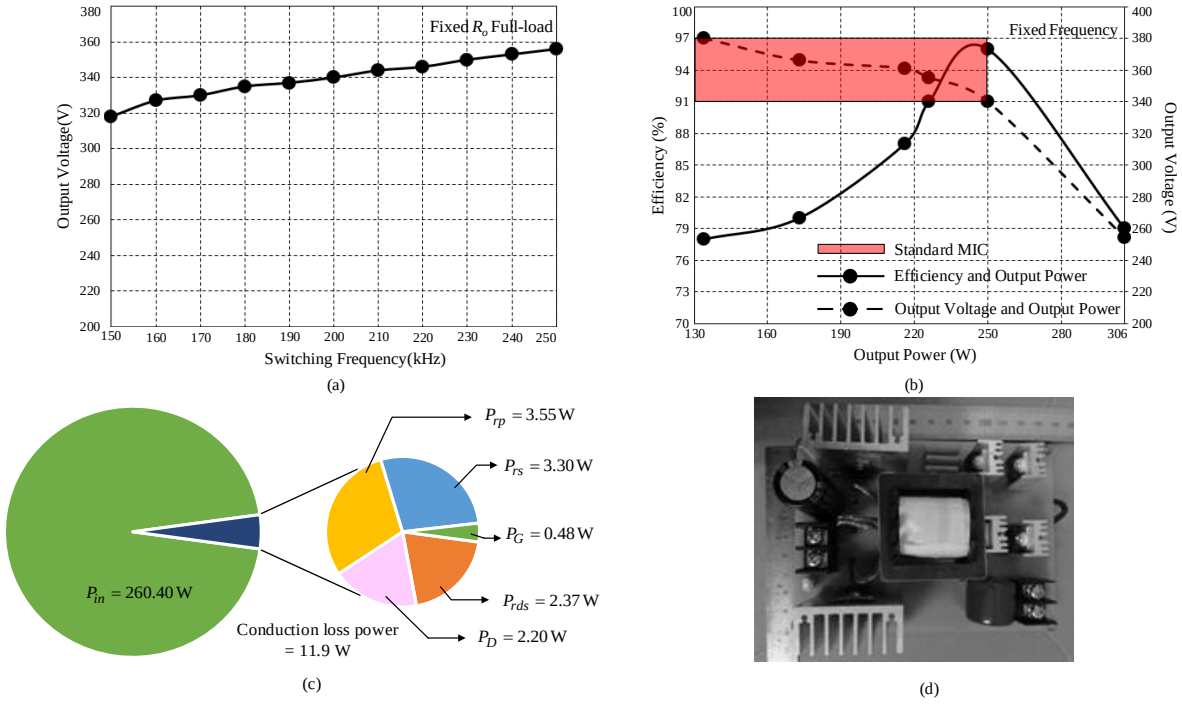


Figure 12. Experimental results of the relationship with a breakdown and photograph. (**a**) Relationship between output voltage V_o and varying frequencies f_s; (**b**) relationship between the efficiency and output power P_o and output voltage V_o; (**c**) breakdown of the overall conduction power loss of the proposed circuit; and (**d**) prototype photograph of the proposed HSPPMRC, including the effected parasitic capacitance parameter.

7. Discussion of the Effected Parasitic Capacitance Diode of the FB-CDCSR and Experimental Results

In this section discussion of the effected parasitic capacitance and comparison of previously proposed are shown Tables 2 and 3. The parasitic capacitance parameter values can be seen in the relationship curves shown in Figures 6 and 7. The results showed some changes in the output voltage with increasing switching frequency and load ranges. When the latent capacitor value generated from the rectifier circuit is used, it changes to a latent parasitic capacitor. When determining the higher switching frequency used in the circuit, the capacitance increased in value, which resulted in the original calculation being inaccurate. This is because parasitic capacitance affects the layout, placement, and response-rate ratio of the output voltage to the input voltage, including the operating point of the resonant frequency that occurs in the circuit. In Figures 8 and 12c, equivalent circuit for the conduction loss analysis and overall loss breakdown of the proposed circuit is given as follows. The most significant losses are those that occur in the primary and secondary windings of the high-frequency eques of 3.55 and 3.30 W. The losses, which amount to 1.36 and 1.26% in this section, can be calculated to be 2.62%. The loss in the following section of the MOSFET push–pull converter and power diode rectifier eques were 2.37 and 2.20 W, with losses from each component of 0.91 and 0.84%, respectively. Finally, loss occurred at the gate-driven power switch owing to its operation in the high-frequency range. The power loss in this section is of importance and was equal to 0.48 W and 0.18%.

Table 2. Comparison of previously proposed high step-up converters and their relevant publications.

Parameter	Ref [4]	Ref [8]	Ref [17]	Ref [19]	Ref [20]	Proposed Circuit
Range input voltage	48 V_{DC}	60 V_{DC}	24 V_{DC}	24 V_{DC}	35 V_{DC}	12 V_{DC}
Range output voltage	400 V_{DC}	380 V_{DC}	400 V_{DC}	200 V_{DC}	400 V_{DC}	340 V_{DC}
Switching frequency	120 kHz	120 kHz	40 kHz	100 kHz	100 kHz	200 kHz
Range output power	400 W	1 kW	400 W	60 W	300 W	250 W
Range efficiency	≥90%	≥90%	≥90%	≥90%	≥90%	≥90%
Conversion ratio	8.33	6.33	16.66	8.33	11.42	28.3
Topology circuit	series 2 boost converters	buck–boost clamp mode	boost voltage multiplier cells	Modify-flyback volt double	Flyback-active clamp voltage multiplier	push–pull traditional
Voltage across switches	normal	normal	normal	high	normal	normal
Number of switches	1 main 1 auxiliary	1 main	1 main	1 main	1 main 1 active clamp	2 mains
Number of capacitors	5	1	3	2	4	1
Number of inductors	1 transformer (2 inductors) nonisolated	1 transformer (2 inductors) nonisolated	2 inductors nonisolated	1 transformer (2 inductors) nonisolated	1 transformer (2 inductors) isolated	1 transformer (2 inductors) isolated
Number of diodes	3	2	3	2	2	4
Component count	11	5	9	6	9	8 + 2 (C_{in} and C_r)

In addition, in Figure 11a,b, the measured zoom voltage v_{ds2} and current waveform i_{M2} of MOSFET M_2 under the turn-off and turn-on conditions show the voltage and current that pass through each other, which resulted in the loss of this part being greatly reduced. This confirms the route voltage and current in the relationship of the routes of switch voltage v_{ds2} and current waveform i_{M2} of MOSFET M_2. The route power loss of voltage v_{D1} and current i_{D1} of the diode in the path of loss of both switches are shown Figure 11c,d. The power loss is also low because the main power switch and diode rectifier are operated under the ZCS condition. In the section operated in full resonant mode, from the power state, it can achieve a reduced maximum peak current of the diode rectifier.

Table 3. Key performance comparison of the state-of-the-art isolated proposed circuit.

Parameter	Ref [27]	Ref [35]	Ref [36]	Ref [38]	Ref [42]	Ref [44]	Proposed Circuit
Range input voltage	50 V_{DC}	30–70 V_{DC}	48 V_{DC}	38–50 V_{DC}	23–38 V_{DC}	30–50 V_{DC}	12 V_{DC}
Range output voltage	400 V_{DC}	350 V_{DC}	400 V_{DC}	380 V_{DC}	350 V_{DC}	350 V_{DC}	340 V_{DC}
Switching frequency	50 kHz	70 kHz	74 kHz	200 kHz	255 kHz	100 kHz	200 kHz
Range output power	250 W	1.5 kW	400 W	500 W	150 W	510 W	250 W
Range efficiency	≥90%	≥90%	≥90%	≥85%	≥90%	≥90%	≥90%
Conversion ratio	8/1	11.6/5/1	8.3/1	10/8.6/7.6/1	15.2/9.2/1	11.6/7/1	28.3/1
Operation mode main state	ZVS	ZVS	ZVS	ZCS	ZCS	ZVS	ZCS
Topology rectifier	volt double 2 modules	volt double 1 module	center tap II 1 module	bridge 1 module	volt double 1 module	volt double 1 module	bridge 1 module
Stress voltage/mode	2 V_o/ZCS	2 V_o/ZCS	2 V_o/ZCS	V_o/ZCS	2 V_o/ZCS	2 V_o/ZCS	V_o/ZCS
Balance flux transformer	N/A	unbalance	unbalance	balance	unbalance	unbalance asymmetrical	balance
Useful parasitic capacitance	neglect	neglect	neglect	adoption	neglect	neglect	utilization
Classify resonant	LC series resonant	LC series resonant	LC series resonant	LC parallel resonant	LC parallel resonant	LC parallel resonant	LC series multiresonant
Number of inductors or transformer/capacitors	2 transformers 3 capacitors	1 transformer 1 inductor 3 capacitors	1 transformer 1 inductor 1 capacitor	1 transformer 1 inductor	1 transformer 2 inductors 1 capacitor	1 transformer 1 inductor 1 capacitor	1 transformer 1 capacitor
Number of main switches	2 switches	2 switches 2 actives	2 switches	2 switches	2 switches	2 switches 1 active	2 switches
Number of rectifiers side	4 diodes 3 capacitors	2 diodes 3 capacitors	2 diodes 3 capacitors	4 diodes 2 capacitors	2 diodes 3 capacitors	2 diodes 3 capacitors	4 diodes 2 capacitors
Component count	14	13	10	10	11	11	10

8. Conclusions

This paper presented the parasitic capacitance of an FB-CDCSR design in the HSPPMRC. Both power switches of the push–pull resonant circuit received 12 V_{DC} input voltage from a battery and converted it to a high output voltage of 340 V_{DC} at an output power of 250 W, when operating at a 200 kHz fixed frequency. The efficiency of the system was measured and a value of 96% was obtained at full power. The advantages of using this method are as follows:

- High voltage gain conversion ratio;
- Less components in the system;
- Leakage inductance and parasitic junction capacitance of the diode rectifier in the designed resonant tank, and simplified calculation;
- Additionally, the magnetic flux current in both main power switches can be easily balanced by a small leakage inductance at the input side.

Therefore, the generation and application of the conversion circuit is necessary to convert low-voltage DC to high voltage, and the effect of the latent charge that occurs in the rectifier circuit should be considered. Parasitic capacitance is important and, therefore, should be considered in the design. Moreover, it was demonstrated that the parasitic junction capacitance of the diode rectifier had a significant impact on the operation point of the resonant tank circuit in the high-frequency range. Furthermore, it had a direct impact on the output voltage of the high-voltage-gain isolated front-end converter.

Author Contributions: Formulation and evolution of overarching research goals and aims, development and design prototype circuit, verification of results/experiments and other research outputs, prepare manuscript (original draft), A.B.; application of mathematical and simulation computational, recheck formal techniques to analyze study data and experimental result, C.E.; Management and coordination responsibility for the research activity planning and execution, preparation, of the published work, specifically writing the initial draft (including substantive translation), V.C.; Mentor advisor, acquisition of the financial support for the project leading to this publication, oversight and leadership responsibility for the research activity planning and core team, P.T. All authors have read and agreed to the published version of the manuscript.

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